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Status Report on the FERMI Project

A digital Front-end and Readout Microsystem for calorimetry at LHC

Spokespersons: G. Goggi, B. Lofstedt

R. Benetta, A. Dell'Acqua, M. Hansen, S. Inkinen, B. Lofstedt, J. P. Vanuxem
CERN, Geneva, Switzerland

C. Svensson, J. Yuan
Department of Physics and Measurement Technology, University of Linköping, Sweden

S. Gong, H. Hentzell
Industrial Microelectronics Center, University of Linköping, Sweden

H. Alexanian*, P. Bailly, F. Blouzon, J. Bezamat*, J. David, J. F. Genat, O. LeDortz, S. Mutz*, P. Nayman, A. Savoy-Navarro, P. Schwemling
LPNHE Universites Paris VI-VII, Paris, France

C. Alippi, L. Breveglieri, L. Dadda, V. Piuri, F. Salice, M. Sami, R. Stefanelli
Dipartimento di Elettronica, Politecnico di Milano, Italy
Sezione INFN, Pavia, Italy

P. Cattaneo, G. Fumagalli, V. G. Goggi, G. Polesello
Dipartimento di Fisica Nucleare e Teorica dell' Universita'
Sezione INFN, Pavia, Italy

S. Brigati, U. Gatti, F. Maloberti, G. Torelli
Dipartimento di Elettronica dell' Universita' e Sezione INFN, Pavia, Italy

A. Kerek, B. Lund-Jensen
Physics Department, Royal Institute of Technology, Stockholm, Sweden

G. Appelquist, S. Berglund, C. Bohm, M. Engström, N. Yamdagni
Fysikum, University of Stockholm, Sweden

I. Höglund
ABB HAFO AB, Järfälla, Sweden

M. Givoletti, G. M. Grieco, C. Landi, M. Lippi
C.A.E.N. S.p.A., Viareggio, Italy

T. Holmberg, A. Ödmark, R. Sundblad
SiCon AB, Linköping, Sweden

(*) also from ESIEE, Paris, France

Abstract

The results of the third year of activity of the FERMI project are presented.

The Analog ASIC, containing the bipolar compressor, the ADC and auxiliary circuits was implemented in a BiCMOS 1.2 μm process. The improved ADC design provides now full 10-bit resolution at 70 MHz. A CMOS compressor and other test structures have also been implemented in rad-hard SOS4 technology from ABB HAFO and in the RD29 DMILL process.

The Channel ASIC, containing the Look-up tables, data memories and first trigger functions, was fully described in VHDL and tested as an array of XILINX FPGAs. Circuits are being delivered in May 1994.

The Service ASIC, containing the clock manager, the test pulse generator, the R/O controller and all the digital filters, was fully described in VHDL and extensively simulated. It will be submitted for fabrication in May 1994.

The fault tolerance strategies, i.e. redundancy, reconfigurability, concurrent processing and coding for error detection and correction have been implemented into the design of the two digital ASICs.

The microsystem substrate has been laid out after extensive simulations of crosstalk, noise and interconnections. It will be fabricated during summer 1994. Techniques for self-test of the entire microsystem are being developed.

The irradiation program with gamma and neutron sources, including thermal cycling of the irradiated samples, is continuing. Detailed results have been obtained on error rates and mechanisms on "reference" commercial digital circuits.

Beam tests on different calorimeter prototypes are being carried out or prepared with the ATLAS and CMS Collaborations.

In total, 24 prototype ICs of different types have been fabricated and tested since the beginning of the project. An additional 5 ICs, including the final FERMI demonstrator, will be realised by the end of year.

Studies of the global FERMI system environment have been started.

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1. Introduction

The RD-16 Project, aimed at developing a Front-End Readout MIcrosystem for calorimetry, was approved by the DRDC in 1991. The FERMI Collaboration, now consisting of nine research institutes and three industrial partners, aims at exploring and developing the technologies required to realise a multi-channel data acquisition and signal processing module implemented as a silicon-on-silicon multichip microsystem [1, 2].

The FERMI microsystem is designed to perform dynamic range compression, digitisation up to 80 MHz, Digital Signal Processing, trigger functions and buffering of calorimeter data up to and including second-level trigger latency. It is intended to be mounted directly on the detector, along with a local system controller performing control, calibration and other system functions. For applications with high level of radiation and limited accessibility, the design incorporates a high degree of redundancy, fault- and radiation- tolerance [3, 4].

The first aim of the project is to produce a microsystem demonstrator containing several functional blocks integrated in three ASICs (see Sect. 2). The activities and the results achieved so far can be summarised as follows :

- The Analog ASIC has been fabricated and is under test.
- The Channel ASIC has been fully described in VHDL and tested as an array of XILINX FPGAs. It has been fabricated and circuits are being delivered in May 1994.
- The Service ASIC has been fully described in VHDL and extensively simulated. It will be submitted for fabrication in May.
- Systematic investigations of more than 20 different digital filter architectures were carried out.
- System test protocols and fault tolerance architectures have bee implemented.
- The microsystem substrate has been laid out after extensive simulations of crosstalk, noise and interconnections. It will be fabricated during summer.
- Beam tests on different calorimeter prototypes are being carried out or prepared with the ATLAS and CMS Collaborations.
- Irradiation studies of different memory technologies were performed as reference for actual FERMI elements.
- The bipolar compressor, together with test structures, has been modified for implementation in the DMILL rad-hard technology (RD29).
- Studies of the global FERMI system environment have been started.

In total, 24 prototype ICs of different types have been fabricated and tested, and an additional 5 ICs, including the final demonstrator, will be realised in 1994.

After the demonstrator phase, a full system environment will be developed. It will include local and remote controllers connected via optical links, interfaces to trigger and readout processes and the system aspects required for integration in actual detectors.

The project is being developed in collaboration with our industrial partners, hi-tech companies in microelectronics and instrumentation with specific expertise in rad-hard CMOS processes (ABB HAFO), analog and digital ASIC design (SiCon), multichip microsystem design and fabrication (IMC) and nuclear instrumentation (CAEN).

2. FERMI architecture

2.1 System overview

FERMI is a multi-channel data acquisition and signal processing module implemented as a silicon-on-silicon multichip microsystem. The microsystem, realised as a large silicon multi-layer substrate with four metal layers, supports ASICs, components, interconnections and transmission lines.

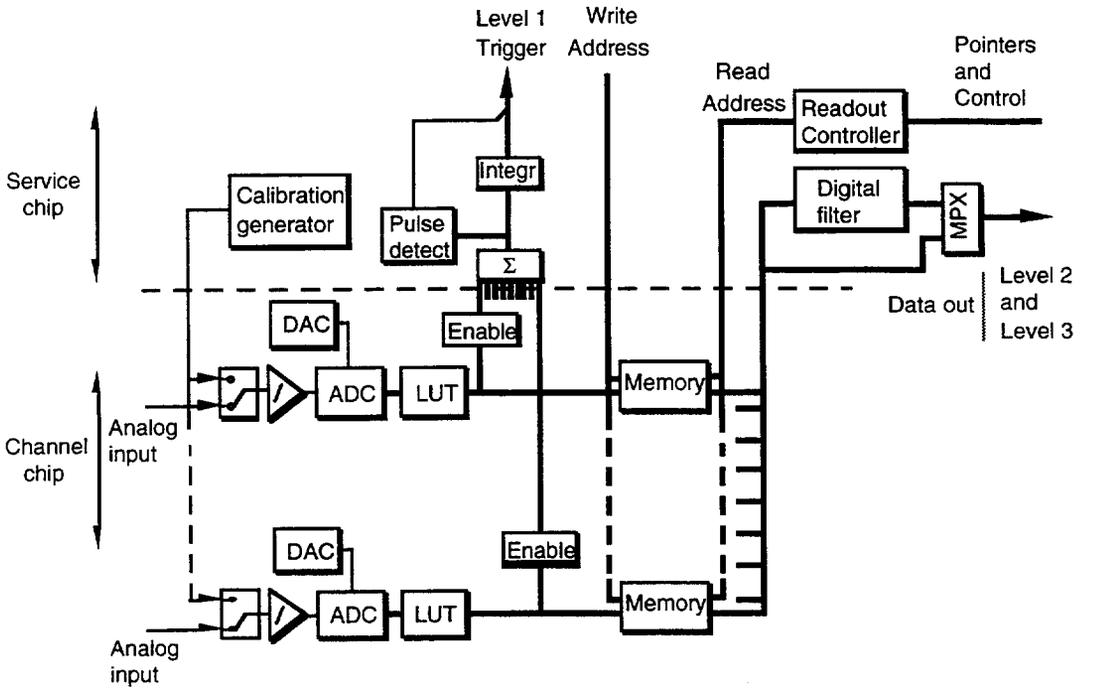


Fig. 2.1. An overview of FERMI

Fig. 2.1 contains all major FERMI components in the form of a simplified block diagram. The demonstrator will contain nine complete channels.

Input signals, with a dynamic range of 15–16 bits, are compressed and digitised at sampling frequencies up to 80 MHz. The resulting 10-bit data are linearised and expanded to the full 16-bit dynamic range by means of a look-up table containing the inverse transfer function of the detector-electronic chain. This provides an absolute calibration for each individual channel.

The expanded data from all channels are individually discriminated with independent programmable thresholds. They are then summed and processed by digital filters in order to extract energy and time information for the first-level trigger process. A module-level pulse detect signal can set a flag to identify possible pile-up conditions for special processing.

The expanded digital data are stored in a dual-port memory until the decisions from the first- and second-level triggers become available. The storage occurs in memory positions given by an external memory management unit. A temporal environment, a time frame of programmable length, is associated with each event accepted by the first-level trigger. All memory locations containing sample points not included in a time frame after the first-level decision are returned to the list of free memory. Time frame memory locations are also returned to the free list after having been rejected by the second-level trigger or read out by the data acquisition.

The FERMI Readout controller supervises the extraction of data, in the form of either complete time frames or digitally filtered values of the energy. In the latter case the information contained in a time frame is extracted by means of adaptive non-linear digital filtering techniques optimised for extracting a precise value of the energy in the presence of noise and jitter. It is envisaged that the filtered readout should be default when pushing data to the second-level trigger process. This could, however, also return for selective readout of full time frames, which might be necessary in order to resolve specific conditions.

All the functions above are implemented into three main parts: an Analog ASIC, a Channel ASIC and a Service ASIC.

A specific feature of the FERMI architecture is provided by its high degree of flexibility, with more than one hundred different programmable parameters under control of a Local Micro Controller. The latter acts as a supervisor for the internal calibration features, the monitoring functions and the architectural configurations of the system.

To achieve a high level of reliability, FERMI is also being designed with a high degree of fault tolerance and for implementation in rad-hard technologies.

2.2 Fault tolerance implementation

Some of the fault-tolerance policies have been implemented in the prototype subsystems. Final decisions will be made on the basis of fault information provided by the ongoing and future irradiation tests on sample chips. The fault tolerance solutions implemented so far use error correction coding, redundancy, reconfigurability and residue-number techniques.

Final decisions have been reached for the Look-Up Table, the Memory and the Digital Filter subsystems. In the two first cases, concurrent error-detection and correction was chosen, since information stored in these memories is critical for any subsequent operation.

In particular, a very strong protection has been devised, with data encoding (Hamming solution) accompanied by a novel triple-redundancy current-voting scheme for the address decoding sections and by error-storage techniques (based on the use of a small associative memory). This grants correction of transient faults without undue redundancy and survival to (a limited number of) multiple faults.

Prior to filtering, the fault tolerance coding is changed from Hamming to a modified residue-number technique. This to allow for the operations of channel addition, truncation and reformatting of the first-level trigger process, which are not compatible with Hamming coded data.

As for the filter section, alternative designs have been pursued, corresponding to different levels of fault-tolerance with respect to different fault distributions in time. The present solution is based on a multiplier-adder module suitably replicated throughout the filter structure, each section allowing host-driven fault detection while concurrent fault detection is available at filter level.

The philosophy adopted involves host-driven fault confinement and reconfiguration. More specifically, filter-level concurrent self-checking (obtained through a modified residue technique, with modulo-3 residues coded in one-out-of three coding) allows to verify correct operation of the filter as a whole. In case of error detection, the filter is confined (i.e., it does not process nominal data any more) and the host process feeds it simple test vectors allowing to identify the individual multiplier-adder section where the error is present. This in turn allows the host process to exclude the faulty multiplier/adder section from operation and either to reconfigure the filter to its nominal operation (if spare units are available) or to proceed through graceful degradation, accepting a filter with a lower number of stages.

3. The Analog ASIC

3.1 Basic architecture

Each of the nine channels in a FERMI microsystem has a its analog input part in the form of an ASIC containing the dynamic range compressor, the Analog to Digital Converter and a pulse injection circuit, together with their respective programming and support functions. The latter consist of a DAC for pedestal control, a local voltage regulator and an amplifier/servo loop for level shift and baseline control.

For the Compressor and ADC functional blocks, we continue to pursue two parallel developments exploring different architectures and technologies. We are developing bipolar and CMOS compressor designs in two different technologies. Similarly, we are developing a Parallel Successive Approximation ADC (PSA-ADC) along with a Two-Step Flash ADC. The most advanced solutions, the bipolar compressor and the PSA-ADC, are being implemented in the first FERMI prototype (see Fig. 3.1).

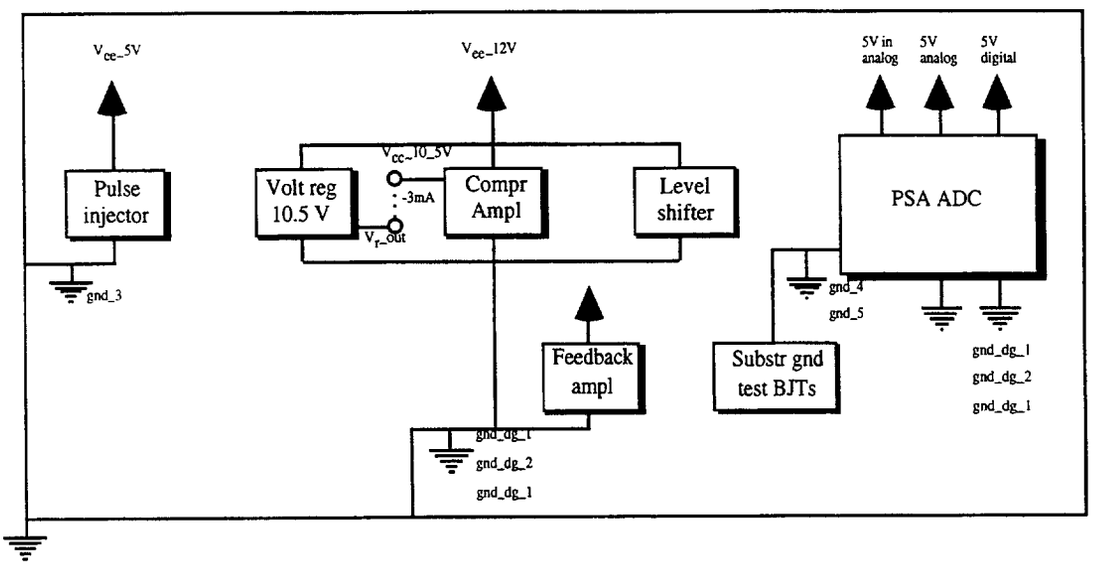


Fig. 3.1. Block diagram of the Analog ASIC

As a parallel development, the compressor is being implemented also in the DMILL (RD29) technology, in order to evaluate a radiation hard solution. Also, test objects have been implemented in the ABB HAFO SOS4 process and the results are reported below (see Sect. 3.5).

The following sub-sections describe the Analog ASIC in more detail.

3.2 The bipolar compressor

Tests of the first prototype implemented in the Gennum Ga911 process showed that the architecture of parallel differential amplifiers generating a piecewise linear response is a working solution. In particular [4]:

- the shape of the transfer curve can be tailored to match the resolution of any practical calorimeter,
- the bandwidth of 50 MHz is in excess of requirements,
- the output noise (250 μV) is low compared to the ADC LSB (2 mV),
- the rms channel-to-channel spread of the transfer curve is ≤1%.

- the thermal stability is good, with a coefficient of 0.4 LSB/°C at the break points of the transfer function.

Based on this experience we have implemented the compressor, together with a pulse injection system, on the Analog ASIC (see Fig. 3.3).The new version includes a local voltage regulator, a level shifter and a comparator in the output section forming a slow servo loop, thus allowing for improved temperature stability and for DC-coupling between the compressor and the ADC.

3.3 The Parallel Successive Approximation ADC

The stand alone PSA-ADC prototypes

In the second stand alone ADC prototype, improvements on reference settling (removal of one serial switch) and on auto-zero timing (4 instead of 2 clock cycles) were implemented. The chip reaches 8 to 9 effective bits at 70 MS/s and 9 to 10 effective bits at 40 MS/s, showing that the improvements were successful.

The last ADC prototype was received in October 1993 and successfully tested with the FERMI test bench installed at CERN. Tables 3.1 and 3.2 summarise the performances of each SA-ADC channel and of the complete PSA-ADC. Detailed results are described in Sect. 7.1.

Table 3.1. The SA-ADC cell characteristics

Digital code	10 bit
Input range	0-2 V
Input capacitance	1 pF+C_{pad}
Input bandwidth	35 MHz
Clock frequency	70 MHz
Sampling rate	5 MS/s
DNL	±0.5 LSB
INL	±0.83 LSB
Power supply	5 V
Core circuit size	0.6 mm^2
Power consumption	18 mW
Technology	1.2 µm CMOS

Table 3.2. The PSA-ADC characteristics

Digital code	10 bit
Input range	0-2 V
Input capacitance	1.7 pF+C_{pad}
Input bandwidth	35 MHz
Clock frequencies	40 MHz, 70 MHz
Sampling rates	40 MS/s, 70 MS/s
DNLs	± 0.5 LSB, ± 0.75 LSB
INLs	±0.68LSB, ± 1.10 LSB
Power supply	5 V
Core circuit size	2.7 x 3.3 mm^2
Power consumptions	225 mW, 267 mW
Technology	1.2 µm CMOS

The PSA-ADC on the Analog ASIC

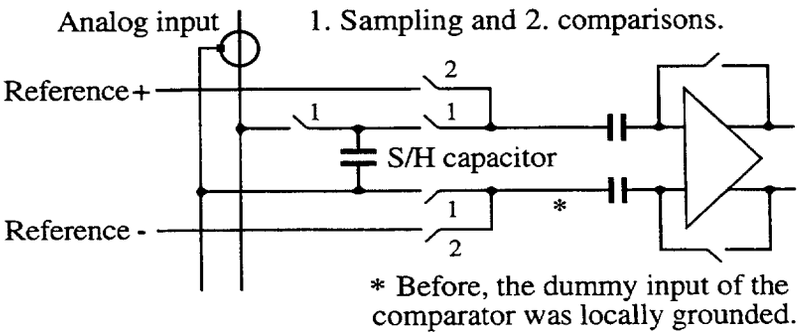


Fig. 3.2. The fully differential input arrangement.

The last stand alone ADC prototype showed some residual coupling between neighbouring channels. In order to reduce this effect, a fully differential input arrangement for the comparator was implemented, as shown in Fig. 3.2. During the auto-zero phase the dummy input of the comparator is connected to the "ground" of the input, and during comparisons the dummy input is connected to the "ground" of reference voltages (coarse and fine). In this way, both the crosstalk noise and DC offsets are further suppressed.

3.4 The Current injector

The first version of the current generator is built around a differential amplifier, with emitter resistance for improving linearity and cascode outputs for increased output impedance.

An improved scheme is under study, which should eliminate the injection of DC levels. It is a symmetric bridge, placed across the inputs of the compressor. During normal data taking, the current flows equally in the two branches, leading to a zero voltage at the inputs of the compressor. A differential voltage generates the test pulse.

3.5 ASIC layout and production

The Analog ASIC implements for the first time a mixed analog/digital FERMI subsystem. It contains an analog part with extreme performance requirements in close proximity to the A/D converter with heavy digital activity.

The layout consists of nine different parts i.e. pulse injector, compression amplifier, level shifter, feedback amplifier, A/D converter (PSA-ADC), 10.5V voltage regulator, test BJT block, clock buffer and pads. All modules can be measured separately, and all interconnections are carried out via pads. The total size of the chip is 5.6 x 4.3 mm and the total number of pads are 68 (see Fig. 3.3). The technology chosen for this prototype run was AMS 1.2 µm BiCMOS process.

ASICs were delivered mid-April. They are mounted in a 68 pin CLCC package. The chip is also designed for flip-chip mounting on the FERMI microsystem module.

Tests show that the compression amplifier have the same basic characteristics as the above mentioned prototype. More detailed measurements are being done. The A/D converter is not yet tested.

3.6 Parallel developments

The Two-stage Pipelined A/D Converter

This alternative converter design has been completed and a prototype of the whole ADC has been integrated using the AMS 1.2 µm CMOS technology.

Testing of the phase generators was successful up to about 100 MHz clock rate, showing that all the phase signals for the different parts of the circuit work correctly. Testing at higher clock frequencies was not possible due to external noise. However, separate tests of some cells show that good performance is achieved above 200 MHz clock rate.

Problems have been observed in the CMOS latches used as comparators in the first flash ADC [5]. After detailed analysis, it was discovered that this behaviour is intrinsic to the comparator architecture. Therefore, only a functionality test of all the parts of the converter was possible. This showed that all of them are working, but no accuracy or speed performance evaluations were possible. This also inhibits the measurement of the converter as a whole.

A new version of the ADC is being fabricated and samples are expected by summer 1994. In the meantime, work is in progress on improved comparator structures, as well as on the Subtract-and-Hold circuit. This could allow the multiplication of the residue by a small factor (2 to 4 at least), relaxing the precision requirements on the subsequent stage (i.e. the 6 bit Two-Step Flash ADC).

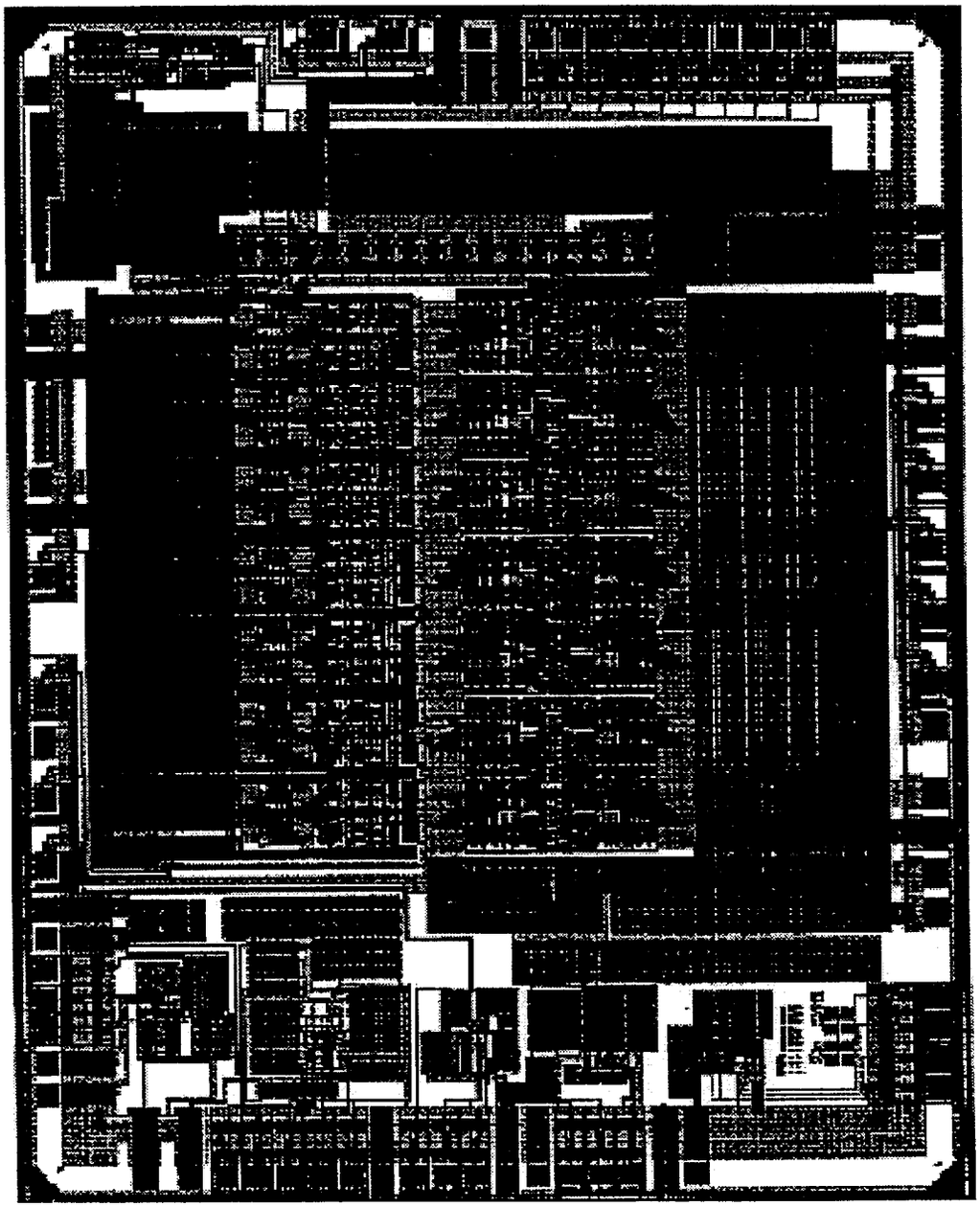


Fig. 3.3. Layout of the Analog ASIC.

Analog applications of the SOS technology.

As a possible alternative to the bipolar compressor already developed, SOS test circuits have been designed and fabricated to evaluate the feasibility of this technology for analog rad-hard design. with the obvious advantages of total latch-up immunity and an inherently good radiation hardness.

Traditionally, only digital circuits could be realised in SOS, since the floating transistor substrate generates a discontinuity in the transistor characteristics. This was

recently overcome by ABB HAFO by realising a good contact to the substrate of the transistors. The aspects of this technology to be investigated are noise and leakage. The former creates problems in the compressor amplifier because of the large amplification, the latter creates problems in the comparator design.

A SOS compressor amplifier.

This compressor is implemented with three parallel gain stages having different gains and saturation points summed into one output amplifier.

The amplifier has been implemented in the 2 μm SOS4 process at ABB HAFO. The substrate connection design rules has been applied to all amplifying transistor while the reset transistor are implemented as digital transistor with floating substrate. The core area of the amplifier is 0.5 x 1.3 mm^2.

The transfer characteristics and the speed of this prototype correspond to the design performance. The noise level is dominated by 1/f noise with an rms of 10 mV. This can be overcome by calibrating the baseline after each reset pulse, in which case the high frequency noise becomes approximately 1 mV_{rms}, to be compared with the LSB value of 2 mV.

A SOS comparator design suitable for A/D converters.

In order to evaluate the performance of an A/D converter implemented in SOS technology, a test circuit containing three slightly different comparators and one complete S&H comparator block has been designed and implemented with transistor dimensions modified to get optimal performance from ABB HAFO's SOS4 process. The complete S&H comparator block has an area of 1.14 x 0.43 mm^2. The separate comparators do work but measurements indicate a large uncertainty, the measured resolution at 40 MHz clock frequency being approximately 30 mV compared to the expected 1 mV. The reasons for that are under investigation.

4. The Channel ASIC

4.1 Basic architecture

Each of the three Channel ASICs in FERMI contains, in turn, three parallel channels deriving their data from three corresponding ADCs (see Fig. 4.1). The 10-bit data from the ADCs are transformed in look-up tables into a linearised, absolute 16-bit representation. The data are then transferred along two paths: one to the local first-level trigger summing circuit, while the other merges with data from the other channels. The result is fed to the data memory at a place determined by the externally provided insert address pointer. An external extract address pointer selects in a similar way a 48-bit memory word from which a data selector chooses a 16-bit data word to be transferred to the Service ASIC.

Each Channel ASIC stores also one of three possible flags, one pulse-detect and two pile-up flags. These flags are generated in the Service ASIC and are sent to each Channel ASIC. A programmable selector chooses which flag should be included in the data stream fed to the data memory of the ASIC in question.

Fault tolerance is achieved by providing each 10- or 16-bit data word with a 5 (respectively 6) bit error correction code (ECC) of Hamming type, allowing single-bit correction and double-bit detection. The 66 bit data (3x22) are merged with their corresponding flags, which are stored in three error protected bits. Further fault protection is achieved by triplicating all fault sensitive logic (shaded in Fig. 4.1) with a hardware current voting. Further protection is given by providing an extra bit in the look-

up table which contains the parity of its address. This feature will signal fatal address decode errors that have escaped the triplicated address decode scheme. All data busses between the different ASICs are also ECC protected. Single bit errors will be corrected, double bit address errors will temporarily disable the memory access to prevent overwriting data.

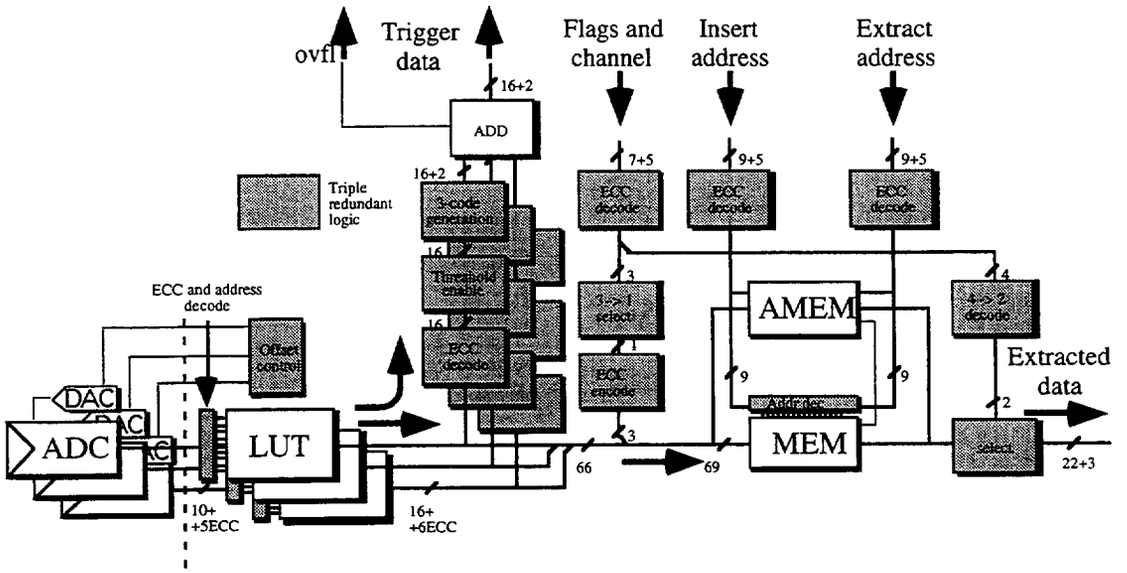


Fig. 4.1. Block diagram of the Channel ASIC

The fault protection of the first-level trigger data is converted from ECC to a 2-bit modulo-3 residue code. This code is convenient for checking arithmetic calculations and will accompany the data through the rest of the system. An additional safety factor is a small associative memory operating in parallel with the main data memory used for patching faulty data cells. It can also be used for diagnostic purposes.

The following sub-sections describe the digital system in more detail. Shadowed boxes in the figures indicate programmable parts which are controlled through the internal serial communication.

Look-up Table

The look-up table (LUT) compensates for all the non-linearities introduced ahead of the ADC, including the detector itself. It can also perform pedestal subtraction thus producing absolute data. A multiplexer has been introduced to provide an emergency bypass path around the LUT. This facility can be used to recover partially from a fatal look-up table failure. The look-up table input is also equipped with a programming multiplexer, allowing to program any given cell via the data register. An auto-increment mode is implemented to facilitate the programming of sequences. A monitoring register on the LUT output is provided for diagnostic purposes.

The programmable counter can also be used in connection with storing a digital test-sequence in the look-up table. In this mode the clock input of the address counter is connected to the bunch crossing clock, causing the stored pattern to be sent to the pipeline and the first-level trigger logic. This option provides a way to generate digital test sequences for both the first and second-level triggers.

First-level trigger data extraction

The threshold function contains a programmable threshold which can be used to discriminate against channel noise. It can also be used to disable malfunctioning channels

entirely so that they will not be included in the trigger summation. This feature allows a precise and programmable tailoring of the contribution of each individual channel to the first-level trigger.

Data Memory

The memory block contains an option for insertion of diagnostic data at its input and a monitor register at its output to allow thorough testing of the memory function. The source insert address can also generate a sequential address stream to the memory.

The memory function will be realised by two toggling single-port memory banks. It is therefore required that the insert addresses alternate between odd and even.

Additional fault tolerance is provided by a small 2-cell two-port associative memory which intercepts the main memory access when an attempt to write into a faulty memory location is detected.

Control and register (MUX, status-, error-registers)

The internal serial link is used to access and control registers and multiplexers throughout the ASIC. The latter are used to inject test data into any of a number of test points along the data path. The programmable clock burst control enables freezing the system state at given points (see below). Suitably placed spy registers monitor the results as well as the error status of different system functions.

Simulation

The equivalence of the ASIC layout and the VHDL specification of the Channel ASIC was investigated by extensive simulations with test vectors.

The VHDL code describing the digital part of FERMI, before prototyping the first ASICs, has been synthesised into FPGA (field programmable gate arrays). This approach alleviate the preparation of the test bench by providing hardware to test the software routines with real signals and comparing them with simulated ones.

The main effort was put onto the Channel ASIC part which was split into two Eurocard boards, one having 3 independent channels with their LUT memories, counters and multiplexers, the other dealing with the main memory and the pointers from the address generator.

As a result of these tests, the serial internal link has been improved on two major points. On one side the protocol is now well refined. On the other, the decoding logic was modified decreasing substantially the gate count.

4.2 Layout

The layout of the Channel ASIC consists of mainly four different parts, i.e. memories, control logic, clock buffers and pads. The total size of the chip is 17.1 x 10.9 mm and the chip has approx. 930 000 transistors (see Fig. 4.2). The technology chosen for this prototype run was AMS 1.0 µm CMOS process.

4.3 Production

The design was submitted to production at the beginning of March and circuits are being delivered in May 1994. The prototype ASICs will be mounted "chip on board" on a small (4.7 x 4.7 cm) PCB with edge-contacts (0.04" contact spacing). The PCB's are then mounted in sockets on the VME prototyping card. The chip is also designed for flip-chip mounting on the FERMI microsystem module.

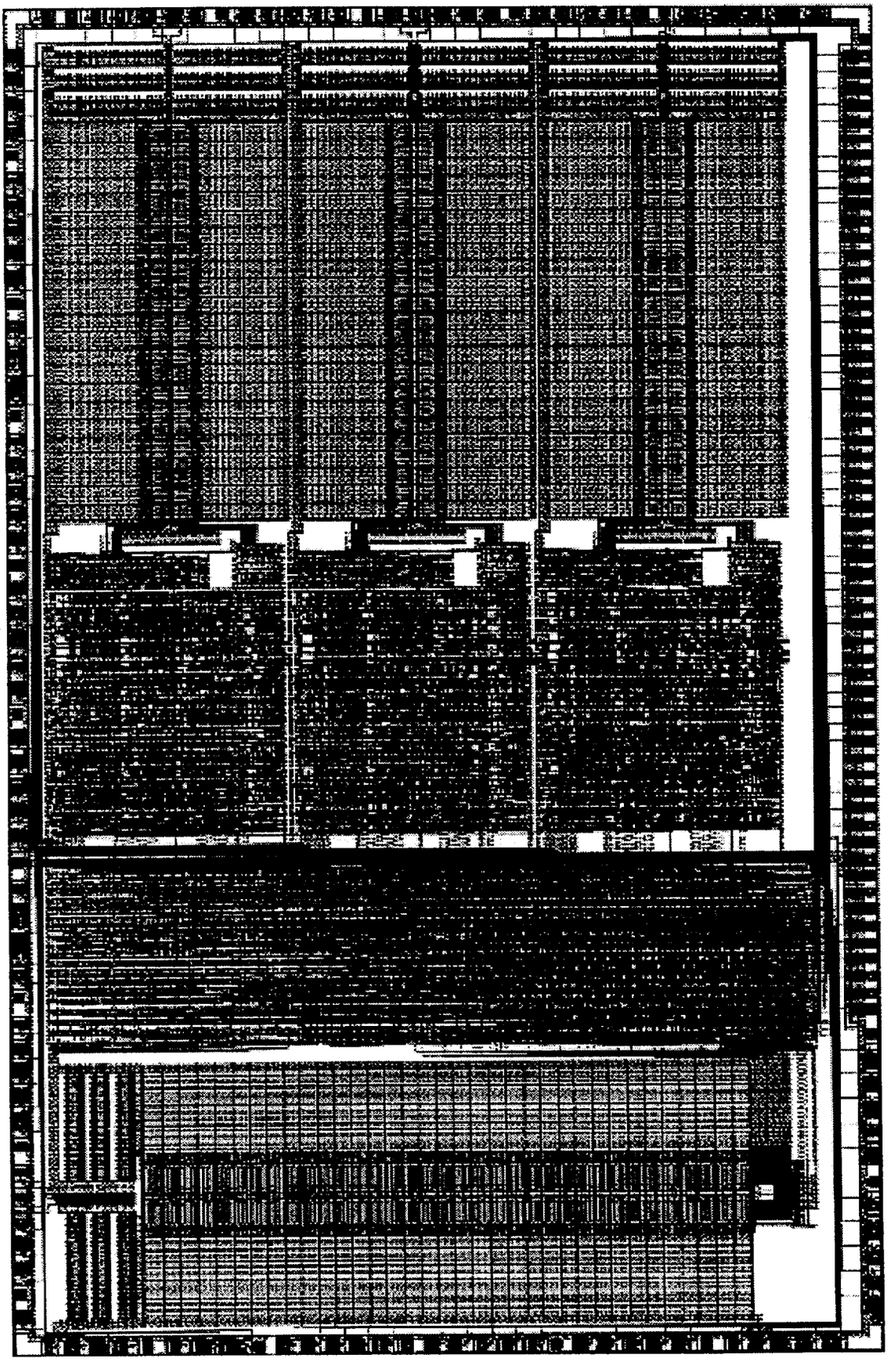


Fig. 4.2. Layout of the Channel ASIC.

5. The Service ASIC

5.1 Basic architecture

The Service ASIC serves all channels. It contains data extraction circuits, providing energy and time information to the first-level trigger, digital filters to process data to the second-level trigger and a readout controller. Also, it contains a programmable Local Micro-Controller (LMC) to manage initialisation, calibration and monitoring of the FERMI system, along with a clock manager and a test pulse generator (see Fig. 5.1).

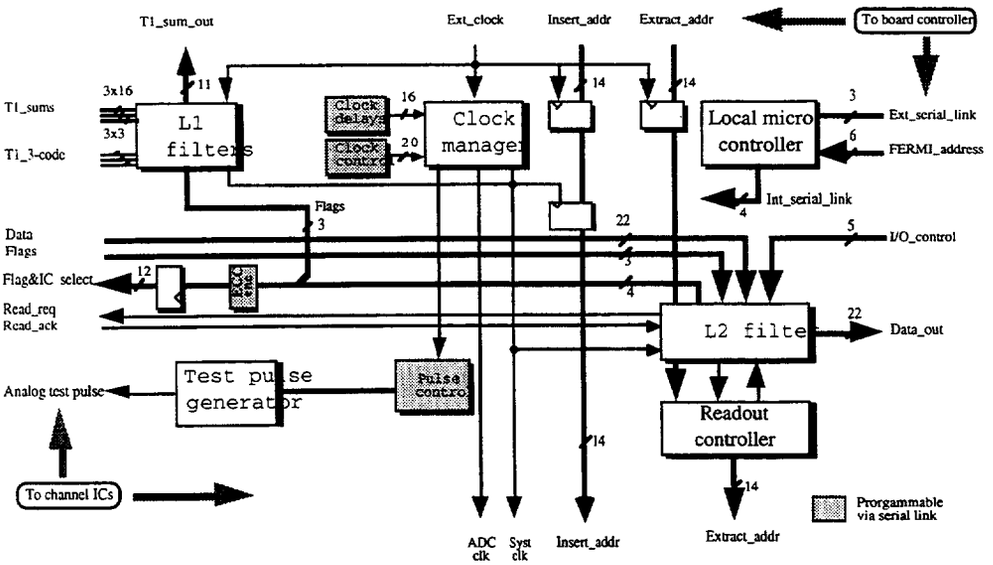


Fig. 5.1. Block diagram of Service ASIC

This chip gathers several circuits which are very different in terms of technology and functions. Some are analog, such as the timing unit in the clock manager which is based on a PLL circuit, and the test pulse generator, whereas others are digital devices such as the Filters, the LMC or the Readout Controller.

Clock Manager

The clock manager is a timing unit which ensures the synchronisation of all the FERMI modules and relates it to the overall external environment. It receives the clock from the FERMI Board Controller (FBC) and control information, stored in five 16-bit registers, through the FERMI serial link. It distributes the timing to:

- the ADC for synchronous sampling of the detector signals,
- the digital readout circuitry such as Look up tables, memory write/read controls, trigger filters, local controllers,
- the calibration pulse generator,
- a circuit generating bursts of pulses for test and calibration.

The delay generator is built around a Voltage Controlled Ring Oscillator, made of 16 differential stages, phase locked to a clock reference. It outputs 16 phases, each delayed by 1/32 of the clock period. For 80 MHz operation, this synchronised coarse delay is 390 ps. An asynchronous fine delay tunes it in steps of 98 ps. Thus, a 7-bit delay word is used. For 40 MHz operation, the coarse delay step is 780 ps, and an 8-bit delay word gets the same 98 ps accuracy.

There are two independent delays, one for sampling, the other for the calibration pulses. The time constant of the Phase Lock Loop is controlled by a low pass filter, whose minimum values are set internally, and can be increased using an external capacitor. Phase lock can be achieved between 25 and 110 MHz.

Test Pulse Generator

The monitoring of the FERMI module, required by the complexity of the system and for fault tolerance purposes, is achieved with a test pulse generator located on the Service ASIC. This device generates a pulse similar to the one from the detector covering a wide dynamic range and adding no perturbation in terms of noise and crosstalk. The complete monitoring system consists of:

- a pulse generator, partly external and partly internal to the FERMI module,
- an injection system, located on the Analog ASIC,
- a set of write- and read- registers and of multiplexers, located at various crucial places of the digital part and,
- a LMC co-ordinating the various actions of the system.

Local Micro Controller

A FERMI microsystem contains 137 programmable registers which could be grouped in three classes. Those in the first class check the operation of each element of the system. The second set loads the different constant values of the system, for example, the filter parameters, the threshold for first-level trigger, the timing and the pipeline memory length. The third one handles the monitoring of the system.

The Local Micro Controller (LMC) has been designed to perform these tasks. It is a custom circuit built around a 16-bit CPU embedded in the Service ASIC. On one side, it is connected, as a slave, to the FERMI Board Controller (FBC) with a serial link (External Serial Protocol). On the other side, it is connected as a master to the four digital ASICs on the FERMI module with another serial link (Internal Serial Protocol). All the serial protocols are clocked synchronously at 10 MHz.

The external protocol consists of a global address field (14-bit), a local address field (12-bit) and a variable-length data field. The internal protocol is similar to the external one but without the external address field. Each address field is protected by Error Correction Codes (Hamming type), allowing to correct one-bit error and to detect two-bit errors. Usually, the FBC loads a task into the LMC memory, which, then executes it. There is also a backup mode, where the FBC controls directly the ASICs, bypassing the LMC.

From the software point of view, an assembly language has been developed with powerful specific instructions (for example, waiting on a flag, reading the serial link, storing in memory, counter decrement in one instruction).

Readout controller

This part contains the circuitry required to read an event from the data memory and present it on the external ports of FERMI. Each event is stored as a time frame in the memory and it can be presented on the outputs either in the form of one value per channel, processed by the second-level filter (see below), or as a sequence of unprocessed data.

Apart from the readout circuitry, this unit also contains status registers that collect all error signals generated on the Service ASIC, one for fatal errors and one for non-fatal errors, each with a mask register so that individual error bits can be disabled. Errors are reported to the LMC through interrupt signals, one for each status register.

For each event a set of flags are also stored in memory, two pile-up flags and one pulse-detect flag. Because these flags are generated by the first-level filter after data has been stored in the memory, the flags corresponding to an event will not be stored together with the data in the time frame. Therefore, a pointer is provided to select the flag word. The flags are read first so that they can be used by the second-level filter (see below) and also presented to the output.

A group of FERMI systems on a board are read out using a daisy chain scheme. The readout chains can be of different lengths (up to 64 FERMI systems), the FERMI systems can be read in any order and faulty modules can be excluded from the sequence by setting their sequence numbers to zero.

5.2 Digital filters

The feature extraction functions of FERMI consist of two different digital filter stages. The structure of the filters to be implemented in the first FERMI prototype was chosen after a systematic evaluation of more than twenty different architectures [6].

Filter 1 is designed to identify a signal, providing accurate timing information and energy information for the first-level trigger unit. It operates on the sum of nine FERMI channels, while the individual channel data are stored in the data memory. These data are later transferred to filter 2 if validated by the first-level trigger unit.

Filter 2 is designed to extract a value of the energy with the highest precision allowed by the set-up and the experimental conditions. It takes as input the time frame data and an overlap flag for each individual signal. The overlap flag indicates that the distance between two consecutive signals is shorter than a given number of clock periods. If required, the whole time frame data can be read out without performing the filter 2 processing.

Filter 1

Filter 1 consists of two parallel finite impulse response (FIR) filters, each with five elementary stages (plus one for redundancy), and a three-point maximum finder (Fig. 5.2). Input data, after summation of nine channels, is 14 bits wide (120 MeV to 2 TeV), the coefficients are 8 bits wide and the output is 17 bits wide (before thresholding and peak detection). The energy extraction FIR is optimised to extract the energy in the presence of several artefacts. Typically it is an *averaging* operator with a relatively wide response on pulses in the time domain to suppress electronics noise and sample timing jitter. The timing extraction FIR has a different optimisation strategy: it produces a sharp maximum for each pulse even if it partially overlaps with another one. This subfilter is close to a *deconvolution* operator which has a narrow response in the time domain and a lower amplitude resolution due to the higher noise gain. Because of the sample timing jitter, the deconvolution operator has to be combined with the maximum finder, as the sharpness of the response deteriorates with changing sampling position.

Filter 1 provides the first-level trigger process with error-free 11-bit data (250 MeV to 500 GeV), and the Channel ASICs with three flags, i.e. peak detection and two different pile-up flags.

The actual coefficient optimisation strategy is based on analytical calculations or a training method. The analytical solution is equivalent to matched FIR filtering, also known as optimal filtering in HEP literature [7]. The alternative strategy, design by training [8], corresponds to the design process of artificial neural networks. The filter coefficients are obtained by minimising the mean squared error (MSE) between the desired output and the filter output. The optimisation is performed using a conjugate gradient algorithm.

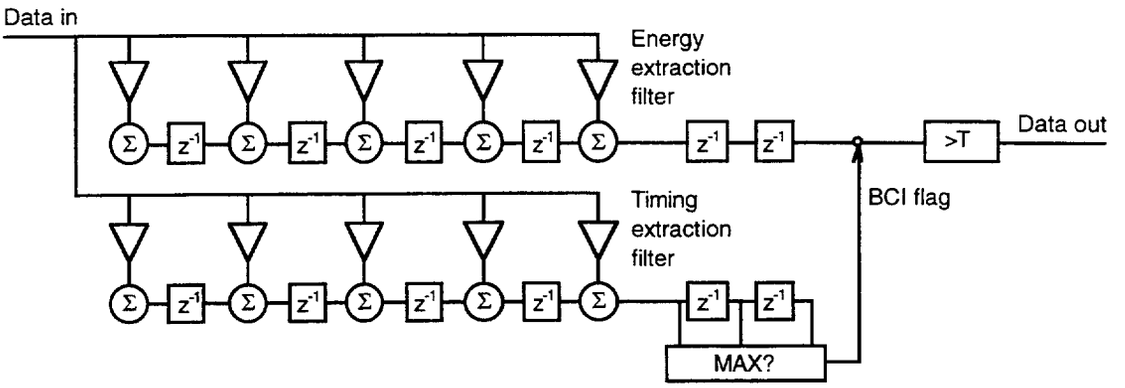


Fig. 5.2. Filter 1 architecture

The performance of filter 1 was evaluated using simulated LAr calorimeter signals. The sequence contains sample timing jitter with 2 ns rms value, and electronics noise with 70 MeV rms. The amplitude resolution representing the system response measured at the output of filter 1 is illustrated in Fig. 5.3. It matches the resolution of a calorimeter with a scaling term of 0.10 and a constant term of 0.01. The timing extraction filter produces correct results for all signal above 2 GeV.

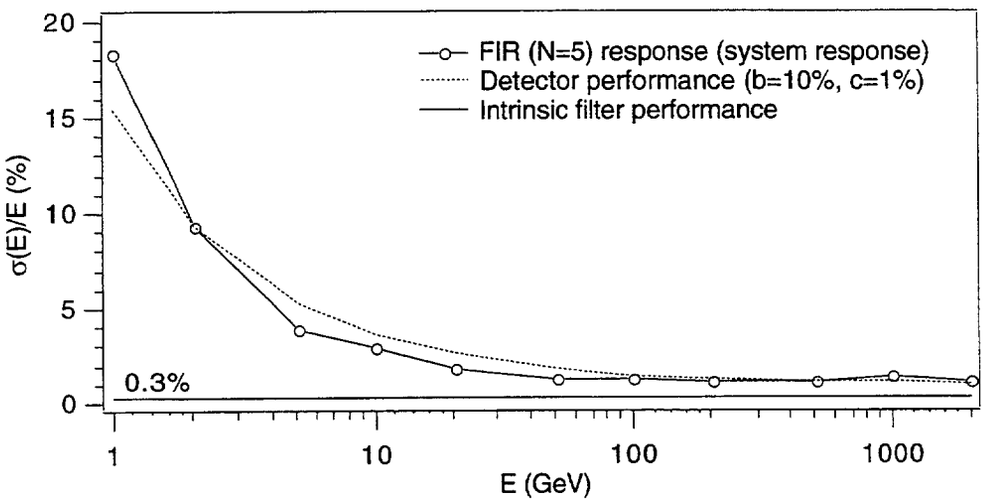


Fig. 5.3. System response at the filter 1 output: amplitude error versus energy. Noise, jitter and pileup are included.

The filter structure is implemented using a register transfer level (RTL) VHDL description of the architecture. A sample-parallel architecture is used for speed optimisation. The FIR filters are realised with the delay elements at the outputs of the adder units: this makes it easy to include fine-grain fault tolerance by bypassing the faulty filter taps.

A modulo-three error detection scheme is used to indicate the presence of a faulty multiplier-adder, in which case the monitor system locates the unit and activates the bypass switch. The timing extraction part is followed by a three-point maximum finder based on parallel comparator units. The output of the timing filter enables the output of the energy filter in positions where the filter output has its maximum value. As an alternative approach, a hand-optimised multiplier with the tap coefficients stored in a modified Booth encoded format is being evaluated. This filter can be implemented in the next FERMI prototype, to further reduce the silicon area and to improve its fault-tolerance. The basic structure of this unit is illustrated in Fig. 5.4. The latency of this system is only 2 clock periods. The total latency for the first-level feature extraction is, what concerns the Service ASIC, 8 clock periods

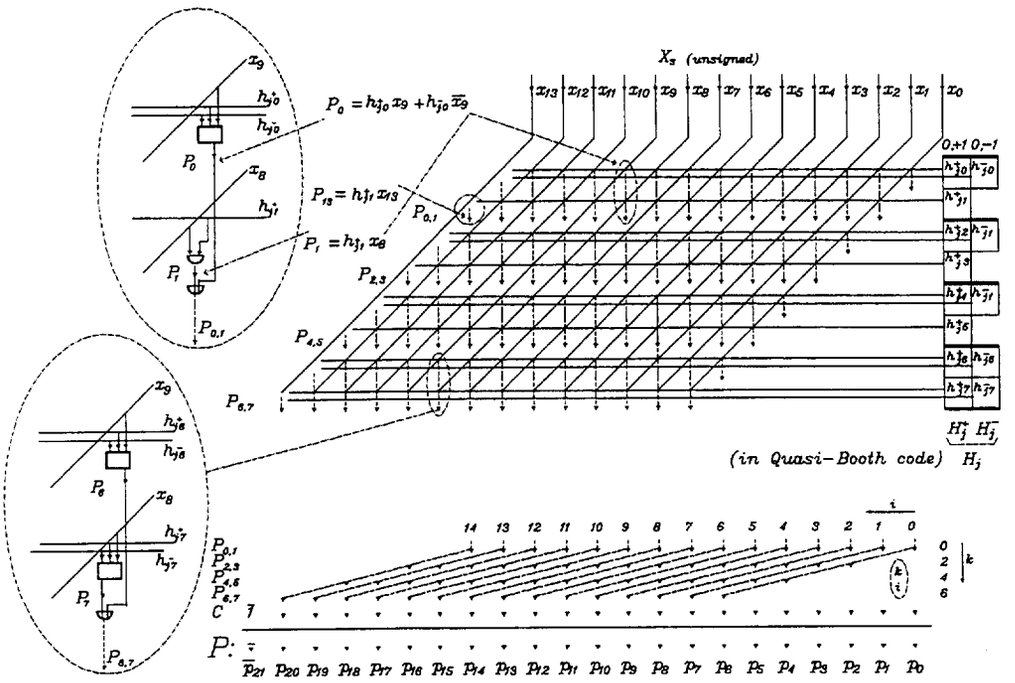


Fig. 5.4. Optimised filter 1 multiplier unit with Booth encoded coefficients

Although the filter structure described above offers already an acceptable performance for first-level triggering purposes, a structural modification is being tested. This structure resembles filter 2, containing an order statistic (OS) operator and two FIR subfilters. The FIR-OS filter performance is compared to the performance of separate FIR filters with different optimisation criteria in Fig. 5.5. The lowest solid line (close to the x-axis) shows the intrinsic performance of the filter without noise and jitter. The FIR filters with a narrow response on pulses, e.g. the 3-point deconvolution, perform well in the low-energy region where pile-up noise and overlapping pulses are the dominant source of error. However, to obtain a good precision in the high-energy region a relatively wide response is required to suppress the effect of sample timing jitter. The FIR-OS filter effectively combines the good amplitude precision and the high time resolution, thus producing an accurate signal amplitude determination over the whole energy range.

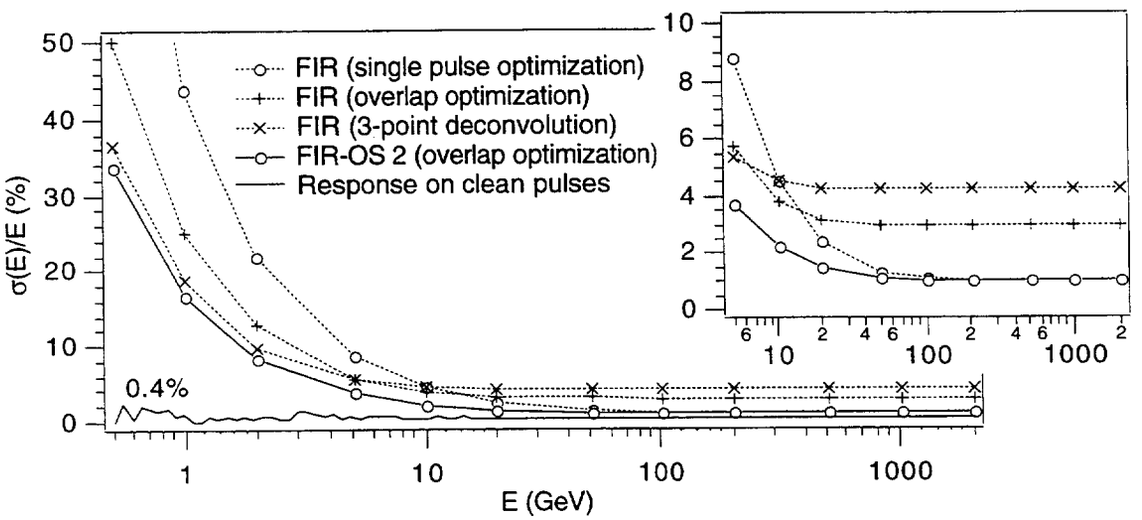


Fig. 5.5. System response at the filter 1 output with overlapping large pulses. Noise, jitter, pileup are included.

Filter 2

Filter 2 is designed to measure the signal amplitude with very high precision using the time frames identified by the first-level trigger. The architecture of filter 2 is based on three sample-serial multiplier-adder units. The number of bits in the input data is 16 and the number of bits in the FIR tap coefficients is 10. All time frames from the nine channels are processed using the same filter. Filter 2 is implemented using a layout generated from the low-level VHDL description.

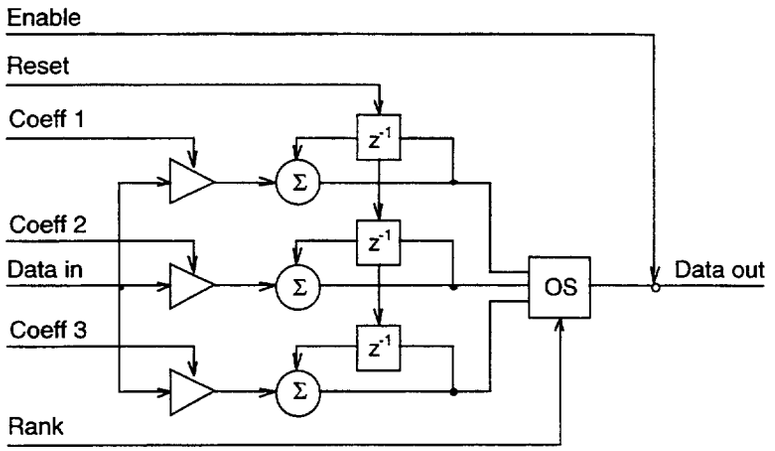


Fig. 5.6. Filter 2 architecture

Two sets of coefficients can be used: one for single pulses and another for overlapping pulses. In special cases (e.g. when a very severe pulse overlapping is detected) the whole time frame can be read out. Filter 2 contains three parallel FIR filters and an OS operator (Fig. 5.6). The filter coefficients and the OS rank value are found using design by training, as the non-linear filter structure is difficult to optimise using analytical methods. The FIR-OS filter structure [9] offers more *degrees of freedom* against the different artefacts present in the acquired sequences, compared to a single FIR filter. It also offers an efficient fault tolerant architecture: if a FIR unit becomes faulty it is switched off from the system, thus degrading gently the number of subfilters and the total performance.

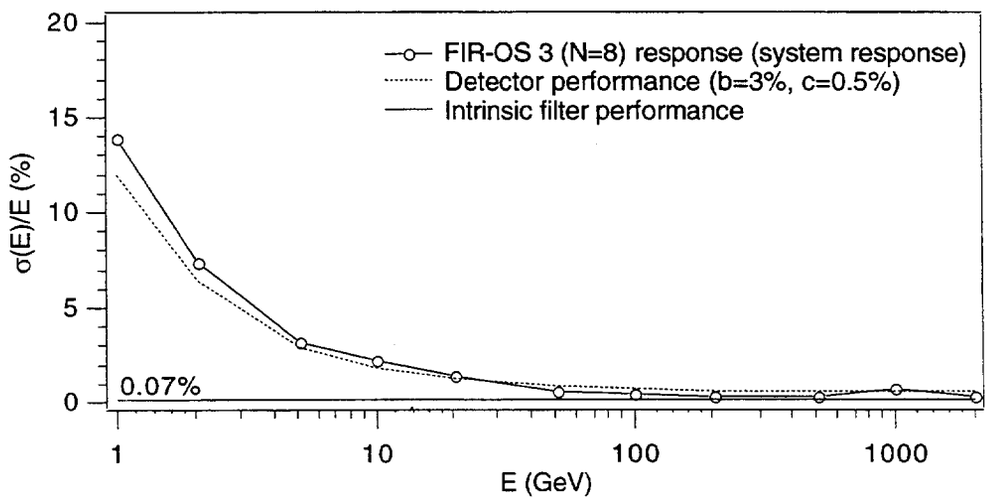


Fig. 5.7. System response at the filter 2 output: amplitude error versus energy. Noise, jitter, pileup are included.

The performance of filter 2 was evaluated using the simulated detector sequence described in the previous section. The system response measured at the output of the filter is again illustrated in Fig. 5.7. The small deviation around 1000 GeV is supposed to be due to the non-linear amplifier. The FIR-OS structure offers a good robustness against several artefacts. It is even able to produce a fairly accurate output in the case of pulse overlaps not detected by filter 1. The performance for single pulses matches a detector resolution with a scaling term of 0.03 and a constant term of 0.005.

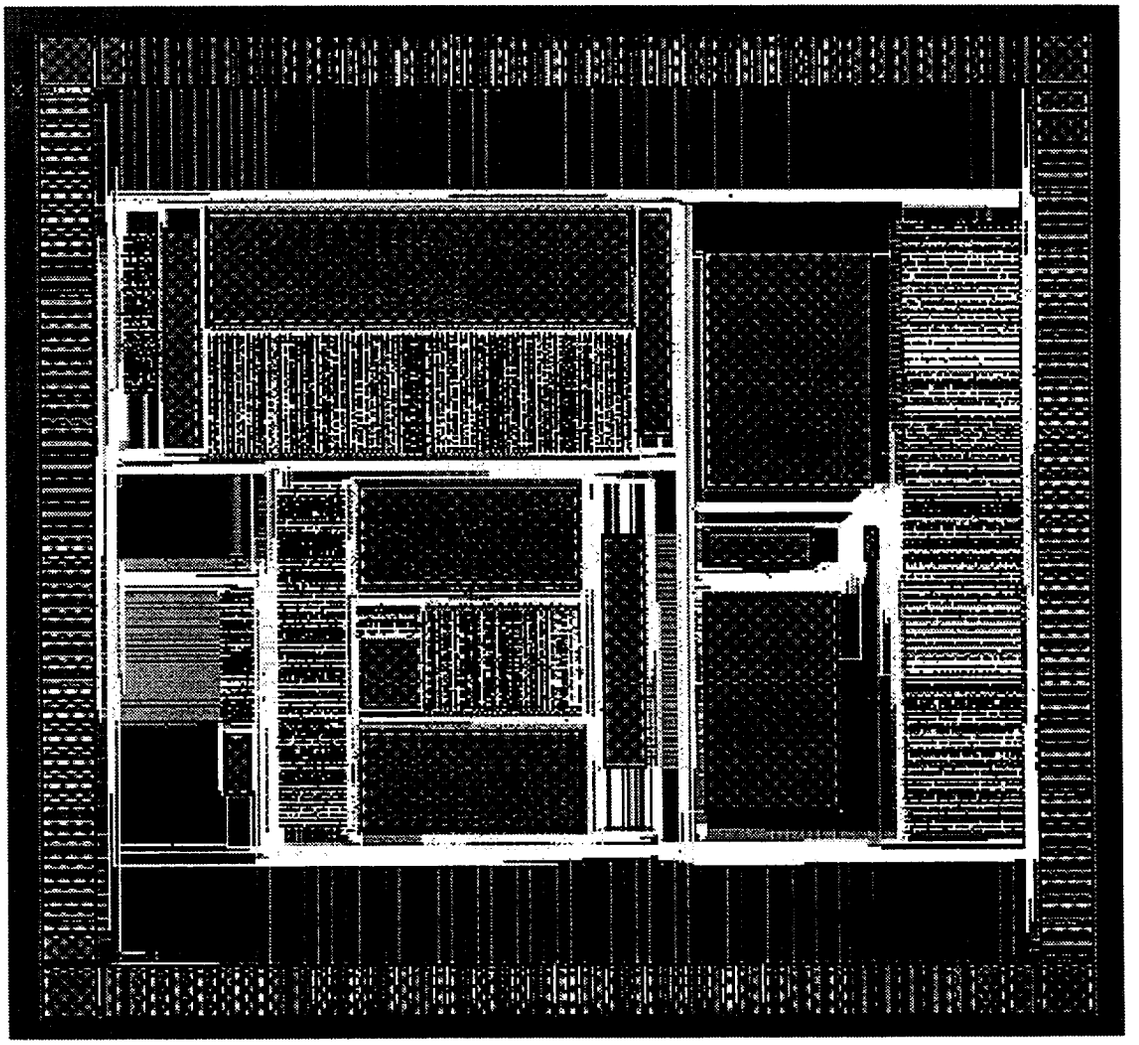


Fig. 5.8. Layout of the Service ASIC

5.3 Layout and simulation

The digital part of the Service ASIC has been developed using the VHDL language. A complete set of CAD ASIC design tools were used to proceed from the top level VHDL description to the implementation on silicon.

The full layout of the Service ASIC, including both the digital and the analog circuits, is shown in Fig. 5.8. It consists of four parts: the PLL timing unit and its associated register, the LMC, the Filters 1 and 2 and the Readout controller. Still missing in this version is the self test pulse circuit, which exists in a discrete version and will be implemented in the next version.

The total size of the chip is 150 mm^2, of which 20 mm^2 for the PLL timing unit, 30 mm^2 for the LMC, 50 mm^2 for the filters and 50 mm^2 for the readout controller. The technology chosen for this prototype run is ES2 0.7 μm CMOS process except for the timing unit, where the ES2 1.0 μm CMOS process is used.

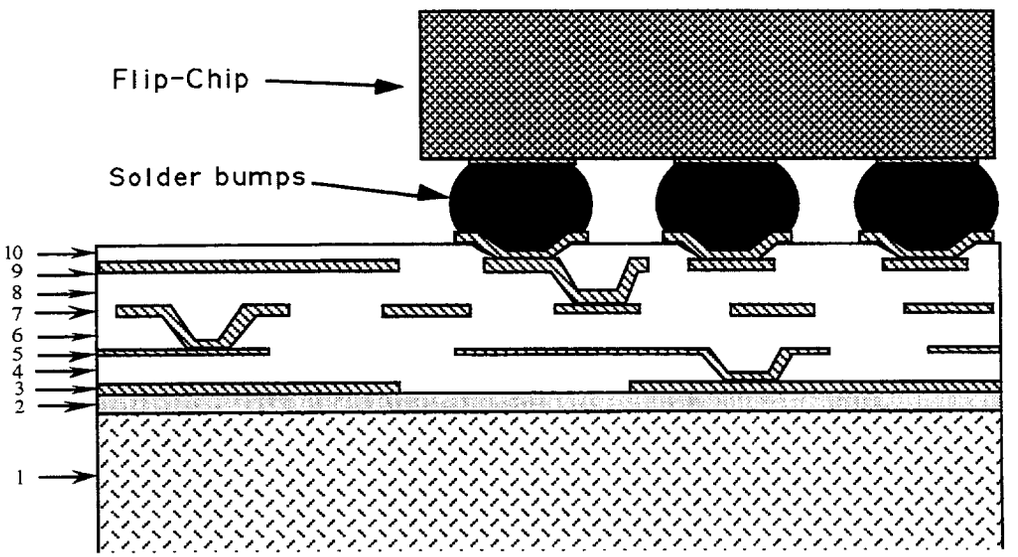
5.4 Production

The Service ASIC will be submitted for production by the end of May. The prototype ASICs will be first tested then encapsulated by the founder, as four different chips (Filters, LMC, Readout controller and PLL timing unit).

The next version of the Service ASIC will be integrated into a single chip.

6. The Microsystem

The FERMI microsystem is implemented as a thin-film Multi-Chip Module (MCM-D) on a silicon substrate with four metal layers. All ASICs are flip-chip bonded to the substrate, which can contain integrated resistors and capacitors. A cross-section of the process is shown in Fig. 6.1 [10].



(1) Si; (2) SiO2; (3) Al (metal 1); (4) BCB1; (50 Al (metal 2); (6) BCB2; (7) Al (metal 3); (8) BCB3; (9) Al (metal 4); (10) BCB4 (passivation).

Fig. 6.1. Cross-section of the microsystem module.

6.1 Design considerations

Noise

In order to reduce noise coupling between the analog and the digital circuits, both the power and the ground planes for the two parts are split in the MCM. The analog part has two power supplies, 5 and 12V, and the digital part has one power supply, 5V. Furthermore, in the analog part signal lines are completely surrounded by ground.

The noise originating from switching currents on the power supply lines has been computed and simulated according to a detailed model of the electrical parameters of the

microsystem and of its layout. The driving capability of the ASIC output pads and the number of power supply connections have been optimised accordingly.

Crosstalk

The coupling coefficients in the FERMI module were computed through a detailed numerical simulation of the entire structure. In this work, the wire-bond length and diameter are assumed to be 1.5 mm and 25 μm, respectively. The flip-chip bump size is assumed to be 100 μm.

The wire-bonds give the greatest contribution to crosstalk; more than two ground/power bonds should be placed between signal bonds in order to obtain a coupling coefficient of less than -30 dB. Replacing wire-bonding with flip-chip bonding reduces cross-talk drastically; a 210 μm pitch results in a coupling coefficient of -40 dB and an impedance of 42 Ω. Traces in the final FERMI substrate will have a coupling coefficient of less than -80 dB.

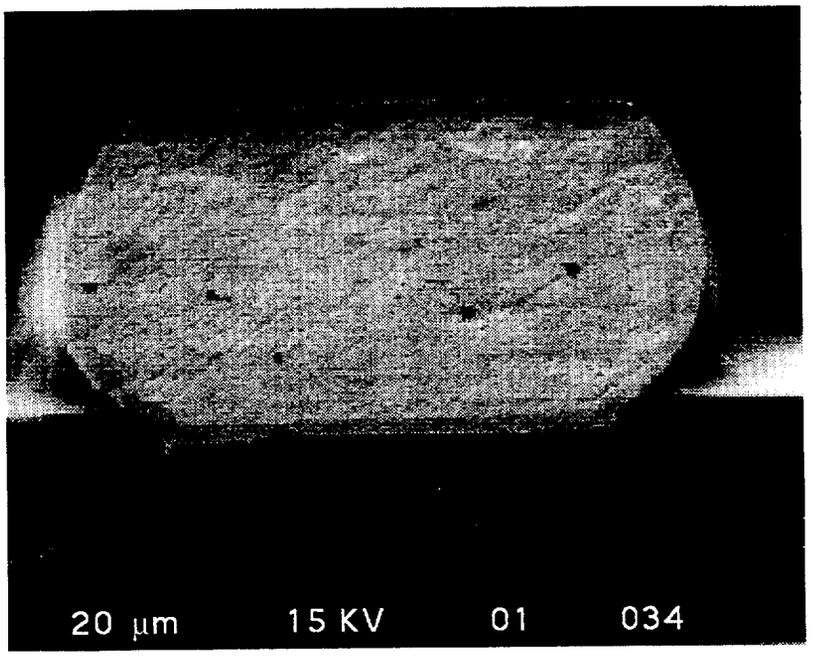


Fig. 6.2. Detail of one bump at the substrate-ASIC interconnection

6.2 Flip-Chip bonding technology

All the FERMI ASICs will be mounted with flip-chip bonding, as shown in Fig. 6.1. This technique is more performant and reliable that conventional wire-bonding. In addition, it allows connecting pads to be optimally placed across the surface of the chip.

The parasitics associated with a solder bump are much smaller than with a wire-bond. For instance, a solder bump with a 100 μm diameter has an inductance of < 0.1 nH, while a wire-bond with a 25 μm diameter and a 2 mm length has an inductance of 2 nH. This drastic reduction in inductance contributes directly to the reduction in switching noise.

Flip-chip MCM demonstrators, each with a size of 20 x 20 mm, have been fabricated at IMC using ABB HAFO's flip-chip technique. Each of the 7 substrates carried 7 ASICs (6.7 x 2.3 mm) mounted with Sn:Pb = 60:40 solder bumps, for a total of 4508 bumps. A detail of a bump is shown in the microphotograph in Fig. 6.2. The

electrical continuity of all these connections was tested after thermal cycling between -55 °C and +125 °C for 100 cycles. No failure was detected [11].

6.3 Layout and production

Fig. 6.3 shows the preliminary floorplan of the FERMI microsystem. The placing of the nine Analog ASICs, of the three Channel ASICs and of the Service ASIC are shown together with decoupling capacitors. The microsystem has an area of 50 x 50 mm^2 and 200 external I/O connections. The internal I/O count is excess of 1500.

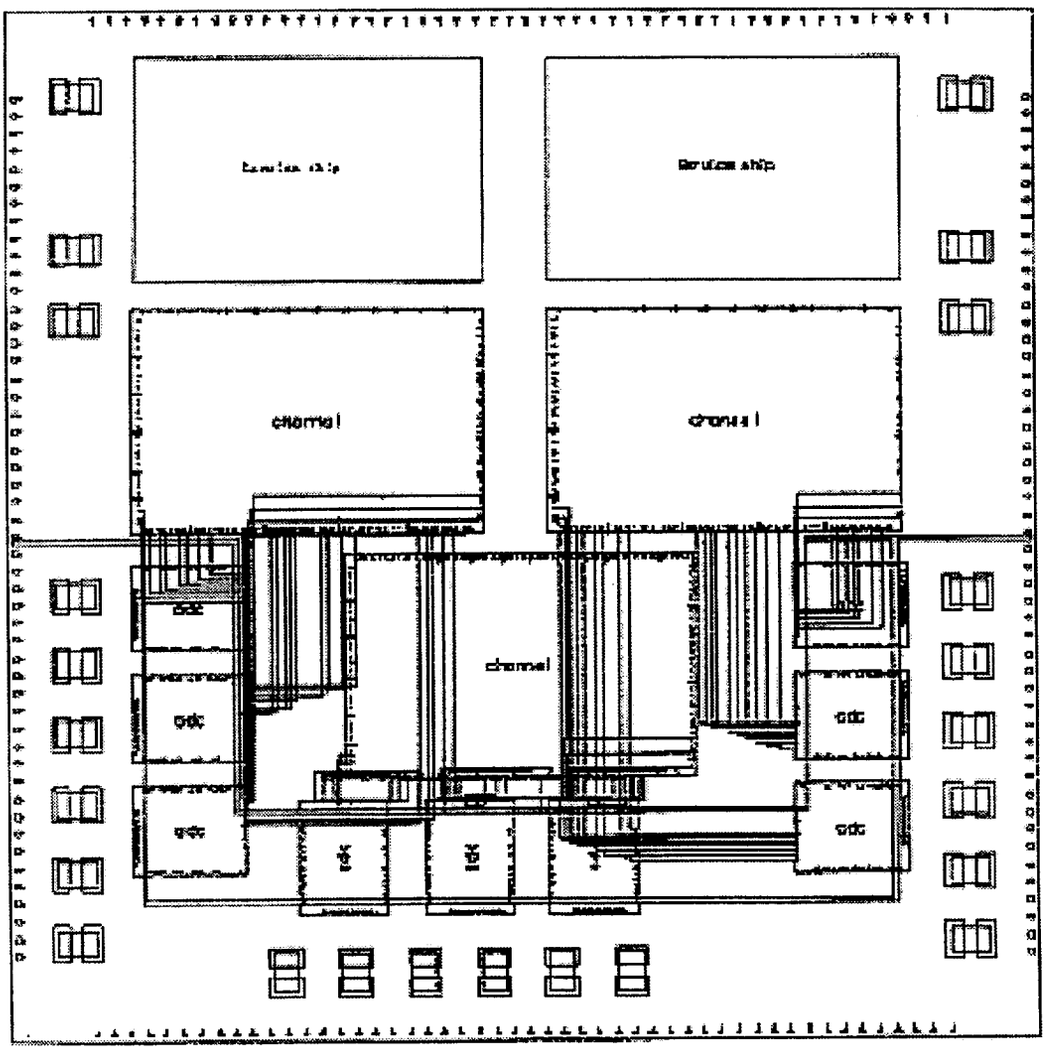


Fig. 6.3. Preliminary layout for the FERMI microsystem.

A number of packaging options are available for the FERMI microsystem. Irradiation studies on various package types have shown that a plastic package should be preferred for the final solution. For the prototypes, however, a readily available 200 pin PGA ceramic package will be used, in spite of the fact that these packages are not optimised for cross-talk, switching noise and radiation effects.

The microsystem substrate for the demonstrator will be produced in summer 1994.

7. Test and evaluation

7.1 Analog ASIC measurements

Linearity

The differential and integral nonlinearities (DNL and INL) of the PSA-ADC have been evaluated using sine waves at different frequencies.

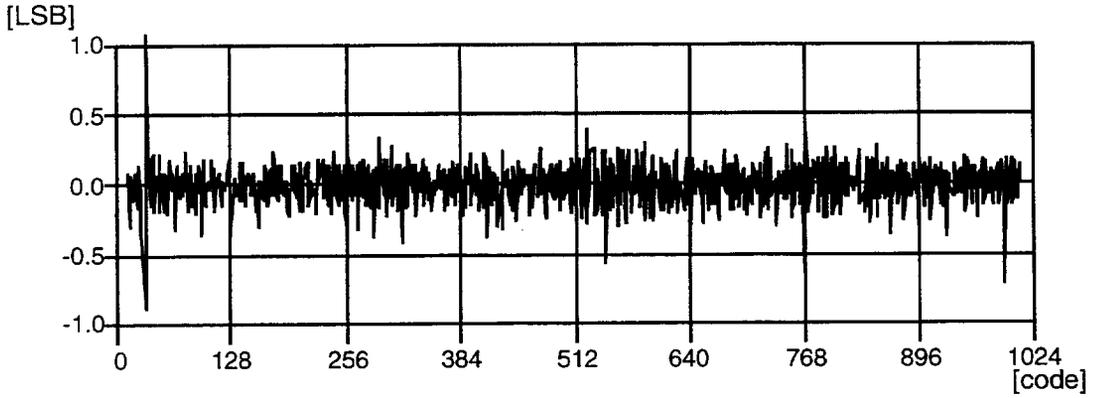


Fig. 7.1. Differential Nonlinearity for a 1.2 MHz sine wave at 40 MHz sampling rate.

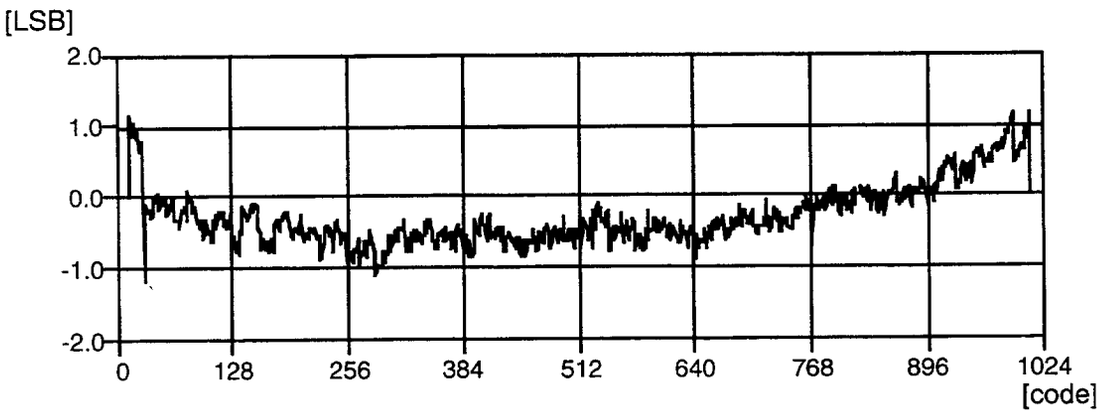


Fig. 7.2. Integral Nonlinearity for the same data as above.

As shown in Figs 7.1. and 7.2., the linearity is generally very good, with a DNL r.m.s. of 0.13 LSB and an INL of at most ±1 LSB. The only exception is at codes 31-32 and at code 991, where the differential nonlinearity reaches its peak values. The reason is the difficulty of matching the fine and the coarse reference ladders at the ends of the range. However, no missing codes are detected. From this point of view, a full 10 bit resolution is achieved at 40 MS/s.

Transient response

Fig. 7.3 shows the response to a very fast changing input signal (t_r, $t_f < 2$ ns, ampl. 0 - 1.6 V). The result shows that the analog part of the converter has sufficient bandwidth.

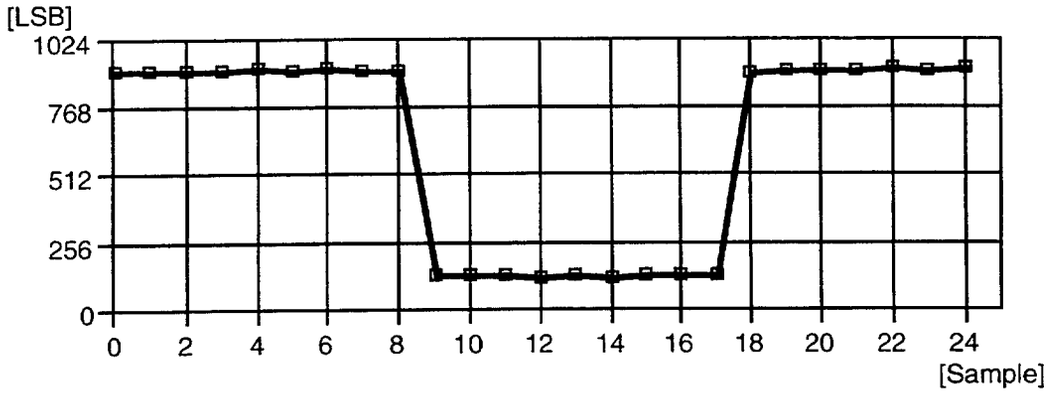


Fig. 7.3. Transient response of the ADC

Resolution

In the FFT power spectrum of a digitised sine wave all systematic errors show up as peaks, and random errors as an elevated "floor".

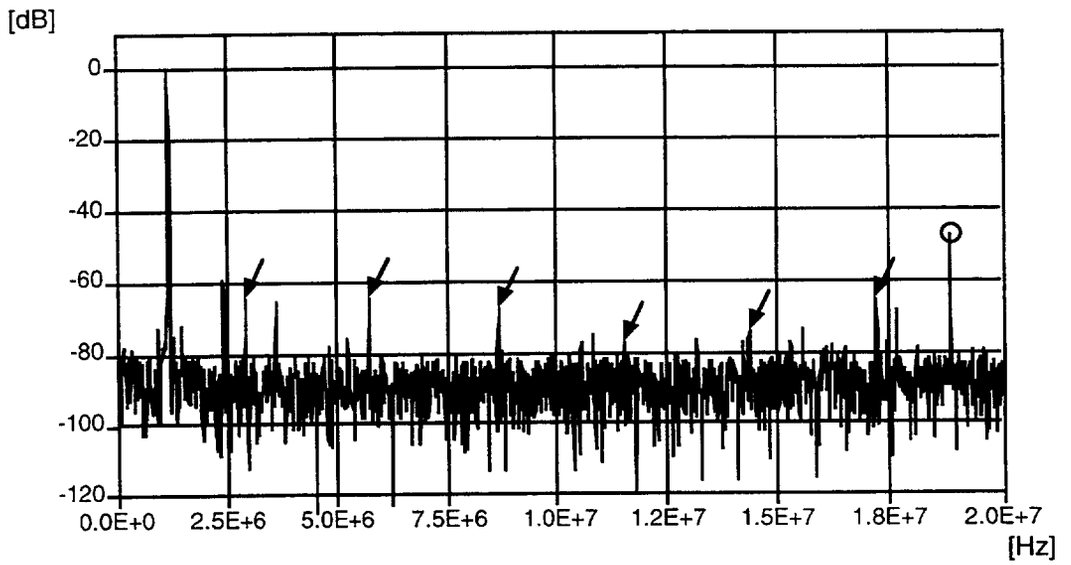


Fig. 7.4. Power spectrum for the PSA-ADC with a 1.2 MHz sine wave at 40 MHz sampling rate.

As shown in Fig. 7.4, the stand alone PSA-ADC prototype still has two anomalies, i.e. the six peaks marked with arrows and the one marked with a circle.

The ADC consists of by 14 parallel SA-ADCs, among which differences can occur. By applying a DC level on the input and splitting the samples in 14 sets (one for each internal ADC), the systematic offset difference was measured by taking the mean for each internal ADC. At 40 MHz sampling rate these errors are very small, but become visible at 60 MHz. By comparing the power spectra, the reason for the arrowed peaks in Fig. 7.4 is understood. It is arises simply from systematic offsets between the 14 internal ADCs. In order to get rid of, or at least reduce, this effect, the Analog ASIC version of the PSA-ADC has a true differential input to the sample-and-hold circuits.

By applying a sine wave on the input and splitting the samples in 14 sets, the properties for the internal ADCs can be investigated. The conclusion is that all the odd channels are sampling late, and the even channels early. This explains the peak marked with a ring, which is the most significant noise contributor. The explanation for this error is, again, to be found in the old layout of the ADC ASIC.

As seen in Fig. 3.3 (Analog ASIC layout plot), the internal SA-ADCs are grouped two by two. The two SA-ADCs in a group are mirror images, and share some circuitry. They also share an external power pad. Since they are sampled just after each other, the two ADCs in a group may not see the same environment, i.e. different delays may be the result. In order to reduce these effect, the last version of the PSA-ADC in the Analog ASIC has all the power supply pads connected internally. In future versions, the SA-ADCs may, if required, be laid out individually.

7.2 Tests of the digital ASICs

In a first stage the digital ASICs will be installed on individual VME boards and exercised by the FERMI test bench. The test vectors will be generated from the respective VHDL high level descriptions of the ASICs.

In a first stage the LMC will be installed on a VME-board and the external serial link will be emulated through a register. It will be possible in this way to download programs and verify through a simple VME set-up the operation of the LMC. The output of the LMC will also be sent to the Channel ASIC or back to the test system. The critical parameters to be checked are, among others, the absolute delay values and the phase jitter in the clock manager, the execution of instructions in the LMC, the function of the current voting circuits, etc.

The filters will be checked in two ways. Firstly, the VHDL description will be used to emulate them with files of true data from beam tests as input (see Sect. 7.3). Secondly, the actual filters will be checked "off-line" in the test bench on files of true data. The results of both approaches will then be compared.

Finally, the operation of the digital ASICs, including the communications between their different sections and the external world, will be tested using the VHDL system modelling facilities.

7.3 Beam tests

A series of beam tests are scheduled during 1994 and 1995. This activity is a natural continuation of the work ongoing since about three years in the laboratory. The main aim in 1994 is to test both the Analog and the Channel ASICs, focusing on the compressor and the A/D converter. Five test periods are foreseen. In the first two periods, only a few channels will be tested with both the LAr and the tile calorimeter prototypes of the ATLAS Collaboration. In the next three periods, it is foreseen to test one hundred channels of the e.m. calorimetry, sufficient to fully contain an electron shower of about 150 GeV. Also, plans for beam tests of FERMI on other types of calorimeters are being prepared together with the CMS Collaboration.

Interfacing FERMI with the detectors

Suitable circuits for interfacing FERMI to existing front-ends are being developed in collaboration with the appropriate groups and R/D projects. Provisions are being made in order to exercise the full dynamic range by controlling signal levels, resolutions and noise across an equivalent LHC energy range. The noise issues will be carefully tested in the real life environment of a test beam.

The FERMI VME-boards.

In order to let the test beam set-up evolve with the FERMI prototypes, in particular with the production of the various FERMI ASICs, a VME-board including subsets of FERMI has been developed. A mother board containing three Analog ASICs and

provisions for different daughter boards has been produced. For the latter three alternatives exist: one with a direct output to a FDPM and a sequencer VME-card (for a few channels only); a second one with FIFOs (two per Analog ASIC) and a VME interface, and a third one including the Channel ASIC and the VME interface.

The FERMI DAQ system

The data read out through the FERMI chain will be directly accessible to the standard data acquisition system installed on the H8 test beam facility. Moreover, an independent FERMI data acquisition, based on the SPIDER OS/9 system, is set-up in parallel according to the scheme of Fig. 7.5, in order to monitor and control the system under test without interfering with the normal running.

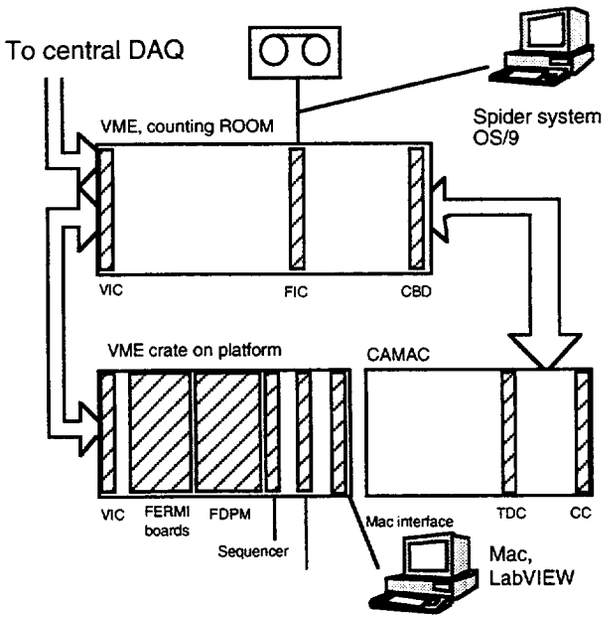


Fig. 7.5. Layout of the FERMI-DAQ system in the H8 beam test

For calibration purposes, two independent systems will be used. First, the existing set-up of the RD3 Collaboration will be used, also in order to refer our results to the ones of the RD3 standard readout chain. In addition, the FERMI system will be monitored using a self-test pulse facility.

8. Irradiation studies

In order to obtain rad-hard reference data for the subsequent investigation of the digital FERMI subsystems, five commercial memory circuits were tested under gamma and neutron irradiation at the Nuclear Research Laboratory, ATOMKI, at Debrecen, Hungary [12, 13]. Both radiation hardened RAMs and standard bulk CMOS memories were used. The RAM ICs were irradiated by a ^{60}Co gamma source (dose rate approximately 200 kRad/day) and by neutrons (2.6×10^8 neutrons/cm^{2}sec, average neutron energy of 3.7 MeV and maximal intensity at 1 MeV).

There are two sources of storage errors in memories, those arising from a temporary change of state and those arising from structural damage, calling for two types of tests. In a dynamic storage test, the content of every cell is read back immediately (<100 ms), i. e. a minimal chance is given to the radiation to modify the content of the cell. The errors detected are caused by the total dose absorbed. In the other measurement,

the static storage test, the information is held in the memory for approximately 1 minute, and subsequently read back and compared to the original information. Fig. 8.1 shows a typical example of the results. It should be noted that no errors have been detected for the HARRIS 64k x 1 bit and 16k x 1 bit ABB HAFO SOS5 memories respectively, which might therefore suggest candidate technologies for the FERMI system.

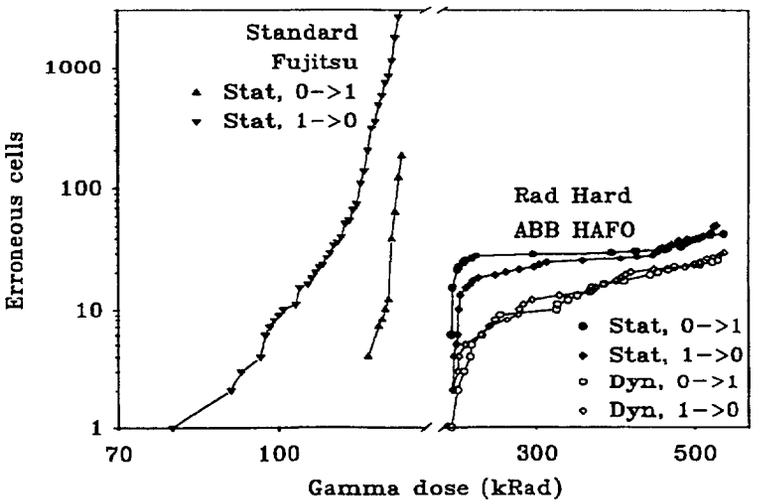


Fig. 8.1. Number of erroneous cells as function of gamma dose.

Other ionising radiation might also have to be taken into account. Heavy particles might damage the crystal structure and alter the circuit properties by modifying the state or the performance of logical circuits. In order to study these effects, the FERMI system should therefore also be tested with slow protons and ions. We foresee measurements at the proton beam of the The Svedberg Laboratory, Uppsala, as well as tests at the heavy ion facility of the CRYRING accelerator of the Manne Siegbahn Laboratory, Stockholm.

9. Activities and milestones

We outline in the following the activities required for the full implementation of FERMI. We then describe the short-term work for the completion of the demonstrator project.

In order to bring FERMI to its final application stage, the implementation phase starting in the second half of 1994 will concentrate on the following basic aims:

- completion of ASIC developments and of the microsystem architecture

  (compressor, ADC, filters, complete fault tolerance and rad-hard implementations),
- production of a pre-series of a few hundred microsystems,
- design and implementation of a multichannel FERMI board
  (development of a FERMI Board Controller and a FERMI Remote Controller for address generation, monitoring, calibration and protocol conversion for I/O and readout),
- beam tests on different calorimeter prototypes equipped with full FERMI front-end and readout (in collaboration with ATLAS and CMS),
- full hardware and software integration on LHC detectors.

We indicate below the relevant steps for the development of the FERMI project in the period 1994 - 1995.

Analog ASIC

- **improved version of the Analog ASIC**
- **study of a 11-bit 80 MHz ADC**

Channel ASIC

- **improved version of the Channel ASIC with complete fault tolerance**

Service ASIC

- **improved version of the Service ASIC with complete fault tolerance**
- **study of alternative filter architectures**

Testing

- **upgrading of the test bench to allow test and evaluation of the complete FERMI system**
- implementation of the (self-)test architecture and related software programs
- beam tests on different calorimeter prototypes equipped with full FERMI front-end and readout (in collaboration with ATLAS and CMS).

Irradiation studies

- **In-beam functional tests of the ASICs**
- Memory SEU tests for heavy ionising objects
- Activation studies of the planned flip-chip technique
- FERMI functional tests under irradiation

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