A new data transfer scheme for the HL-LHC upgrade of the ATLAS Tile Hadronic Calorimeter

A Cervelló[1], A Valero[1], F Carrió[1], J Torres[2], J Soret[2] and R García[2] on behalf of the ATLAS Collaboration

[1] Institut de Física Corpuscular (CSIC-UV), catedràtic José Beltran 2, Paterna, València, Spain
[2] Escola Tècnica Superior d'Enginyeria (UV), Av. de la universitat, Burjassot, València, Spain

antonio.cervello@cern.ch

Abstract. The Large Hadron Collider (LHC) is undergoing a series of upgrades towards a High Luminosity LHC (HL-LHC) that will deliver five times the LHC nominal instantaneous luminosity. The ATLAS experiment is one of the experiments at the LHC that investigates elementary particle interactions in collisions of high-energy proton beams. To prepare for data taking in high-luminosity conditions, the ATLAS Tile Hadronic Calorimeter (TileCal) will replace completely on- and off-detector electronics using a new read-out architecture. The TileCal detector signals will be digitized by on-detector electronics and transferred to the TileCal PreProcessors (TilePPr), which comprise the main component of the off-detector electronics. In the TilePPr, the digitized data will be stored in pipeline buffers and be packed and read out to the Front-End LInk eXchange (FELIX) system upon the reception of a trigger decision. FELIX is a new detector readout component being developed as part of the ATLAS upgrade effort. FELIX is designed to act as a data router between the data acquisition detector control and TTC (Timing, Trigger and Control) systems and the new or updated trigger and detector front-end electronics. Whereas previous detector readout implementations relied on diverse custom hardware platforms, the idea behind FELIX is to unify all readout across one well supported and flexible platform.

ATL-TILECAL-PROC-2021-004
21/06/2021

1. Introduction

The Tile Calorimeter (TileCal) is the central section of the hadronic calorimeter of the ATLAS detector at the LHC [1]. It is a sampling detector constructed of steel and scintillating tiles with fibers, and readout by 9852 PhotoMultipliers Tubes (PMTs). In the present system, the PMT signals are digitized with a 40 MHz clock that is synchronous with the beam crossing. The digital samples are stored in pipeline memories during the Level 1 (L1) trigger latency of 2.5 μs. Simultaneously, analog boards sum the PMT pulses into pseudo-projective towers and transmitted to the Level-1 calorimeter trigger system. Events selected by the Level-1 trigger are read out over 256 redundant pairs of optical links to the Read-Out Drivers (RODs) located in the back-end system at a maximum rate of 100 kHz. The optical links in the current system have a line rate of 800 Mbps, providing a data bandwidth of 640 Mbps for readout of up to 48 PMTs each [2].

The HL-LHC is planned to deliver more than ten times the integrated luminosity (3000–4000 fb^{-1}) before the HL upgrade. To achieve this integrated luminosity in a reasonable amount of time, an instantaneous luminosity corresponding to an average of 200 simultaneous pp interactions per bunch crossing is required. This peak luminosity is required, corresponding to 7.5 times the original design value, where there were approximately 25 interactions per bunch crossing.

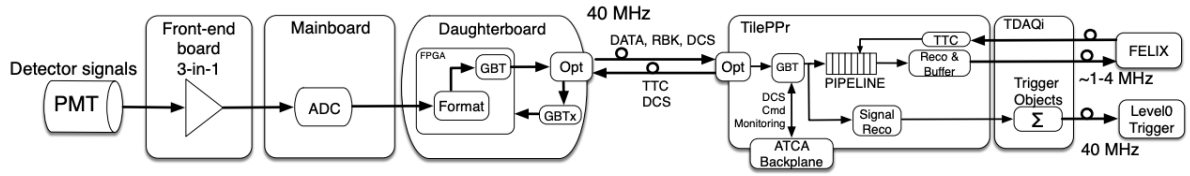

Figure 1. Schematic signal and data path for the upgraded Tile Calorimeter Phase-II [2].

To prepare for the challenges of high-luminosity running, a full replacement of the TileCal on- and off-detector electronics is planned, as shown in Figure 1. In contrast with the present system, all PMT outputs are to be digitized with two gains by pairs of ADCs at 40 MHz on so-called Mainboards. Daughterboards receive and format the ADC data are for transmission off-detector over redundant pairs of fiber optic links at a line rate of 9.6 Gbps. A total of 1792 link pairs will be received by the off-detector TileCal PreProcessor (TilePPr) modules. The PPr will both store the ADC data in digital latency pipeline memories, and produce digital trigger tower sums for transmission to the new Level-0 hardware calorimeter trigger system with ~1.5 us latency. Upon the reception of the Level-0 and/or Level-1 acceptance signal, the reconstructed energy, the time, and a quality factor for each cell will be sent out to the data network for event aggregation and storage [3].

2. New data transfer scheme in the Tile Calorimeter

In the current system, the TileCal ROD reads and processes data from the front-end electronics. The ROD is able to process the data at the Level 1 trigger rate of 100 kHz and send it to the High-Level Trigger (HLT) with reconstructed data.

In the new TileCal system, the TilePPr will process and transmit triggered event data over optical links to the new Front-End Link eXchange (FELIX) system. The FELIX system in turn passes the data to commercial processors, where detector-specific data processing previously implemented in the ROD hardware has been migrated to software (SWROD).

2.1. Front-End LInk eXchange (FELIX)

FELIX will function as a router between custom serial links and a commodity switch network using standard technologies to communicate with commercial data collecting and processing components [4]. The downlink, capable to work up to 4.8 Gbps, shall be implemented using the latency optimized GBT protocol for recovery of the LHC clock with deterministic latency. It will be responsible for the receiving of slow control commands, TTC commands, and the LHC clock. The uplink can transmit at a rate up to 9.6 Gbps in Full Mode and it is used to transmit triggered data to FELIX. This link does not require deterministic latency but demands more data bandwidth depending on the trigger scheme.

The worst-case scenario from point of view of the required total data bandwidth to FELIX is the L0-only scheme, where the PPr must transmit triggered data at 1 MHz. The complete TileCal readout system will include 161 bidirectional links with FELIX where 128 links will be used for data readout, 32 links for trigger primitives monitoring and 1 link for the Laser calibration system.

2.2. Tile Pre-Processor (TilePPr)

The TilePPr module, whose schematic is shown in Figure 2, is the core element of the back-end system. It provides the interface between the front-end electronics and the ATLAS global data acquisition and trigger systems. Each TilePPr module is composed of an ATCA Carrier board equipped with four Compact Processing Modules (CPM) and one Trigger and Data Acquisition interface (TDAQi) in the form of a Rear Transition Module [5]. A total of 32 TilePPr modules are needed to operate the TileCal detector.

The CPM is responsible for distributing the LHC bunch-crossing clock to the detector, configuration of the on-detector electronics, data acquisition, cell energy reconstruction, and data transmission to the

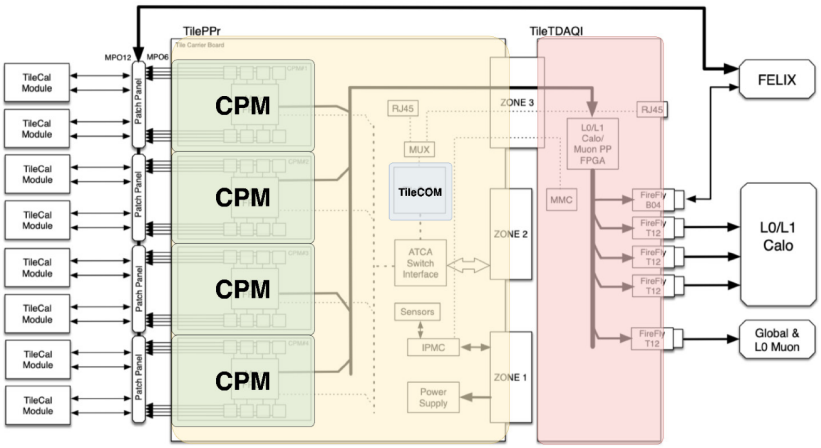

Figure 2. Schematic diagram of the PPr system. A complete PPr system can process the data from eight Tile super-drawers, consists of an ATCA motherboard blade with four CPMs plus one TDAQi RTM [2].

TDAQi. The interface with FELIX for data readout will be implemented in the CPMs, whereas the TDAQi will provide the trigger primitives readout and monitoring [6].

2.3. SoftWare Read-Out Driver (SWROD)

SWROD is envisaged to act in the ATLAS dataflow chain as the data handling interface between the FELIX system and the ATLAS HLT. This facility should house detector-specific processes which for the architecture used in Runs 1 and 2 are implemented in hardware RODs.

Data-handling features, like fragment building and formatting, as well as subsystem specific functionality such as fragment validation and monitoring, will be added to the DAQ chain to perform detector specific data processing without data buffering, including configuration, calibration and control [7].

2.4. Interface for the Laser system to the New Acquisition infrastructure (ILANA)

ILANA is the TileCal Interface for the Laser system to the New Acquisition infrastructure. ILANA will be designed following the same structure as the current laser calibration systems (LASCAR) used during Run 1 and 2. ILANA will be responsible for:

- control of the LASER pump, filter wheel and shutter,
- injection of a known charge to calibrate the photodiode,
- measurement of the PMTs and photodiodes signals,
- measurement of the time of arrival of the PMTs signals.

ILANA will transmit data to FELIX at a rate of approximately 1 MHz (L0A rate) and will receive the TTC and control signals from FELIX.

3. Test bed and test beams

We have constructed a test bed (Figure 3) composed of a TilePPr Demonstrator module connected to a Daughterboard and a Mainboard that emulates a mini-drawer of the Tile Calorimeter system and feeds the Mini-FELIX with pseudorandom generated data. The Mini-FELIX is a prototype version of the FELIX board based on a commercial Xilinx VC709 with a custom TTCfx mezzanine card used to connect the FELIX card to the ATLAS TTC system.

The SWROD is integrated into the official ATLAS TDAQ Software and has been configured to be used with our testbed. TTC information, Data Integrity Check, and Data Processing Tile Custom functions are being developed for the Tile custom specifications. These functions will be capable of generating histograms from received data and reconstructed energy. Further integration tests will be

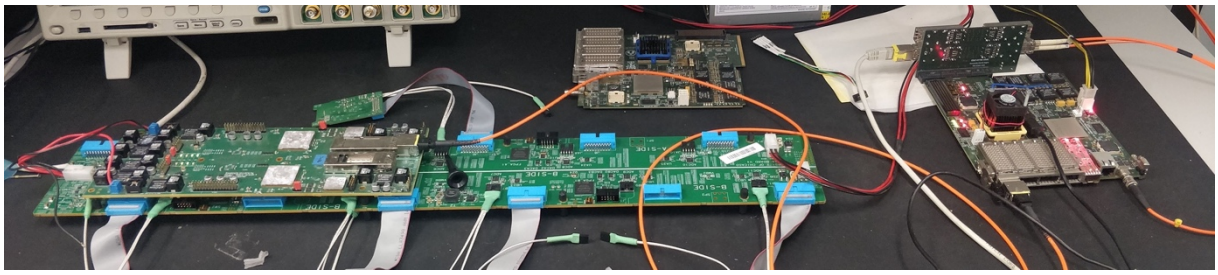

Figure 3. Testbed at the IFIC Laboratory in Valencia composed of front-end boards, Motherboard, Daughterboard and the TilePPr Demonstrator.

done with the first final TilePPr prototype module, which is currently under fabrication, and the FLX-712 in Full Mode.

4. Conclusions

The ATLAS Tile Hadronic Calorimeter upgrade for the HL-LHC will completely replace the on- and off-detector electronics, with a new read-out architecture.

With the new FELIX system combined with SWROD, the new readout will replace the legacy one and will achieve a much higher data rate. The implementation of custom processing functions for the data received into SWROD is ongoing and aims to be ready for the TileCal test beams at the SPS later this year.

References

[1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider," *J. Instrum.*, vol. 3, no. 08, pp. S08003–S08003, Aug. 2008, doi: 10.1088/1748-0221/3/08/S08003.

[2] ATLAS Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter," Geneva, Sep. 2017. [Online]. Available: https://cds.cern.ch/record/2285583.

[3] A. Camplani, "ATLAS Trigger and Data Acquisition Upgrades for the High Luminosity LHC," *PoS*, vol. LeptonPhot, p. 55, 2019, doi: 10.22323/1.367.0055.

[4] Panduro Vazquez, William, "FELIX: the new detector interface for ATLAS," *EPJ Web Conf.*, vol. 245, p. 1037, 2020, doi: 10.1051/epjconf/202024501037.

[5] F. Carrió and A. Valero, "The PreProcessor module for the ATLAS Tile Calorimeter at the HL-LHC," *Nucl. Instr. Meth. A*, vol. 958, p. 162487, Apr. 2020, doi: 10.1016/j.nima.2019.162487.

[6] F. Carrió, "Design of the Compact Processing Module for the ATLAS Tile Calorimeter," *IEEE Trans. Nucl. Sci.*, p. 1, 2021, doi: 10.1109/TNS.2021.3085490.

[7] S. Kolos, G. Crone, and W. P. Vazquez, "New software based readout driver for the ATLAS experiment," *IEEE Trans. Nucl. Sci.*, p. 1, 2021, doi: 10.1109/TNS.2021.3083987.