GEORG-AUGUST-UNIVERSITÄT GÖTTINGEN

Fakultät für Physik

Master's Thesis

Optimierung der Frontend-Ausleseelektronik für den Belle II DEPFET Sensor

Optimization of the front-end read-out electronics for the Belle II DEPFET Sensor

prepared by

Philipp Wieduwilt

from Stade

at the II. Physikalisches Institut

CERN-THESIS-2016-437
01/08/2016

Thesis number: II.Physik-UniGö-MSc-2016/04

Thesis period: 1st February 2016 until 1st August 2016

First referee: Prof. Dr. Ariane Frey

Second referee: PD Dr. Jörn Große-Knetter

Zusammenfassung

Das Belle Experiment am KEKB e^+e^--Beschleuniger in Tsukuba, Japan lieferte insgesamt eine integrierte Luminosität von $1\,\mathrm{ab}^{-1}$. Die gewonnenen Daten wurden für B-Physik Studien und für Suchen nach Physik jenseits des Standardmodels genutzt. Für noch detaillierte Studien und um noch höhere Sensitivität auf neue Physik zu erreichen, wird der KEKB Beschleuniger zu SuperKEKB ausgebaut. SuperKEKB wird dabei eine 40 mal höhere instantane Luminosität erreichen als sein Vorgänger. Ebenfalls wird der am KEK benutzte Belle Detektor verbessert zu Belle II. Neben der Optimierung der bei Belle benutzten Subdetektoren, wird Belle II zusätzlich mit zwei Lagen eines Silizium-Pixeldetektors nahe des Wechselwirkungspunktes ausgestattet sein. Dieser auf der DEPFET Technologie basierende Pixeldetektor kann sehr dünn gebaut werden und verringert dadurch unerwünschten Energieverlust und Vielfachstreuung der gemessenen Teilchen. Zur Auslese der DEPFET Pixelmatrizen werden zur Zeit drei dedizierte Frontend-Chips entwickelt. Die Funktionalität dieser Chips muss zurzeit untersucht und bestätigt werden, um einen erfolgreichen Einsatz des Belle II Pixeldetektors zu gewährleisten. In dieser Arbeit werden Testalgorithmen vorgestellt und diskutiert, die entwickelt wurden, um die Leistungsfähigkeit der Frontend-Ausleseelektronik zu untersuchen und zu optimieren. Die entwickelte Software wird benutzt, um Scans der Operationsparameter der Chips auszuwerten und Schwächen der aktuellen Chip-Designs zu untersuchen, um so eine Rückmeldung an die Chip-Designer für zukünftige Designiterationen zu geben.

Abstract

The Belle experiment at the KEKB e^+e^--collider in Tsukuba, Japan yielded an integrated luminosity of $1\,\mathrm{ab}^{-1}$. The collected data was used for in depth B-physics studies, as well as beyond standard model searches. For even more detailed physics studies and higher sensitivity to new physics contributions, the KEKB collider is being upgraded to SuperKEKB, which is expected to deliver a 40 times higher instantaneous luminosity. Also the Belle detector will be upgraded to Belle II. Besides the upgrade of the Belle-proven sub-detector components, Belle II will be equipped with additional two layers of a silicon pixel detector closest to the interaction point, which will improve vertex resolution. This pixel detector will be based on the DEPFET technology, which allows for very thin sensors to reduce energy loss and multiple scattering effects. For the read-out of the DEPFET pixel matrices, three dedicated front-end chips are being developed. Confirming and studying the functionality of the chip designs is crucial. In this thesis, testing algorithms will be presented and discussed, that were developed for investigating and optimizing the performance of the current designs of the front-end read-out electronics. The software is used to evaluate parameter scans, tune the chip parameters and investigate weaknesses of the existing chip designs, in order to provide feed-back to the chip designers for future design iterations.

Keywords: Belle II, silicon pixel detectors, DEPFET sensors, read-out electronics, analog-digital conversion, optimization of operation parameters

Contents

1 Introduction: The Belle II Detector at the SuperKEKB Collider **1**

2 The DEPFET Pixel Detector for Belle II **3**
- 2.1 Principles of DEPFET Sensors 4
- 2.2 The Front-end Electronics for the Pixel Detector 6
  - 2.2.1 The SWITCHER 7
  - 2.2.2 The Drain Current Digitizer (DCD) 8
  - 2.2.3 The Data Handling Processor (DHP) 11

3 Analog-Digital Conversion **13**
- 3.1 Characteristics of Transfer Curves: Dynamic Range, Noise and Linearity . 13
- 3.2 Cyclic Redundant Signed-Digit Analog-Digital Conversion Algorithm . . . 16

4 The Front-end Electronics in Detail **17**
- 4.1 Analog-Digital Conversion Implementation in the Drain Current Digitizer . 17
  - 4.1.1 Current Memory Cells and Comparators 19
  - 4.1.2 Parameters for Adjusting the Analog Performance 20
- 4.2 Inter-ASIC Communication 22
  - 4.2.1 Data Links Communication: Signal Delay Compensation 23

5 Experimental Setups for ASIC Testing **27**
- 5.1 The Hybrid5: A PCB-based ASIC Testing Interface 27
- 5.2 Electrical Multi-Chip Modules 28
- 5.3 Back-end Read-out and Laboratory Setup 29

6 Read-out ASICs Failure Identification **33**
- 6.1 Drain Current Digitizer: Analog Performance and Failure Identification . . 33
  - 6.1.1 Dynamic Range 34
  - 6.1.2 Noise and Linearity 34
  - 6.1.3 Comparator Offsets and Long Codes 36

6.2 Inter-ASIC Communication Failures 41
6.2.1 Bit Error Recognition in Transfer Curves 42
6.2.2 Digital Test Pattern 46
6.2.3 Indications of Cross-Talk among Communication Links 48

7 Read-out ASICs Optimization: Parameter Scans and Tuning 51
7.1 Optimization of the Inter-ASIC Communication 51
7.1.1 Using the Digital Test Pattern 52
7.1.2 Using Transfer Curves 55
7.2 Optimization of the Drain Current Digitizer Analog Performance 57
7.2.1 Optimization of the DAC Currents 59
7.2.2 Optimization of the Supply Voltages 60

8 Results from Test System Measurements and Irradiation Campaigns 63
8.1 Working Point Variations among Modules 63
8.2 Inter-ASIC Communication Stability at High Clock Frequencies 67
8.3 ASICs Operation Stability and Irradiation Damage 68
8.3.1 Stability of the Working Point 69
8.3.2 Stability of the Inter-ASIC Communication 70

9 Summary & Conclusion 75

Nomenclature

Abbreviations

Abbreviation	Meaning
A	
ADC	analog-to-digital conversion or converter
ADU	arbitrary digital unit
ASIC	application specific integrated circuit
C	
CMC	current memory cell
CMP	comparator
CRSD	cyclic redundant signed-digit analog-digital conversion algorithm
D	
DAC	digital-to-analog converter (used as parameter/settings)
DAQ	data acquisition
DCD	the Drain Current Digitizer
DEPFET	depleted (p-channel) field effect transistor
DHH	the Data Handling Hybrid
DHP	the Data Handling Processor
DNL	differential non-linearity (of an ADC curve)
DUT	device under test
G	
GCK	global reference clock
I	
INL	integrated non-linearity (of an ADC curve)
J	
JTAG	joint test action group, IEEE standard 1149.1 for testing, debugging and controlling of integrated circuits
L	
LSB	least significant bit $\equiv$ ADU

Abbreviation	Meaning
M	
MSB	most significant bit
O	
OWP	optimal working point
P	
PCB	printed circuit board
PXD	the Belle II DEPFET pixel detector
S	
SVD	the Belle II silicon strip sensor as part of the vertex detector
SWITCHER	front-end matrix steering chip for PXD
T	
TC	transconductor
TIA	transimpedance amplifier
V	
VXD	the Belle II vertex detector

1 Introduction: The Belle II Detector at the SuperKEKB Collider

The SuperKEKB collider at the KEK research complex in Tsukuba, Japan is an asymmetric e^+e^--collider, it is the upgrade of the former KEKB collider. SuperKEKB is expected to deliver a 40 times higher instantaneous luminosity compared to its predecessor [1]. KEKB and SuperKEKB are so called *B-Factories*, the center-of-mass energy of the e^+e^--system is at 10.58 GeV, which is right at the $\Upsilon(4s)$ resonance. Thus, mainly $\Upsilon(4s)$ mesons are produced, which in turn, predominantly decay into pairs of B mesons (branching fraction of $B\bar{B} > 96\,\%$ [2]). Due to its short lifetime, the $\Upsilon(4s)$ decays practically immediately at the interaction point. By employing an asymmetric collider, the B mesons are boosted along the beam-axis and, due to their larger lifetime of $\sim 1\,\mathrm{ps}$, travel a measurable path in the detector, resulting in displaced vertices for the individual B-decays. Reconstruction of the decay vertices allows for measurements of the time-dependence of B-decays, with which CP-violation in the B-meson system can be studied. The Belle experiment at KEKB accumulated $1\,\mathrm{ab}^{-1}$ of data over 10 years. With the significantly increased luminosity, SuperKEKB is expected to deliver an integrated luminosity of $50\,\mathrm{ab}^{-1}$ over 5 years of running, which will allow for B-physics studies with much higher statistics [3]. With the analysis of this data, uncertainties on CP-violation parameters can be decreased and sensitivity to beyond standard model contributions will be increased [4, 5].

To be able to measure at such high collision rates and to improve the resolution of vertex reconstruction, also the former Belle detector is now being upgraded to Belle II [6]. Figure 1.1 shows a comparison of the layout of the Belle detector (bottom half) to the designed layout of Belle II (top half). Specifically to improve vertex resolution, Belle II will be equipped with additional two layers of high resolution silicon pixel sensors, which are located very close to the interaction region (labelled "PXD (2 layers)" in 1.1). The sensors in this inner pixel detector (PXD) will be based on the DEPFET technology. Using DEPFET pixels as an active silicon pixel detector, very thin sensors with low material

budget can be built, which reduces the effects of energy loss and multiple scattering on the measured particles. Increased luminosity also means an increase in background and an overall higher particle flux through the tracking detectors, especially for the innermost layers. It is therefore crucial to design the PXD DEPFET sensors and the front-end electronics for radiation hardness. Current estimations state a $1-2$ Mrad/y irradiation level for the PXD system, the design target is that all PXD components should survive at least a 10 Mrad irradiation dose [6]. The front-end electronics of the Belle II pixel detector will consist of three dedicated chip types. Each of these read-out and steering chips are supposed to fulfil specific tasks, therefore a verification of their functionalities is crucial. In this thesis, I will present and discuss methods and algorithms that were developed in order to investigate certain chip functionalities and to define a strategy to optimize the chip performances. These optimization strategies were applied to several testing systems, and the effects of chip production variations and irradiation on the chip performances were investigated.

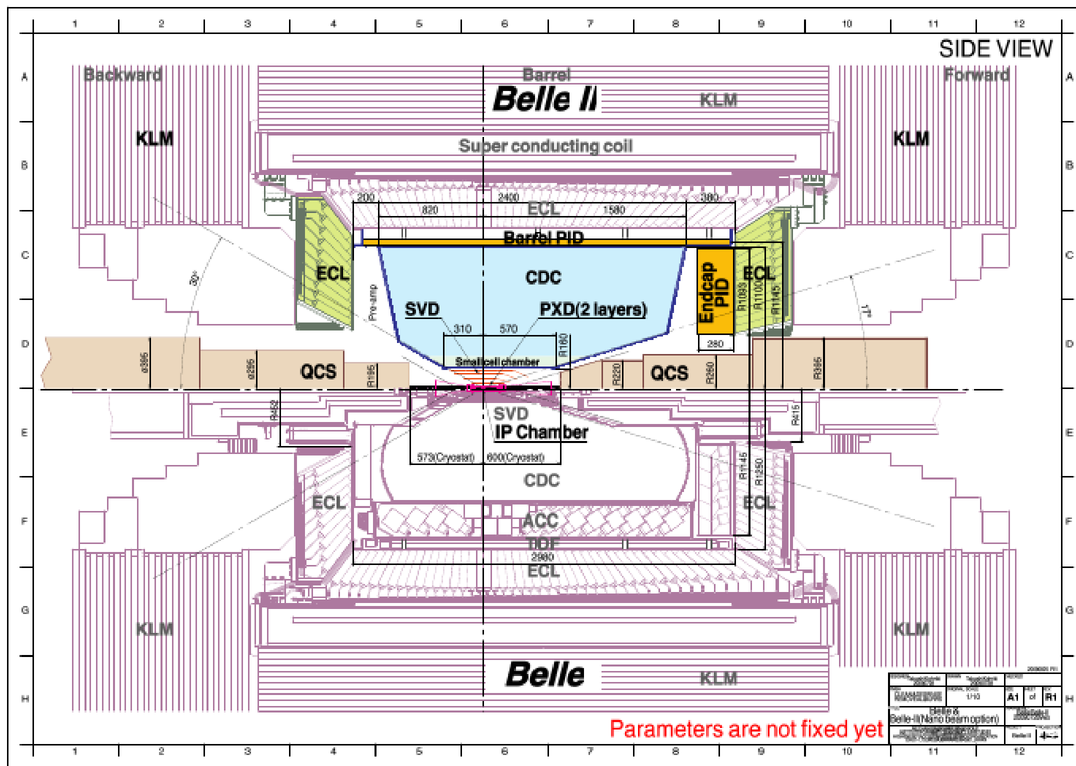

Figure 1.1: Comparison of the layout of the former Belle detector (bottom half) and the design layout of the future Belle II detector (top half) as presented in [6]. The Belle II detector design is very similar to the proven Belle design, one major improvement is the additional DEPFET pixel sensor (PXD) close to the interaction point (IP). All other sub-detector systems also undergo a design upgrade.

2 The DEPFET Pixel Detector for Belle II

Tracking and vertex reconstruction in the Belle II experiment will be based on two sensor types, together forming the six layers of the Belle II vertex detector (VXD). From the interaction point outwards there are

- two layers of DEPFET pixel sensors (PXD) closest to the beam-pipe and
- four layers of silicon strip sensors (SVD) [7].

The combined impact parameter and vertex resolution design value is $\approx 20\,\mu$m, dependent on the incident angle and momentum of the measured particle, which maintains and even improves the Belle performance, while operating at much higher background [6]. Figure 2.1 shows a 3D model of the two PXD layers, as well as a cross-section through the PXD system indicating its dimensions. The inner layer is located at a radius of 14 mm, the outer layer at a radius of 22 mm around the beam pipe. These small radii are possible due to the small beam pipe radius of only 10 mm, which is large enough for the nano beam technology developed for SuperKEKB in order to increase the luminosity [3]. Each layer consists of multiple ladders, aligned parallel to the beam pipe, the inner layer has eight and the outer layer has twelve ladders. Each ladder consists of two half-ladder modules, one forward and one backward module, which are glued together. Each half-ladder module has a sensitive DEPFET pixel matrix (light-grey coloured), read-out and steering electronics (not indicated here) and a Kapton cable connection (light-brown) for powering and data connection to the outside. The front-end ASICs are bump-bonded directly onto the half-ladder modules support frame (dark blue coloured), which also implements the routing of powering and data lines. A half-ladder module can be considered the building block of the PXD detector

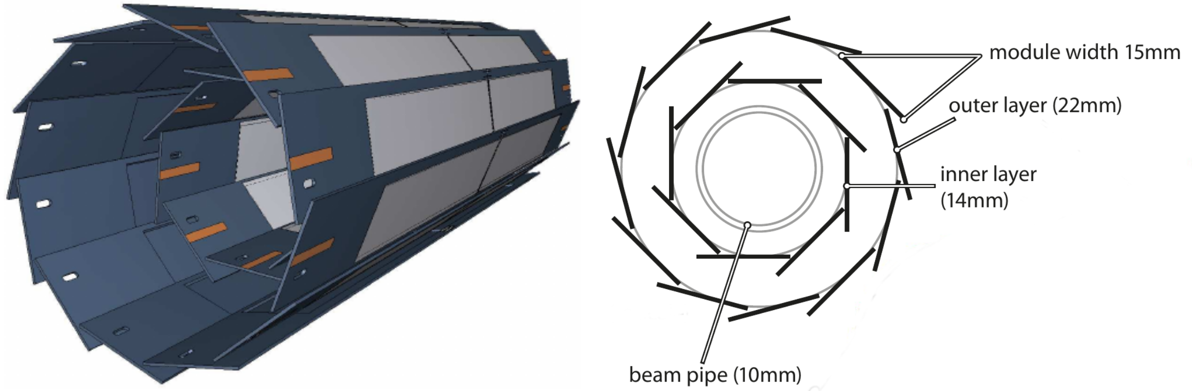

Figure 2.1: 3D model of the two layers of the Belle II DEPFET pixel detector and its individual sensor modules (left, [6]) and a cross-section indicating the dimensions of the PXD system and the radii at which the PXD layers are located (right, [8]).

2.1 Principles of DEPFET Sensors

To understand the requirements on the front-end electronics for the PXD system, one needs to understand the principles of DEPFET pixel signals. DEPFET stands for ***de****pleted* ***p****-channel* ***f****ield* ***e****ffect* ***t****ransistor*, the schematic of a DEPFET pixel is illustrated in figure 2.2. In short, a DEPFET pixel is a MOSFET[1], with source, gate and drain electrodes, located on top of a depleted silicon bulk with an additional deep n-well implant below the gate electrode (*internal gate*) [9, 10]. A negative high voltage between the source electrode and the $p+$ back-side contact depletes the bulk via side-ward depletion. Due to the n-implant, the potential minimum will form just below the gate electrode in the internal gate. A charged particle traversing the bulk material will generate electron-hole pairs. The holes drift to the back-side contact, whereas the electrons drift to the potential minimum in the internal gate. When the transistor is switched on, i.e. a negative gate voltage is applied, a current is flowing from the source to the drain electrode. Any accumulated charge in the internal gate will modulate the potential landscape and will increase the transistor current. This internal amplification, denoted g_q, is defined as

$$g_q = \frac{\Delta I_d}{e^-} \quad , \tag{2.1}$$

i.e. the the current modulation ΔI_d, per accumulated electron e^-. The g_q value characterizes the DEPFET pixel, typical values are $400 - 700\,\text{pA}/e^-$ for PXD DEPFET pixels [6]. The DEPFET operation principle has some useful properties:

[1] MOSFET = metal-oxide field effect transistor

- The signal (accumulated electrons) is already amplified during read-out.
- The accumulated charge can be read out multiple times (non-destructive read-out).
- No lateral charge transfer over large distances is necessary, this reduces charge loss.
- The internal gate has very small capacitance, thus very low noise performance also at room temperature is possible.
- The DEPFET pixel only dissipates power in the small time window when being read out. Thus no cryogenic cooling of a DEPFET pixel matrix is necessary.

After the accumulated charge was read out, one needs to remove the signal charge. This is achieved by applying a positive voltage to a neighbouring n^+ contact. Via a punch through to the internal gate, all charges are collected and removed. After this *clear* procedure, the pixel is sensitive to new signals. The total DEPFET pixel current signal must be corrected for the pedestal current to measure only ΔI_d. It holds

$$I_{\text{pixel}} = I_{\text{ped}} + \Delta I_d \tag{2.2}$$

where I_{pixel} is the measured pixel current, I_{ped} is the pedestal current and ΔI_d is the additional current flowing due to accumulated charge in the internal gate, i.e. the actual signal current. Pedestal correction can be done using a *double sampling* read-out procedure, where performing a consecutive read-clear-read allows for the subtraction of a highly correlated pedestal value. However, read-out speed and small dead-times are favoured, so a *single sampling* read-clear sequence is done, where the pedestal values are recorded once and are stored in registers and are assumed to be constant for a specific period of time.

The Belle II PXD DEPFET matrices will have pixel sizes of $50 \times 55\,\mu\text{m}^2$ (central part) and $50 \times 70\,\mu\text{m}^2$ (forward and backward part) for the inner layer and $50 \times 60\,\mu\text{m}^2$ (central part) and $50 \times 85\,\mu\text{m}^2$ (forward and backward part) for the outer layer [9]. Each half-ladder sensor matrix consists of 768×250 DEPFET pixels. Special efforts have been taken to adjust the DEPFET technology to meet the Belle II requirements. This includes a thinning-technology, which allows for production of $75\,\mu\text{m}$ thick substrates. Another concern is the radiation hardness of the sensors. Thin oxides in conjunction with reduced gate lengths yield radiation hard sensors with reasonably high expected signal-to-noise ratios of 20-30 [6].

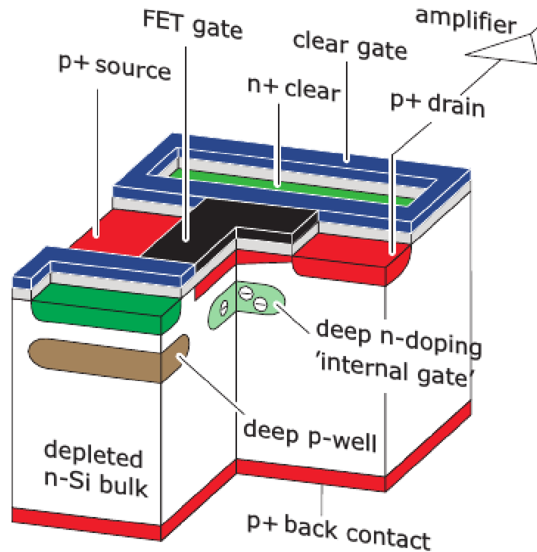

Figure 2.2: Schematic of the principle components of a DEPFET pixel [6]: Signal charges (electrons) are generated in the depleted bulk and are collected in the internal gate and modify the source-drain current of the DEPFET transistor. After read-out, the accumulated charge is removed via a clear potential.

2.2 The Front-end Electronics for the Pixel Detector

For steering and reading out a full DEPFET pixel matrix, the following tasks must be performed for each DEPFET pixel:

- Activating the pixel by applying an appropriate gate voltage.
- Sampling the pixel current (pedestal + signal current),
- subtracting the pedestal current and
- digitizing the signal current.
- Clearing the accumulated pixel charge by applying a clear voltage pulse.
- Processing of the digital signal.

The Belle II DEPFET sensors use three dedicated application specific integrated circuit (ASIC) chips for these tasks. The read-out needs to be fast with about $20\,\mu$s for a 768×250 pixel matrix and the front-end read-out chips need to be placed on the sensor module with a limitation in available space, their power consumption and dissipation

should not exceed a few Watts. Using ASICs as the front-end chips is the preferred way to meet these constraints, as they allow for fast processing at low power consumption and small physical dimensions. In contrast to programmable microprocessors, an ASIC implements a fix electric circuit consisting of analog blocks and digital logic blocks. The circuitry of an ASIC cannot be changed after production, if implemented, its functionality can be influenced by adjustable current sources (analog blocks) or by setting configuration bits (digital blocks). The *SWITCHER* ASIC for the Belle II PXD system activates and clears the DEPFET pixels in a rolling-shutter read-out mode, as indicated in figure 2.3, by applying the appropriate gate and clear voltages. Segments consisting of four geometrical pixel rows are selected consecutively and the drain currents flow into the *Drain Current Digitizer (DCD)* chips via the drain lines. Each DCD receives 250 input currents, performs an analog pedestal correction for each input and digitizes all currents in parallel using analog-digital converters (ADCs) with 8-bit resolution. The 250 8-bit digital output codes per DCD are sent to the *Data Handling Processor (DHP)* chips. The DHP buffers the digital data, performs a digital pedestal correction and zero-suppression and implements a hit finder. Hit data is send out to the back-end electronics upon trigger request. To reduce the material budget as much as possible, the PXD half-ladder modules are realized as all-silicon modules, as shown in figure 2.4. The read-out ASCIs are directly bump-bonded on the silicon support frame, which also implements the routing of power and data lines within three different metal layers (Al and Cu). The DEPFET pixel matrix dissipates only very little power and low-noise operation is possible even at temperatures in the order of 20 °C, indirect cooling of the matrix is sufficient and is provided by a cold air flow, with a temperature of -5 °C, through the whole vertex detector system and by heat conduction through the half-ladder silicon support frame [6]. The front-end ASICs, on the other hand, dissipate power in the order of $0.5 - 2$ W, active cooling is necessary and provided by cooling pipes filled with a liquid coolant [6, 11, 12].

2.2.1 The SWITCHER

The SWITCHER selects segments of four geometrical rows of the DEPFET pixel matrix by applying a negative high voltage, around -5 V, to the gate electrodes. Selection of row segments is controlled by shift registers and strobe signals and is configurable by uploading a specific *SWITCHER sequence*. One SWITCHER chip can address 32 row segments of a DEPFET pixel matrix, multiple SWITCHER chips can be cascaded for steering the read-out of a large matrix [14]. For the 768×250 pixels of the PXD half-ladder matrices, six SWITCHERs are needed and are located on the module rim, alongside the DEPFET matrix. The SWITCHER ASIC dissipates power in the order of 0.4 W.

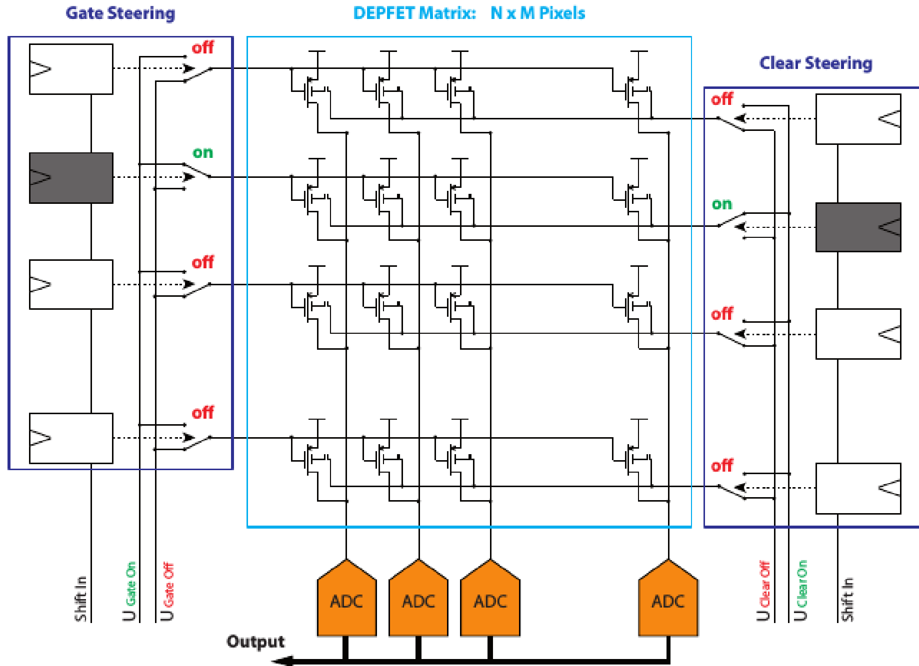

Figure 2.3: Sketch of the rolling-shutter read-out mode controlled by the SWITCHER chip [13]. Segments of four geometrical matrix rows are activated consecutively, the pixels of one segment are connected to the drain lines (common for one pixel column) and are read out.

2.2.2 The Drain Current Digitizer (DCD)

The Drain Current Digitizer (DCD) chip has 256 analog inputs to receive the drain currents from DEPFET pixels. In fact, one DEPFET matrix segment consists of four geometrical rows and 250 columns, in total 1000 pixels, which are read out by four DCD chips. Thus, each DCD receives only 250 drain currents, six DCD inputs are not connected to the matrix and are not used. Each input current is fed into a separate analog channel of the DCD. The basic structure of the analog circuit present in each DCD channel is shown in figure 2.5, the description is based on [15]. The analog input stage (*Receiver*) is based on a transimpedance amplifier (TIA), which keeps the drain line potential at a constant level. This way, no line capacitance is charged, which increases the read-out speed and reduces noise. Analog pedestal subtraction is realized via a 2-bit DAC (*VP-DAC*), variable for each channel, and an adjustable current (*VNSubIn*), which is the same for all channels. The TIA can be programmed to perform an amplification (*gain*) of the (pedestal corrected) input signal. The TIA also acts as a low-pass filter, which, together with the signal sampling and shaping, reduces the signal noise. The current is then fed into a current-mode *pipeline analog-digital converter (ADC)*, which digitizes the analog input with 8-bit resolution. The pipeline ADC will be discussed in more detail in sec-

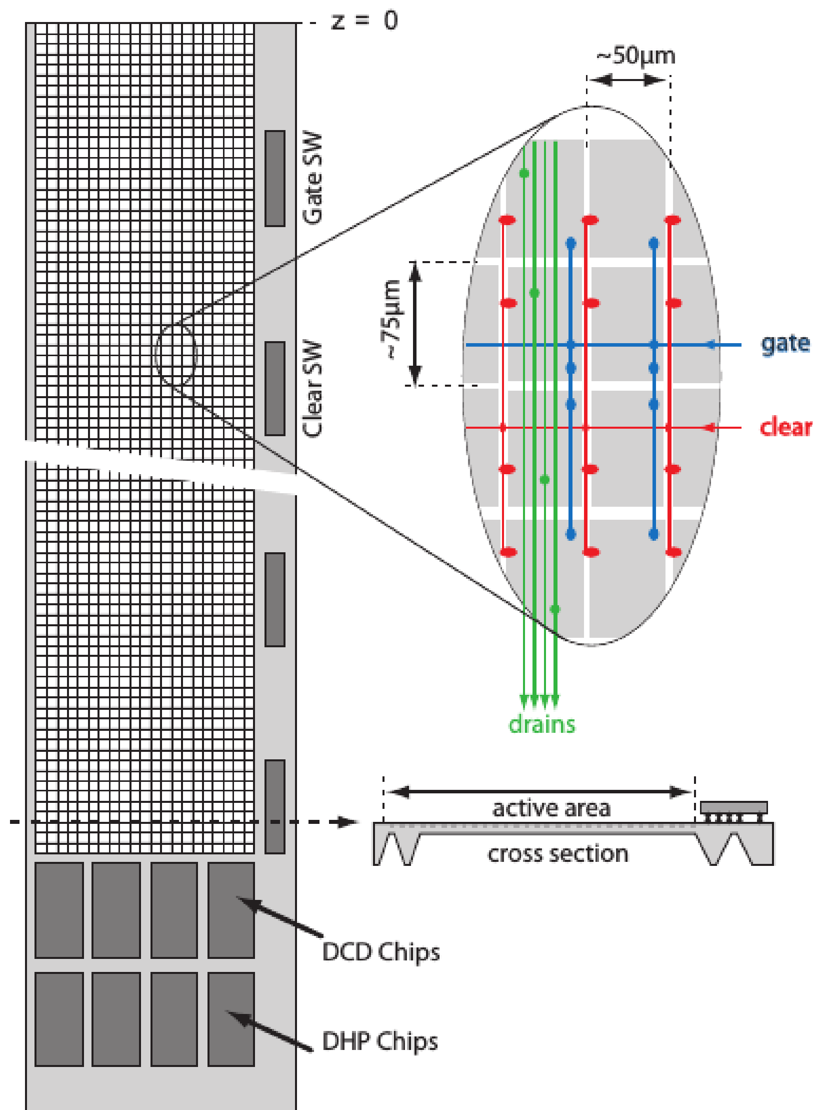

Figure 2.4: Schematic of a PXD half-ladder module [6]: The read-out chips are bump-bonded on the silicon frame, routing of power and data lines is implemented in the silicon. The result is a thin all-silicon module, reduction of the overall material budget is a major design target of the Belle II PXD system to reduce energy loss and multiple scattering effects.

tion 4.1. The digital data of all DCD channels is processed in a digital block. It decodes and derandomizes the data and sends it partly multiplexed, partly parallel to the next ASIC. The timing requirement for Belle II is a read-out frequency of at least 10 MHz, i.e. a read-out time of ≤ 100 ns, per row segment. One DCD dissipates power in the order of $1 - 2$ W.

Different versions of the DCD chip have been developed. The current version for Belle II PXD is labelled DCD-Bv4-Pipeline. My discussions and all presented measurements are

based on this DCD version. Previous versions implemented cyclic ADCs instead of the current pipeline version and are extensively discussed in [13] and [8].

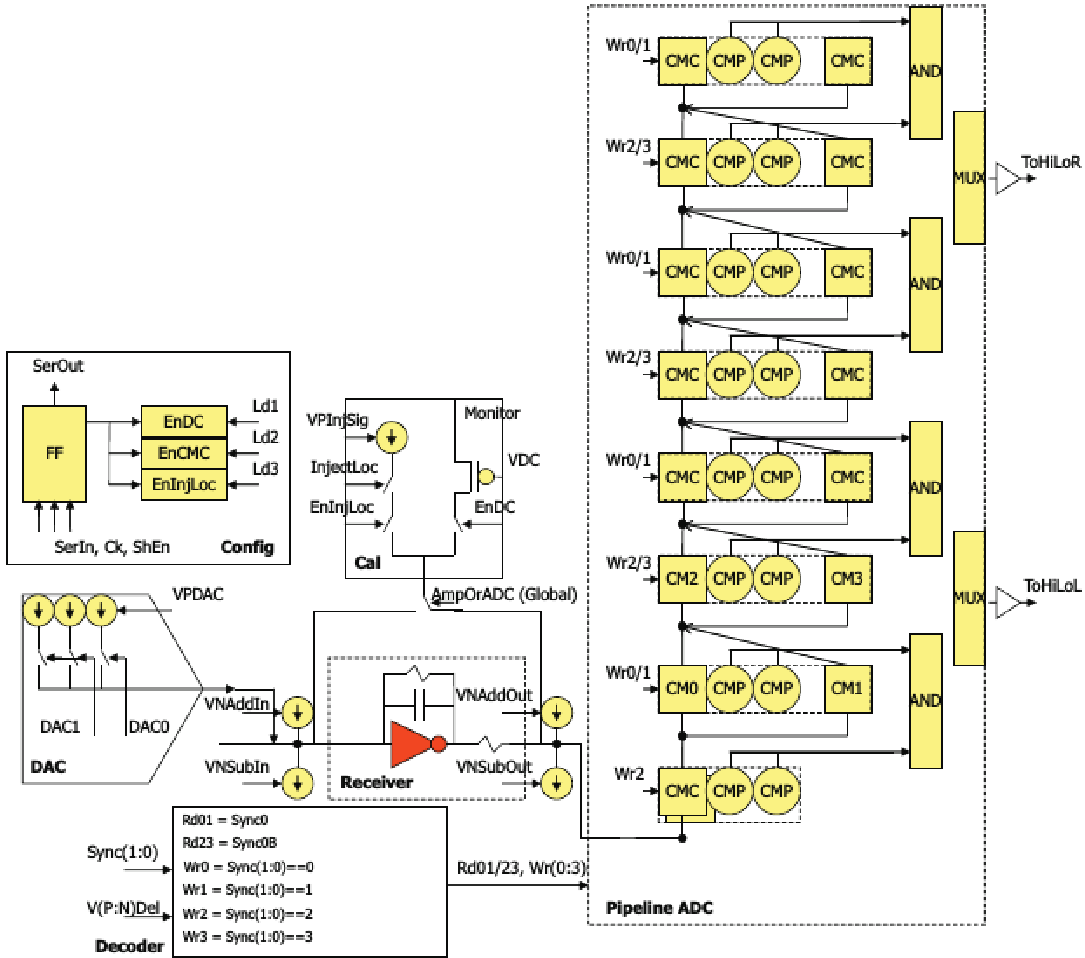

Figure 2.5: Basic circuit of one analog channel of the DCD-Bv4-Pipeline chip [15]. The channel receives the DEPFET drain current, subtracts a pedestal current, amplifies the signal and then digitizes it with 8-bit resolution in a pipeline analog-digital converter (ADC).

2.2.3 The Data Handling Processor (DHP)

A 768×250 pixel matrix produces a data rate of about 80 Gbit/s, which is impossible to send off-module to back-end electronics. The purpose of the Data Handling Processor (DHP) is further processing of the digital data received from the DCD chip to reduce the overall data rates. The data communication between DCD and DHP uses 64 physical links to send the digital data. The incoming raw data from the DCD is buffered in the DHP. A pedestal subtraction is realized by subtracting cached, digital pedestal values, additionally, a common mode correction is applied. The common mode is a signal offset shared by all pixels in one row segment. After pedestal and common mode correction, the data is zero-suppressed, that means only signals above a set threshold are kept. A hit finder searches for hits inside a full matrix frame and stores the information, hit position and signal strength, in a hit buffer. Upon receipt of a trigger signal, the data is send out to the back-end electronics via high speed links. The *data handling hybrid (DHH)* system provides the primary back-end read-out. Figure 2.6 sketches the back-end electronics read-out chain. The DHP reduces the overall data rate to about 1.6 Gbit/s per DCD-DHP pair or 6.4 Gbit/s per half-ladder module. It is possible to send out the DCD digital raw data directly for testing measurements. The DHP also generates and distributes all timing signals (clocks) to the other ASICs and provides the joint test action group (JTAG) control interface for configuring all ASICs. The DCD and DHP chips are located at the end-of-stave region of a PXD half-ladder module. The current design version of the DHP is labelled DHPT-1.0 as described in [16]. The suffix "T" denotes the TSMC[2] 65 nm technology, the process the DHPT is implemented in.

[2] The Taiwan Semiconductor Manufacturing Company Limited (TSMC) is a manufacturer of semiconductor technology.

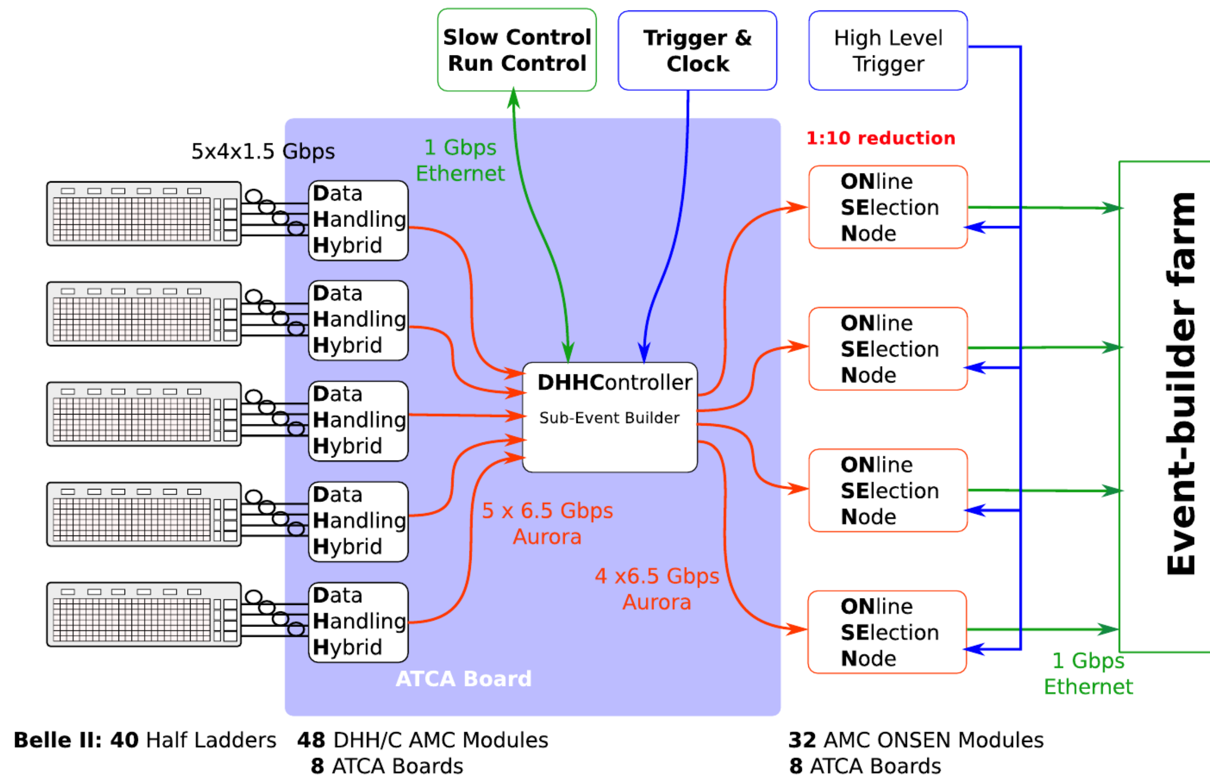

Figure 2.6: Sketch of the back-end read-out electronics chain [17]. Each Belle II half-ladder (four DCD-DHP pairs) is read out by one DHH system. Data from five DHH boards is collected in one DHH-Controller (DHHC) that processes and distributes slow control commands and low-level trigger information. The ONSEN system implements online event selection and receives high-level trigger signals.

3 Analog-Digital Conversion

An analog-digital conversion is necessary where digital processing of analog signals is desired. A continuous signal within a specific dynamic range is discretized with a finite digital resolution. The read-out of the DEPFET pixels for the Belle II pixel detector requires the digitization of signal currents up to $20\,\mu$A. The Drain Current Digitizer (DCD) ASIC essentially implements multiple analog-digital converters (ADCs) working in parallel. The performance of a single analog-digital converter can be visualized and measured via an ADC transfer curve. To record the transfer curve, one varies the continuous analog input signal and measures the corresponding discrete digital output code. This chapter will discuss the basics of characterizing ADC transfer curves.

3.1 Characteristics of Transfer Curves: Dynamic Range, Noise and Linearity

Figure 3.1 shows a prototype example of an ADC transfer curve. Several characteristics of the curve can be measured and are used to evaluate the ADCs performance. A 2-dimensional histogram representation is used, where the x-axis bins measure the analog input value and the y-axis bins measure the digital output code. The ADC transfer curve is recorded multiple times, the color code indicates the frequency at which each input-output bin was recorded.

The analog-digital converter translates the analog inputs to a specific range of digital output codes. In the given example (figure 3.1), the output code range is the interval $[0, 255]$, which means an 8-bit digitization. Smaller input values have lower codes, higher input values have higher codes. Output code 0 corresponds to the minimal input value, while the maximal output code 255 corresponds to the maximal input value. Any input values below or above will be digitized to code 0 or code 255, respectively. The minimal and maximal input values determine the dynamic input range of the ADC, here $[-8, 8]\,\mu$A (see figure 3.1). One must ensure that the dynamic input range of the employed ADC covers the expected signal range. The analog-digital conversion can be subject to electrical noise. To determine the electrical noise, one records the ADC curve multiple times, i.e.

for each input value i, the output code o is recorded multiple times. Let f_{io} denote the occurrence of the input i and output o bin. The ADC curve noise σ_i as a function of the input value can then be defined as the standard deviation of the output codes per input value bin. A measure for the overall ADC noise σ can be defined as the median over all σ_i. The measured ADC noise is a convolution of the noise of the input signal (independent from the ADC performance) and the noise introduced by the analog-digital converter itself.

Another concern is the linearity of the ADC curve. Ideally, the ADC operation should be perfectly linear, i.e. a doubled input value should result in a doubled output code (within the given ranges). The linear behaviour ensures, that the digital resolution is constant over the full dynamic range of the ADC. The digital resolution can be defined as the width of the input value interval for which the output code is constant, this is exactly the slope of the ADC curve. A constant, homogeneous resolution thus means a constant slope, i.e. a linear behaviour. Any deviation from a linear behaviour, that is a non-linearity, can be measured as a local deviation or *differential non-linearity (DNL)* or as an *integrated non-linearity (INL)*. Using the 2-dimensional histogram representation, the total occurrence of one output code o is denoted as f_o (i.e. projecting out the input value bins i). Let m denote the mean over all f_o, that is the mean occurrence of all output codes. The differential non-linearity (DNL) can then be defined as

$$\mathrm{DNL}_o = \frac{f_o}{m} - 1 \tag{3.1}$$

which is the non-linearity per output code o. The integrated non-linearity is then simply defined as the cumulative sum of all DNL values up to output code o

$$\mathrm{INL}_o = \sum_k^o \mathrm{DNL}_k \ . \tag{3.2}$$

Ideally, for a perfectly linear ADC curve, the DNL of each output code is 0 and thus also the INL is 0 for all output codes. An output code with no readings, i.e. a gap in the ADC curve, has a DNL of -1. A code that appears more often than all others is assigned a positive DNL. One may define a single measure for the ADC curve linearity as a peak-to-peak INL value, which is

$$\mathrm{INLpp} = |\max(\mathrm{INL}_o) - \min(\mathrm{INL}_o)| \ . \tag{3.3}$$

Another possibility to determine the ADC curves linearity would be to perform a least-squares fit of a linear function to the two-dimensional ADC histogram and using the χ^2

value as a measure for linearity. However, the fit χ^2 value is influenced by various effects. Higher ADC curve noise, for example, would increase the χ^2 value, although the linearity is unchanged. Also, if for some reason the ADC curve is fragmented into multiple linear parts, the linear fit is no longer accurate and no reasonable information can be drawn from it (see discussion on bit errors in chapter 6). DNL and INL are much more robust measures to use for characterizing an ADC curve.

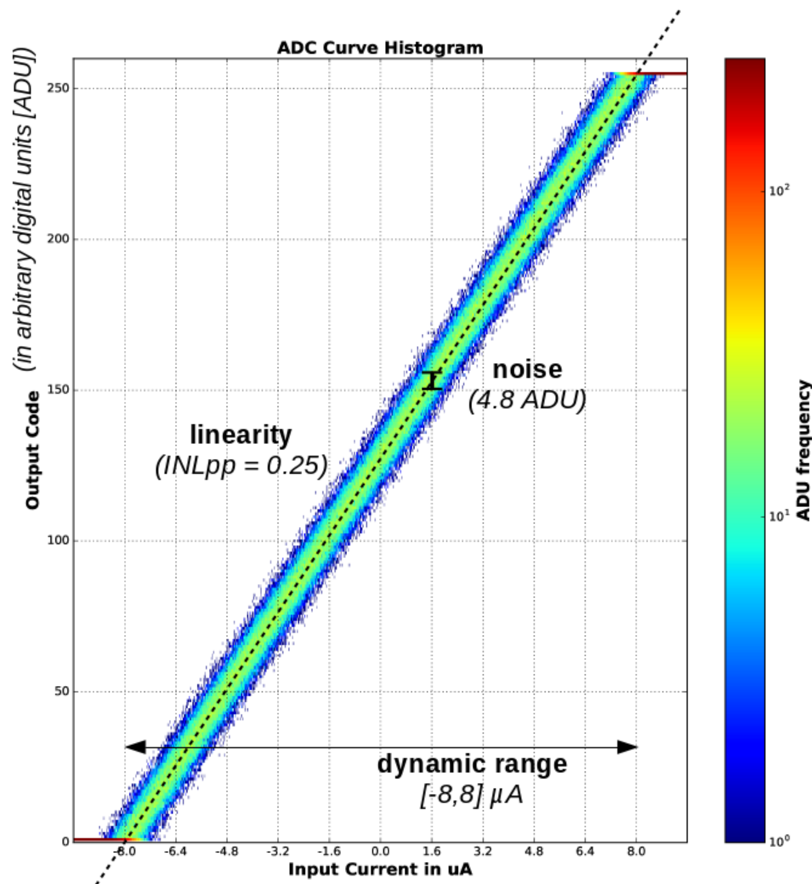

Figure 3.1: Prototype example of an ADC transfer curve used to investigate the performance of a current-mode analog-digital converter. On the x-axis the analog input values (current I_{in}) are binned, the y-axis measures the corresponding digital output code bin in arbitrary digital units (ADU). The transfer curve was recorded multiple times, a 2-dimensional histogram representation is chosen, where the color code indicates the frequency at which each input-output bin was recorded. The characteristic properties of the ADC transfer curve are the dynamic input range, the electrical noise and the linearity.

3.2 Cyclic Redundant Signed-Digit Analog-Digital Conversion Algorithm

The ADCs in the Drain Current Digitizer (DCD) ASIC convert the DEPFET pixel currents (in the order of some μA) to digital 8-bit signals. The conversion algorithm used in the DCD design is a cyclic redundant signed-digit (CRSD) conversion as described in [18]. The algorithm is an iteration over several n identical stages. In each stage i, the input current I_{in} is compared to two thresholds, one negative t_- and one positive t_+ threshold. Per stage two bits are set, a TooHigh and a TooLow bit. If $I_{\mathrm{in}} > t_+$ then TooHigh $= 1$ and TooLow $= 0$, or simply said the redundant bit code is 10. In this case a reference current I_{ref} is subtracted from the input current. If $I_{\mathrm{in}} < t_-$ the redundant bit code is 01 and the reference current I_{ref} is added to the input current. In case $t_- \leq I_{\mathrm{in}} \leq t_+$ the redundant bit code is 00 and no current is added or subtracted to I_{in}. The residual current I_{res} has by construction half the range of the input currents. I_{res} is thus multiplied by a factor of two to match the next stages input range. The output current $2 \times I_{\mathrm{res}}$ then undergoes the same operation in the next stage $i+1$. The final conversion result for the ADCs output code D after n stages is computed from the TooHigh-TooLow bit pair streams of all stages as

$$D \equiv 2^0(\textsc{TooHigh}_n - \textsc{TooLow}_n) + \cdots + 2^n(\textsc{TooHigh}_0 - \textsc{TooLow}_0) \quad . \tag{3.4}$$

The first stage (stage 0) determines the most significant bit (MSB) of the output code D. Each additional conversion stage yields an additional TooHigh and TooLow bit pair and improves the digital resolution. For an n-cyclic conversion process, D is the $(n+1)$-bit binary representation, a signed integer, of the input current I_{in}.

4 The Front-end Electronics in Detail

This chapter will present in more detail some aspects of the read-out ASICs, namely the implementation of the analog-digital conversion in the Drain Current Digitizer (DCD) and the digital communication among the DCD and the DHP ASICs. Both aspects are critical for the front-end read-out to work properly. The design of the ASICs implement several parameters that allow for adjusting the AD conversion in the DCD and the inter-ASIC communication.

4.1 Analog-Digital Conversion Implementation in the Drain Current Digitizer

As described in section 2.2.2, the DCD chip provides 256 analog channels, each with a pipeline analog-digital converter implementing the redundant signed-digit (CRSD) conversion algorithm as it was described in section 3.2. The schematic implementation is sketched in figure 2.5, right-hand side. The CRSD-algorithm requires arithmetic operations, i.e. addition and subtraction of currents[1]. In the pipeline ADC implementation of the DCD, current-memory cells (CMC) are used for storing currents and allow for arithmetic operations with currents. The second requirement is the implementation of current comparisons, analog comparators (CMP) are used for this purpose. Each conversion stage of the pipeline ADC, corresponding to one stage of the CRSD conversion algorithm, contains two double cell blocks (each consisting of two CMCs) and two comparators. In this implementation, the ADC uses a reference current REF, which defines the thresholds $t_+ = \mathrm{REF}$ and $t_- = -\mathrm{REF}$ of the CRSD-algorithm. The reference current I_{ref}, that is added or subtracted after comparison, is set to be $I_{\mathrm{ref}} = 2 \cdot \mathrm{REF}$. The design value is $\mathrm{REF} = 2.0\,\mu\mathrm{A}$. The ideal input/output relation of one conversion stage is graphically represented in figure 4.1. It is vital to adjust the reference current I_{ref} and

[1]The algorithm requires a multiplication by two of the residual current per conversion stage. This can be realized as a simple addition of two equal currents.

the thresholds t_+ and t_- properly to achieve an ideal analog-digital conversion. The DCD pipeline ADCs implement an 8-cycle CRSD-conversion, which yields a 9-bit digital result D. To simplify digital data processing, the least significant bit (LSB) of D is omitted. The reduced digital code D^* is an 8-bit code in standard binary two's complement representation, where $D^* \in [-127, 127]$. Note that the DHP reinterprets these codes in an 8-bit unsigned representation $\in [0, 255]$. The pipeline ADCs sample the input currents at a rate of 100 ns. The dynamic range for each ADC is in the order of 32 μA but can be adjusted (see next section) and depends on the dynamic ranges of the current memory cells. Nominally, the current memory cells have a dynamic range of $[-8, 8]\,\mu$A, i.e. a 16 μA range. The first stage of the pipeline ADCs is implemented slightly differently than the following stages, both double cell blocks are written simultaneously, which extends the overall nominal ADC dynamic range to 32 μA. Table 4.1 states the design specifications of the DCD-Bv4-Pipeline version.

Via the calibration circuit it is possible to inject a know current, either into the TIA or directly into the ADC of one channel at a time. The *fast or internal injection* uses a DCD internal current source, controlled by the 9-bit DAC VPInjSig, for injecting currents into a selected channel. This procedure is fast, but allows only coarse current steps. The *external injection* uses an external current source, which is connected through a monitor pin. The DHH back-end electronics provide a highly linear, finely tunable current source that can be connected via the monitor pin. Currently under study is the idea of using the DEPFET transistors as an adjustable current source for injecting currents into all DCD channels in parallel.

property	**value**
number of ADCs	256
ADC resolution	8-bit
ADC sampling rate	100 ns
ADC noise	80 nA - 120 nA
signal-to-noise ratio (for a MIP)	> 17
input amplification factor (TIA)	1 / 2
ADC LSB value	160 nA / 80 nA
max. dynamic input range	40 μA / 20 μA

Table 4.1: Overview of the design specifications of the DCD-Bv4-Pipeline ASIC as given in the design manual [15].

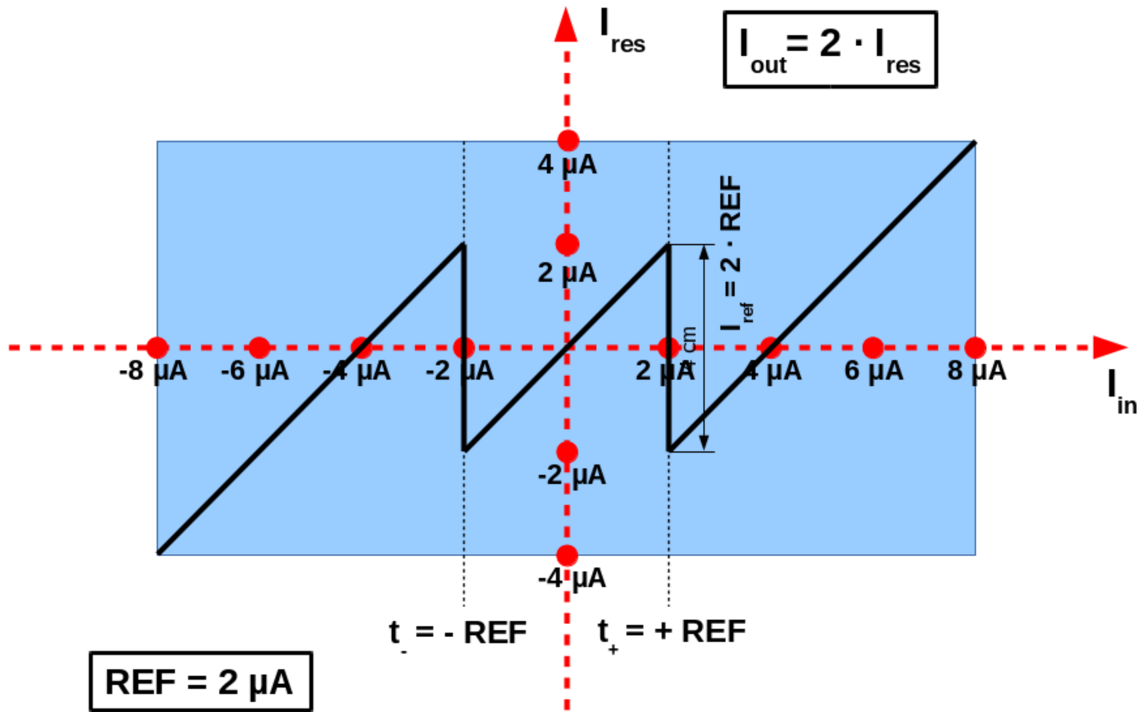

Figure 4.1: Input/output current relation of one pipeline ADC stage in the ideal case. The positive and negative thresholds are at $t_\pm = \pm 2\,\mu$A, the reference current added or subtracted is $4\,\mu$A. The blue box indicates the dynamic range of the current memory cell (here $[-8, 8]\,\mu$A) storing the input current on the x-axis. The effective dynamic range of the CMC of the next stage (y-axis) is halfed, as the residual current I_{res} is multiplied by a factor of two when fed into the next ADC stage. The figure was adapted from [19].

4.1.1 Current Memory Cells and Comparators

The pipeline ADC operation relies on the functioning of the current memory cells (CMC). Figure 4.2, left hand side, shows the basic layout of a single current memory cell as it is used in the DCD design. It makes use of an amplifier (A) and a transconductor (TC), the capacity C_f acts as the memory element. The current memory cell is designed to store currents in the range of $[-8, 8]\,\mu$A while keeping the input potential at a value of 1 V. For writing a current to the cell at node 1, switches 1 and 2 are closed and the capacity C_f is charged. The amplifier, which is assumed to have infinite gain and no offset, generates a potential proportional to the input current at node 3. The transconductor generates a feed-back current at node 4, that increases until it compensates the input current completely. When switch 1 is opened again, the potential across C_f is frozen. For reading, only switch 3 is closed and the stored current, generated as the TC feed-back current via the frozen potential at node 3, is flowing out of the cell. The operation of the current

memory cell can be adjusted by changing several DAC settings and supply voltages (see figure 4.2, right hand side). The amplifiers use the ground potential labelled as *AmpLow*. The transconductors have adjustable sourcing (*FBPBias*) and sinking (*PSource2*) current sources. To be able to add and subtract currents, as required by the CRSD-algorithm, the current source *PSource* is present at node 4. The nominal value of *PSource* is 8 μA, but it is configurable via a DAC called *IPSource*. According to the output of the comparators, *PSource* is changed by $\pm 4\,\mu$A, thus acting as the reference current I_{ref} which is added or subtracted in the CRSD conversion algorithm.

The implementation of the comparators is very similar to that of the current memory cells. The transconductor with the current source *PSource* acts as the input stage and is almost identical to the one used in the current memory cells and uses the same biasing current sources *FBPBias* and *PSource2*. The difference is the value of *PSource*, which is changed by $+2\mu$A for a high comparator or $-2\,\mu$A for a low comparator, thus acting as the thresholds $t_{\pm}$ used in the CRSD-algorithm. The comparators also implement amplifiers which share the ground potential *AmpLow*. The supply *RefIn* is used at several nodes as a current dump and as a fixed potential reference, both in the CMCs and the comparators.

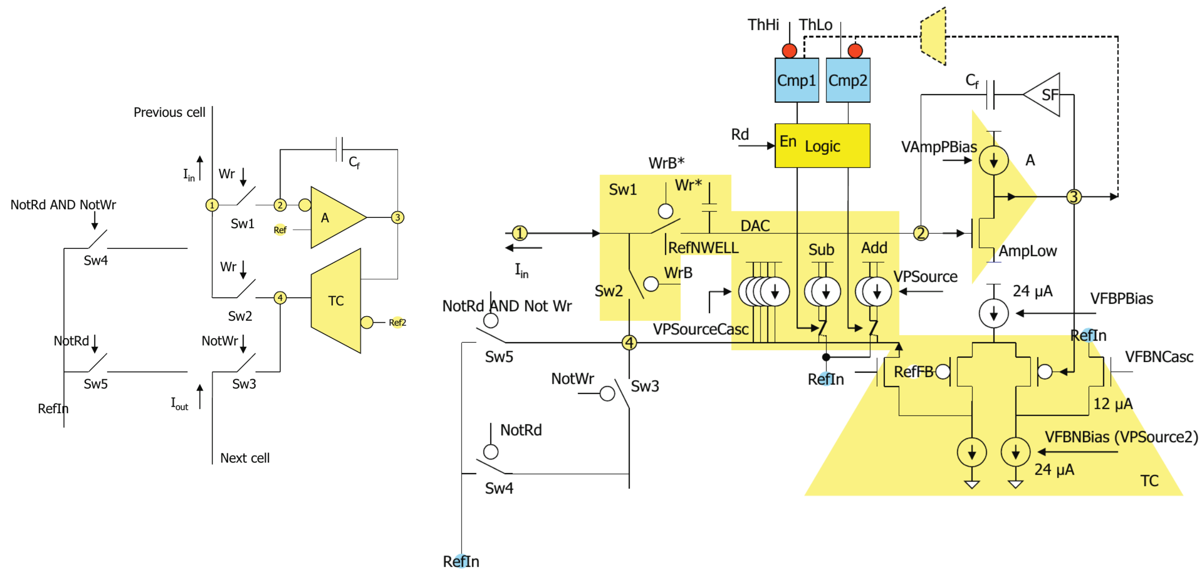

Figure 4.2: Basic (left) and more detailed (right) layout of the current memory cells used in the pipeline ADCs implementation as part of the analog channels of the DCD [15].

4.1.2 Parameters for Adjusting the Analog Performance

As already seen, there are several parameters, DACs and supply voltages, that influence the operation of the pipeline ADCs in the analog channles of the DCD. For optimizing the

DCD operation, one needs to find the optimal working point, i.e. the set of settings for which all ADC channels show best performance. There are three important DAC settings that influence the functionality of the current memory cells and the comparators [13, 15]:

- **IPSource** [**DAC**] shifts the comparator reference current REF and determines the total dynamic range of the ADC. A value of 64 corresponds to a total dynamic range of 16 μA, while a value of 120 corresponds to a 32 μA range.
- **IPSource2** [**DAC**] controls the working point of the transconductors used in the current memory cells and the comparators. From design its value should be equal to IPSource.
- **IFBPBias** [**DAC**] is the biasing current of the transconductors in the CMCs and the comparators. From design its value should be equal to IPSource. IFBPBias and IPSource determine specifically the dynamic range of the current memory cells.

There are three analog supply voltages for the DCD [13]. The powering of the analog part is supplied by DCD_AVDD, which is set to 1.8 V. The two other voltages are:

- **RefIn** [**voltage**] is used as a reference at several nodes in the CMCs and the comparators. The design value is 1 V at 50 mA.
- **AmpLow** [**voltage**] is the ground potential for the amplifiers in the CMCs and the comparators. A change in AmpLow can shift the input characteristic of the CMCs and can also affect their dynamic input range. The design value is 300 mV at -247 mA.

The DCDs on one half-ladder module share the same RefIn and AmpLow voltages while the DACs can be configured individually. Figure 4.3 indicates the dependence of the current-memory cells dynamic range on the DAC settings and on the position on the DCD chip. A higher bias (higher DAC values) increases the CMCs dynamic range. However, the dynamic ranges are not necessarily symmetric and the asymmetry may grow with higher DAC settings. Also, there seems to be a shift of the dynamic range for CMCs far away from the supply pins, which hints to voltage drops across the DCD chip. The dependence of the CMC dynamic range on the voltages RefIn and AmpLow is indicated in figure 4.4. RefIn does not change the characteristic of the CMC. Lower AmpLow values reduce the CMC dynamic range and shift the input characteristic towards the positive range.

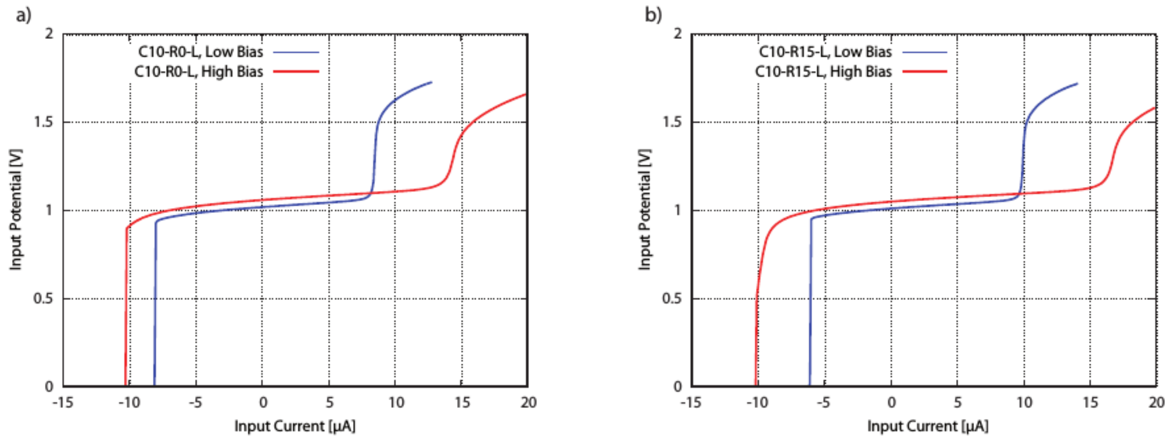

Figure 4.3: Dependence of the current memory cells input characteristics on the DACs IPSource, IPSource2 and IFBPBias. High bias means all three DACs at 120, low bias means all three DACs at 60. On the left, a CMC close to the power supply pins of the DCD is shown, on the right a CMC on the other end of the DCD chip [13].

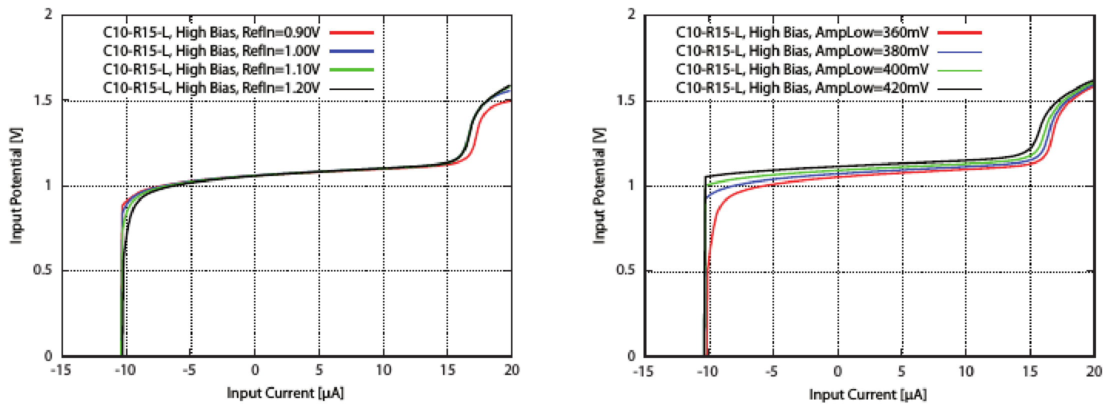

Figure 4.4: Dependence of the current memory cells input characteristics on the voltages RefIn (left) and AmpLow (right) [13].

4.2 Inter-ASIC Communication

The digital 8-bit codes computed by the ADCs in the DCD channels are sent to the DHP ASIC via several links. The 256 analog channels of the DCD are arranged in eight so called *column pairs*, thus each column pair contains 32 ADCs. Each column pair has eight communication links on which the eight bits of one ADC code are sent in parallel. The total 32 ADC codes per column pair are sent one after another, serially, over the eight links. In total, this requires 8 links $\times$ 8 column pairs, 64 links from DCD to DHP for the ADC data transmission. The serialization is necessary as the number of links is

limited due to the available space for routing on the module. The timing requirement, as mentioned in section 2.2.2, is a read-out time of 100 ns per row segment of the DEPFET matrix. That means, the serial data of 32 ADC codes per column pair has to be sent in 100 ns, which translates into a required clocking frequency of 320 MHz. This 320 MHz high clock DCD_CLK is provided by the DHP to the DCD. A second clocking signal SYNC_RESET is used to synchronize all digital logic in the DCD and is also provided by the DHP. All clocking signals are derived from a global reference clock GCK, which is provided by the back-end electronics in the DHH. The value of GCK can be adjusted to operate the front-end electronics at different frequencies. The high frequency DCD_CLK clock is generated via division by four of GCK, thus the nominal GCK value is 80 MHz. The timing of all eight column pairs of the DCD is identical.
The analog channels of the DCD provide the possibility of an analog pedestal correction via a 2-bit DAC (see section 4.1). This DAC value can be set for each geometrical pixel of the DEPFET matrix individually and is stored in a pedestal memory in the DHP. During the rolling-shutter read-out, it is necessary to consecutively upload these pedestal values to the corresponding DCD channels to perform a proper pedestal correction. This is done in a similar way as for the ADC data transmission. Each DCD column pair has two additional links, over which the 2-bit pedestal DACs are uploaded to the DCD. This requires additional 2 links $\times$ 8 column pairs, 16 pedestal upload links from DHP to DCD. The clocking behaviour is similar to that of the data links and identical for all pedestal upload links. Issues concerning the pedestal upload link communication will not be discussed here, details can be found for example in [20]. In this thesis, the discussion will concentrate on the communication over the 64 data links. Figure 4.5 sketches the signal and data flow between the front-end read-out ASICs.

4.2.1 Data Links Communication: Signal Delay Compensation

The 64 data links from DCD to DHP, as well as the 16 pedestal upload links from DHP to DCD, share the clock timing at which data is send and received. The routing of the links and the strength of the output drivers, however, may differ slightly between links. As a result, the data is send out synchronously on DCD side, but it not necessarily arrives synchronously on DHP side. The receivers on DHP side will sample all data links synchronously at the same time, which introduces the question of how to cope with the asynchronism induced by the varying routing and output driver strengths. Several delay elements have been added to the DHP design to allow for delaying of individual signals. As described above, data from the DCD is send out according to DCD_CLK, which is generated in the DHP. Delaying the DCD_CLK signal thus introduces a phase shift

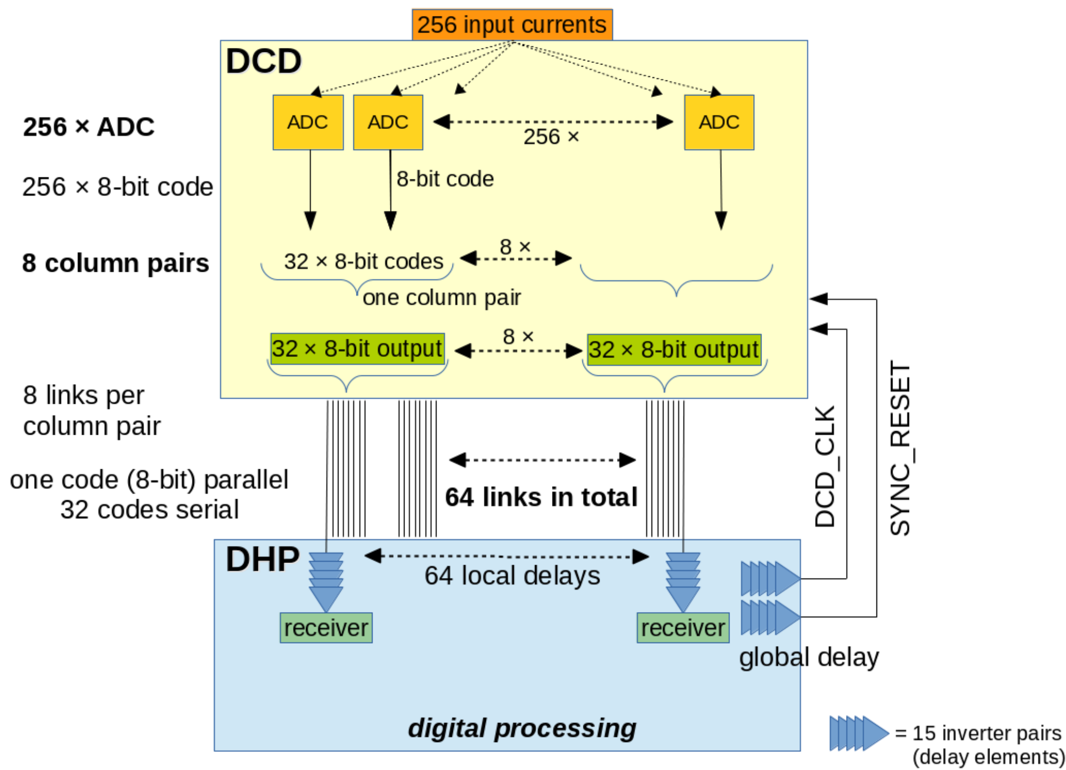

Figure 4.5: Sketch of the data flow in the front-end read-out system and the communication among the ASICs.

between the DCD data sending and the DHP data sampling. The delay is achieved via a cascade of inverter pairs (delay elements). In total, 15 inverter pairs are cascaded, each adding a delay in the order of some 100 − 1000 ps. The number of inverter pairs, by which the clock signal is delayed, can be set with a 4-bit JTAG register entry. The same delay architecture is also available for the SYNC_RESET signal. It is reasonable to always delay DCD_CLK and SYNC_RESET by the same amount to ensure synchronicity of the clock signals, so both JTAG register entries will always be set to the same 4-bit value and we call this the *global delay*, as it affects all DCD-DHP communication links in the same way (see figure 4.5). The global delay can take values between 0 (no delay) and 15 (maximal delay, all inverter pairs active). Individual delay of the data links is also possible via the same mechanism. Each link can be delayed through 15 inverter pairs and has its own 4-bit JTAG register for configuring the amount of delay. The 64 4-bit data link delays are denoted *local delays* (see figure 4.5). These delay elements delay the actual signal on the link line. For one specific link, local and global delay accumulate, thus a total delay of 30 inverter pairs is possible. The exact value each inverter pair adds to the delay of the signal depends and the clock frequency and the digital supply voltage of the

DHP. Additionally, it cannot be assumed that a global delay element and a local delay element add the same amount of delay. Optimal values for the 64 local delays and the single global delay have to be found to assure proper DCD-to-DHP data transmission. The optimization of the delay settings will be discussed in chapter 7.

The data transmission uses low voltage single-ended signalling (LVSE) for sending the ADC output codes from DCD to DHP. The voltage swing and the reference potential are generated in the DCD and are fixed by design, it is not possible to tweak these parameters to improve the data transfer. Measurements of the current DCD and DHP ASICs showed asymmetric rise and fall times of the data signals, a new iteration of the DHP chip, the DHPT1.1, was submitted with improved data signal receivers [21].

5 Experimental Setups for ASIC Testing

Several testing systems and setups have been developed and are used to investigate the performance of the read-out ASICs and the full front-end read-out system. Extensive work on the testing and the debugging of previous iterations of the DCD chip have been carried out by [8] and [13]. A versatile interface system is needed to test the ASIC functionalities. Several such systems are available, two of these, the Hybrid5 boards and the electrical multi-chip modules (EMCMs) have been used for measurements in the scope of this thesis and will be discussed in the following.

5.1 The Hybrid5: A PCB-based ASIC Testing Interface

In the final PXD system, the read-out ASICs will be bump-bonded onto the all-silicon modules. It is, however, useful to decouple the module design (metallization and routing) from the pure ASIC testing. For this purpose the Hybrid5 boards were developed, which implement all routing on a genuine PCB[1] and provide several probing and testing pads on PCB-level [8]. The ASICs are bump-bonded to a silicon wire-bond adapter, which is glued to the PCB. The adapter routes the ASIC pads to be accessible by wire-bonds, the inter-ASIC communication links are routed purely on the adapter. The wire-bond interconnection from the adapter to the PCB connects all power supply, JTAG control and high-speed data lines. Figure 5.1 shows a picture of a Hybrid5 board. Each Hybrid5 is equipped with one DCD and one DHP ASIC. Optionally, a SWITCHER ASIC and a DEPFET matrix can be added, thus providing a small scale testing emulation of the full front-end read-out chain. All power supply and voltage sensing lines are connected to the PCB via a 30-pin Samtec[2] connector. The DHP sends out data to the back-end electronics via high speed links and it provides the JTAG interface for configuration of all ASICs.

[1] PCB = printed circuit board

[2] Samtec is a company focussed on electronic interconnections (www.samtec.com).

Both links, the high speed data link and the JTAG link, are realized as two separate InfiniBand[3] connections. With the Hybrid5 PCB, it is possible to probe all power supply potentials and also several clocking signals, thus providing an in depth ASIC testing tool.

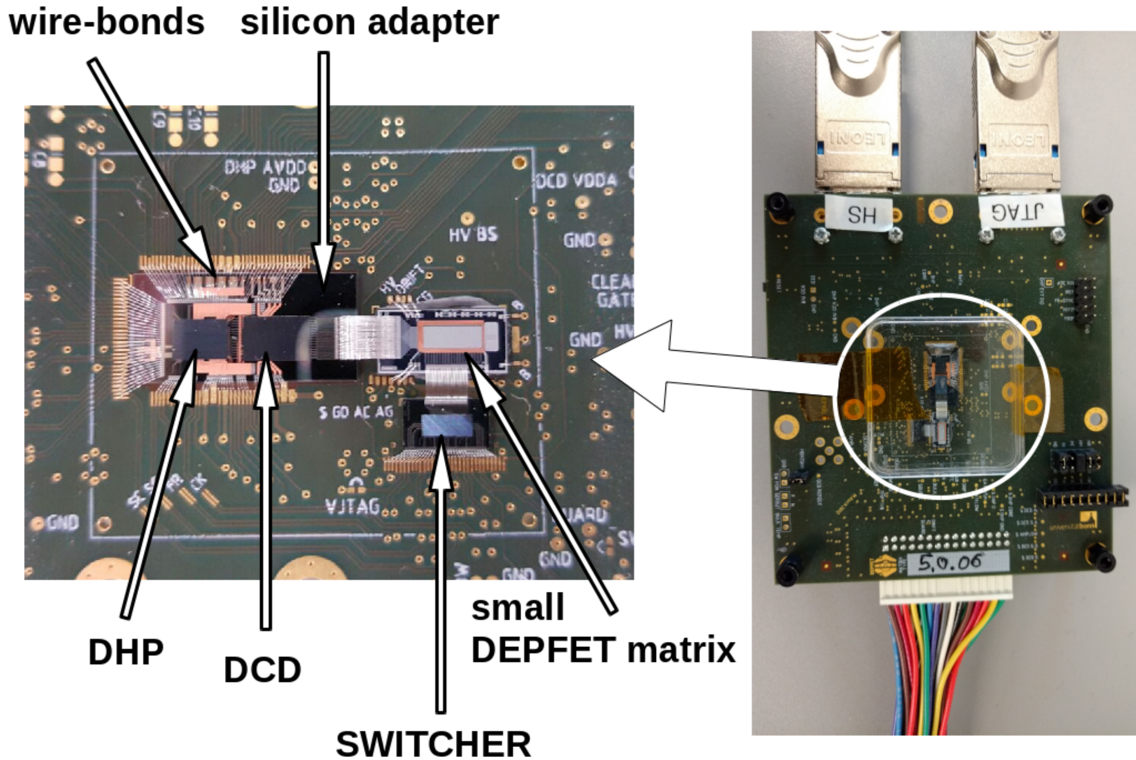

Figure 5.1: Picture of a Hybrid5 board equipped with a DCD and DHP ASIC and a small DEPFET matrix steered by one SWITCHER ASIC. The DCD and DHP are bump-bonded to a wire-bond adapter, which is glued on the Hybird5 PCB board. Interconnection between ASICs and the PCB is done via wire-bonding. The right-hand side shows the full Hybrid5 board with the InfiniBand (top) connections for the JTAG and high speed link interface to the DHH and the Samtec connector (bottom) for the powering.

5.2 Electrical Multi-Chip Modules

The electrical multi-chip modules (EMCMs) follow a more integrated approach. While a Hybrid5 board can be used to measure and debug a single ASIC pair (DCD+DHP) in great detail, an EMCM is much closer to the final sensor module situation. In fact, an EMCM is designed as a fully functional PXD half-ladder module, but without a DEPFET matrix.

[3]InfiniBand is a computer-networking communication standard providing very high bandwidth at low latency

Figure 5.2 shows a picture of an EMCM module. In total 4 ASIC pairs are present and bump-bonded onto a silicon support frame. The routing of power and data lines is done on the support frame and is close to the final sensor module design. Also, six SWITCHER chips are cascaded alongside the balcony of the EMCM module, with which the interplay of multiple SWITCHERs can be tested. The area normally occupied by the DEPFET matrix provides some testing and monitoring pads. With an EMCM, it is possible to study the full front-end read-out system in a final-like configuration and in addition, the routing on the silicon support frame is being tested. Still, the ASIC properties are measured completely decoupled from any DEPFET matrix properties. It is, however, possible to add a small matrix to an EMCM by gluing it onto the module and connecting it via wire-bonds to the provided pads. The connection of powering and data lines to and from the module is realised via a Kapton[4] cable connection. A three-layer Kapton cable is glued to the support frame and wire-bonds connect several Kapton cable pads to three banks of corresponding pads on the module. The same interconnection principle will be used for the final PXD half-ladder modules. The Kapton cable is attached to a PCB, serving as a patch panel, from which powering and data connections to the back-end electronics are maintained.

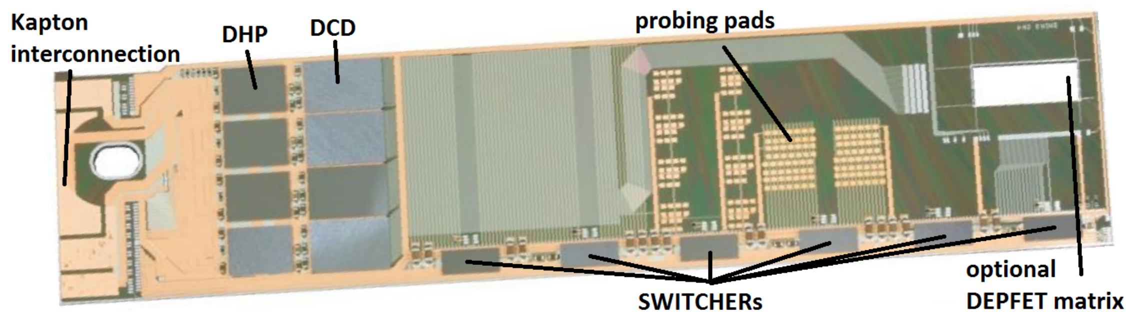

Figure 5.2: Picture of an electrical multi-chip module (EMCM) used to study the front-end read-out ASICs in a final module like configuration, including the routing on the silicon support frame. EMCMs can be equipped with a small DEPFET matrix, connection to the module is realized via a Kapton cable (not shown here).

5.3 Back-end Read-out and Laboratory Setup

The Hybrid5 and EMCM modules provide the interface to the ASICs and are now denoted as devices under test (DUTs). For testing of the read-out ASICs, a back-end read-out

[4]Kapton is a trade name for poly-amid films used in flexible electronics.

system is necessary. In the laboratory setups, the back-end electronics is represented by a single Data Handling Hybrid (DHH) system, which provides direct interface to a control PC. The DHH system is based on a field programmable gate array (FPGA), for fast data processing and the possibility of updating the firmware. The DHH communicates with the DHP ASICs on the DUT, this includes slow control via the JTAG interface and data reception, and provides a UDP[5] interface to a control PC. The DHH also implements a pedestal memory and a finely tunable current source, it is powered from a standard laboratory bench power supply. The powering of the DUT, and thereby the powering of the ASICs and an optional DEPFET matrix, is supplied by a self-developed power supply unit (PSU), which will also be used in the final Belle II experiment. The PSU needs a general, static powering provided from a standard bench power supply and an active emergency-stop voltage. Analog and digital supply voltages are routed separately via self-developed and self-fabricated cables to a break-out board (Hybrid5) or a patch panel (EMCM and final modules) and from there to the DUT via a Kapton cable (EMCM and final modules) or a 30-pin Samtec connector (Hybrid5). Figure 5.3 sketches the components and connections used in the laboratory setups. Figure 5.4 shows a picture of a Hybrid5 laboratory setup.

Slow control on the control PC is implemented using the EPICS[6] environment, from which the ASICs can be configured and the PSU voltages can be set. The same PC is also used for data acquisition (DAQ), a DAQ software reads the UDP data stream form the DHH and saves it to disk. In the final experiment the back-end read-out is more complex as multiple modules have to be read-out and data streams have to be merged. There, several DHH boards will be connected to one DHH-Controller (DHHC) device, handling low-level trigger signals and distribution slow control commands.

[5]The User Datagram Protocol (UDP) is a minimalistic, connectionless networking protocol.
[6]Experimental Physics and Industrial Control System (http://www.aps.anl.gov/epics/)

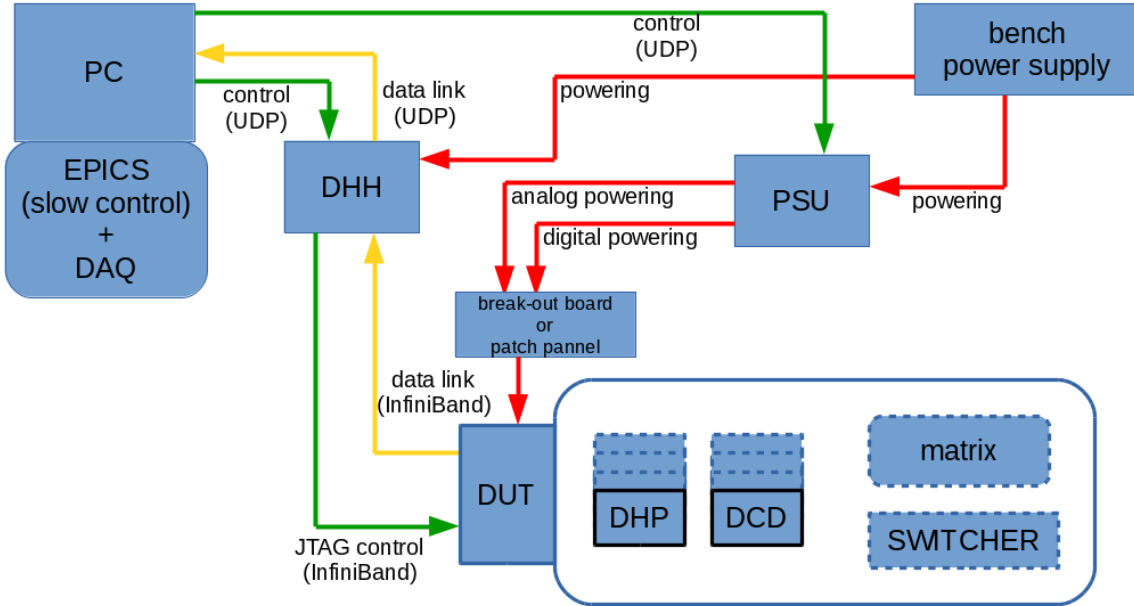

Figure 5.3: Sketch of the general laboratory setup for operating and investigating a device under test (DUT), an EMCM or Hybrid5 boards, providing the interface to the read-out ASICs. Slow control is provided from a normal PC via network packages (UDP) and JTAG (via InfiniBand cables) and indicated by green lines. Data is likewise send via InfiniBand and network connection (yellow lines). Power supply lines are marked in red.

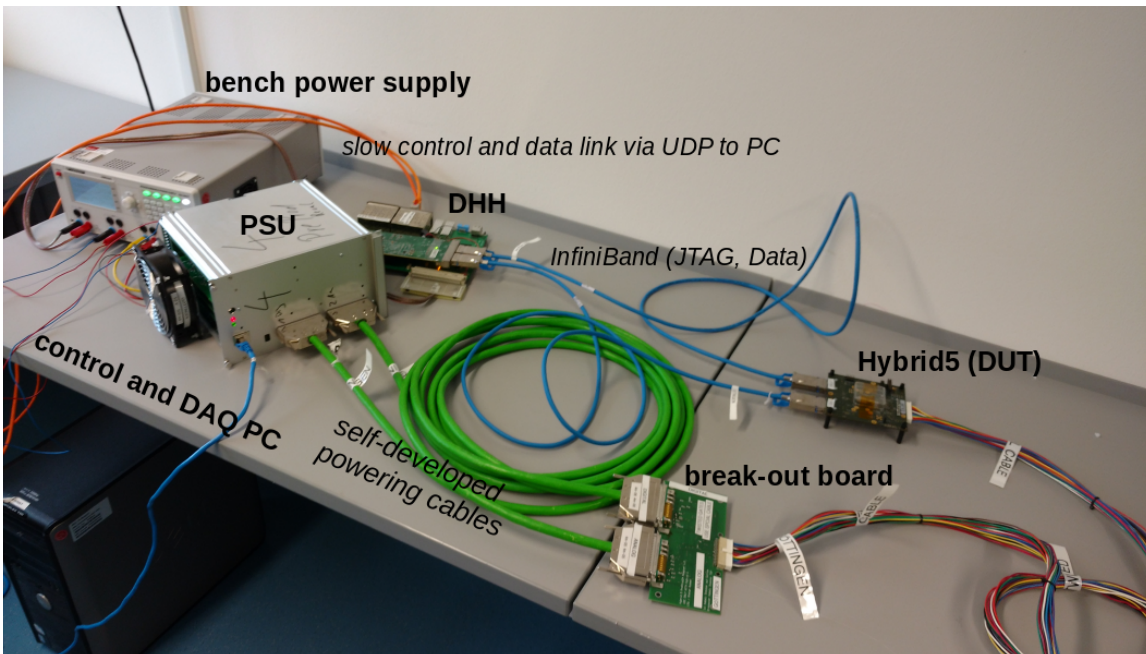

Figure 5.4: Picture of a laboratory setup with a Hybrid5 board as device under test (DUT).

6 Read-out ASICs Failure Identification

In the previous chapters, the read-out ASICs for the Belle II DEPFET sensor have been presented and the most important aspects of their current design implementations and functionalities have been discussed. Additionally, the testing setups used for measuring ASIC properties have been introduced. Section 4.1 discussed the ideal analog-digital conversion in the analog channels of the DCD ASIC. In order to study and optimize the functionality of the Drain Current Digitizer (DCD) ASIC and the inter-ASIC communication, several testing algorithms have been developed in the scope of this thesis. Simulation studies of the DCD analog-digital conversion and the DCD-to-DHP data transmission have been conducted, respecting the respective implementation details. Based on these results, testing algorithms were defined, that are able to identify specific failure scenarios in the ASIC operation. The figure of merit for evaluating the ADC performance and identifying failures therein is the ADC transfer curve as it was discussed in section 3.1. All testing algorithms run on these transfer curves and will be discussed in this chapter.

6.1 Drain Current Digitizer: Analog Performance and Failure Identification

The DCD chip implements 256 analog channel, each with a current-mode pipeline ADC. The functionality of all ADCs can be modified mainly by the three DACs IPSource, IPSource2 and IFBPBias, and the two supply voltages RefIn and AmpLow (see section 4.1.2). For each ADC, a separate ADC curve can be measured and analysed. The quality of the ADC curve, and thereby the functionality of the ADC, is evaluated regarding the dynamic range, noise and linearity.

6.1.1 Dynamic Range

The nominal dynamic range of the current memory cells is $[-8, 8]\,\mu$A. The TIA, acting as the current receiver in the analog channels, can be programmed to perform an additional amplification of the input current by a factor of two (gain = 2) or no amplification (gain = 1). Thus the effective input range for the analog channel is either $32\,\mu$A (gain = 1) or $16\,\mu$A (gain = 2), a higher gain means a finer AD conversion. However, the possibility for using gain = 2 is dependent on the overall pedestal spread of all DEPFET pixels and how much the spread can be compensated for by analog pedestal correction. The DCD ADCs digitize with 8-bit resolution, i.e. the nominal code range is 256. The fraction of dynamic input range over code range can be understood as the slope of the ADC curve and is 62.5 nA/ADU for gain = 2 and 125 nA/ADU for gain = 1, ADU stands for arbitrary digital unit and is used as the unit for the digital codes. This can also be understood as the smallest current that can be resolved by the ADC, i.e. the current corresponding to the least significant bit (LSB) which is exactly one ADU. This value can be measured by fitting a linear function to the ADC curve and extracting the slope of the fit. The value of the ADC curve slope depends on the relation and interplay of the CMCs dynamic ranges and the values of the positive and negative thresholds used in the comparators. Both depend on the previously explained DACs IPSource, IPSource2 and IFBPBias and the supply voltages RefIn and AmpLow. For a fixed slope a reduction in the dynamic range translates directly into a reduction of the code range. Thus, for analysing the ADC curve we determine the minimal and maximal ADC code, that were recorded for this curve, as code_min and code_max. A reduced code range means a smaller than nominal dynamic input range of the ADC. A slight reduction of the code range is accepted. Thresholds for the minimal and maximal codes are defined, if the maximal code is below or the minimal code is above the corresponding threshold, a code_min or code_max error is identified for the ADC curve. Figure 6.1 shows a simulated ADC curve with a reduced dynamic range. The simulation was implemented according to the CRSD-algorithm of the DCD with the nominal CMCs dynamic ranges, except for stage 0 where the CMC ranges were reduced to $[-6, 8]\,\mu$A.

6.1.2 Noise and Linearity

The noise σ_i of the ADC curve at input current DAC i is defined as the standard deviation of the output codes at that DAC, it has units of ADU. As a measure for the noise of the ADC channel the median of all σ_i of the ADC curve is used. Of course, low noise performance is favoured. The noise measured via the ADC curve is the combined noise

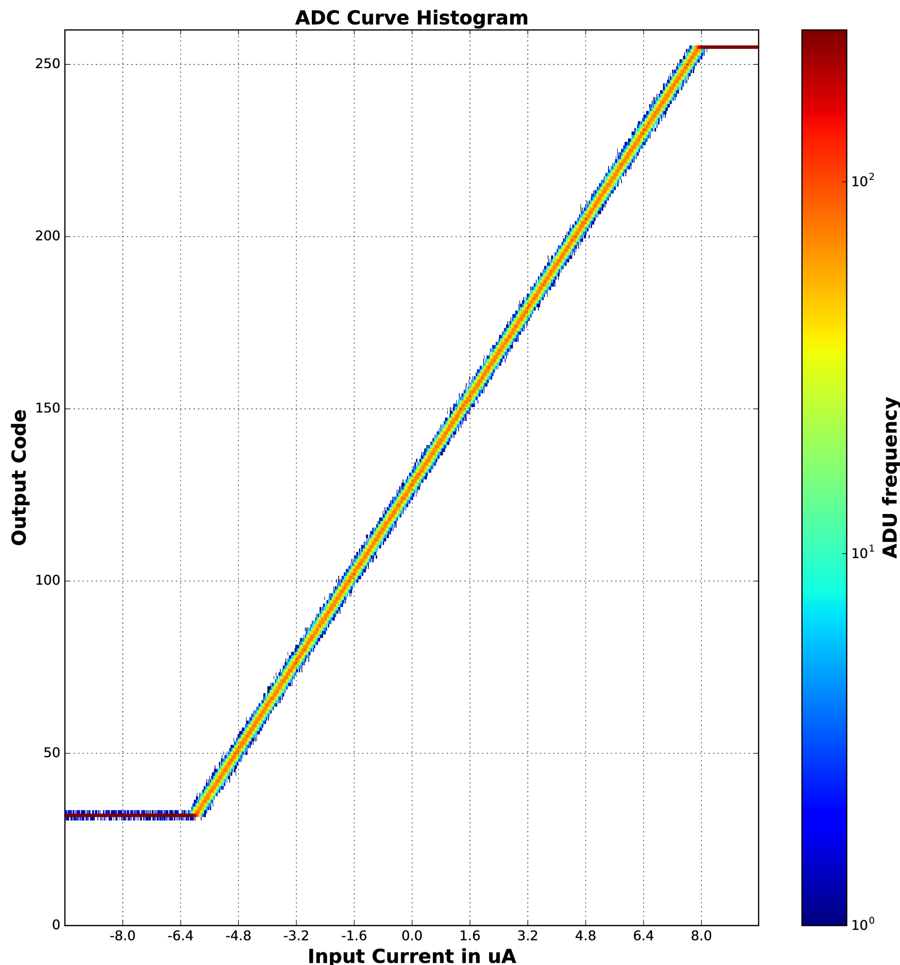

Figure 6.1: Simulated ADC curve with a reduced dynamic range resulting when the CMCs dynamic ranges of stage 0 are reduced to $[-6, 8]\,\mu$A.

of several sources:

- the current source noise σ_{source},
- noise introduced by routing of the current σ_{route},
- noise introduced by the current receiver σ_{TIA},
- and the noise of the pipeline ADC σ_{ADC}, which in turn is a convolution of the noise of the current memory cells and the comparators.

Only when using an external current source, its noise can be measured separately. The individual noise sources of the analog channel cannot be disentangled easily with the Hybrid5 and EMCM setups. Previous measurements done by [13] show a significant noise contribution from the current memory cells and some contribution from the TIA.

The DCD-Bv4 reference manual states an expected average noise per ADC of around 80 nA and a maximal system noise of around 120 nA, this translates to a noise value of $1 - 2$ ADU [15]. For evaluation of the quality of the ADC operation regarding noise, the ADC curve noise value is compared to a testing threshold, which is usually in the expected order of $1 - 2$ ADU. If the noise exceeds the given threshold, a noise failure of the ADC is identified.

A high linearity of the ADC curve assures a constant digital resolution over the full dynamic input range of the ADC. As a single measure for the non-linearity of the ADC curve, the INL peak-to-peak (INLpp) value as defined in equation 3.3 is used. According to the DCD-Bv4 reference manual, an INLpp value of < 6 ADU is allowed for the ADC non-linearity [15]. By setting an appropriate testing threshold for the INLpp value, the ADC curves are tested for high non-linearities. If the INLpp value exceeds the threshold, an INLpp failure for the ADC curve is identified. The code range, noise and INLpp values can be considered the fundamental measures for evaluating the quality of an ADC curve. However, they do not provide detailed information on the malfunction of the ADC. By conducting simulation of the functionality of the pipeline ADCs used in the DCD, and the DCD-DHP communication, we are able to link specific ASIC failure scenarios to clearly identifiable topologies and patterns in the ADC curves. These will be discussed in the next sections.

6.1.3 Comparator Offsets and Long Codes

Section 4.1 discussed the ideal analog-digital conversion of the pipeline ADCs. The conversion algorithm relies on the proper relation between the CMCs dynamic range, the values of the positive and negative comparator thresholds and the value of the added or subtracted reference current. The influence of non-optimal CMC dynamic ranges have already been discussed. The CMCs use the current defined by the DAC IPSource as the added/subtracted reference current. The comparators also make use of IPSource and derive the thresholds from it (see section 4.1.1). Thus, the reference current is properly defined by the DAC, while the thresholds can be subject to variations that arise due to mismatches of transistors that derive the thresholds from IPSource. Starting from the ideal input-output relation of one ADC stage (figure 4.1), let us consider the case of a small positive offset of the threshold of the high comparator of $+1.8\,\mu$A. Figure 6.2 shows the input-output relation for this case, the positive threshold is at $3.8\,\mu$A as opposed to the nominal $2\,\mu$A. Figure 6.3 shows a simulated ADC curve where the high comparator in conversion stage 0 has an offset of $+1.8\,\mu$A. A small positive offset ($< 2\,\mu$A) does not seem to have any influence on the AD conversion, the ADC curve does not show any arte-

facts. This is true for any offset, positive or negative, of the high or the low comparator threshold, as long as the absolute value is $< 2\,\mu$A. Thus, to some extend, the implemented AD conversion is robust with respect to small threshold shifts.

Let us now consider the case where the positive comparator threshold has a large offset, i.e. the threshold is shifted to a value $> 4\,\mu$A. Figure 6.4 shows the input-output relation for this case ($t_+ = 4.5\,\mu$A). For a certain range of input currents, as indicated by the red circle, the output currents lie outside of the output range, i.e. dynamic range of the next CMC. All currents outside of the output range will be stored as the same current, the maximal current of the next CMC cell. In these cases, information on the exact currents is lost and all following stages will produce the same digital output for all input currents in the indicated range. Especially, the final 8-bit output code computed by the ADC will be the same for these input currents, that means the output code is clamping to a specific value for a range of input currents. This behaviour can clearly be seen and identified in the ADC curve as shown in figure 6.5, which is a simulation of the described offset case. A certain output code is clamping for a specific input range and a range of output codes is not observed at all (*missing codes*).

A large comparator threshold offset causes one or multiple output codes of the ADC to appear more often than all other codes (*long codes*) and is accompanied by a gap of missing codes with a width equal to the length of the long code. The ADC curves DNL is the ideal measure to identify long codes and missing codes. Figures 6.6 and 6.7 shows two examples of simulated ADC curves with comparator offset errors and their corresponding DNL curves. Output codes that are long codes show a high DNL peak, while missing codes produce DNL $= -1$ valleys. We developed a testing algorithm that scans the DNL curve for long code peaks and missing code valleys and that is able to infer on the specific comparator offset error type and the value of the threshold offset by considering the number and periodicity of DNL peaks and measuring the width and position of negative DNL valleys relative to the DNL peaks. We observed that large comparator offsets can be present in all ADC stages and in all combinations of positive/negative offsets in the high/low comparators. We are, however, able to optimize the DCD operation parameters and thereby reduce the number of comparator offset errors significantly (see section 7.2) by employing our testing framework. The optimization of the DCD analog performance relies extensively on the comparator offset DNL testing algorithm.

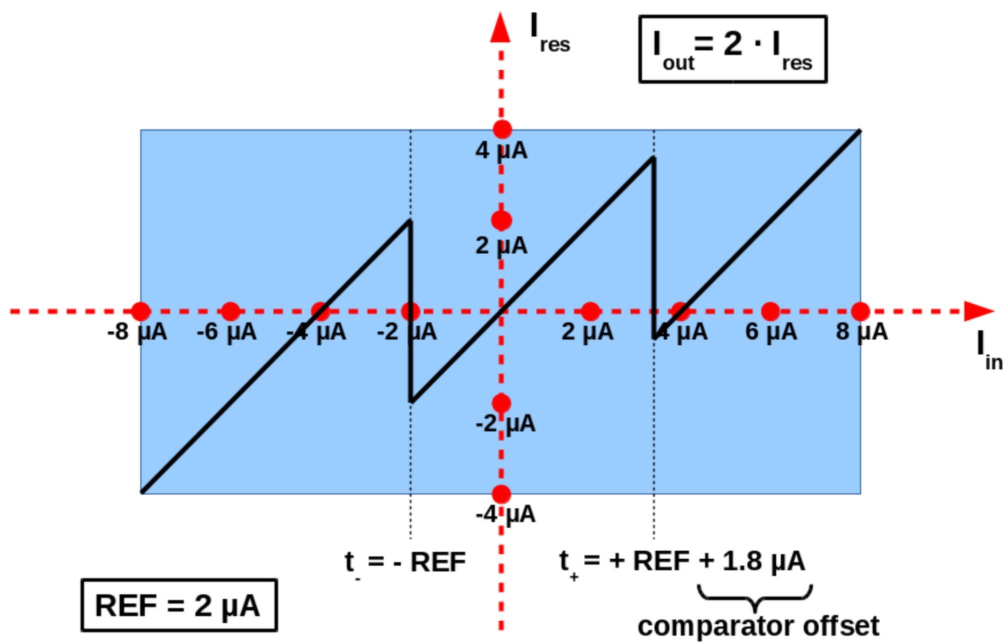

Figure 6.2: Input-output current relation of one pipeline ADC stage in the case of a small positive offset of the positive comparator threshold of $+1.8\,\mu$A.

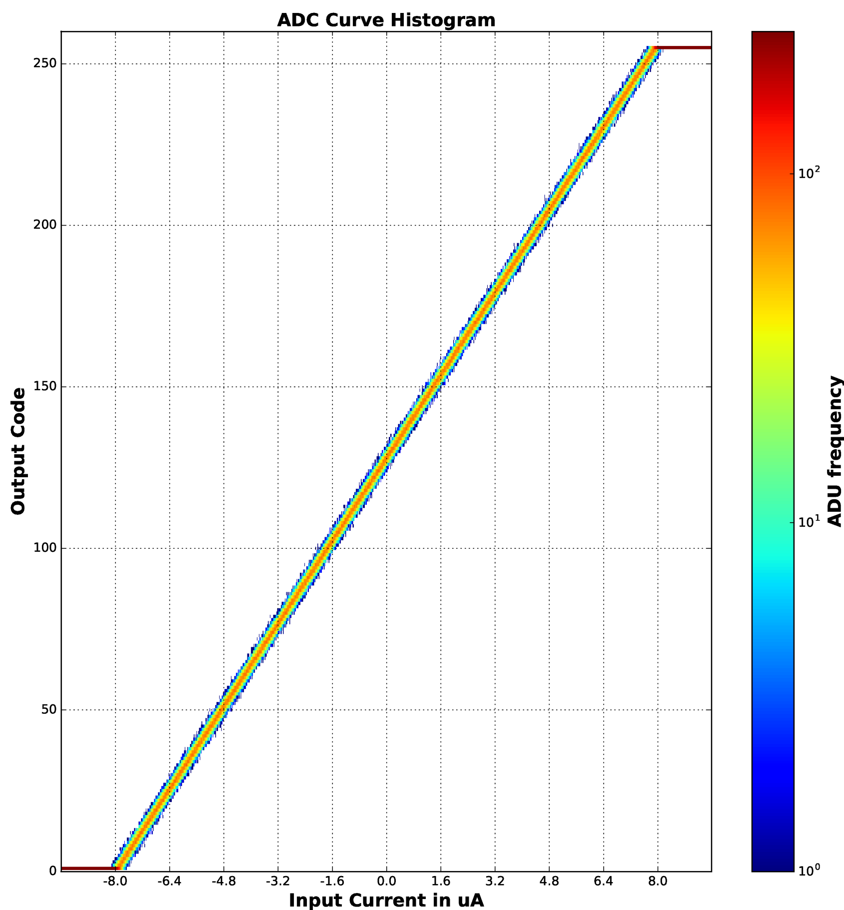

Figure 6.3: Simulated ADC curve for the case of a small positive offset ($+1.8\,\mu$A) of the high comparator in stage 0. The small offset does not cause any artefacts in the ADC curve.

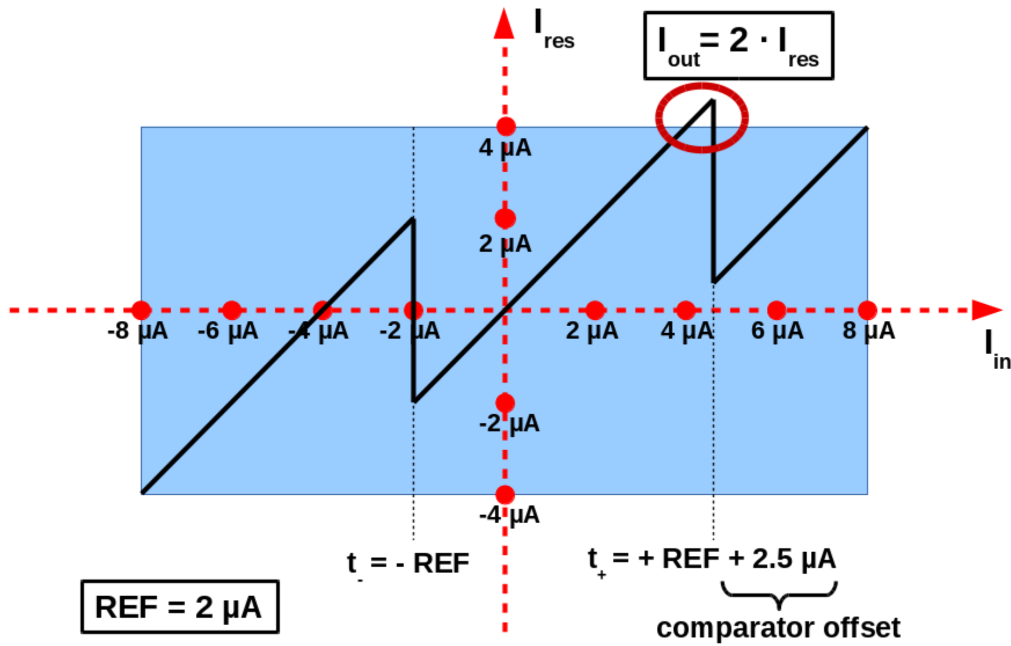

Figure 6.4: Input-output current relation of one pipeline ADC stage in the case of a large positive offset of the positive comparator threshold of $+2.5\,\mu$A.

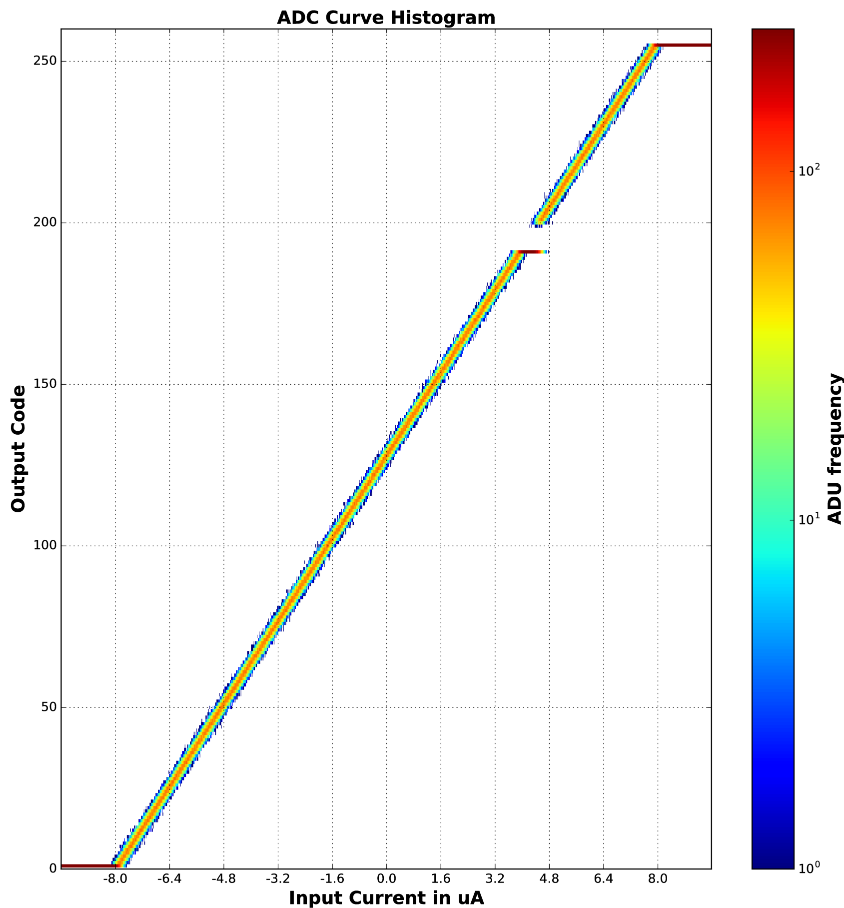

Figure 6.5: Simulated ADC curve for the case of a large positive offset ($+2.5\,\mu$A) of the positive comparator in stage 0. A large comparator offset causes a long code and a gap of missing codes in the ADC curve.

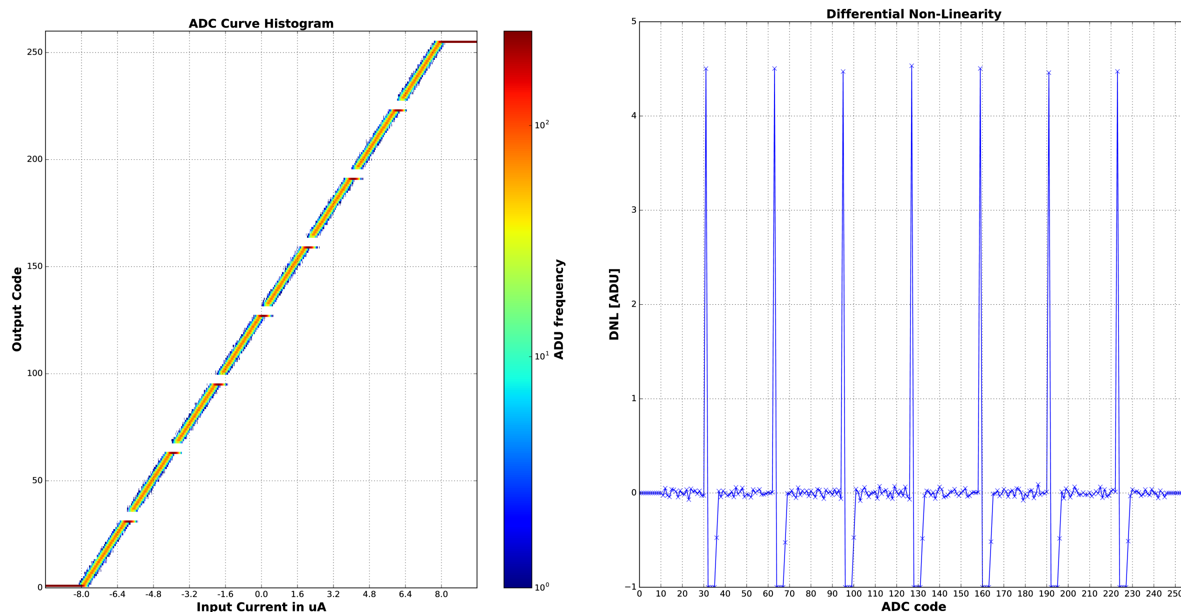

Figure 6.6: Simulated ADC curve (left) with an offset of $+3.0\,\mu$A of the low comparator threshold in stage 2 resulting in a periodic pattern of long codes and missing code gaps. Te right plot shows the corresponding DNL curve.

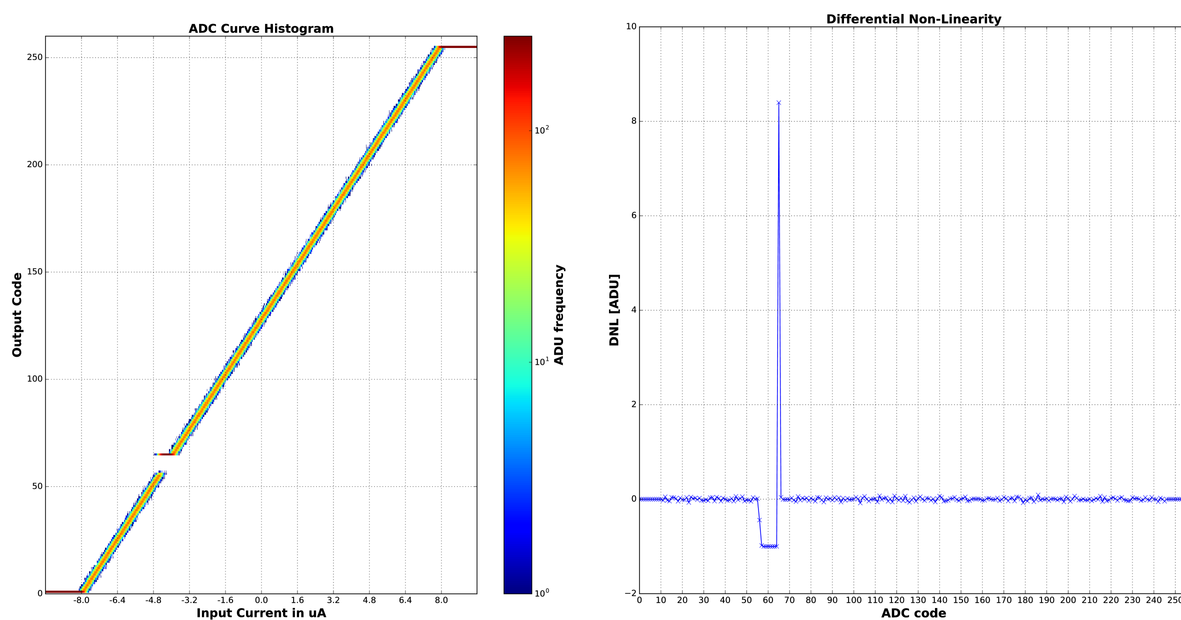

Figure 6.7: Simulated ADC curve with an offset of $-2.5\,\mu$A of the low comparator threshold in stage 0 (left) and the corresponding DNL curve (right).

6.2 Inter-ASIC Communication Failures

The first critical step of the front-end read-out chain is the correct digitization of the DEPFET currents in the analog channels of the DCD. The next critical phase is the transmission of the ADC codes from the DCD to the DHP ASIC. The 8 column pairs of the DCD, each made up of 32 analog channels, send their ADC codes over 8 physical links each. 32 ADC codes per 8 links are send serially in 32 clock cycles. For each link there is an output driver on DCD side. The output drivers task is to pull the line potential up to the voltage representing the digital 1, if the currently transmitted code in the respective clock cycle requires the transmission of bit value 1 on that link. Let us consider the total failure of one of the 8 links. This could mean

- the physical line is damaged and the signal is not received at DHP side, or
- the links output driver is too weak or failing completely to pull the link up to the digital 1 voltage.

In either case, the DHP will always receive a digital 0 on this link. Let us assume an ideal ADC converting the input current interval $[-8, 8]\,\mu$A to the output code range $[0, 255]$ and a totally failing link 7, which transmits the most significant bit (MSB) of the 8-bit ADC codes. In this scenario, the input currents $[-8, 0]\,\mu$A will be correctly mapped to the output codes $[0, 127]$. However, all currents in the interval $(0, 8\,\mu]$A will also show the output codes $[0, 127]$, instead of $[128, 255]$, because the MSB is always received as 0. The resulting ADC curve will show a sawtooth behaviour as seen in figure 6.8. A completely failing link will, however, only affect the analog channels and the ADC curves for the 32 ADCs belonging to the corresponding DCD column pair. In our nomenclature we refer to these cases as *stuck bits*. These are rare extreme cases, where a DCD-to-DHP communication link is completely broken. We may also investigate more subtle communication issues. The communication links between DCD and DHP are routed very densely between the two ASICs on the silicon support frame (EMCMs and final modules), or on the ASIC wire-bond adapter (Hybrid5), respectively. Because of the dense routing, cross-talk effects between links cannot be excluded. Cross-talk means that due to capacitive coupling, pulling up or down the potential on one link can influence the potential on the neighbouring links. Assume link i is supposed to pull up from digital 0 to digital 1, while the two neighbouring links $i + 1$ and $i - 1$ pull down to digital 0. In such cases it can happen, that the cross-talk is strong enough to prevent the pull-up on link i. However, this situation would occur only rarely and the output codes are mainly transmitted correctly. We call this a *toggling bit*, where the bit has a certain probability

to be transmitted wrongly. Not only the transition $0 \rightarrow 1$ can be affected, cross talk may also prevent the transition $1 \rightarrow 0$. In general, we refer to any communication issues as *bit errors*.

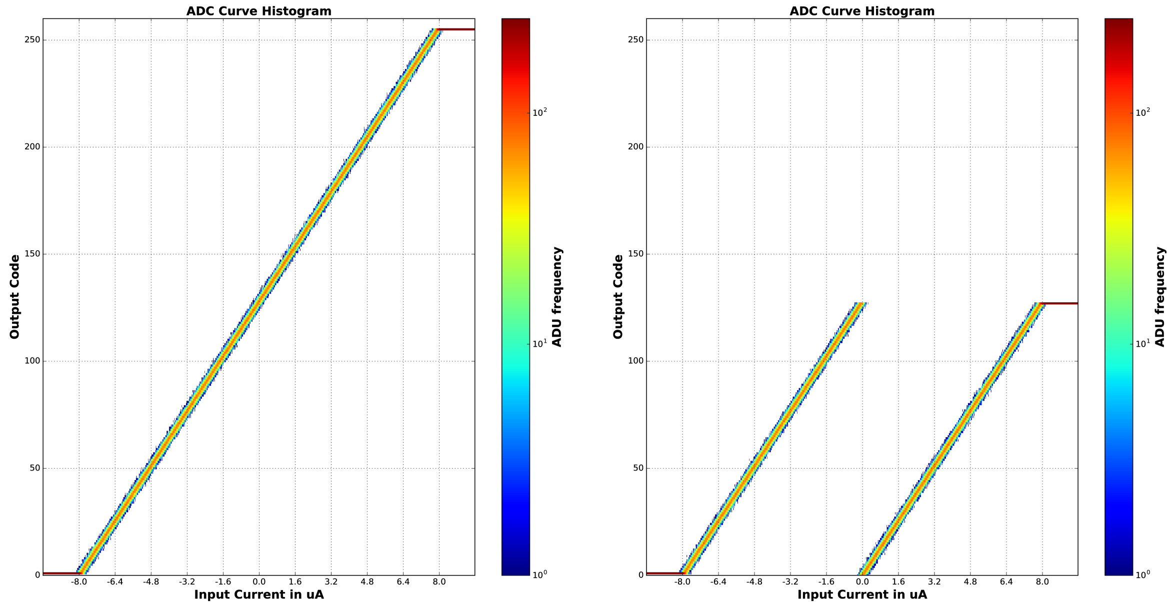

Figure 6.8: Simulated ADC curve in the ideal case (left) and in case the MSB of the output codes is always 0 due to a failing DCD-DHP communication link.

6.2.1 Bit Error Recognition in Transfer Curves

When recording ADC curves with the presented laboratory setups, it is not possible to decouple DCD-DHP communication issues from the DCD analog testing. We need to develop tests that are able to distinguish between DCD analog issues and communication issues. From simulating total or partial failures of DCD-to-DHP communication links, some interesting observations can be made. A toggling or stuck bit i shows a very distinct pattern in the ADC curve by which it can be identified. In general, a bit error of bit i causes a fragmented ADC curve, where parts of the curve are shifted up or down regarding the ADC code axis. For bit i the shift of the fragmented parts with respect to the nominal curve is exactly 2^i and the length of the fragments is 2^i codes. An upward shift means bit i is received as digital 1 when it should nominally be digital 0, i.e. the transition $1 \rightarrow 0$ for link i is problematic. Analogously, a downward shift indicates a problematic $0 \rightarrow 1$ transition. The number and position of fragmented parts is clear, as an upward shift can only happen for codes for which bit i is 0 and a downward shift only for codes where bit i is 1. For a stuck bit i all possible curve fragments are shifted up or down,

resulting in a very periodic pattern. When bit i is toggling, only parts of some fragments will show an up or down shift. From these observations, testing algorithms have been developed, which can be used to identify specific bit errors in ADC curves. Figure 6.9 shows simulated ADC curves generated for different toggling and stuck bit scenarios.

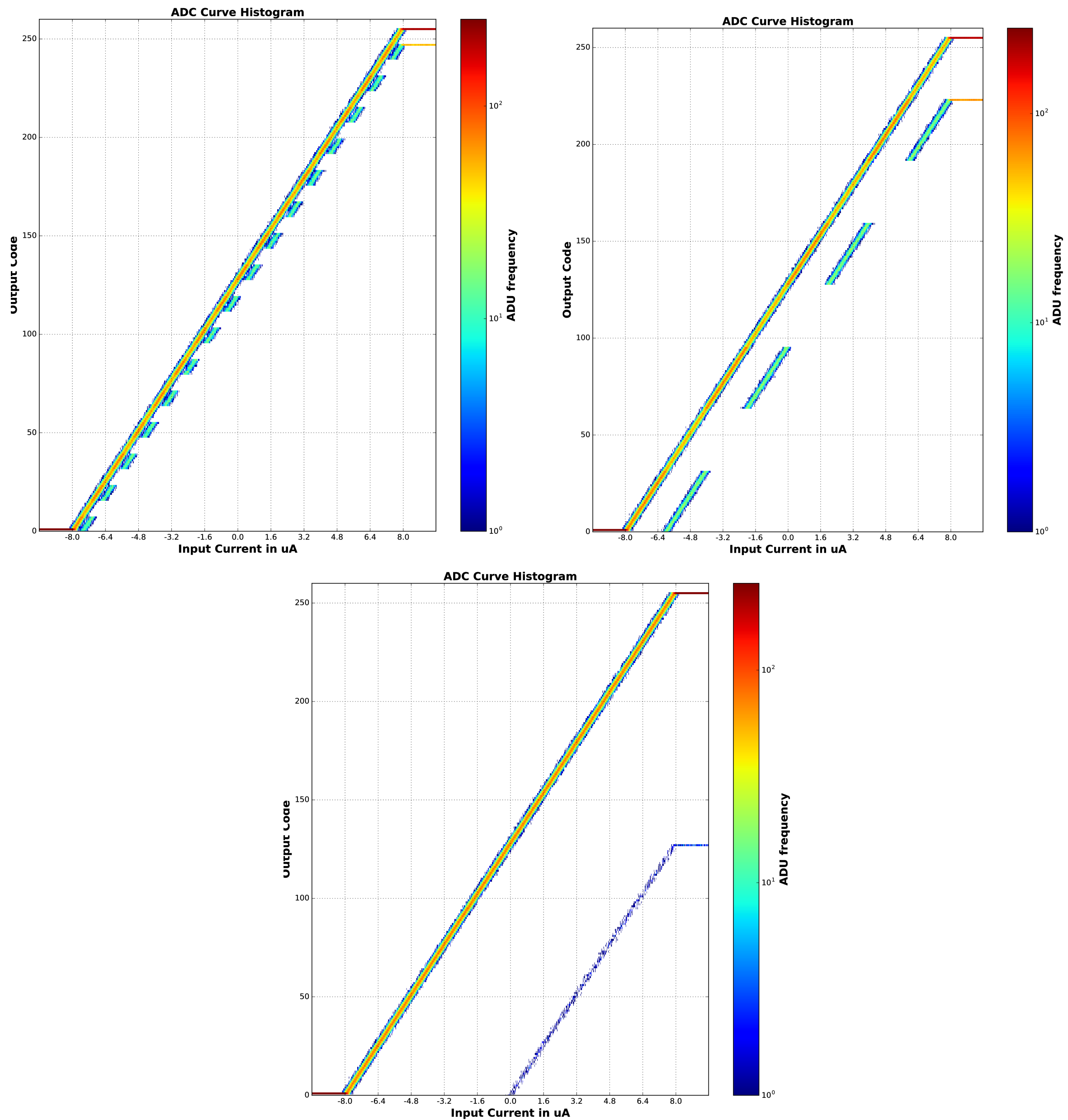

Figure 6.9: Several simulated ADC curves for different toggling and stuck bit errors. Top left: Bit 3 toggling down with a a small probability. Top right: Bit 5 toggling down with 50 % probability. Bottom: Bit 7 (MSB) toggling down with very low probability.

Outliers Test: Due to bit errors, the nominal, linear ADC curve is fragmented with fragments shifted up or down. Fragments caused by different bit errors cause different and distinct patterns. Most importantly, these patterns do not overlap. This makes testing for individual bit errors easy, one simply checks if any reading of the ADC curve was recorded in the expected fragments. If so, a communication issue of the corresponding link is identified. These readings appear as single or few outliers with respect to the nominal ADC curve, we thus call this testing algorithm the *outliers test*. As the ADC curve is noisy, also the shifted fragments are. Thus, when testing the fragments for readings, a certain margin is defined in which readings are checked. These margins should be chosen large enough to accommodate the noise, but should not create any overlap among fragments of different bits. Figure 6.10 shows an example of a measured ADC curve with a toggling bit that is identified by this outliers test. The red areas show the expected fragments corresponding to specific bit errors, farthest away from the nominal ADC curve are the bit7 (MSB) fragments, then bit6, bit5 and so on. If a reading was found in one fragment, the fragment is shown in green and the single readings in blue. There are two concerns regarding this testing algorithm. The noisiness of the ADC curve prevents testing of small bit errors, i.e. bits < 3, as the shifted fragments are too close to the noisy nominal curve. The testing algorithm can be tweaked by defining which bits are tested for, what margins per bit are used, how many readings per fragment are required before considering a fragment "activated" and how many different fragments need to be activated to identify the corresponding bit error. In general, for the high bits 5, 6 and 7, the margins can be chosen larger and the requirements for identification are at least one reading and at least one fragment active. For bits 4 and 3 higher thresholds and smaller margins are set. The second concern is the definition of the reference curve, i.e. the nominal ADC curve. This is required as the up and down shifting of the fragments is only relative to the nominal curve. The nominal ADC curve is defined by a linear least-χ^2 fit that is performed in the inner part of the curve[1]. The fit is robustified by excluding all high DNL codes from the transfer curve. Of course, this approach is problematic if the linear fit does not describe well the nominal ADC curve. This can happen if there are strongly toggling or stuck high bit errors present, which will heavily distort the linear fit. In conclusion, the outliers test is very successful in identifying high bit errors > 3 with a low toggling probability.

DNL Bit Test For bit errors with high toggling probability, or even stuck bits, the outliers test is not the method of choice due to the requirement of an appropriate linear fit. These cases can be identified using the DNL information. The DNL curve, i.e.

[1]Specifically the fit takes into account all readings in the region code_min + 10 and code_max − 10.

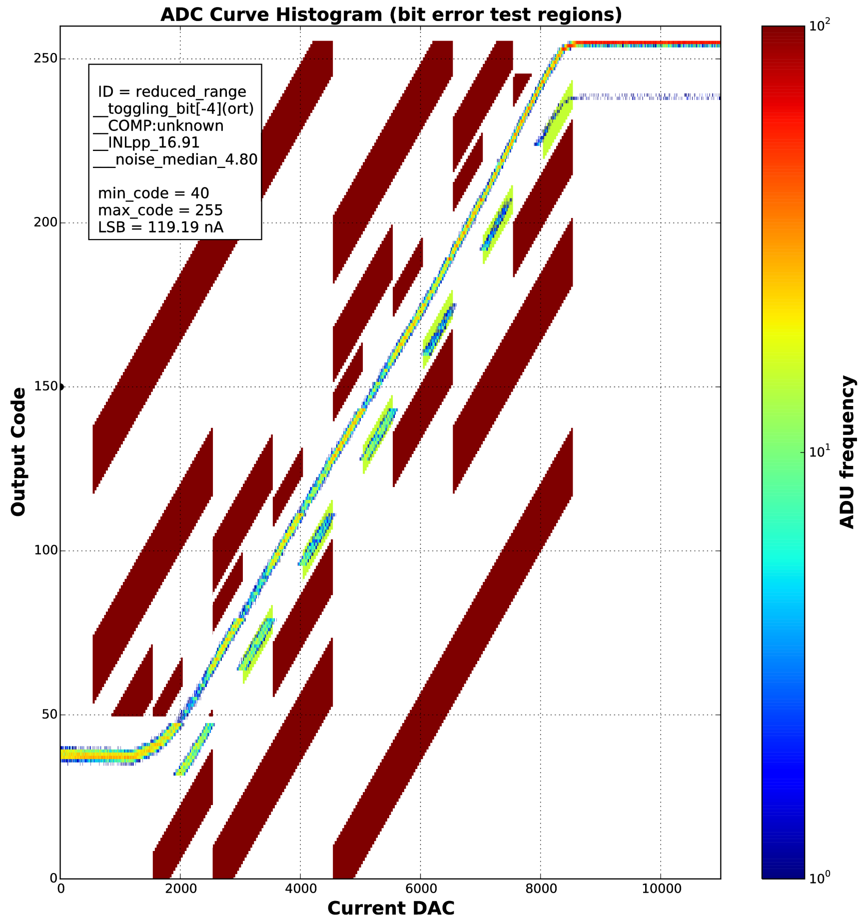

Figure 6.10: ADC curve recorded with a Hybrid5 module showing a toggling bit 4 that is identified by the outliers test. Indicated in red are the expected ADC curve fragments due to specific bit errors, any fragment activated by outlier readings is shown in green. Additionally, a reduced range (code_min = 40), a high INLpp value of 16.91 and a high noise of 4.8 ADU were found for this transfer curve.

the DNL value versus the ADC output code, can also be understood as a normalized projection of the ADC curve onto the ADC code axis. Figure 6.11 shows two examples of high toggling probability bit errors and their corresponding DNL curves. As the lengths and positions of the shifted fragments are uniquely defined by the affected bit i, one can in turn search for the positions and length of the negative DNL valleys to infer on the affected bit. This is implemented in the *DNL bit test*. For each bit i, the expected DNL valleys are scanned. Within each valley, all DNL values below a certain DNL threshold are counted. If this number exceeds a certain counting threshold, dependent on the bit i, the valley is "active". A certain number of active valleys is necessary to identify a bit i error. The DNL threshold is set to be -0.5 ADU to be also sensitive to toggling bits

with medium severity. Due to the projection on one axis, the negative DNL valleys for each bit are now overlapping, in contrast to the non-overlapping fragments in the full ADC curve. Thus, the required valley filling levels, i.e. the number of DNL values below the DNL threshold per valley, cannot be set arbitrarily. To ensure an unambiguous bit identification, the minimal filling level for bit i valleys has to be larger than the maximal filling level for bit $i-1$ valleys. Note that bit 0 transmission errors are identified in a slightly different way by determining the average readings of all even ADC codes and all odd ADC codes, respectively. If the even/odd ratio exceeds a value of 4 or is below a value of 0.25, a bit 0 error is identified. Concluding, the DNL bit test reliably identifies bit errors for all bits, if the toggling probability is higher than 50 %. It is thereby complementary to the outliers bit test. Note that bit errors with high toggling probability will also show increased INLpp and ADC noise values.

When analysing an ADC curve, the DNL bit test algorithm is applied first. This will identify any severe DCD-to-DHP communication failures. If no bit error was raised, the outliers test is applied to identify slightly toggling bits. If both tests passed without raising a bit error, we are very confident that there is no DCD-to-DHP communication issue present for the respective DCD column pair.

6.2.2 Digital Test Pattern

The DCD chip provides another possibility to check for DCD-to-DHP data communication issues. Instead of sending out the 8-bit digitization results of the ADCs, the DCD can be configured to transmit a predefined set of digital codes. By knowing the transmitted code pattern and comparing it to the received code pattern, communication failures can be recognized. The digital test pattern can be activated by setting a configuration bit in the JTAG register. The test pattern is the same for the 8 column pairs of the DCD and consists of 32×8 bits, one 8-bit code is send out per clock cycle, after 32 clock cycles the pattern repeats. Practically, this can be considered a well-defined output code assigned to each of the 32 ADCs in one column pair. Data from the DCD column pairs is send out in the sequence ADC00, ADC01, . . . , ADC31, for each column pair link 0 transmits the LSB, link 7 transmits the MSB of the 8-bit code. When the test pattern is active,

- ADC00 sends out 10000001 (MSB→LSB),
- ADC01 sends out 00000000,
- ADC02 to ADC30 send out 01111111,
- and ADC31 sends out 00000000.

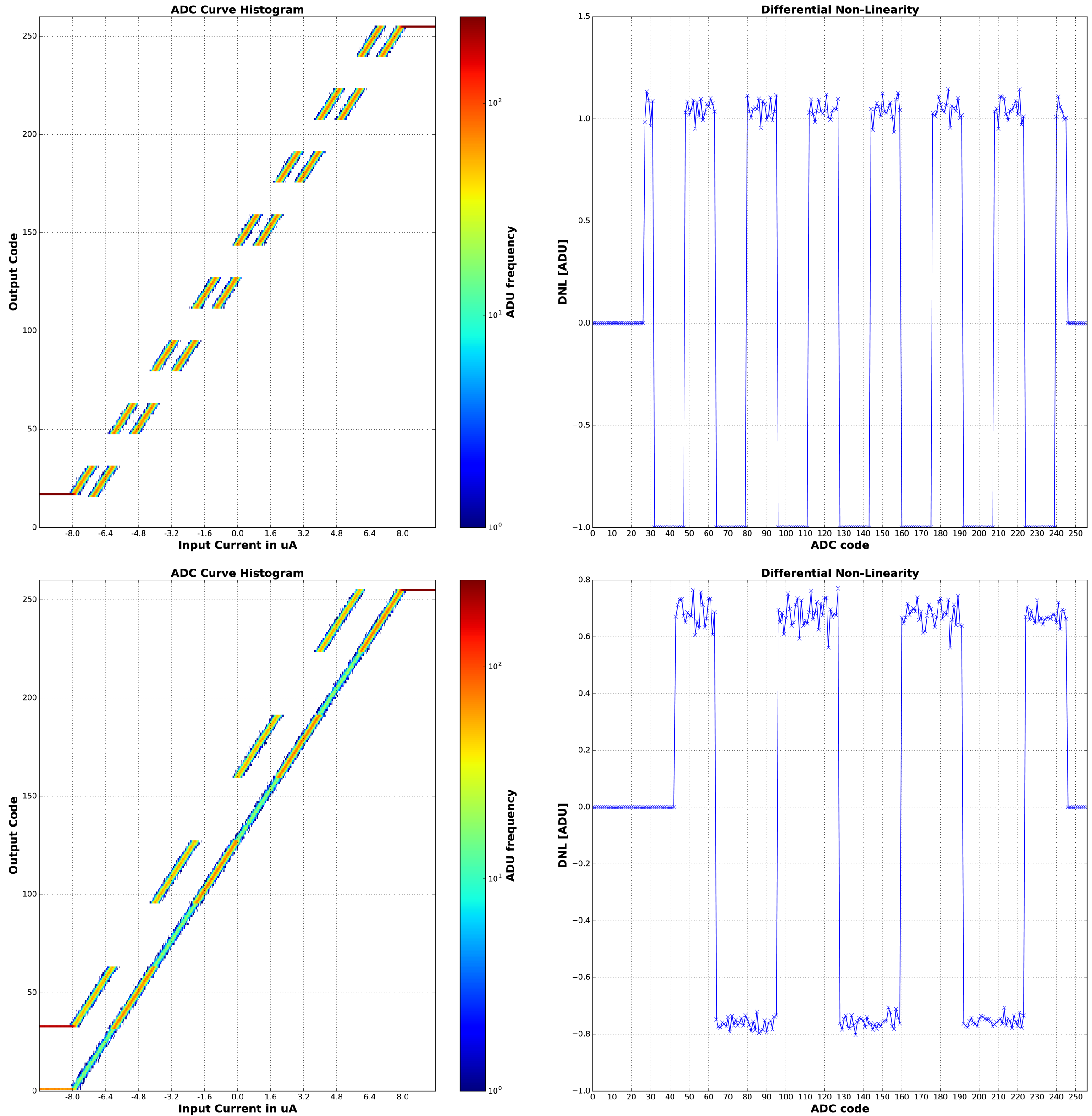

Figure 6.11: Simulated ADC curves with high toggling probability bit errors (left) and the corresponding DNL curves (right), top is a stuck bit 4, bottom is a strongly toggling bit 5.

Figure 6.12 represents this test pattern in a graphical way. Obviously, the pattern is highly repetitive, it is constant for clock cycle $2 - 30$ and the same for clock cycle 1 and 31. The bit error rate R_i evaluates for each link i, how many bits were received wrongly over 32 clock cycles. In principle, the error rate can take integer values between 0 and 32. $R_i = 0$ means that all bits are received correctly on link i, i.e. no communication issue on this link. Assume the physical line of link 0 (LSB) is broken and the DHP receives

only digital 0 for that link. According to the test pattern 30 digital 1's are expected, thus the error rate would be $R_0 = 30$. If there is no actual failure of one link but rather the link delays are set to improper values, then one would observe a shifted pattern with respect to the transmitted test pattern. This is due to the fact that with improper delays the phase difference between data transmission and data sampling is wrong. When the received pattern is shifted by one clock cycle in either direction, the error rates will be $R_0 = 4$ for the LSB link and $R_{1-7} = 2$ for all other links, due to the regularity of the test pattern. Improper settings for the link delays will maximally cause a shift of the received pattern by one clock cycle.

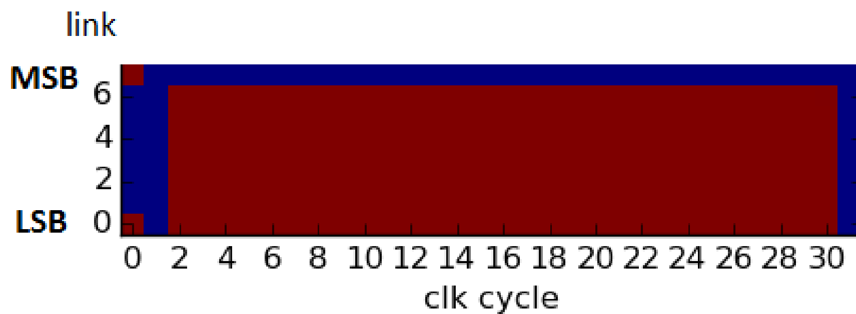

Figure 6.12: Predefined digital test pattern send out by each column pair in the DCD to investigate the DCD-to-DHP data transmission. The x-axis indicates the clock cycle, after 32 clock cycles the pattern repeats. The y-axis indicates the link number and thereby the bit number per column pair. The colour code indicates the bit value: red for digital 1 and blue for digital 0.

6.2.3 Indications of Cross-Talk among Communication Links

Figure 6.13 shows the result of the outliers bit error test on an ADC curve recorded on an EMCM with the external DHH current source. A slight toggling of bit 7 (MSB) is present and identified by the algorithm. Apparently, the MSB is mainly toggling down to digital 0 for high ADC output codes > 230, shifting these output codes down to codes around 130. The toggling probability seems to be dependent on the output code itself. Using the DHH current source, only one DCD analog channel at a time can be measured, that means the calibration current is injected into only one ADC of the DCD. However, at each calibration current DAC step, all ADCs are transmitted over the DCD-DHP data communication links and only in the DHP all non-measured channels are masked out. These non-measured channels are not connected to the current source and will therefore send out low output codes (inflowing leakage currents are maximally a few 100nA). Remember that the DCDs output codes are in the range $[-127, 127]$ and

represented in two's complement, the DHP maps these to the code range $[0, 255]$. Low code are thus negative and have the sign bit, which is the MSB, set to 1 and all other bits mainly 0, the highest code 127 is represented as 01111111, i.e. high output codes are mainly digital 1's except for the MSB. The column pair, the measured channel belongs to, will send out 32 8-bit codes, 31 of these will be low codes. For high calibration input currents, the measured ADC will send out high output codes, DHP codes > 230 require to send mainly digital 1's over the data links while pulling the MSB down to digital 0. In case of cross-talk between the communication links, the MSB will be incapable of pulling down to digital 0 if the neighbouring links are mainly pulling up to digital 1. This is exactly the case for high DHP codes > 230 and indeed one observes a tendency for the MSB to toggle for these high codes. Thus, the shown ADC curve is a strong indication of cross-talk effects among the DCD-DHP data communication links.

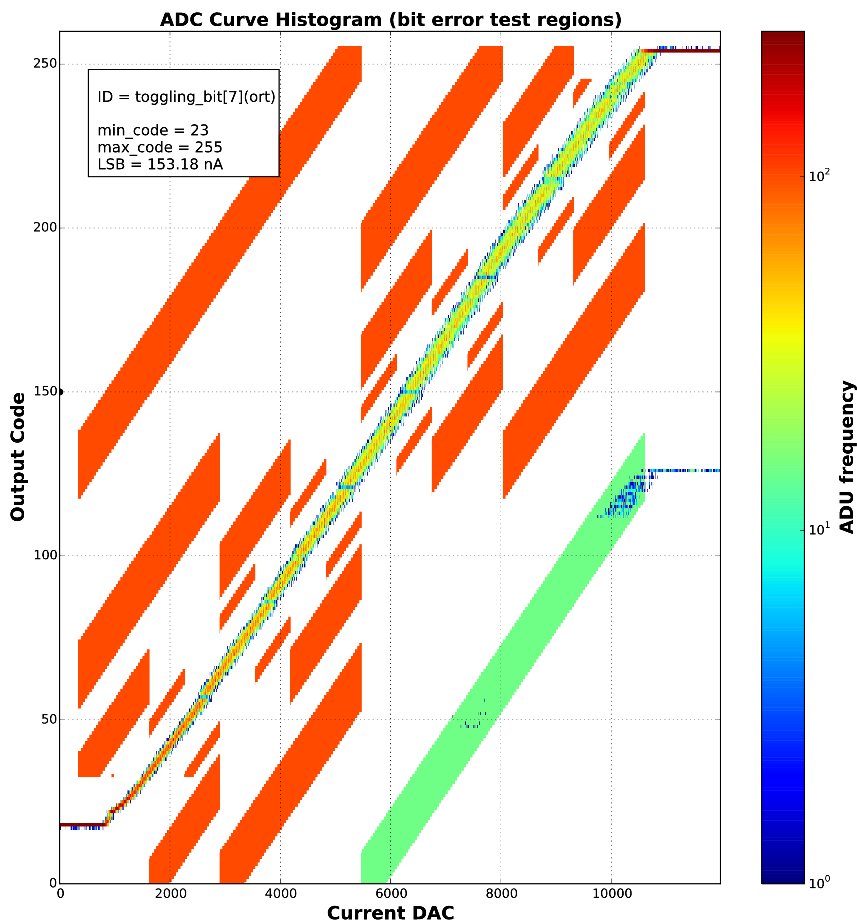

Figure 6.13: ADC curve recorded on an EMCM with the external DHH current source. The outliers bit tests identifies a toggling bit 7 (MSB), which is mainly toggling for high output codes. This behaviour is a strong indication of cross-talk effects among the DCD-DHP data communication links.

7 Read-out ASICs Optimization: Parameter Scans and Tuning

With the discussed testing algorithms we can evaluate the performances of the analog channels of the DCD, as well as the DCD-to-DHP data communication. Having these tools at hand, we can now define optimization strategies with which a stable DCD-DHP communication can be defined and with which optimal values for the parameters steering the ADC functionalities can be found. In addition, specific information on the nature of analog and communication failures will be obtained, that will give feedback to the ASIC designers and may help when considering potential resubmissions of the ASICs. The aim is to define and implement a largely automated optimization procedure for the two front-end read-out ASICs. The result should be a well working DCD-DHP read-out pair, or at least detailed information on why the front-end read-out is not working properly. Ideally, the procedure should consume only a small amount of time for running on a Belle II PXD module.

7.1 Optimization of the Inter-ASIC Communication

The first step in optimizing a DCD-DHP ASIC pair will be the optimization of the DCD-to-DHP data communication. This is reasonable as communication failures, i.e. bit errors, dominate the ADC curve topology and analog DCD failures may be hidden. Consider for example the stuck MSB case in figure 6.8 on the right, the code range of the ADC curve is dramatically reduced, but this is not due to an analog DCD error that reduces the dynamic range of the ADC. To disentangle the effects, the optimization of the data link delays is performed first. In principle one could think about an offline bit error correction with which the nominal, bit error free ADC curve could be reconstructed. When the affected bit is clearly identified, the fragmentation of the curve may be corrected for. For optimizing the data link delays between DCD and DHP either the digital test pattern, or the ADC curves can be used. Both approaches will be discussed in the following.

7.1.1 Using the Digital Test Pattern

As described in section 6.2, the digital test pattern is a fixed sequence of 8-bit codes send out by each column pair of the DCD. It can be used to define an error rate R_i for each of the 64 data links, which measures how often a wrong bit was received on DHP side on link i. For each link, a global delay and a local delay setting can be used to individually delay the send signal. Both global and local delay are realised as a cascade of 0 to 15 inverter pairs (delay elements), the number of active delay elements can be configured individually, but all links share the same global delay. The delay elements are used to compensate for different natural delays present on each link. These natural delays are different among all links and depend on the link routing. Figure 7.1 illustrates, how global and local delays are used to compensate for the varying routing delays. For each link, a combination of 15 global delays $\times$ 15 local delays, 225 settings in total have to be scanned. Finally, the optimal combination of the common global delay and the individual local delays has to be found. For scanning the parameter space, all combinations of global delay and local delays are processed, where all 64 links are scanned simultaneously. At each scanning point, the digital test pattern is read out n times and the received bits are written to a file on disk. In the offline analysis, the recorded bit codes are compared to the expected test pattern and the error rates R_i, now averaged over the n readings, are computed for each link and for each scanning point. Obviously, the optimal global and local delay setting per link is where the error rate is lowest, ideally $R_i = 0$. The analysis results can be represented in a so called *delay matrix*, a 16×16 matrix, where one dimension is the global delay setting, the other dimension is the local delay setting and the matrix entry is the error rate R_i. For each link we get an individual delay matrix. Figure 7.2 shows two examples of graphical representations of delay matrices. The example on the left is a typical delay matrix for an optimizable link. It has a clear diagonal band of $R = 0$ error rate, which we call the *good region*. Figure 7.2, right hand side, shows an example of a not optimizable link, that means the link has a non-zero error rate for all global and local delay settings. This suggests a broken link or a failing output driver. From all 64 delay matrices, an algorithm computes the optimal settings as follows:

- For each link i calculate the width of the good region as a function of the global delay. The result is a set of 64 arrays (64 links) of length 16 (16 global delay settings).
- Project these arrays onto one array of length 16, by taking the minimum per global delay, i.e. take the minimum per entry j of the 64 arrays. The resulting array contains the minimal width of the good region per global delay over all links.

- Find the maximum in the resulting array, the corresponding entry j is the optimal global delay. This means, use the global delay at which the minimal widths of all links good regions is maximal.

When the optimal global delay is found, the local delay for each link is defined as the middle of the good region for that specific global delay. The whole process, taking and analysing the data, is rather fast for one ASIC pair and takes only some minutes. In principle, the process can be parallelized for multiple ASIC pairs. This optimization algorithm using the digital test pattern was already implemented and used for optimizing the DCD-DHP communication.

Apart from the mere optimization of the link delays, a detailed analysis of the DCD-DHP communication optimizability was implemented by us. The figure of merit for evaluating the link quality is the width of the good region, which we call *delay tolerance*. If there is no good region at all, that means no global delay/local delay setting for which the error rate is zero, than the link quality is obviously bad as it cannot be optimized and will most probably always show bit errors. If, on the other hand, a good region exists but with a very small width (minimally only one specific working setting), then the link can be optimized but is likely to become unstable at times. The reason is that the amount of delay of the inverter pairs is depended on supply voltages, which my suffer from small fluctuations over time. A wide good region has a stable optimization point and a good delay tolerance, meaning small fluctuations are unproblematic. We can thus categorize the link qualities according to the delay tolerance. To reduce the complexity of the 2-dimensional delay matrices and to simplify the analysis, a 1-dimensional projection of the delay matrix is used. The error rates of the matrix are projected on the diagonal going from delay point $(0, 0)$ to delay point $(15, 15)$, the projection is done by averaging the error rate values, respecting the number of the possible combinations for the total delay value. The resulting 1-dimensional curve measures the averaged error rate versus the total delay in the range $[0, 30]$. Figure 7.3 shows, that the delay tolerance can now be measured as the width of the $R = 0$ valley. As mentioned before, the amount of delay of a global delay inverter and a local delay inverter are not necessarily identical. However, all measurements for different supply voltages and clock frequencies indicate a reasonable proximity of the values. Moreover, even if the diagonal projection is not fully accurate due to a small difference of global and local delay, the delay tolerance measured this way will always be smaller than the actual one. Thus, the presented procedure will yield the most conservative estimation.

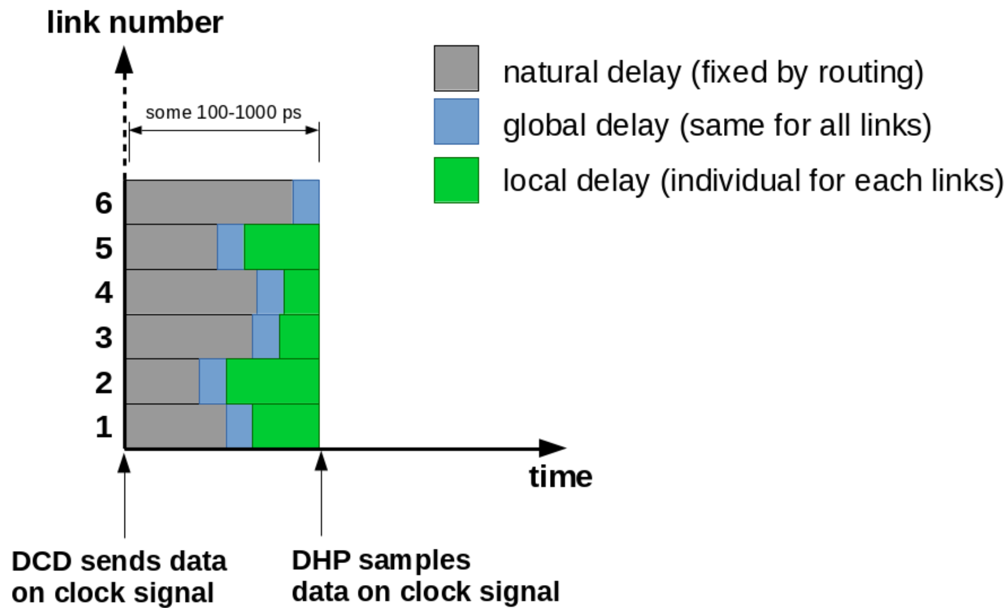

Figure 7.1: Illustration of the use of local and global delay elements to adjust the data transmission timing between DCD and DHP to compensate for varying signal delays due to the routing of the data links and to ensure correct signal sampling on DHP side.

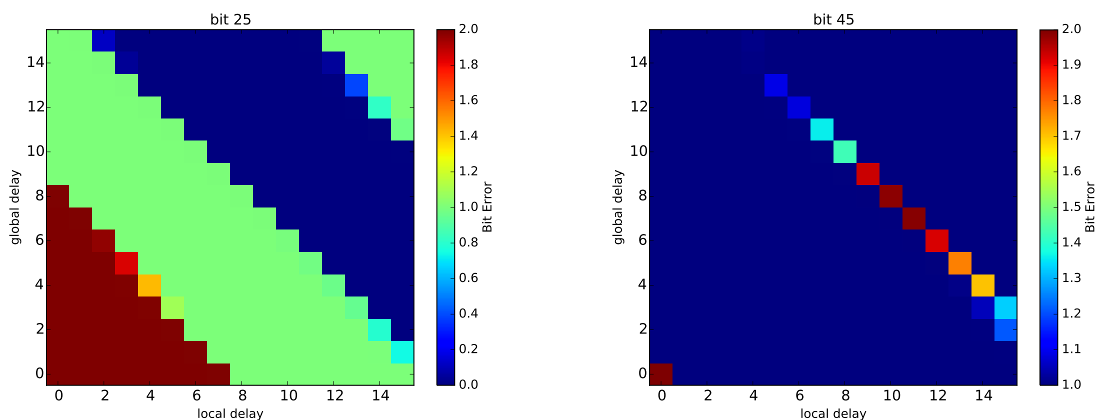

Figure 7.2: Graphical representation of the delay matrix of a specific link used for finding the optimal local and global delays. The color code indicates the bit error rate R, blue is $R = 0$, i.e. the good region where the test pattern is received correctly. On the left the typical delay matrix of an optimizable link is shown (link 25), the good region is wide and for nearly all global delays an optimal local delay can be found. The right-hand plot shows a delay matrix of a broken link (link 45), there is no $R = 0$ region, the test pattern on this link is always received with errors (note the color scale, here color blue is $R = 1$).

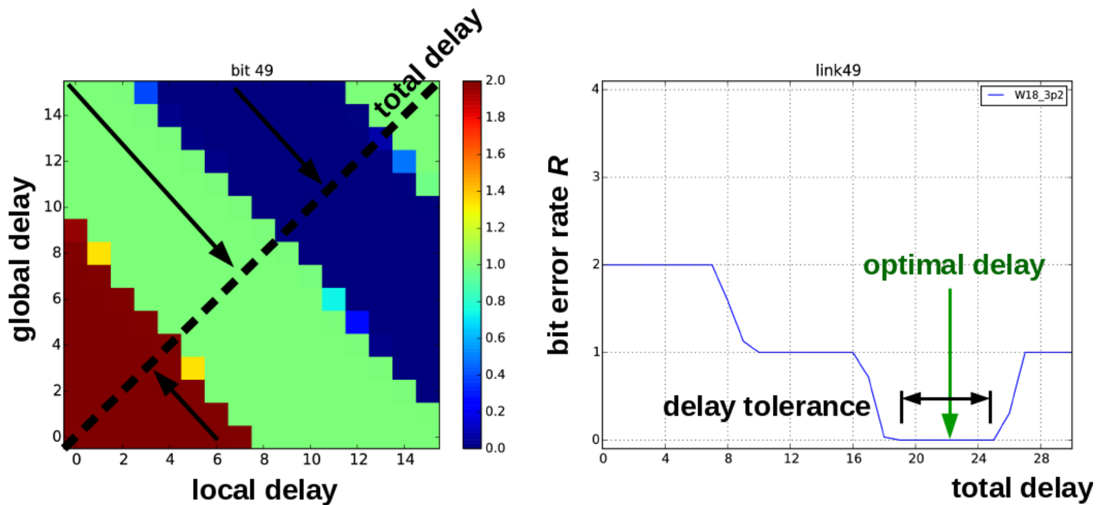

Figure 7.3: To simplify the analysis of delay matrices we use a 1-dimensional, diagonal projection as indicated in the left plot. The result is an error rate R versus total delay curve as indicated in the right plot. The width of the $R = 0$ valley is used as a measure for the delay tolerance. The larger the delay tolerance of a link, the more stable it is. A link must have a delay tolerance > 0 to be optimizable with respect to the local and global delay setting. The optimal delay is found as the middle of the $R = 0$ valley.

7.1.2 Using Transfer Curves

A not yet well understood observation has been made on several laboratory setups (using EMCM and Hybrid5) with respect to delay optimization and communication issues. Although the above described delay optimization, employing the digital test pattern, was successfully conducted and all links were found to be optimizable, often a variety of bit errors were still observed in the afterwards recorded ADC curves, without any settings being changed in the meantime. This means either the test pattern is not sensitive enough to detect all communication issues, or, while recording ADC curve and injecting currents into the DCD, the output drivers are influenced significantly. One concern is the regularity of the test pattern, being constant for 29 clock cycles. A modifiable digital test pattern would be preferred and is in discussion for future DCD submissions. A consequence of this inconsistency could be, to use ADC curves for optimizing the data link delays in the first place. As our analysis tools allow for identification of affected bits, and thereby of the affected links, an optimization similar to the test pattern procedure should be possible. For this, we record ADC curves for all 256 channels of the DCD at each global delay/local delay scanning point. Instead of comparing to the expected test pattern, we now analyse the ADC curves for bit errors. For each bit $i = 1, \ldots, 7$ the number of ADC curves showing a corresponding bit error are counted in each global delay/local delay bin.

The number of ADC curves showing no bit error i replaces the error rate R_i of the test pattern measurements. Figure 7.4 shows a graphical representation of this procedure, where only the local delay of link 7 was scanned, all other local delays where kept at their optimized values. The x-axis shows the local delay, while the y-axis shows the global delay. The colour code indicates the number of good ADC curves, i.e. the number of curves without bit7 error. Note, in this plot only 10 ADC curves of the ADCs belonging to the DCD column pair with link number 7 are used. Indeed, the observed pattern is in very good agreement between ADC measurement and test pattern measurement. With the current testing algorithm parameters, it seems that only a slightly better optimization of the link delays is possible by using ADC curves, the error free region is only slightly more constrained for the ADC method than for the test pattern method. Additionally, taking ADC curves is rather slow compared to the fast test pattern measurement. In conclusion, performing delay optimization using ADC curves cannot compete with the test pattern approach when the slow external current injection is used. It may, however, become feasible if a faster ADC recording method is available and the testing algorithms are adjusted to higher sensitivity to further constrain the good delay region.

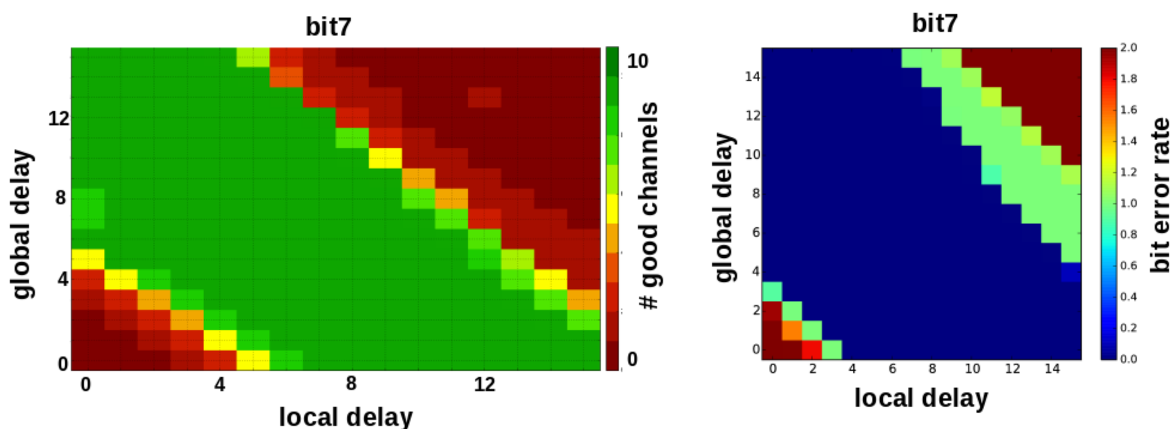

Figure 7.4: Delay optimization using ADC curves. On the left, an ADC delay optimization result, where the global delay and the local delay of link 7 where scanned over. The x-axis indicates the link 7 local delay settings, the y-axis indicates the global delay settings. The colour code shows the number of ADC curves (of the corresponding DCD column pair), that do not show a bit7 error. On the right, the corresponding test pattern delay scan for link 7 is shown.

7.2 Optimization of the Drain Current Digitizer Analog Performance

After optimization of the DCD-to-DHP data link communication, the number of bit errors should be minimized. Now a detailed analysis of the ADC curves is possible in order to investigate the DCD analog performance. As described, the performance of the pipeline ADCs in the DCD depend mainly on the three DACs IPSource, IPSource2 and IFBPBias, which have severe influence especially on the dynamic ranges of the current memory cells. Additionally, together with the supply voltages RefIn and AmpLow, they can have influence on the operation of the comparators. Thus, improper settings of the DACs and supply voltages are likely to result in reduced dynamic ranges of the ADC and possibly cause comparator offsets, and by that long codes in the ADC curves. This 5-dimensional parameter space has to be scanned, to find the optimal set of settings, i.e. the set of settings at which the performance of all 256 ADCs in the DCD is optimal. We call this point in the parameter space the *optimal working point (OWP)*. The developed ADC curve analysis algorithms will set the appropriate error flags for each recorded curve. We may define the optimal working point as the point, at which the number of ADC curves, that are not assigned any error flag, is highest. The quality of that working point is than the fraction of error-free ADC curves over the total number of measured ADC curves. Using this definition, a large number of recorded ADC curves is desired to reduce the statistical uncertainty. Ideally that means, that all 256 ADCs of the DCD should be recorded. In conjunction with the large parameter space this poses a certain problem. As already mentioned, taking ADC curves with the external DHH current source is rather slow, and only one ADC channel at a time can be recorded. It takes several seconds to record one ADC curve. Assume we use 5 scanning steps for each of our 5 parameters, that makes 3125 combinations. For each combination one would like to record 256 ADC curves, i.e. $800,000$ ADC curves in total. Even if each ADC curve took only $1\,\mathrm{s}$ to be recorded, the total measurement would take more than 9 days. Of course, the number of ADC channels can be reduced, but due to statistics it should not be smaller than 50. This still makes 1.8 days of data recording alone, for only one DCD chip. We must reduce the parameter space to be able to optimize the DCD in a reasonable amount of time. Also, the accumulated data should not exceed several GB per DCD chip. The necessary measurement time is reduced, by slicing the parameter space. As a first step only the parameters IPSource and IPSource2 are scanned in a coarse mode, while the other three parameters are kept constant at their nominal design values. Optimal values for IPSource and IPSource2 are found and now the supply voltages RefIn and AmpLow are scanned in a coarse mode.

After optimizing both voltages, another IPSource-IPSource2 scan is done in a fine mode, but now at pre-optimized RefIn and AmpLow voltages. The same iteration is done with a second, fine RefIn-AmpLow scan. At last, IFBPBias is scanned in a fine mode. This way the overall optimal working point is iteratively approximated and the overall scanning time is reduced to a few hours. Figure 7.5 shows a graphical representation of how the optimal working point is found. The plot shows an IPSource-IPSource2 scan (x-axis is IPSource, y-axis is IPSource2), at each parameter scan point 256 ADC curves were taken and analysed. The number of error-free ADC curves is counted and shown in colour code. The optimal working point is where this number is highest, i.e. the "most green" point in the plot, that lies in a region of comparably good working points (stability). The black cross indicates, where the optimal working point would be chosen in this example.

When the optimal working point is found, a detailed analysis is performed. That means detailed statistics on all ADC curves at this working point are collected. This includes for example noise and INLpp versus channel number plots, code_min/max value distributions, or pin-out maps of several quantities, that show the respective value as a function of the physical position of the ADC channel input pin on the DCD bump-bond pads. This gives detailed information on the quality of the optimal working point.

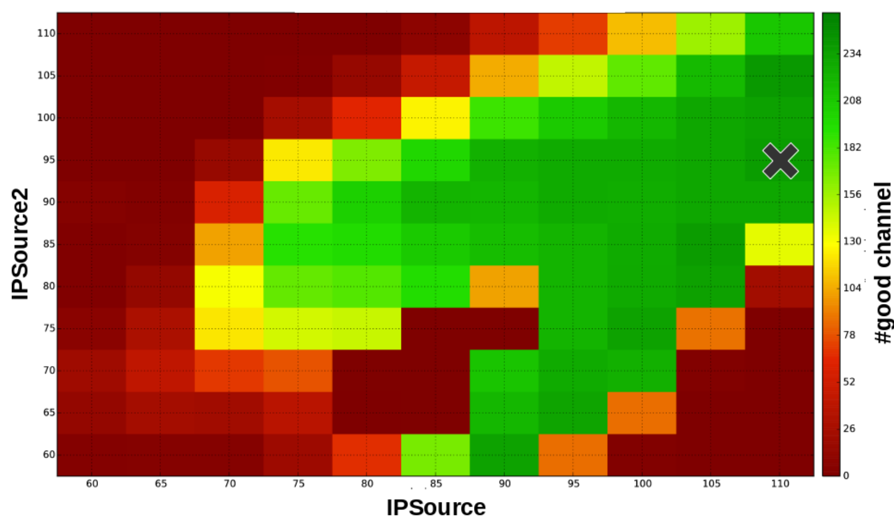

Figure 7.5: Graphical representation of an IPSource-IPSource2 scan analysis. The x-axis indicates the IPSource DAC value, the y-axis indicates the IPSource2 DAC value. The colour code indicates the number of error-free ADC channels (good channels). all 256 ADC channels were recorded at each scanning point. The optimal working point is chosen as the point with the highest number of error-free channels that lies in a reasonably large region of comparably good working points to ensure operation stability and is marked.

7.2.1 Optimization of the DAC Currents

Several things can be learned, when studying the optimization plots of the individual parameters split up into the specific error types. Figure 7.6 shows a typical IPSource-IPSource2 scan analysis result. The x-axis of each plot indicates the value of the IPSource DAC, while the y-axis indicates the value of the IPSource2 DAC. The individual tiles show the ADC curve analysis with respect to a certain testing algorithm. The colour code indicates the number of ADC channels that are error-free with respect to the specific testing algorithm, green means a high number of error-free curves, red means low number of error-free curves. The top left tile is testing the code_min criterion, i.e. it tests if the minimal code of the ADC curve is below the threshold given in parenthesis. Analogously, the top right tile gives the code_max criterion. These two tests indicate reduced dynamic ranges. The middle left tile counts the number of ADC curve that are free of comparator offset errors (i.e. long codes or clamping codes). The middle right tile indicates curves with INLpp error flags, that means these curves show a too high non-linearity. The plot in the bottom left tile tests if the ADC curve noise exceeds a certain value, that is given in parenthesis. Finally, the bottom right tile is the product of all criteria, i.e. here all ADC curves are counted that do not show any of the failures mentioned before. The last plot is used to define the optimal setting of the two scanned parameters.

In the first tile, the code_min criterion, a diagonal band structure can be seen. A good (green) band goes from small IPSource and IPSource2 values diagonally to high IPSource and IPSource2 values. Combinations where either IPSource is small and IPSource2 is large, or the opposite case, are clearly disfavoured. We know that both DACs influence the dynamic ranges of the current memory cells in the pipeline ADCs and thus steer the overall dynamic range of the ADCs. Non-optimal settings thus lead to code_min errors. From design IPSource and IPSource2 should be set to the same value. This is confirmed by the diagonal good band structure. The code_max criterion (top right) shows a similar behaviour. However, the good band is much wider and much less constrained by the code_max criterion compared to the code_min criterion. This is also reasonable as we saw, that non-optimal DAC settings tend to shift the current memory cells (CMCs) dynamic ranges to positive values. Hence, reduced negative dynamic ranges are much more likely (see figure 4.3).

The comparator offset test (middle left) also shows indications of the diagonal good band structure. Extremely reduced CMC dynamic ranges can have similar effects as large comparator offsets and cause long codes. Additionally, a region of small IPSource-IPSource2 values is strongly disfavoured. IPSource is responsible for setting the comparator thresholds for the AD conversion algorithm. When the thresholds are chosen too small

(small IPSource DAC value), large comparator offsets towards zero are the result. The INLpp test result (middle right) is strongly correlated the comparator offset test. Comparator offset errors cause long codes in the ADC curves, which are identified as large peaks in the DNL curve. As the INL is the cumulative sum of the DNL, the presence of long codes will clearly cause an increase in the INL. This explains the correlation. Finally, the ADC noise test shows two isolated high noise islands. Comparison with the bit error tests show, that the high noise is not due to an extreme increase of bit errors. It seems that specific combinations of the IPSource and IPSource2 settings cause a sudden and significant increase of the ADC noise. The causality of this effect is not yet understood. In the product of all criteria plot, the optimal working point is found as IPSource = 100 and IPSource2 = 90.

An IFBPBias optimization is in principle identical to the IPSource-IPSource2 optimization. However, since this is a 1-dimensional parameter scan only, the graphical representation of the analysis result is changed slightly. Figure 7.7 shows an example of an IFBPBias optimization. Here, the x-axis indicates the IFBPBias value, while the y-axis indicates the number of error-free ADC curves with respect to the individual testing algorithms. The colour code is in this case redundant but it is kept for visual clarity. The strongest constraint on the IFBPBias value comes from the code_min test. Too low values of IFBPBias are degrading the dynamic ranges of the ADCs significantly. The comparator offset test (middle left) constrains the value of IFBPBias slightly at high values. The optimal value of the IFBPBias DAC would be found to be IFBPBias = 85 in this example.

7.2.2 Optimization of the Supply Voltages

Apart from the three DAC settings, also the two supply voltages RefIn and AmpLow for the DCD have to be optimized. Figure 7.8 shows a typical example of a RefIn-AmpLow scan analysis. On the x-axis the value of AmpLow in mV is shown and on the y-axis the value of RefIn in mV. The code_min criterion puts a very strong constraint on the AmpLow voltage, for values $< 200\,\mathrm{mV}$ and $> 500\,\mathrm{mV}$ all ADC curves show a reduced dynamic range. The code_max criterion, on the other hand, does not seem to put any constraint on both voltages. It seems that for non-optimal AmpLow voltages the negative dynamic range is heavily influenced. From figure 4.4 one does not observe a strong dependence of the CMCs dynamic ranges on the AmpLow Voltage. However, the measured voltages in 4.4 are only in the range $[320, 420]\,\mathrm{mV}$ and do not cover the full range as shown here. It could be that for very badly chosen AmpLow voltages the current memory cells and/or the comparators stop working completely. The RefIn voltage,

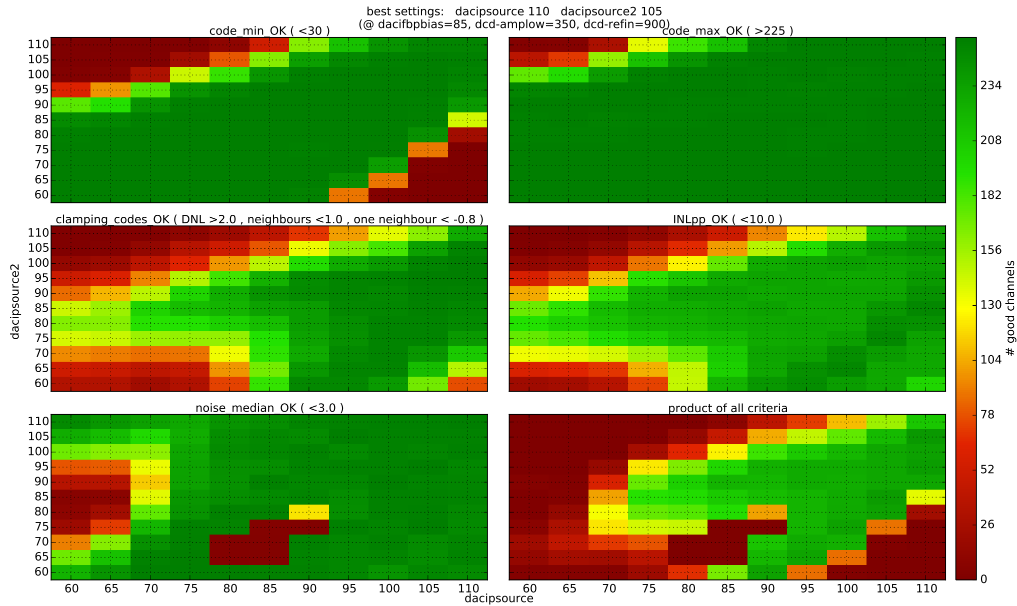

Figure 7.6: Typical analysis result of an IPSource-IPSource2 parameter scan. The individual tiles correspond to the specific ADC curve testing algorithms, the colour code counts the number of ADC curves that are error-free with respect to the testing result. On the x-axis the IPSource value is shown, the y-axis shows the IPSource2 value. This scan was done on the EMCM module W31-3 on ASIC pair 3.

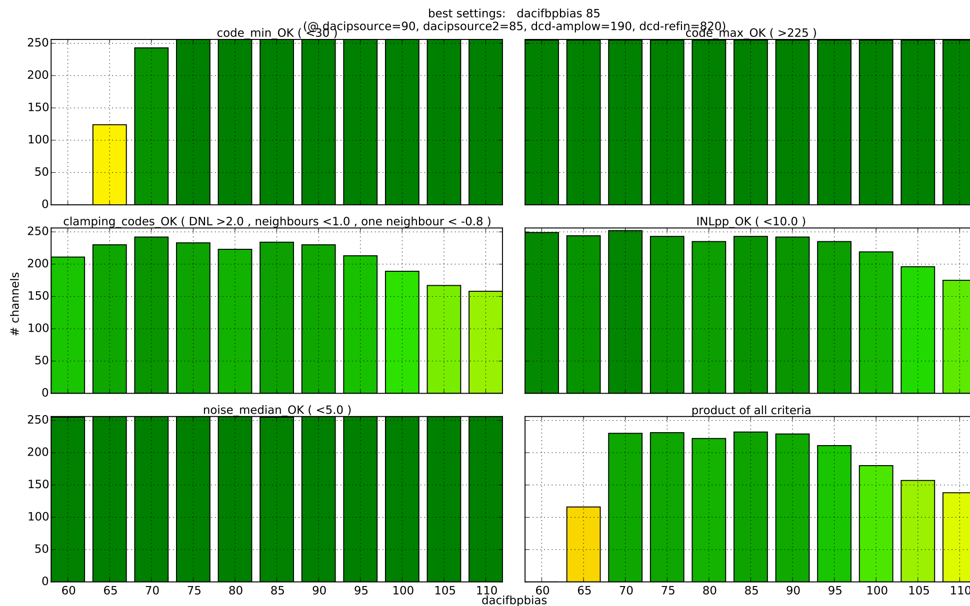

Figure 7.7: Typical analysis result of an IFBPBias parameter scan. The individual tiles correspond to the specific ADC curve testing algorithms, the y-axis (and the colour code) counts the number of ADC curves that are error-free with respect to the testing result. The x-axis indicates the IFBPBias value. This scan was done on the EMCM module W31-4 on ASIC pair 2.

in contrast, does not seem to have a strong influence on the dynamic ranges, but it is constrained by the comparator offset test. Small values of RefIn increase the number of ADC curves showing long codes (i.e. comparator offsets errors). Comparator offsets do not seem to be very sensitive to changes in the AmpLow voltage. Again, small and isolated high noise islands are seen for particular combinations of the two voltage parameters. Also here the causality is not well understood yet. The optimal combination of both voltages is found to be RefIn = 850 mV and AmpLow = 350 mV.

In conclusion, we can note that the discussed ADC analysis algorithms put clear constrains on the DCD parameter DACs and supply voltages. The stated design values for the parameters and their dependencies can be confirmed. Usually, we are able to define an optimal working point with a reasonable good performance that lies within a region of good working points. That means, we are able to optimize the analog performance of the DCD ASIC and can choose a working point that is stable with respect to small fluctuations of the parameters.

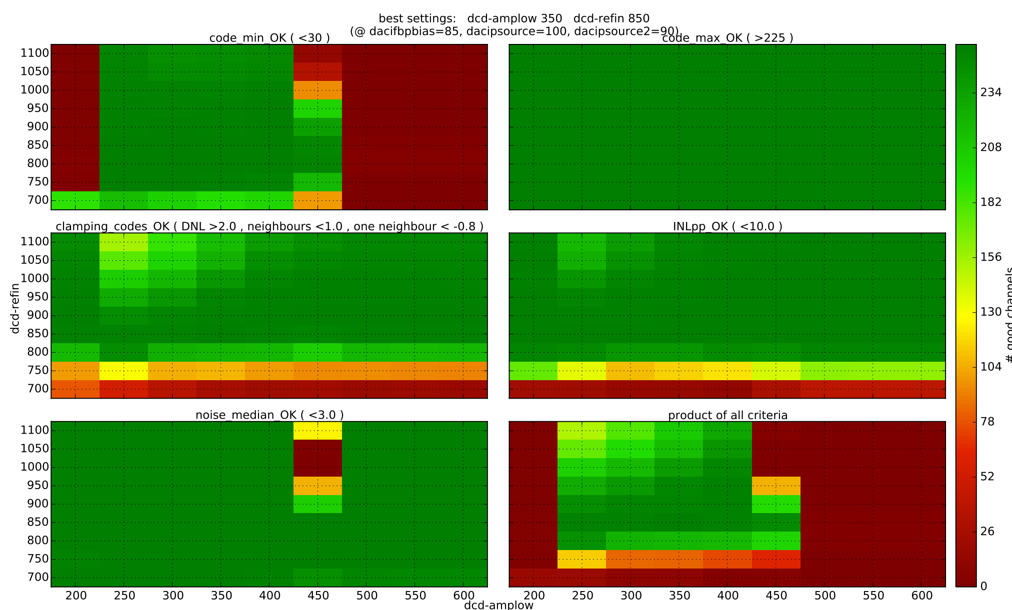

Figure 7.8: Typical analysis result of a RefIn-AmpLow parameter scan. The individual tiles correspond to the specific ADC curve testing algorithms, the colour code counts the number of ADC curves that are error-free with respect to the testing result. The x-axis indicates the AmpLow value in mV, the y-axis shows the RefIn value in mV. This scan was done on the EMCM module W31-3 on ASIC pair 1.

8 Results from Test System Measurements and Irradiation Campaigns

With the developed framework for characterizing and optimizing the analog operation of the DCD and the DCD-DHP data communication, we studied several testing systems operating EMCM and Hybrid5 modules. We investigated how the optimal working points for the DCD ASICs on different modules are distributed and studied the DCD-DHP communication stability at different global reference clock (GCK) values. In addition, two irradiation campaigns have been conducted in order to study the effects of irradiation on the functionalities of the current designs of the front-end ASICs. The results of these studies will be presented and discussed in this chapter.

8.1 Working Point Variations among Modules

During production, small material and implantation variations on wafer level can cause small variations among the produced DCD chips. It cannot be expected that all employed DCD ASICs show the exact same behaviour, it is thus reasonable that also the optimal working points of all DCDs are subject to variations. We applied our DCD analog optimization strategy to two EMCM modules and seven Hybrid5 modules, in total 13 DCD ASICs were characterized and optimized[1]. The measurements on the individual modules were done at different laboratory setups with different power supply units, DHH boards and cables. The general measurement setup, however, was the same as described in section 5. For two Hybrid5 boards only a full channel scan at a fixed working point was available, which allowed us only to perform a characterization of that specific working point. One EMCM module was measured after being irradiated with a 60 keV X-ray source at a total ionization dose of 20 Mrad, the γ-beam was focussed on ASIC pair 4 (on

[1]One EMCM is equipped with four DCD-DHP ASIC pairs, however, both tested EMCMs showed one failing high speed link to one DCD-DHP pair each.

EMCM W31-3). Table 8.2 summarizes the optimal working points found for all ASIC pairs on all investigated modules. Also indicated is the measured LSB value averaged over all recorded channels, as well as the working point quality. The latter one is defined as the number of good ADCs (error-free ADC curves) divided by the total number of recorded ADC curves. The quality measure is a number $\in [0, 1]$, where 1 means no error was found in any recorded ADC channel. The supply voltage scanning steps were usually 50 mV, the DACs were usually scanned at step sizes of 5. The optimal working points found for the three ASIC pairs on EMCM W31-3 are very much in agreement, no systematic variation can be seen. This indicates that effects like voltage drops across the module have only minor influence on the DCD working points. The irradiated ASIC pair 4 does not show any significant difference to the other two pairs. Also the LSB values are very close among the three DCDs, which means all DCDs on the module have identical digital resolution of the input currents. The quality of all working points is reasonably well at > 0.8. Regarding the optimal working points for the DCDs on EMCM W31-4, we see a similar picture, the results for all three ASIC pairs are in very good agreement with each other. All working points show a very good quality of > 0.9. The LSB values are also at similar values. Comparing the results of both EMCM modules, we observe that all optimal working points are found in a rather small parameter space window. We note, however, a difference of factor 1.8 between the LSB values of both modules. This is the effect of the chosen TIA gain setting, data on module W31-3 was recorded at a TIA setting of gain = 1 (the same holds for all Hybrid5 data), while for W31-4 gain = 2 was used. As a result, the digital resolution improves by a factor of roughly 2, which means a reduction of the LSB by a factor of 2.

All optimal working points found for the ASIC pairs on Hybrid5 modules are similarly in good agreement with each other, as well as the LSB values are. The DCDs on Hybrid5 modules seem to prefer slightly higher RefIn voltages, which might be connected to the PCB routing on Hybrid5 as opposed to the on-module routing on EMCM. The overall working point qualities for Hybrid5 measurements are worse compared to the EMCM results. The EMCM measurements and measurements of H5.0.06 and H5.0.07 were done at a slow operation frequency of 62.5 MHz, all other Hybrid5 modules were measured at the nominal GCK clock frequency of 80 MHz (technically this is implemented as GCK = 76.23 MHz). The DCD-DHP data communication seems to become unstable at higher clock frequencies and more bit errors are induced (see next section 8.2). Thus, worse optimal working point qualities for most Hybrid5 modules are probably due to an increase of bit errors.

All measured optimal working points are in agreement with the parameter values that

are expected from chip design. We can state that the variation of the optimal DCD working points is small, DCDs on the same module show very similar working points and also among modules of the same type, the working points do not differ significantly. We do, however, observe a small difference between EMCM and Hybrid5 modules regarding the optimal RefIn voltage, which is probably connected to the very different routings on the two module types. From our results we can recommend standard working points for EMCM and Hybrid5 modules, as shown in table 8.1, that are expected to work reasonably well.

Module Type	IPSource	IPSource2	IFBPBias	RefIn [mV]	AmpLow [mV]
EMCM	100	90	80	850	350
Hybrid5	90	95	90	1000	350

Table 8.1: Recommended standard working points for EMCM and Hybrid5 modules that are expected to show reasonably good DCD analog performance.

Module	Type	ASIC pair	IPSource	IPSource2	IFBPBias	RefIn [mV]	AmpLow [mV]	LSB [nA]	Quality	Comment
W31-3	EMCM	1	100	95	85	850	350	142.6	1	
		2	-	-	-	-	-	-	-	no HS link
		3	100	90	85	850	450	139.6	0.81	
		4	100	90	85	850	400	143.5	0.86	irradiated
W31-4	EMCM	1	-	-	-	-	-	-	-	no HS link
		2	90	85	70	800	300	81.1	0.96	
		3	95	85	70	800	350	80.6	0.95	
		4	100	80	70	900	350	84.7	0.94	
H5.0.05	Hybrid5	1	90	95	90	1050	400	126.8	0.68	irradiated
H5.0.06	Hybrid5	1	100	80	90	850	350	126.7	0.97	
H5.0.07	Hybrid5	1	90	70	85	950	400	121.8	0.88	
H5.0.08	Hybrid5	1	90	95	90	1050	400	114.9	0.79	all channel scan
H5.0.09	Hybrid5	1	90	95	90	1050	400	131.9	0.71	all channel scan
H5.0.10	Hybrid5	1	90	95	90	1000	300	n/a	0.67	
H5.0.11	Hybrid5	1	90	100	90	1000	300	128.1	0.71	

Table 8.2: Optimal working points found for several ASIC pairs on EMCM and Hybrid5 modules. The LSB values found for the measurements on EMCM W31-4 are smaller than the W31-3 and Hybrid5 LSB values by a factor of around 1.8. This is due to the fact, that the W31-4 measurements were done at the gain = 2 TIA setting, while all other measurements used gain = 1. The working point quality measure is the fraction of the number of good ADC curves over all recorded ADC curves. On each EMCM one ASIC pair could not be measured due to a failing high speed link. For two Hybrid5 boards only all channel scans were available, no parameters were scanned, all ADC curves were recorded at the given working point. That means no optimization could be performed, however, the chosen working points seem to work reasonably well. The data for the Hybrid5 modules H5.0.05, H5.0.08, H5.0.09, H5.0.10 and H5.0.11 were recorded at the nominal GCK clock frequency of 76.23 MHz, all other data was recorded at a low clock frequency of GCK = 62.5 MHz. Note that the optimal working points indicated in the headings of figures 7.6, 7.7 and 7.8 are different from the ones indicated here. The optimal working point finding algorithm was improved to find the values indicated here, the plots, however, were generated with the old algorithm and thus indicate wrong values.

8.2 Inter-ASIC Communication Stability at High Clock Frequencies

Measurements indicated a dependence of the number of observed bit errors on the operation frequency of the DCD-DHP pair. The amount by which the data link signal is delayed in each of the inverter pairs (delay elements) changes with the frequency at which the signal is send through the inverters. A dependence of the delay optimization result on the operation frequency, i.e. on the global reference clock GCK, is thus expected. We performed the test pattern delay optimization method an a Hybrid5 module for different GCK frequencies. From the 1-dimensional projections of the resulting delay matrices we extract the delay tolerance, i.e. the width of the error rate $R = 0$ valley (in number of inverter pairs) and histogram the values of all 64 links. Figure 8.1 shows the results for GCK values of 62.5 MHz, 65.0 MHz and 67.84 MHz. Due to a high speed link problem we were not able to operate the Hybrid5 module at higher frequencies and receive data. Already for these small clock frequencies, we observe a degradation of the delay tolerances when increasing GCK. That means, the optimizability of the data link delays becomes worse at higher operation frequencies, and in turn, a higher number bit errors can be expected. The DCD and DHP chip designs are being reworked, such that the next chip iterations will implement a more stable data link communication also at the nominal operation frequency.

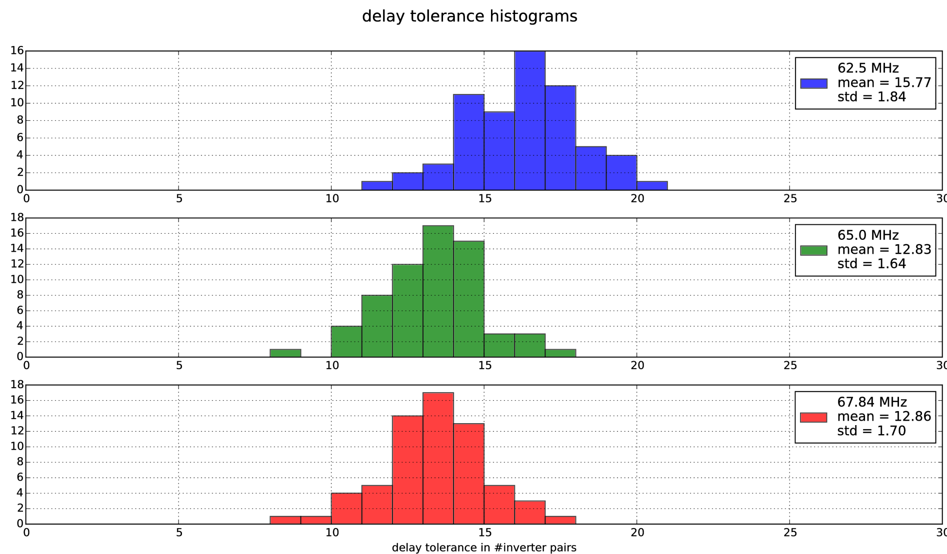

Figure 8.1: Distributions of the delay tolerances of all 64 links (measured in number of delay elements) for three different values of the global reference clock GCK. The delay tolerance is a measure for the optimizability of the DCD-DHP data communication links.

8.3 ASICs Operation Stability and Irradiation Damage

The expected irradiation levels for the PXD system are in the order of $1-2$ Mrad/y, the PXD modules should survive at least a 10 Mrad dose to ensure functionality over the full Belle II lifetime. Two irradiation campaigns have been conducted within the last year in order to study the effects of irradiation on the DCDB-v4-Pipeline and the DHPT ASICs. One EMCM and one Hybrid5 module have been irradiation with a 60 keV X-ray source up to doses of 20 Mrad. Figure 8.2 shows the setup used for irradiation measurements, the tested modules were cooled by a water chiller at 10 °C while the modules were mounted on an aluminium cooling block. The irradiation was done in dose steps of 250 krad, the modules were powered during the process. After each irradiation step, several measurements, test pattern scans and ADC curve measurements, were performed. No specific annealing process was done, the modules were cooled constantly. Dose rates were around $300-500$ krad/h, the EMCM was irradiated from 10 Mrad to 20 Mrad at a dose rate of about 1000 krad/h. The X-ray beam was focussed on DCD-DHP ASIC pair 4 during the EMCM measurement. The Hybrid5 module was already equipped with the new DHPT1.1 ASIC.

Figure 8.2: Setup of the irradiation measurements: The module was put in a 60 keV X-ray chamber and cooled with an aluminium cooling block and water chiller, all back-end electronics were put outside of the chamber.

8.3.1 Stability of the Working Point

Irradiation damage causes the generation of fixed oxide charges in the Si-oxides of transistors and may change their characteristics. As we already saw, the DCD relies heavily on the proper functionality and interplay of the current memory cells and the comparator thresholds, while both might be affected by transistor degeneration. We therefore investigate how stable the optimal working point of the DCD is over several irradiation dose steps. The following results are based on the irradiation measurement done with the Hybrid5 module. The optimal working point found for the specific Hybrid5 module was IPSource = 90, IPSource2 = 95, IFBPBias = 90, RefIn = 950 mV and AmpLow = 300 mV. A full parameter and full channel scan was only performed at major irradiation steps (1,2,3 and 4 Mrad), at each minor irradiation step, only 12 ADC channels were recorded at the fixed working point. In order to study the working point quality evolution, we only consider the ADC curves of the same 12 channels at the fixed working point at each irradiation step. Again, we use the fraction of the number of good ADC curves over all recorded ADC curves as a measure for the quality of the working point. Figure 8.3 shows this fraction as a function of the irradiation dose step, the statistical error bars are computed according to Poisson statistics, as the measure is based on counting good ADC curves and are large because of the limited statistics of only 12 ADC channels. Nevertheless, we observe a rather constant working point quality that is > 0.6 for nearly all irradiation steps. The strongest degradation of the quality is seen at 2500 krad down to 0.5. Figure 8.4 shows the evolution of the median of the LSB values, the median noise values and the INLpp values of the 12 channels per irradiation step. The LSB and noise values are constant over the full irradiation dose, the INLpp values show a slight increase towards higher irradiation doses. We can conclude that the chosen working point is stable up to a total irradiation dose of 4.1 Mrad and that the DCD functionality does not seem to be degraded significantly.

Performing an analog re-optimization procedure at each irradiation step revealed, that also the optimal working point does not change significantly. We do observe some variations of the re-optimized working points, however, these are in the order of the scanning step sizes for the DACs and supply voltages and may as well be caused by voltage or temperature fluctuations. Especially, there is no preferred direction of the working point shifts, it rather seems like a small jitter within the optimal working point region.

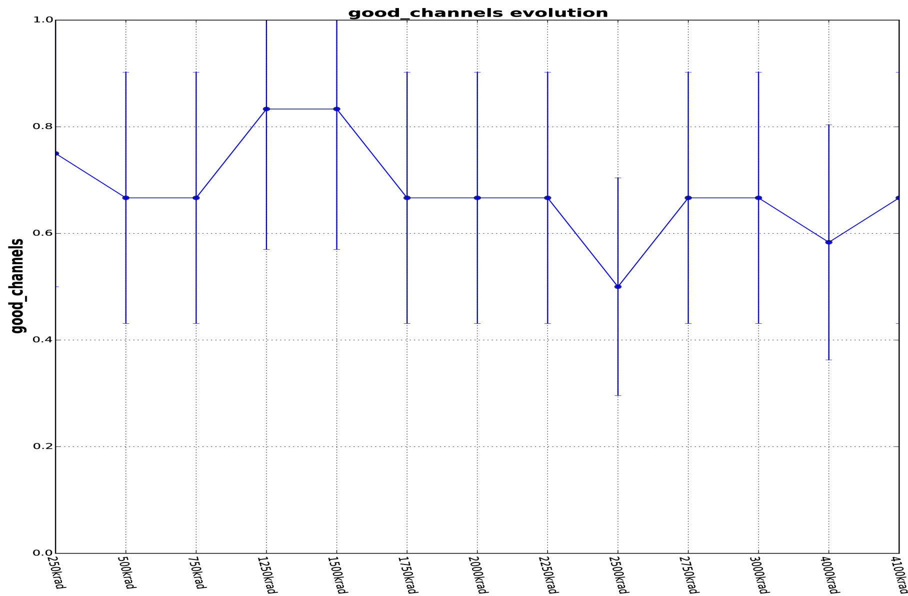

Figure 8.3: Evolution of the optimal working point quality over the irradiation dose steps for a Hybrid5 module. The quality is measured as the fraction of good ADC curves over all recorded ADC curves. At each irradiation step 12 ADC curves were recorded. The error bars indicate the statistical Poisson errors.

8.3.2 Stability of the Inter-ASIC Communication

Irradiation may also affect the strength of the output drivers of the 64 DCD-DHP communication links and the inverters used as delay elements for delaying the DCD_CLK clock signal and the data transmission on each link. Therefore, we also investigate, to what extend the inter-ASIC communication is degraded by irradiation damage. We use the digital test pattern method and the 1-dimensional projections of the delay matrices as described section 7.1. The figure of merit for the quality and optimizability of the data links is again the delay tolerance, i.e. the width of the error rate $R = 0$ (good region) valley in the 1-dim. projection. For all 64 links we measure these widths and histogram them for different irradiation doses. Figure 8.5 shows the results for the irradiated ASIC pair of the EMCM module, note that the delay tolerance is not given in the absolute number of delay elements, but as the fraction with respect to the full delay range of 30 delay elements. The top histogram (blue) indicates the delay tolerance distribution before irradiation, most links show a sufficiently large delay tolerance, there are no links with a delay tolerance of 0, meaning no broken links. The situation changes after a total dose of 2 Mrad (red histogram), the distribution is shifted towards smaller delay tolerance values,

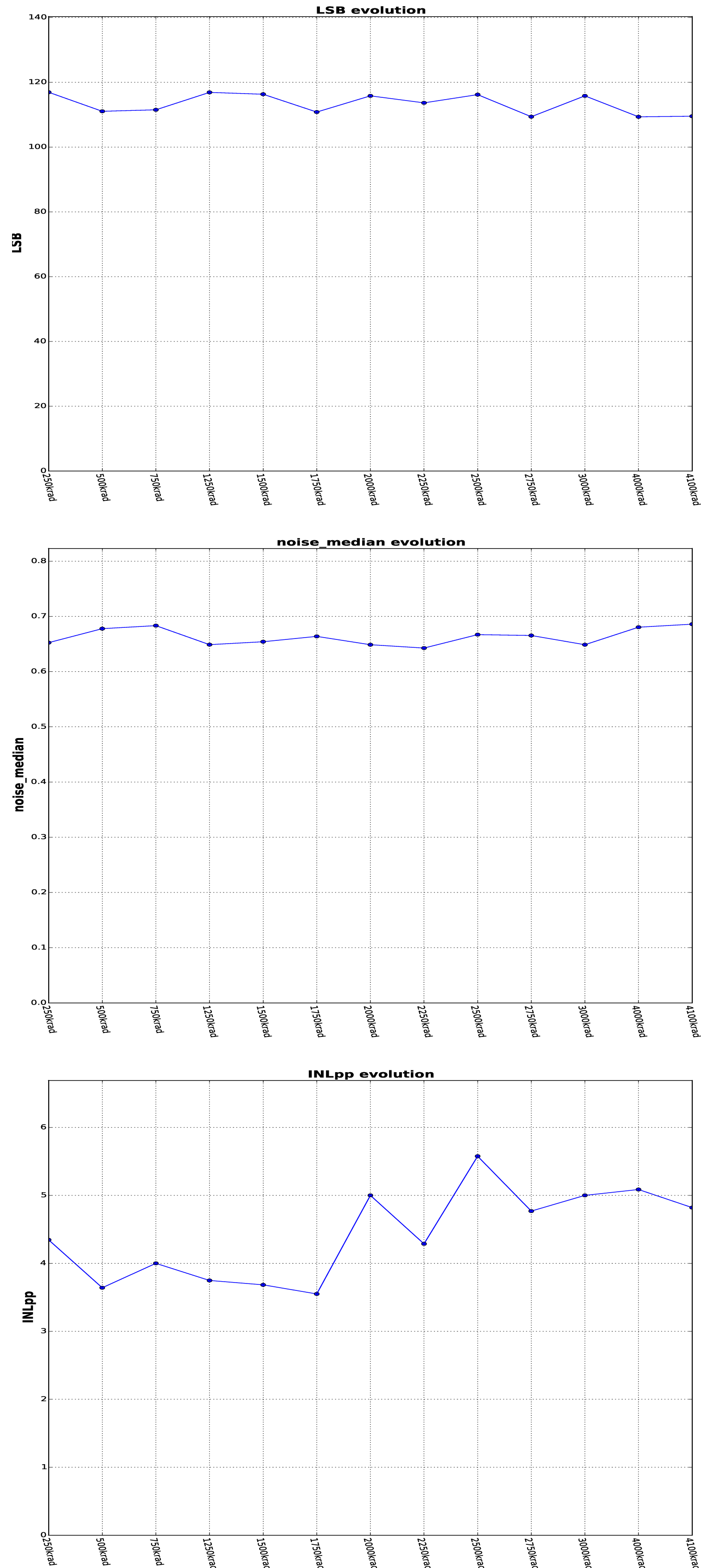

Figure 8.4: Evolution of the median of the LSB, median noise and INLpp values of the 12 recorded ADC channels over the full irradiation range.

the mean tolerance is smaller by 0.04 with respect to the unirradiated situation. Also, there are some links with delay tolerance 0, meaning some links are lost and are no longer optimizable. For a total irradiation dose of 10 Mrad the delay tolerances recover, the lost links become stable and optimizable again and the distribution is shifted towards higher delay tolerance values.

Figure 8.6 summarizes the histogram information for each irradiation step in a candlestick chart. The massive bar indicates the 1σ interval around the mean value, the top and bottom lines indicate the 95 % and the 5 % quantiles, respectively. For 0.5 Mrad, 10 Mrad and 20 Mrad multiple measurements were done and are shown time ordered. The test pattern delay measurements have been started at $15 - 60$ min after the irradiation was stopped. Overall, the data indicates a slight degradation of the delay tolerances starting at small doses, which stays constant for irradiation doses up to 2 Mrad. For higher irradiation doses, the delay tolerances seem to recover to higher values and data indicates even a slight improvement with respect to the situation before irradiation. The multiple measurements at 0.5 Mrad and 20 Mrad do not show large variations, the respective first measurement were started at 77 min (0.5 Mrad) and 10 min (20 Mrad) after irradiation stopped. The following measurements were done around 145 min (both) and $10 - 15$ h (only for 20 Mrad) after irradiation stopped. Again, there was no specific annealing procedure applied and the module was cooled with a water chiller at 10 °C. The ASICs, however, were probably at higher temperatures especially during the analog ADC measurements. For the 10 Mrad measurements we see a large variation of the delay tolerances. The first measurement started 27 min after irradiation stopped, the second and third measurements were done $72 - 100$ min after irradiation stopped and the final measurements started 4 h after irradiation stopped. The first measurement at 10 Mrad shows very small delay tolerances and a large number of lost links, this recovers to the $0.5 - 2$ Mrad level for the following two measurements. Only the last measurement shows high delay tolerances and no lost links again at the level of the 20 Mrad measurements. This behaviour seems to hint to some kind of intrinsic annealing process, although it is not clear why this is not seen for the other measurements, given similar timings at which the measurements where started after stopping the irradiation. It might be, that other measurements, especially ADC curve measurements, were usually done before the delay measurements, thus causing higher temperatures and a stronger annealing, while for 10 Mrad the delay measurements were performed first. Unfortunately, the exact measurement procedures cannot easily be retraced due to insufficient logging of the measurement procedures.

Concluding, we can state that a small degradation of the DCD-DHP data link communication for irradiation doses of 0.5 Mrad to 2 Mrad were observed for the EMCM

measurements and hints of annealing processes were seen. The Hybrid5 data link communication measurements similarly indicate a slight degradation of the delay tolerances, which is worst at a total irradiation dose of 2.5 Mrad. As presented in the previous section, the DCD analog performance does not show any significant degradation when being irradiation up to doses of 4 Mrad. Despite the slight degradation of data link qualities, the overall DCD-DHP ASIC pair performance seems reasonably stable for the expected irradiation doses at Belle II.

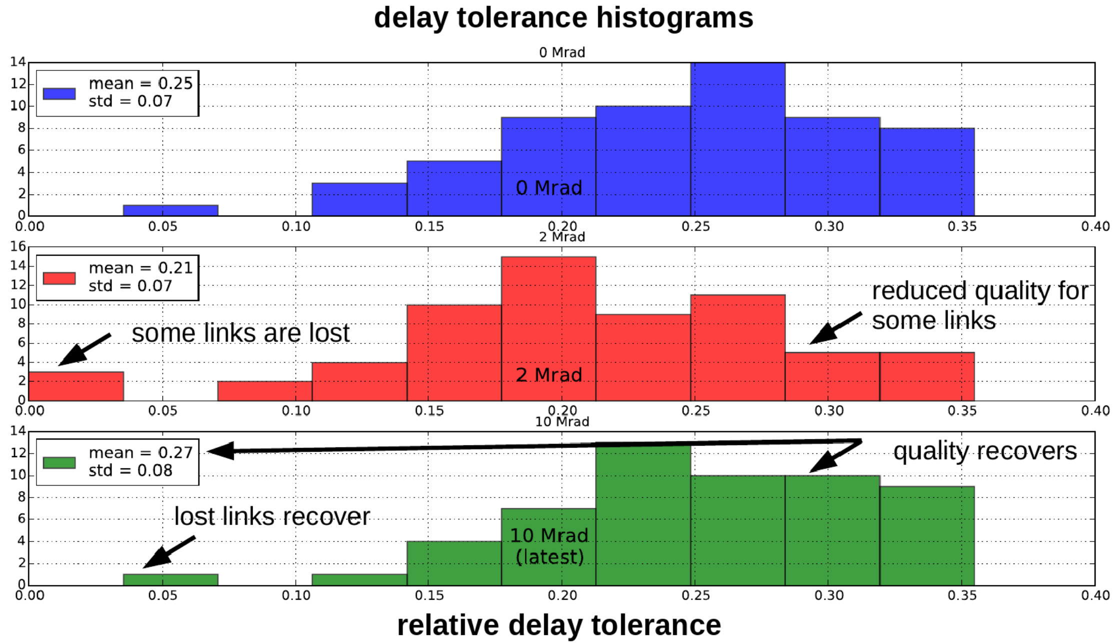

Figure 8.5: Histogram of the delay tolerance of the 64 DCD-DHP data communication links for the irradiated ASIC pair of EMCM W31-3. The delay tolerance is the measure of the stability and optimizability of the data link, a higher value is better. Here, the delay tolerance is given as the width of the bit error rate $R = 0$ valley in the 1-dim. delay matrix projection in number of inverter pairs divided by the total delay range of 30. The histograms are given for the situation before irradiation and after a total dose of 2 Mrad and 10 Mrad.

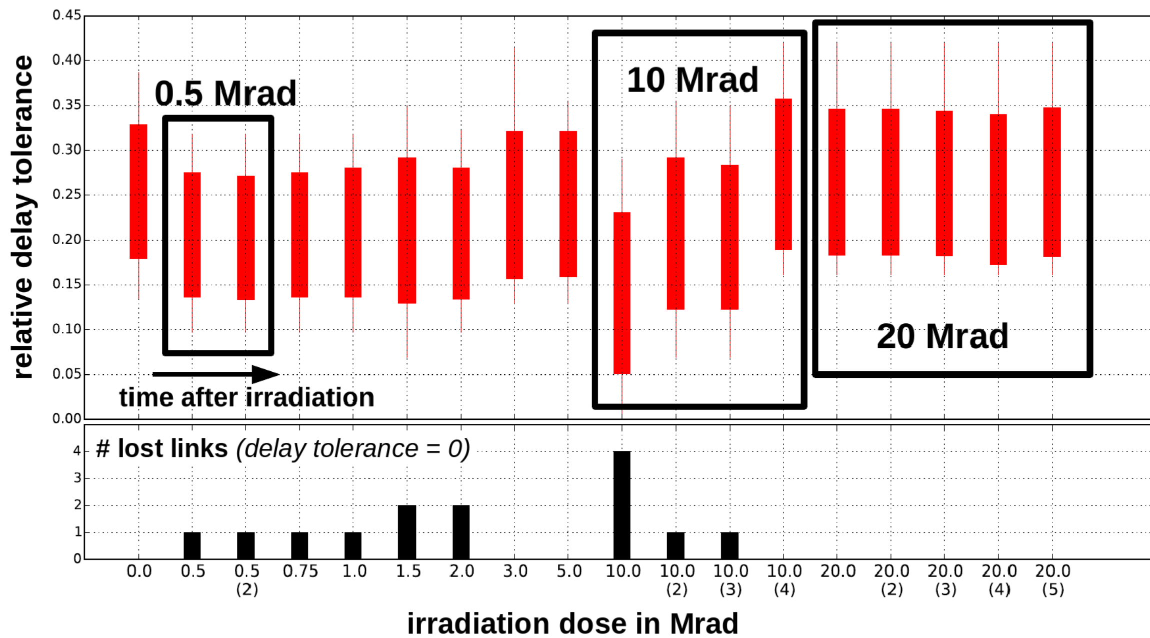

Figure 8.6: Delay tolerance evolution over all irradiation steps on the irradiated ASIC pair of EMCM W31-3 shown as a candlestick chart. At each irradiation step, the bar indicates the 1σ interval of the respective delay space histogram, the middle of the bar is the mean of the histogram, the lines at top and bottom indicate the 95 % and the 5 % quantiles, respectively. For several irradiation steps (0.5, 10 and 20 Mrad) multiple measurements have been done and are indicated by the black squares. The individual measurements are time ordered. The bottom plot indicates the number of lost links (links with delay tolerance 0) per irradiation step.

9 Summary & Conclusion

The new DEPFET pixel sensor for Belle II is expected to significantly improve the tracking and vertex resolution compared to the Belle experiment. DEPFET pixel detectors are a very promising concept also for future linear colliders, as they can be build as very thin sensors. For reading-out DEPFET pixel matrices, new front-end read-out concepts are necessary, new chip designs need to be developed and tested. The Belle II PXD system will use three dedicated ASICs, the DCD, the DHP and the SWITCHER, for steering and reading out the DEPFET matrices. The first step in the read-out chain is the digitization of the DEPFET signal currents, which is done by the DCD. The DCD is essentially an implementation of 256 analog-digital converters working in parallel. Several parameters allow for tweaking the operation of the ADCs and one needs to find optimal values for these parameters to optimize the overall DCD performance. In the scope of this thesis, testing algorithms were developed in order to characterize the analog performance of the current DCD design and to scan and tune its operation parameters. With the implemented analysis framework, the optimal working point of a given DCD ASIC can be found and the quality of each of its 256 ADCs can be studied. The DCDs on multiple testing systems were investigated and optimized, the optimal operation parameter values for all DCDs are found in a small parameter space window. Recommended standard values for the DCD parameters were defined, that are expected to work reasonably well for all DCDs. In the scope of two irradiation campaigns, the testing systems and their ASICs have been irradiated with an X-ray source up to doses of 20 Mrad, which is the expected dose for the Belle II PXD system after 10 years of operation. No significant degradation of the DCD analog performance was observed over several irradiation dose steps. The optimizability of the data link delays between the DCD and DHP ASICs was the second subject of this thesis. An analysis of the delay matrices, obtained from the digital test pattern scan of the global and local delay settings, was implemented and the delay tolerance was defined as the figure of merit indicating data link delay optimizability. The analysis of test pattern scans performed at different global reference clock voltages indicate, that the DCD-to-DHP data communication becomes less stable at higher operation frequencies, especially when going to the nominal 76.23 MHz GCK clocking frequency for the PXD system. As a

consequence, the next ASIC iterations will have improved output drivers (DCD) and signal receivers (DHP). Data from the irradiation campaigns indicate, that the DCD-DHP data communication stability decreases slightly for irradiation doses of 0.5 Mrad to 2.5 Mrad, some links are found to be lost, i.e. not optimizable any more, for these doses. There are also hints of annealing processes which improve the communication stability over time. For in depth studies of the data communication failures, we developed testing algorithms that identify bit errors by using ADC transfer curves. We observed that in some cases the bit error probability is dependent on the sent output code itself, i.e. the probability for a bit to be transmitted wrongly depends on what is being sent on neighbouring inks. This is a strong indication of cross-talk among the data communication links. Resulting form these observations, the design of the link routings for the PXD modules was changed and the spacing between links was increased. In order to improve the data link delay optimization, we studied the possibility to use the bit error recognition in ADC transfer curves instead of employing the digital test pattern. Results show that the ADC method is a valid alternative and yields a little more constrain on the delay parameters. However, it is not yet competitive to the test pattern method as measurement times are much larger. Currently, the option to use the DEPFET transistors, i.e. the pixels of the DEPFET matrix, as adjustable current sources is under study. This method for measuring ADC curves promises much faster measurement times compared to using the external DHH current source. In conclusion, the following achievements are the result of this thesis:

- Detailed testing algorithms were developed and implemented for investigating and optimizing the performance of the front-end read-out ASICs. This testing framework is now being used in the collaboration for studying the current ASIC generations and will also be applied to characterize future ASIC iterations.

- Functionality of the current versions of the DCD and DHP ASIC were proofed. The read-out chips are optimizable and show good performance. The data from two irradiation campaigns indicate, that both ASICs are radiation hard and their performance is expected to not significantly degrade over the expected irradiation doses for the Belle II PXD system.

- Cross-talk effects among the DCD-DHP data communication links were observed and it was proven that this is an issue with the current routing layout. As a result, the spacings of the data links were improved in the new routing design for the PXD half-ladder modules. That means, the developed testing framework and the conducted analyses provide a valuable feed-back for the ASIC and module designers.

Bibliography

[1] T. Aushev (Belle II Collaboration), *Status and prospects of SuperKEKB collider and Belle II experiment*, in *Proceedings, 15th Lomonosov Conference on Elementary Particle Physics (LomCon)*, pages 296–300 (2013), `1201.1248`

[2] K. A. Olive, et al. (Particle Data Group), *Review of Particle Physics*, Chin. Phys. **C38**, 090001 (2014)

[3] B. Wang (Belle II Collaboration), *The Belle II Experiment and SuperKEKB Upgrade*, in *10th International Workshop on e+e- collisions from Phi to Psi (PHIPSI15) Hefei, Anhui, China, September 23-26, 2015* (2015), `1511.09434`

[4] B. Wang, *Searches for New Physics at the Belle II Experiment*, in *Meeting of the APS Division of Particles and Fields (DPF 2015) Ann Arbor, Michigan, USA, August 4-8, 2015* (2015), `1511.00373`

[5] A. G. Akeroyd, et al. (SuperKEKB Physics Working Group), *Physics at super B factory* (2004), `hep-ex/0406071`

[6] T. Abe, et al. (Belle II Collaboration), *Belle II Technical Design Report* (2010), KEK-REPORT-2010-1, `1011.0352`

[7] G. B. Mohanty, *Belle II Silicon Vertex Detector*, in *10th International 'Hiroshima' Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD-10) Xian, China, September 25-29, 2015* (2015), `1511.06197`

[8] M. Koch, *Development of a Test Environment for the Characterization of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for the Belle II Experiment at SuperKEKB*, Ph.D. thesis, Bonn U. (2011), CERN-THESIS-2011-084

[9] J. Schieck, *DEPFET pixels as a vertex detector for the Belle II experiment*, Nucl. Instr. Meth. Phys. Res. A **732**, 160 (2013), Vienna Conference on Instrumentation 2013

[10] J. Kemmer, G. Lutz, *New detector concepts*, Nucl. Instr. Meth. Phys. Res. A **253(3)**, 365 (1987)

[11] C. M. Marinas Pardo, *DEPFET: A silicon pixel detector for future colliders. Fundamentals, characterization and performance*, Ph.D. thesis, Valencia U., IFIC (2011), CERN-THESIS-2011-101

[12] A. Oyanguren, *Air cooling for Vertex Detectors*, in *International Workshop on Future Linear Colliders (LCWS11) Granada, Spain, September 26-30, 2011* (2012), 1202.6239

[13] J. Knopf, *Developement, Characterization and Operation of the DCDB, the Front-End Readout Chip for the Pixel Vertex Detector for the Future BELLE-II Experiment*, Ph.D. thesis, Heidelberg U. (2011)

[14] P. Fischer, I. Peric, C. Kreidl, *SwitcherB18 (Gated Mode) Reference Maunal*, DEPFET Collaboration (2015), not published

[15] I. Peric, C. Kreidl, P. Fischer, *DCD-Bv4-Pipeline Reference Manual*, DEPFET Collaboration (2015), not published

[16] H. Krueger, M. Lemarenko, L. Germic, *DHPT 1.0 Manual*, DEPFET Collaboration (2015), not published

[17] D. Levit, I. Konorov, S. Paul, D. Greenwald, *FPGA based data read-out system of the Belle II pixel detector*, IEEE Trans. Nucl. Sci. **62(3)**, 1033 (2015), 1406.3864

[18] J. Knopf, P. Fischer, C. Kreidl, I. Peric, *A 256 channel 8-Bit current digitizer ASIC for the Belle-II PXD*, J. Instrum. **6(01)**, C01085 (2011)

[19] I. Peric, et al., *DCD: The multi-channel current-mode ADC chip for the readout of DEPFET pixel detectors*, IEEE Trans. Nucl. Sci. **57**, 743 (2010)

[20] F. Lütticke, *Offset on H5 and operational experience of H6*, talk for the 19th International Workshop on DEPFET Detectors and Applications, May 2015, Seeon, Germany (2015), not officially published

[21] H. Krüger, *Design Changes for DHPT 1.1*, talk for the 19th International Workshop on DEPFET Detectors and Applications, May 2015, Seeon, Germany (2015), not officially published

Danksagung

Mein Dank gilt Frau Prof. Dr. Ariane Frey für die Möglichkeit, meine Master-Abschlussarbeit in Ihrer Forschungsgruppe schreiben zu dürfen. Es war eine großartige Erfahrung, in Ihrer B-Physik-Arbeitsgruppe an aktueller Forschung mitarbeiten zu können und im Rahmen dieser an den verschiedensten Messkampagnen teilnehmen zu können. Des Weiteren möchte ich mich bei Herrn Dr. Jörn Große-Knetter dafür bedanken, dass er die Rolle des Zweitgutachters für meine Arbeit übernommen hat. Ich hoffe, es war für Sie beide eine interessante und aufschlussreiche Lektüre! Weiterhin danke ich im Besonderen Herrn Dr. Benjamin Schwenker für seine unermüdliche und engagierte Betreuung meiner Forschungsarbeit. Ich bedanke mich für die angenehme Atmosphäre innerhalb der Arbeitsgruppe und bei allen weiteren Mitgliedern der B-Physik-Gruppe, Harrison Schreeck, Ulf Stolzenberg, Uwe Gebauer, César Beleño und Dr. Philipp Hamer, die stets ein offenes Ohr für Probleme und Diskussionen haben. Abschließend möchte ich mich ganz herzlich bei meiner Familie und meinen Freunden bedanken, die während der fünf Jahre meines Studiums stets für mich da waren, mich aufgebaut haben, wenn ich es brauchte und die sich mit mir gefreut haben über meine Erfolge. Ohne Eure Unterstützung hätte ich es nicht geschafft, vielen Dank!

Erklärung nach §17(9) der Prüfungsordnung für den Bachelor-Studiengang Physik und den Master-Studiengang Physik an der Universität Göttingen:

Hiermit erkläre ich, dass ich diese Abschlussarbeit selbständig verfasst habe, keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe und alle Stellen, die wörtlich oder sinngemäß aus veröffentlichten Schriften entnommen wurden, als solche kenntlich gemacht habe.
Darüberhinaus erkläre ich, dass diese Abschlussarbeit nicht, auch nicht auszugsweise, im Rahmen einer nichtbestandenen Prüfung an dieser oder einer anderen Hochschule eingereicht wurde.

Göttingen, den 19. Mai 2016

(Philipp Wieduwilt)