PROCEEDINGS OF SCIENCE

Development of the Compact Processing Module for the ATLAS Tile Calorimeter Phase-II Upgrade

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Abstract: The Phase-II Upgrade of the ATLAS TileCal requires a new readout architecture with a fully digital trigger system in order to cope with the HL-LHC requirements. The on-detector readout electronics will transmit digitized data to 32 Tile PreProcessor modules in the counting rooms at the LHC frequency, transmitting selected data to the FELIX system and interfacing with the trigger systems. Each Tile PreProcessor module is composed of 4 Compact Processing Modules with single-width AMC form factor and one full-size ATCA carrier with 4 slots. This contribution presents the design of the first Compact Processing Module prototypes, and reviews the design of the Tile PreProcessor Demonstrator board for the TileCal Demonstrator programme.

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1. Introduction

The Tile Calorimeter (TileCal) [1] is one of several subdetectors forming the ATLAS experiment [2] at the Large Hadron Collider (LHC). TileCal is a sampling calorimeter made of steel plates and plastic scintillators which are read out using approximately 10,000 PhotoMultipliers Tubes (PMTs).

The Phase-II Upgrade of TileCal (2024-2026) [3] will expose the detector to High Luminosity LHC (HL-LHC) conditions. This upgrade requires a complete redesign of the on- and off-detector electronics, and the implementation of a completely new readout architecture with new interfaces to a fully digital trigger system.

After the Phase-II upgrade, the on-detector readout electronics will transmit the detector data to the Tile PreProcessor (TilePPr) modules in the counting rooms at every bunch crossing (~25 ns), requiring a data bandwidth of ~40 Tbps to read out the entire subdetector. The TilePPr module will store the digitized samples in pipeline memories until the reception of a trigger acceptance signal, after which the data will be transmitted to the Front End LInk eXchange (FELIX) system. The data received from the detector is processed in real time, and calibrated energy and time per cell for every bunch crossing are transferred to the first level of trigger through the Trigger and DAQ interface system (TDAQi). Figure 1 shows a detailed block diagram of the envisaged trigger and readout architecture at the HL-LHC.

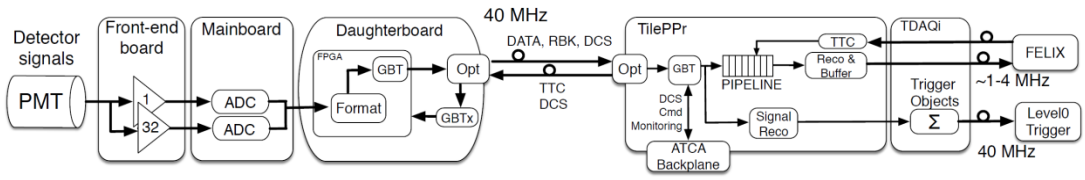

Figure 1. Block diagram of ATLAS Tile Calorimeter at the HL-LHC [3].

1.1 Tile PreProcessor

The TilePPr is the core element of the TileCal off-detector electronics at the HL-LHC. This module will distribute the sampling clock to the on-detector electronics for synchronization with the LHC clock with fixed and deterministic latency, providing a high-speed link for the readout, operation and monitoring of the on-detector electronics. In addition, the TilePPr will transmit calibrated cell energies to the TDAQi system, which will compute and send trigger primitives to the ATLAS trigger systems with improved granularity and precision. A total of 32 TilePPr modules will be required for the complete readout and operation of the detector, and each TilePPr module will read out and operate eight of total 256 TileCal modules.

A TilePPr, in turn, comprises four Compact Processing Modules (CPM) with single-width Advanced Mezzanine Card (AMC) form factor, one full-size Advanced Telecommunications Computing Architecture (ATCA) carrier with 4 slots, and two mezzanine cards: one for a GbE switch and one for a ARM-based computer. The high-speed communication with the on-detector electronics, the data acquisition and the core processing functionalities relies on the CPMs, while functionalities for power management, control and configuration of the TilePPr modules are implemented in the mezzanine cards. Figure 2 shows a block diagram of the TilePPr module describing the different elements and interconnections.

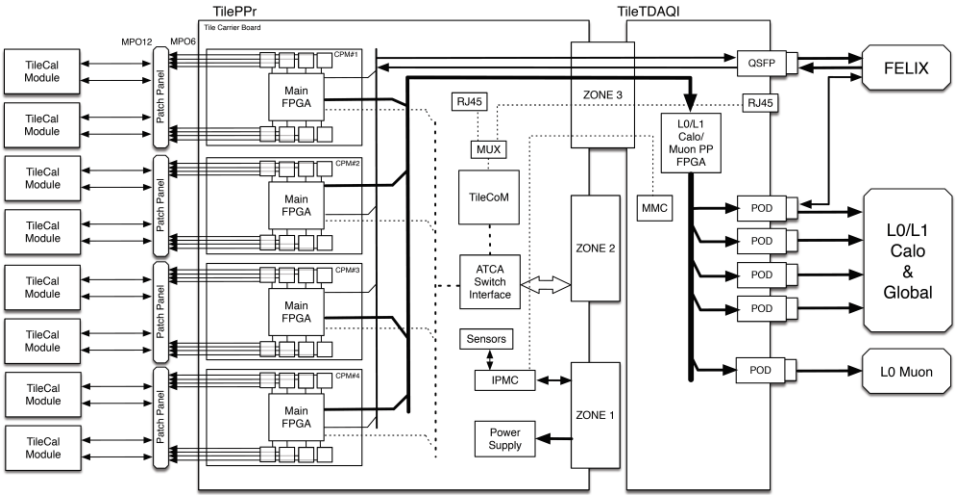

Figure 2. Block diagram of the TilePPr module.

1.2 TilePreProcessor Demonstrator

The TilePreProcessor Demonstrator, shown in Figure 3, was designed to evaluate the performance of the upgraded electronics and trigger interfaces before the design of the final versions for the HL-LHC. This board can operate and read out one TileCal module, representing 1/8th of the final TilePPr module.

The TilePreProcessor Demonstrator is a double mid-size AMC form factor board equipped with one Xilinx Virtex 7 FPGA connected to 4 QSFP optical modules to read out and operate one upgraded TileCal module, and one Kintex 7 FPGA connected to one Avago MiniPOD to perform trigger preprocessing tasks.

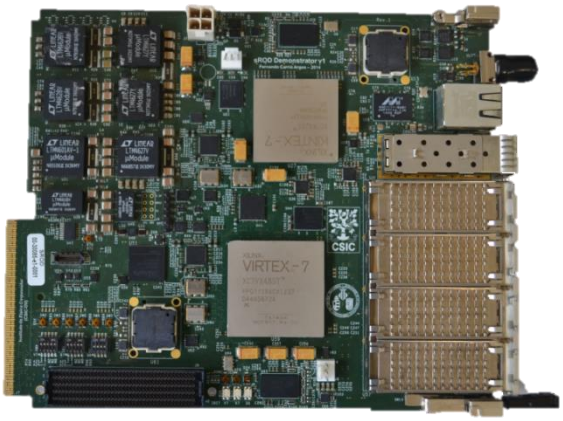

Figure 3. Picture of the Tile PreProcessor Demonstrator board.

This board has been used to validate the upgraded on-detector electronics and readout architecture during six test beam campaigns at the Super Proton Synchrotron accelerator facilities between 2015 and 2018. The TilePreProcessor Demonstrator is currently installed in USA15 for the readout and operation of the Demonstrator module inserted in ATLAS.

1.3 Compact Processing Modules

Each CPMs of a TilePPr will read out and operate two TileCal modules, transmitting the LHC clock through high-speed links with fixed and deterministic latency. The CPMs will process the detector data in real-time, providing calibrated cell energy to the TDAQi FPGA. The detector data will be stored in circular pipeline memories with a maximum depth of 10μs until

the reception of a trigger acceptance signal. The selected data will be transmitted to the FELIX system with a maximum trigger rate of 1 MHz.

The design of the CPM is largely based on the experience and results obtained with the development of the Tile PreProcessor Demonstrator. The CPM is a single AMC form factor board equipped with 8 Samtec FireFly modules terminated with MXC connectors; a Xilinx Kintex UltraScale FPGA for data buffering, digital processing and control; a Xilinx Artix 7 FPGA for slow control and monitoring; and a large number of high-speed interconnections for the communication with the TDAQi.

The PCB stack-up consists of 14 layers, where 6 layers are devoted to signals and 8 to power and ground planes. ISOLA FR408HR dielectric material was selected due to its reduced dielectric constant (~3.68) and its reduced loss tangent (~0.01) compared with other FR4 materials. The PCB interconnects were designed to match 100 Ω for the differential signals and 50 Ω single-ended signals. Figure 4 shows a picture of the layout of the CPM showing all the internal signal layers.

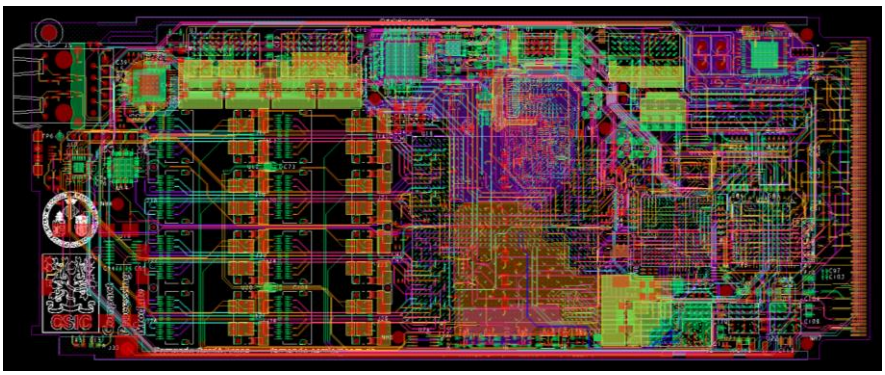

Figure 4. Layout of the Compact Processing Module.

Several signal integrity studies were performed using ANSYS Electromagnetics during the pre-layout and post-layout stages of the design. Differential vias were simulated to minimize the impedance mismatch when high-speed signals travel between layers. In addition, the high-speed communication paths were simulated using IBIS-AMI models and S-parameter models to ensure the proper signal integrity.

Figure 5 shows a simulated eye diagram corresponding to the high-speed lines connecting the Samtec FireFly modules and the FPGA (left); and the Time Domain Reflectrometry (TDR) results of the simulation of the differential vias when varying the via ground distance and antipad diameter (right).

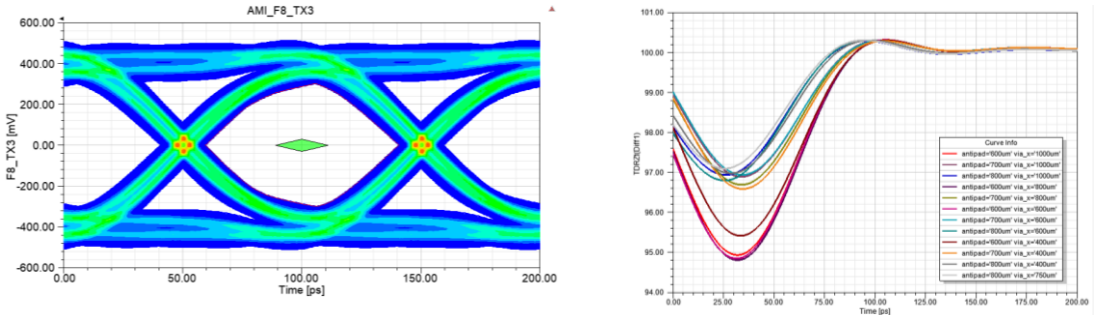

Figure 5. Simulated eye diagram of the lines between the Samtec FireFly and the Kintex UltraScale FPGA (left). Results of the TDR simulations of the differential vias for different positions of the ground vias and antipad diameter (right).

One critical part of this design is the fibre routing on the CPM. The high density of fibres increases the complexity of the component assembly while respecting the minimum allowable bend radius of the fibres [4]. In order to evaluate the fibre layout, a mechanical mockup of the CPM was designed prior to the production of the complete prototypes. Figure 6 shows a picture of the mechanical mockup of the CPM.

Figure 6. Mechanical mockup of the Compact Processing Module.

Although the fibre layout presented in Figure 6 complies with the manufacturer specifications, the fibre density close to the optical modules will be relaxed by using longer fibres passing through the FPGA heatsink.

Conclusions

The on-detector radiation levels and the larger data bandwidths required for the new readout architecture in the HL-LHC era lead to the complete redesign of the on-detector and off-detector electronics of the ATLAS Tile Calorimeter system.

This contribution describes in some detail the design of the Compact Processing Module for the HL-LHC. The CPMs will be the core of the off-detector electronics reading out and operating the TileCal modules. They are also responsible for transmitting selected events to the FELIX system at the L0 trigger rate and reconstructed cell energy to the TDAQi system for every bunch crossing. The design and status of the Tile PreProcessor Demonstrator during the last years are also reviewed.

Acknowledgments

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References

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