

# Hardware production quality control for the ATLAS Phase-I readout upgrade

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The off-detector data acquisition system upgrade of the LHC ATLAS experiment at CERN is based on the Front-End LInk eXchange framework. As part of this upgrade, approximately 120 custom PCIe cards are being produced by an industrial partner, based on a hardware design developed within the ATLAS collaboration. This production requires detailed Quality Assurance and Quality Control procedures to ensure the hardware being produced is fully functional and robust for many years.

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## 1. Introduction

The Large Hadron Collider (LHC) has been successfully delivering proton-proton collision data at the unprecedented center of mass energy of 13 TeV with an instantaneous luminosity already above design. Figure 1 shows the road-map of the LHC and the increasing performance in terms of luminosity, requiring important upgrades on both machine and experiments. ATLAS [1] is performing several upgrades on the detector, the trigger and the data acquisition system for the data taking in Run 3 (after the Phase-I upgrade [2], starting in 2021) and Run 4 (Phase-II upgrade [3], starting in 2026).

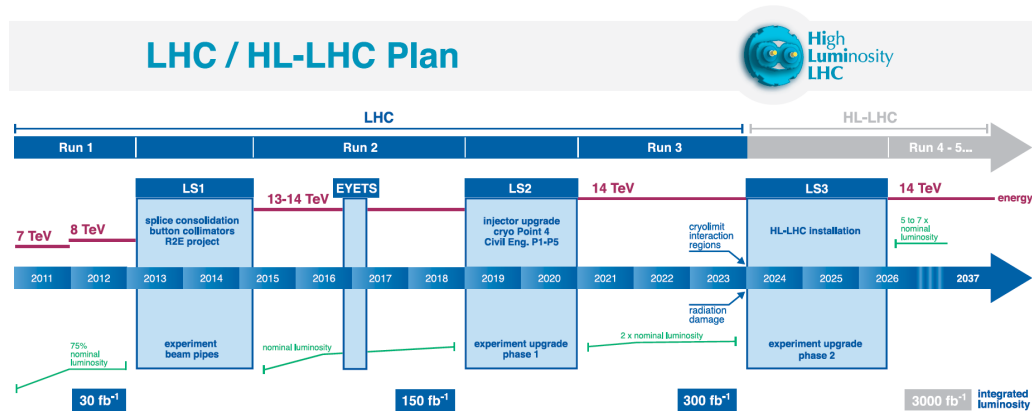


Figure 1: LHC storyline and future plans.

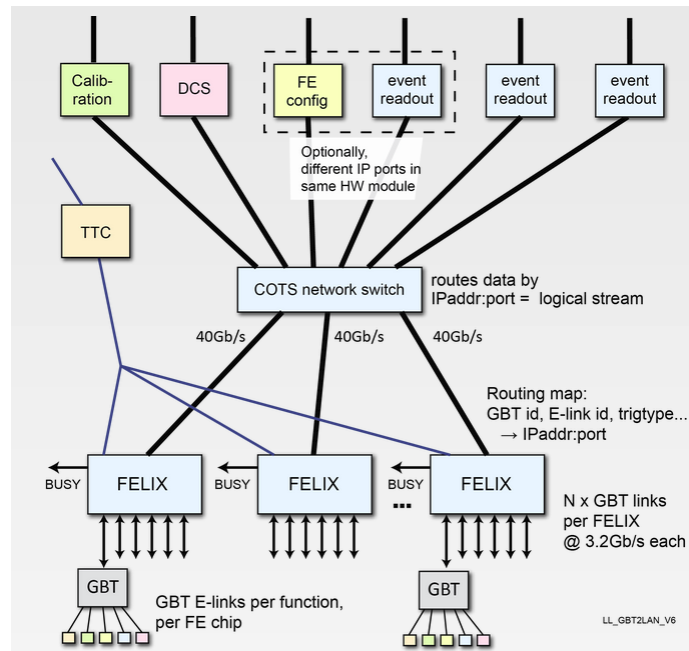
One of the most relevant upgrades in ATLAS Phase-I will be the implementation of the New Small Wheel (NSW) subdetector, as part of the Muon Spectrometer, and a new set of off-detector FLX-712 DAQ (Data Acquisition) cards developed by the FELIX collaboration [4]. These are currently under production and commissioning and will be used to read out the NSW.

## 2. FELIX Architecture

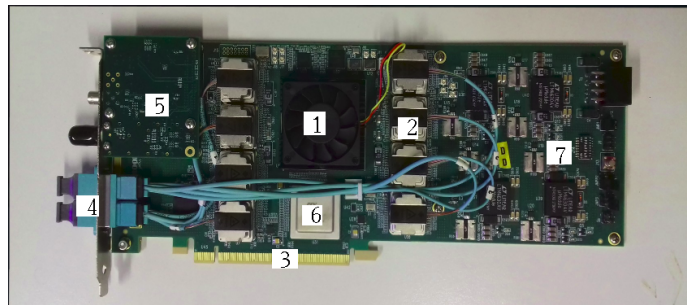
The FELIX (Front-End Link eXchange) [5] architecture is based on the idea of reading out the detector with a dedicated common readout system, integrated in commercial off-the-shelf servers. Figure 2 shows a scheme of the DAQ infrastructure, which will be used to read out several upgraded ATLAS subsystems after the Long Shutdown 2. Figure 3 shows the FELIX FLX-712 board developed for use in ATLAS already in Run 3. The card data acquisition is based on 48 links tested at 9.6 Gb/s using the high-speed serializer-deserializers available on the on-board FPGA. A 24 link version of the card exists as well. The FLX-712 uses two data protocols: the GBT (4.8 Gb/s) and the FELIX custom FullMode (9.6 Gb/s). An AN2814 chip filters the clock from data and a Si5345 jitter cleaner handles the TTC input and the high-quality clock for the high-speed transmission in the FPGA.

## 3. Test Plan

To ensure the quality of the FLX-712 cards after the production a list of checks and tests was



**Figure 2:** FELIX infrastructure [5].



**Figure 3:** FLX-712 card. The board is based on a Xilinx XCKU115 FPGA [6] [7] (1) and is composed of a 16 stackup PCB (7). FLX-712 features a PCI Express Gen3 with 16 lanes (3) managed in a 8x2 structure with a PCIe switch (6) and an opto-electrical converter. The conversion is performed by eight devices called miniPODs (2), four in transmission and four in reception. The miniPODs gather together 12 links each and are connected to the output MTP coupler device (4). In the end a TTC (Trigger Timing and Controller) card (5) copes with the ATLAS global clock cleaning it and asserts the Busy signal from the DAQ PC in case of back-pressure.

prepared. This test suite includes standard industrial tests and specific cross-checks prepared by the FELIX collaboration. These tests were implemented because of the high complexity of the cards due to high-quality standard used for manufacturing the PCB and for the high-connectivity of the components. Further the Quality Assurance and Quality Control (QA/QC) is performed to verify the firmware stability, the functionality of the communication between the Linux software tool commands and the cards through PCI Express on the new set of cards.

#### 4. Functionality Test Setup

The motherboard used for the functionality tests executed after the mechanical assembly is a SUPERMICRO X10DRG-Q [8] that features 5 PCI Express (PCIe) Gen3x16 lanes connections and 2 CPU slots populated with 2 Intel Xeon E5-2660 v3 at 2.60 GHz. This configuration allows to manage 4 FLX-712 cards concurrently on the PCIe bus. The operating system used is Scientific Linux CERN 6. The system was set up by the author with the support of the Bologna group. The required scripts to run all the tests were developed following the FELIX team specifications, using FPGA tools to stress the performance and FELIX software scripts to check the card functionalities.

#### 5. Test Description

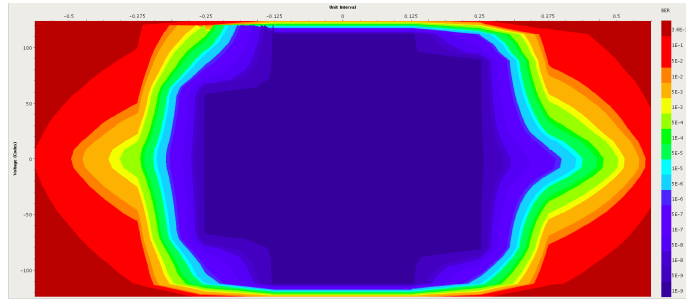
Industrial specifications concerning the PCB quality standard requested by CERN, for example the NADCAP (National Aerospace and Defense Contractors Accreditation Program), had to be fulfilled for the FLX-712 production. In addition, before populating the PCB, the electrical I/O ports were fully tested. Other checks were performed on the cards after the soldering operations to verify the connections and the robustness to mechanical stresses. In particular we have paid attention to the X-rays controls of the biggest BGA pads of the FPGA. After the cards passed the industrial tests and were completely assembled, they were sent to CERN to start the qualification and final acceptance tests. These tests included:

- a further visual check on the cards to make sure their integrity was acceptable;
- Bit Error Ratio (BER) tests on the transceivers side of the FLX-712s. An error bit ratio  $< 10^{-13}$  using a Pseudo Random Binary Sequence was obtained. Figure 4 shows the typical eye diagram that passed the acceptance criteria, based on the shape and the value of the open area of the eye;
- the jitter measurements on several clocks nets in the board to obtain the maximum accepted value of 10 ps;
- the propagation time of L1A signals from the cards to the emulated front-end: the accepted value had to be constant around 500 ns;
- a long-term test of at least 8 hours to stress the stability of the overall data acquisition flow;
- a check of the busy signal from the FLX-712s and the slow control to the simulated front-end;
- two thermal cycles from 0 to 100 °C on a small sample of cards.

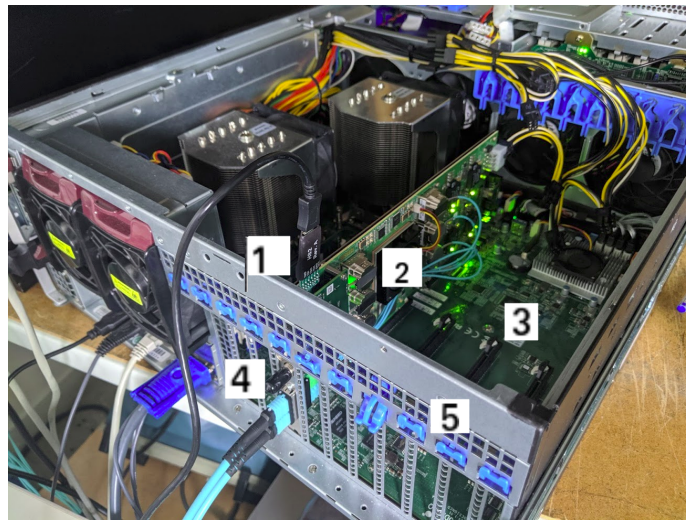
Figure 5 is a picture of one of the setups used during these tests.

#### 6. Summary and Plans for the Future

On December 2018 the Long Shutdown 2 started and the ATLAS Phase-I upgrade begun. The FLX-712 electronic boards, developed within the FELIX collaboration, are under production and



**Figure 4:** One of the many eye diagrams checked.



**Figure 5:** Test setup for fully assembled cards. This image shows the FLX-712 (2), the JTAG connection to communicate with the card (1), the motherboard (3) on the PC, the loopback optical cable for data transmission and reception (4) and the 4U PC case (5).

will be used for some upgraded subdetector readouts as the New Small Wheel in Run 3. For this purpose a new batch of FLX-712 cards was produced and fully validated. All the tests were passed by 18 cards, proving the stability of the hardware design, which was the goal of these tests. The two defective cards are going now through further controls. Some minor modifications will be added to the board design for the next batch of production to avoid possible critical conditions. Some further firmware stability issues occurred during the long-term tests. All these issues are solved now, demonstrating the efficiency of the firmware and of the hardware and software environment. 20 cards were produced as a pre-series and the rest of the production of 100 cards is still ongoing. The validated cards were already delivered to the ATLAS subdetectors for commissioning.

## References

- [1] ATLAS Collaboration , JINST 3 (2008), S08003.
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- [5] J. Anderson et al, *FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrade*, 2015, *J. Phys.: Conf. Ser.* 664 082050.
- [6] Xilinx, *UltraScale Architecture GTH Transceivers*, [http://www.xilinx.com/support/documentation/user\\_guides/ug576-ultrascale-gth-transceivers.pdf](http://www.xilinx.com/support/documentation/user_guides/ug576-ultrascale-gth-transceivers.pdf).
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- [8] SUPERMICRO, *SUPERMICRO X10DRG-Q User Manual*, MNL1677.