Institut für Maschinenelemente
Direktor: o. Prof. Dr.-Ing. Bernd Bertsche Prof. Dr.-Ing. habil. Werner Haas
UNI STUTTGART Lehre und Forschung: Antriebstechnik • CAD • Dichtungstechnik • Zuverlässigkeitstechnik

Volker Schramm

Zuverlässigkeit des Renesas 16 Mbit SRAM in der Strahlungsumgebung des LHC

Reliability of the Renesas 16 Mbit SRAM in the radiation environment of the LHC

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Abstract

To operate the Large Hadron Collider (LHC), the biggest particle accelerator of the European Organization for Nuclear Research (CERN), a new module to control the power converters which deliver the current for the beam influencing magnets of the machine is currently in the development. This Function Generator Controller lite (FGClite) unit uses the 16 Mbit «R1LV1616RSA-7SI#B0» Static Random Access Memory (SRAM) from the Renesas Electronics Corporation as a storage memory for operational data.

Reliability and availability of this functional chain is becoming more and more important due to the planned increase of energy and the upcoming high luminosity environment of the accelerator, meaning an increase of radiation levels which local control equipment is expected to be exposed to. To achieve the reliability requirements for the whole system an analysis needs to start on the lowest functional level investigating components like the «Renesas SRAM» and, if possible and reasonable, improving them. Using this «bottom-up» approach the following work investigates the dependability of the memory divided into electrical- and radiation reliability to predict its' performance in the LHC environment. The main part deals with radiation tolerance executing an irradiation test of the SRAM at a proton beam energy of 24 GeV. This test, performed at the Cern High energy AcceleRator Mixed-field facility (CHARM), is already the fourth irradiation campaign of the memory aiming at qualifying it for the high energy environment of the LHC.

Kurzfassung

Um den Large Hadron Collider (LHC), den größten Teilchenbeschleuniger der Europäischen Organisation für Kernforschung (CERN), zu betreiben ist momentan ein neues Modul in der Entwicklung, das die Stromumrichter, welche den Strom für die strahlbeeinflussenden Magnete bereitstellen, kontrolliert. Diese Function Generator Controller lite (FGClite) Einheit benutzt das 16 Mbit «R1LV1616RSA-7SI#B0» «Static Random Access Memory» (SRAM) der Renesas Electronics Corporation als einen Speicher für operative Daten.

Aufgrund der geplanten Steigerung der Energien und der zukünftigen Hochluminositätsumgebung des Beschleunigers, was mit einer steigenden Strahlungsbelastung einhergeht, bei der anzunehmen ist, dass das lokale Kontrollequipment ihr ausgesetzt ist, wird Zuverlässigkeit und Verfügbarkeit dieser Funktionskette immer wichtiger. Um daher die Zuverlässigkeitsanforderungen an das gesamte System zu erfüllen muss eine Analyse auf der niedrigsten Funktionsebene beginnen, indem sie einzelne Kompenenten wie das «Renesas SRAM» untersucht und falls möglich, sowie auch begründbar, verbessert. Nach diesem «bottom-up» Ansatz untersucht die folgende Arbeit die Verlässlichkeit des Speichers, welche sich in elektrische- und strahlungstechnische Zuverlässigkeit gliedert, um dessen spätere Funktionssicherheit vorherzusagen. Um die Strahlungstoleranz zu erkunden wird im Hauptteil ein Bestrahlungstest des SRAMs bei einer Protonenstrahlenergie von 24 GeV ausgeführt. Dieser Test, welcher an der Versuchseinrichtung Cern High energy AcceleRator Mixed-field facility (CHARM) durchgeführt wurde, ist bereits die dritte Bestrahlungskampagne des Speichers mit dem Ziel ihn für die hohen Energien in der Umwelt des LHC zu qualifizieren.

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Symbols

Symbol	**Meaning**	**Unit**
D_d	Displacement damage dose	MeV/g
K	Kaon	-
n	Neutron	-
p (1) / P+	Proton (both)	-
p (2)	Particle	-
π	Pion	-
σ	SEE cross section	cm^2
ϕ	Fluence	Particles/cm^2

Symbol	**Meaning**	**10^n**
T	Tera	10^{12}
G	Giga	10^9
M	Mega	10^6
k	Kilo	10^3
c	Centi	10^{-2}
m	Milli	10^{-3}
μ	Micro	10^{-6}
n	Nano	10^{-9}
p	Pico	10^{-12}

Abbreviations

Abbreviation	Meaning
A&M	Agricultural and Mechanical (Texas A&M University)
AB	Analogue Board (FGClite)
ADC	Analog-to-Digital Converter
ALICE	A Large Ion Collider Experiment
ASCII	American Standard Code for Information Interchange
ATLAS	A Torroidal LHC Apparatus
CB	Communications Board (FGClite)
CCC	CERN Control Center
CERN	The European Organization for Nuclear Research
CHARM	Cern High energy AcceleRator Mixed field facility
CHF	Swiss Franc (Confoederatio Helvetica Franc)
CMOS	Complementary Metal-Oxide-Semiconductor
CMS	Compact Muon Solenoid
CNRAD	CERN Neutrinos Radiation
COTS	Commercial-Off-The-Shelf
DD	Displacement Damage
dev	Device
DUT	Device Under Test
e.g.	Exempli gratia (for the sake of example)
EN-STI-ECE	Engineering Department – Sources, Targets and Interactions – Equipment Controls and Electronics (CERN)
EN-STI-EET	Engineering Department – Sources, Targets and Interactions – Emergency Energy Technologies (CERN)
ESA	European Space Agency
FGC2	Function Generator Controller version 2
FGClite	Function Generator Controller lite
FIT	Failure In Time
FLUKA	FLUktuierende KAskade (german: fluctuating cascade)
FPGA	Field Programmable Gate Array
GSI	Gesellschaft für SchwerIonenforschung (Darmstadt, Germany)
H	Height
H4IRRAD	Irradiation facility installed in the H4-beamline
HEH	High-Energy Hadrons
HL-LHC	High-Luminsoity-LHC
i.e.	Id est (that is)
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IRRAD	Irradiation proton facility (CERN)
ISSI	Integrated Silicon Solution Incorporated
IUCF	Indiana University Cyclotron Facility

JIS	Japanese Industrial Standard
KAZ	Forschungszentrum Karlsruhe
KVI	Kernfysisch Versneller Instituut (Groningen, Netherlands)
L	Length
LED	Light Emitting Diode
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LINAC2	Linear Accelerator 2
LL	Lower Limit
MB	Main Board (FGClite)
MBU	Multiple-Bit Upset
MCU	Multiple-Cell Upset
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean Time Between Failure
MTTF	Mean Time To Failure
MWPC	Multi-Wire Proportional Chamber
NanoFIP	Nano Factory Instrumentation Protocol
NASA	National Aeronautics and Space Administration
NCC	New Control Card
NMOS	N(egative)-Channel Metal-Oxide-Semiconductor
N-P	Negative-Positive (Transistor)
NSREC	Nuclear and Space Radiation Effects Conference
PAULA	Proton fAcility in UppsaLA (Sweden)
PC	Personal Computer
PCB	Printed Circuit Board
PIF	Proton Irradiation Facility (Paul Scherrer Institute)
PMOS	P-Channel Metal-Oxide-Semiconductor
POT	Particles On Target
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
PSI	Paul Scherrer Institute (Villigen, Switzerland)
PSU	Power Supply Unit
R2E	Radiation To Electronics
Rad	Radiation (-> Rad-hardened)
RadDIM	Radiation tolerant Diagnostic Interface Module
RADEF	RADiation Effects Facility (Jyväskylä, Finland)
RadFET	Radiation sensing Field-Effect Transistor
RadMon V6	Radiation Monitoring System Version 6
RR	LHC area; cavern
RS	Recommended Standard
SBU	Single-Bit Upset
SEB	Single Event Burnout
SEE	Single Event Effect
SEETF	Single Event Effects Test Facility (Texas A&M University)

SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SPS	Super Proton Synchrotron
SRAM	Static Random Access Memory
TCC	Test Control Card
TE-EPC-CCE	Technical Department – Electrical Power Converters – Converter Controls Electronics (CERN)
TID	Total Ionizing Dose
TRIUMF	Tri University Meson Facility (Vancouver, Canada)
TSOP	Thin Small Outline Package
UA	LHC area; parallel tunnel
UCL	Université Catholique de Louvain (Louvain-la-Neuve, Belgium)
UJ	LHC area; cavern
UL	Upper Limit
US	United States
W	Width
XB	Auxiliary Board (FGClite)
XS	SEE cross section (σ)

Indices

Index	**Meaning**
0.01	1%
0.1	10%
d	Dose
eq	Equivalent
th	Threshold

1 Introduction

In the framework of this work the «reliability of the 'R1LV1616RSA-7SI#B0' SRAM of the Renesas Electronics Corporation in a radiation environment» like the environment in the tunnel of the Large Hadron Collider (LHC), is investigated. This work considers the radiation generated by the machine, induced by protons escaping from the circulating beams of the LHC. To set the scene this chapter starts with an introduction to the European Organization for Nuclear Research (CERN) and its research field with later describing the accelerator environments and component requirements there. Subsequently, an irradiation test campaign at the new Cern High energy AcceleRator Mixed-field facility (CHARM) is described and analysed.

1.1 The European Organization for Nuclear Research (CERN)

CERN was founded in 1954 in Meyrin next to the city of Geneva, Switzerland. Its main objective is the research in the fields of particle and high-energy physics. To achieve this CERN operates several particle accelerators including the LHC, the largest single machine in the world. The tunnel of the LHC has a diameter of 27 km in which either proton-, or lead ion-beams, are accelerated in two pipes in opposite directions. These two beams can be merged together at four intersection points, the so called experiments, where they collide. At these four experiments named ATLAS, ALICE, CMS and LHCb (Figure 1-1) the energy of a proton beam can be up to 7 TeV, producing a total centre-of-mass collision energy of 14 TeV for the two beams. By monitoring these collisions the scientists and researchers at CERN try to answer different questions of humanity like:

- What happened after the Big Bang?
- What is dark matter?
- Does the «God particle» (Higgs boson) exist?
- Why is our universe made only of matter? [1]

Just recently the elementary particle Higgs boson was discovered what brought the 2013 Nobel Prize of physics to Peter Higgs and François Englert, the two original researchers.

1.2 The accelerator complex

Currently CERN operates nine different particle accelerators with various applications and experiments. To illustrate how the particles are accelerated one example is described how particles follow a chain to get to the largest accelerator: the LHC.

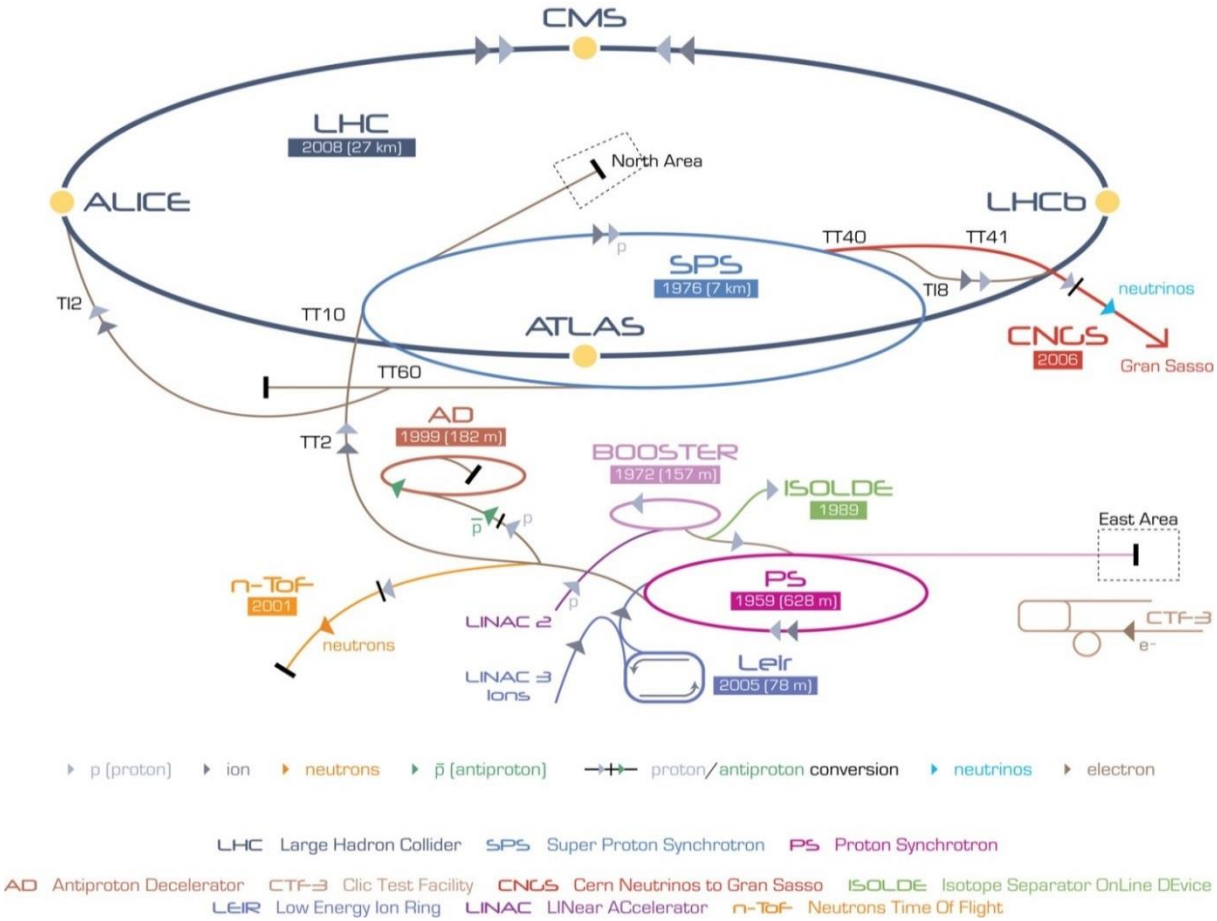


Figure 1-1 : The CERN accelerator complex [2]

The process starts with releasing pure hydrogen into a metallic cylinder, containing a Duoplasmatron accelerator. There, the gas is broken down into protons and electrons (after the chemical equation $H_2 \rightarrow 2H^+ + 2e^-$) by an electrical field. From there, the protons begin their journey. First through LINAC2 (LINear ACelerator 2) which accelerates the particles in an almost perfect vacuum like all the other following pipes. In this machine the protons increase their velocity in an electric field produced by a set of electric magnets until they pass with the energy of 50 MeV and 31.4 % of the speed of light to the circular PS Booster (PSB). After the PSB, they get to the Proton Synchrotron (PS) where they accelerate on a circumference of 628.3 m to already 99.93 % of the speed of light corresponding to the energy of 24 GeV. Following through the Super Proton Synchrotron (SPS) with 6.9 km in circumference the protons get finally injected into the two pipes of the LHC at an energy of 450 GeV. Until the two years long technical stop from 2013 to 2015 the particles in this last accelerator have

reached a maximum energy of 3.5 TeV, which is half of the energy for which the LHC is constructed. Just recently the machine has reached 6.5 TeV which is almost its' design energy. When running at the maximum energy of 7 TeV, the roughly 9300 magnets of the LHC produce a magnetic field of 8.33 T. Giving a comparison, the magnetic field on the surface of the earth is with a maximum value of 65 μT at least 125 000 times weaker. To give another impression about the physics there, the protons velocity is then 99.999999991 % of the speed of light, their kinetic energy of 362 MJ then is comparable to a 1800 kg car at a speed of 2280 km/h and their mass is, after the relativity theory of Einstein, 7460 times the mass of their rest mass when they are not moving [3, 4].

1.3 Component requirements in accelerator environments

As mentioned above the LHC operates just below its design energy. In the following years this energy will be presumably constantly increased up to its limit of 7 TeV in the year 2024. From this point it is planned to upgrade the LHC to a higher-luminosity machine (the so-called High-Luminosity-LHC or HL-LHC). The increase of energy, and increase in beam intensities, increases the radiation in the LHC tunnel, which occurs when particles get accelerated and interact with other particles, e.g. residual particles in the vacuum of the beam pipes or during the intended collisions. Due to this radiation, all components and systems of the LHC, and also of other accelerators which are installed in radiated areas, should be qualified for such corresponding exposures. The «R1LV1616RSA-7SI#B0» Static Random Access Memory from the Renesas Electronics Corporation (from now on called «Renesas SRAM»), described more detailed in the next chapter, is foreseen as one of these components. It is a memory on one printed circuit board (PCB) of the Function Generator Controller lite (FGClite). This FGClite module is foreseen to be installed in the LHC-tunnel in 2016 to control the LHC power converters. For context and to complete the functionality chain, these power converters deliver the current to the either beam bending, accelerating or focussing magnets of the accelerator. In the LHC the FGClite is the more radiation tolerant replacement for the current installed FGC2, of which the predicted radiation performance is not acceptable for the upcoming rise of energy. The next two subchapters explain radiation effects on electronic components and define reliability and availability requirements for the FGClite project, while the second subchapter also presents the cost and budget factor of the project.

1.3.1 Radiation effects on electronic components

Radiation induced effects on electronic components can be divided into three groups, the so called Single Event Effects (SEEs), the Total Ionizing Dose (TID) and the Displacement Damage (DD). The DD and the TID can be grouped into cumulative long-term effects while the SEEs are transient respectively single particle effects. It is called TID when protons or electrons are causing ionizing damage to the atoms of the semiconductor substrate of electronic

components. The TID is measured as absorbed radiation dose in the unit kilorad (krad), Sievert (Sv) or Gray (Gy). To ionize atoms or molecules the incoming particles need to carry enough energy to liberate electrons from them. The effects of this ionization can be threshold shifts, leakage current, timing changes or functional failures. On the other side, protons, electrons and uncharged neutrons can also cause the non-ionizing DD. Measured with the Displacement Damage Dose D_d in MeV/g the effect occurs, when these particles have enough kinetic energy to liberate an atom of the crystal lattice by colliding with it. These defects result in device degradation. Therefore both effects lead sooner or later to a component failure. More various are SEEs which are nuclear interactions of only one single particle with the semiconductor material. Induced by either heavy ions, protons or neutrons, SEEs can be classified into Single Event Latchup (SEL), Single Event Upset (SEU), Single Event Transient (SET), Single Event Burnout (SEB), Single Event Gate Rupture (SEGR) or Single Event Functional Interrupt (SEFI), not to mention that other more precise designations exist. Furthermore they are classified into two groups, with SEFI, SEL, SET and SEU as soft errors and SEB, SEGR and SEL as hard errors. An SEL appears mostly as a soft error, however in some cases it can be a hard error. Soft errors cause a temporary malfunction and may be recovered by a reset, rewrite or power cycle of the device, while hard errors cause a permanent error which is not recoverable. Figure 1-2 illustrates an SEE by showing the impact of a high-energy particle on a transistor. The impact in the depletion region of the N-P junction can shift charges and create voltage as well as current transients, which leads to a loss of information and can also destroy the transistor. A unit to display SEEs with their stochastic appearance is the fluence ϕ of high-energy hadrons (HEH) per cm^2. For accelerator environments HEHs are «typically defined as all hadrons (p, n, π±, K±) with a kinetic energy above 20 MeV» [6]. However, there are at least four effects that need to be considered by making this assumption [6, 7]. The HEH_{eq} value takes the influence of neutrons between 0.2 and 20 MeV into account, which can cause an SEE in this energy range. Also thermal neutrons (0.025 MeV) can create an SEE when producing energetic ions. A so-called risk-factor (R-factor) considers this. As third point the variables $H_{0.1}$ and $H_{0.01}$ are used to compensate a dependence of the SEE cross section (XS) when reaching higher energies up to the GeV-range. They express that either 10 or 1 % of the actual HEH-fluence lies above the estimated value. The SEE cross section expresses the number of SEE errors per fluence, while the fluence is describing the number of energetic particles passing per cm^2, see equation (1.1). Often the Greek letter σ is used for the SEE cross section.

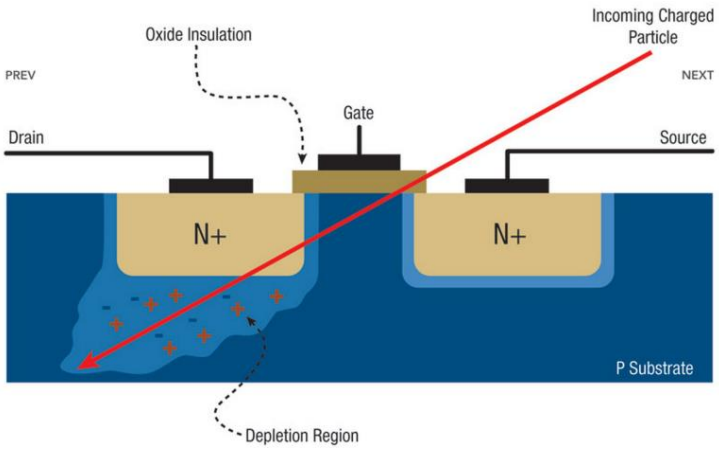


Figure 1-2 : Single Event Upset [5]

$$Errors\ (\#SEEs) = \sigma(cm^2) \times \phi\left({}^{particles}/_{cm^2}\right) \tag{1.1}$$

The last effect regards the influence of low energy singly-charged particles, especially in SRAM technologies. Until now, no describing factor is existent for this, but there is an ongoing study about it [7]. In compliance with the HEH-fluence per cm^2, there are two other definitions respectively units used in this work to represent and illustrate the appearance of SEEs. For irradiating proton beams the beam energy (eV) is commonly used and for an irradiating set of particles, heavy ions for example, the Linear Energy Transfer (LET), displayed in $MeV*cm^2$ per mg or in MeV per µm, is used. The LET describes how much energy an ionised particle transfers to a transversed material per unit length.

1.3.2 Reliability and availability requirements for the FGClite project

For the FGClite project, and therefore the Renesas SRAM, reliability and availability requirements are split into pure electrical on one hand and radiation requirements on the other hand. Taking this into account and looking at the predicted HEH-fluences for the installation locations in table 1-1, radiation requirements for the FGClite are defined as follows [8]:

« 1. Maximum of 10 radiation induced failures per year of operation for all installed FGClite systems that lead to a beam dump of LHC in nominal conditions […]. Taking into account that 1094 units will be installed in the LHC and the respective yearly particle fluences […], a SEE cross-section of the FGClite is required to be lower or equal to 3×10^{-12} cm^2.

2. The FGClite is being designed for the lifetime of the LHC, i.e. around 20 years. The highest doses that are expected in the LHC range between 1 and 10 Gy […]. The minimum TID requirement is then estimated to 200 Gy […]. Taking into account all locations of power converters, a mean value expected at the end of lifetime of the LHC to be around 60 Gy per unit. »

Table 1-1 : Location, number of units and yearly particle fluences for power converters installed in the LHC [8]

Location	Fluence after 2015 (HEH/cm2/year)	Converter 60A-08V	Converter 120A-10V	Converter 600A-10V	Converter 4-6-8kA-08V
Tunnel	4.00E+09	752			
shielded:RR	5.00E+08		92	104	60
shielded:UJ	5.00E+07		10	16	4
shielded:UA	2.00E+07		20	28	8
		752 Units	**122 Units**	**148 Units**	**72 Units**

With the FGClites projects' main goal of maximum ten controller-induced beam dumps due to radiation, respectively SEEs, per year, what simply means a loss of the LHC operation and its availability, the FGClite functionality with its availability has a big target to achieve, especially

by taking into account the number of 1094 installed units. It needs to be mentioned, that for this target of ten radiation induced beam dumps per year only the above described either proton-, neutron-, pion- or kaon-radiation is considered, because other radiation like, heavy ions should not appear in a considerable amount in the LHC tunnel. For context, a beam dump is simply a planned respectively triggered redirecting of the particle beam for safety reasons to an extra tunnel with several graphite blocks at the end for dumping. To qualify the FGClite for the radiation availability target, irradiation testing for SEEs is performed. With the SEE cross section as a result of these tests it is easy to convert this into the goal of ten beam dumps by multiplying the cross section with the respective fluence. The following chapters give a detailed description of these tests. On top of this availability, long-term reliability and availability also play a big role with the system lifetime target of approximately 20 years. It is split into two parts: the cumulative radiation effects and the pure electrical reliability.

For the cumulative effects the concerning requirements are just defined for the TID because DD effects are regarded as not of concern for the operating conditions and the lifetime of the FGClite. The goal for the TID robustness can only be achieved by using tested and qualified components that withstand a dose of at least 200 Gy. A detailed description of the concerning tests and results also follows in the next chapters.

The electrical reliability requirements are defined with a Mean Time To Failure (MTTF) of one million hours as a target for one complete FGClite module. This means by definition, that the average failure of an installed FGClite module occurs after one million hours. It needs to be mentioned, that the MTTF is a statistical value of reliability prediction and cannot be fully adapted to real operation. For example, an MTTF of one million hours for just one module in operation would mean a lifetime of 114 years, which is far from reality. However it helps a lot for qualitative and reliable designing. Thus, in addition to the radiation related goal, another goal of ten controller-induced beam dumps due to electrical failures is also defined in dependence to the MTTF of one million hours. It is generated with the assumption that failures of the FGClite appear constant in a statistical manner during the whole lifetime. Simplified it can be calculated with the premise that within 114 years 1094 units fail. This makes 9.6 predicted beam dumps per year when dividing 1094 failures by 114 years. In order to explain, the MTTF is specified by accelerated lifetime tests of components performed by the component manufacturers after certain norms and regulations. It is calculated with this running time, sample size and failure data of the tests. In addition to this paragraph it also needs to be mentioned that often the Mean Time Between Failure (MTBF) including a possible repair of the component and its repair time is used. In order to simplify calculations the FGClite project uses the MTTF to set clear reliability requirements for the design process. An MTBF value can always be added to the existing MTTF prediction.

By once again coming back to the irradiation testing, this extensive testing is just needed with the necessity of using Commercial-Off-The-Shelf (COTS) components for the FGClite which leads to other requirements that are specific for the FGClite circumstances concerning the costs of the project. With 1094 units installed and the necessities of pre-series, prototypes, radiation testing and spares, 1600 units in total will be produced. Therefore the pure component,

manufacturing and burn-in testing costs are a big factor in the project budget, planned to be at maximum 3.5 million CHF. With this number of units and the relatively small budget it is not possible to design only with highly reliable components or only with radiation-hardened integrated circuits (IC). Also the short project timeframe of around four years and the restricted available manpower is not sufficient to design these customized radiation tolerant components for all the parts needed. Therefore the component selection needs to be decimated to mostly the above mentioned COTS components. In terms of radiation tolerance, the disadvantages of this necessity are in the beginning according to different components, often a lack of data concerning tests and documentation. And afterwards when it comes to radiation testing disadvantages are compromises in quality and also the fact that compromises in the configuration due to less availability may be accepted depending on the results. It is also needed to control each production lot of COTS components. Especially the lack of radiation related data is a big disadvantage, therefore it is necessary to test every COTS component that is suspected to perform different in a radiation environment to predict its performance under radiation. Thus components are pre-chosen regarding their functions, susceptibility to radiation, electrical performance and electrical reliability and then they are tested for their radiation tolerance to confirm the possible use in the radiation environment. An additional criteria to this is the availability of other COTS alternatives. A detailed description how the TE-EPC group of CERN is managing the validation, classification, selection and the testing of COTS components can be accessed under [9]. The main flowchart which illustrates how the execution of the validation process is defined is shown in the appendix. The Renesas SRAM, which is foreseen for a use in the FGClite is such a COTS component. The main part of this work deals with irradiation testing of the memory and therefore its performance under radiation and its radiation tolerance. The next chapter starts with describing the Renesas SRAM.

2 The Renesas SRAM for the FGClite project

The Renesas SRAM, see figure 3-7 (bottom, right), is a memory of the FGClite module. The following three subchapters describe its technology, its electrical as well as its radiation reliability, its function in the controller and previous irradiation tests that have been performed with the memory. Supplementary a small insertion is added in chapter 2.2 concerning a second SRAM that is used in the FGClite with a different purpose than the Renesas SRAM, however strongly related to the main subject of this work.

2.1 The technology of the Renesas SRAM and its electrical reliability

The «R1LV1616RSA-7SI#B0» of the Renesas Electronics Corporation [10, 11] is a 3.3 V low voltage, 16 Mbit static random access memory using 0.15 µm CMOS- and thin film transistor technologies. It can be either organized as 1 M word x 16-bit or 2 M word x 8-bit. Table 2-1 summarizes the product specifications.

Table 2-1 : Product specifications R1LV1616RSA-7SI#B0

Parameter	Value
Memory capacity	16 Mbit
Process technology	0.15 µm CMOS
Supply voltage range	2.7 – 3.6 V
Operating current	25 mA (40 mA max)
Stand-by current	2 µA
Access time	70 ns
Operating temperature	-40 – 85 °C
Transistors per cell	6
Number of pins	48
Dimensions (LxWxH)	18.4 x 12 x 1.2 mm
Mass	0.5 g
Package type	TSOP (Thin Small Outline Package)

An SRAM is a volatile memory exhibiting data remanence. The data gets stored without a need of refreshing it as long as a power supply is provided (compare figure 2-1). The low voltage SRAM of the Renesas Electronics Corporation realizes this with the technology of six transistors per cell. Figure 2-1 shows such a cell with two PMOS (1) and two NMOS transistors (2) to store the bit value and two other NMOS transistors on the most left and the most right to read and write the information via the wordline on top and the two bitlines left and right. Per definition such a transistor configuration is considered as CMOS-technology, however for this SRAM the two PMOS transistors are not integrated in the silicon substrate, as those implemented in the most other commercial CMOS SRAMs. Instead these two transistors are placed on top of the substrate. In addition to that a cell of the Renesas SRAM consists of two capacitors (3). These capacitors help to store the respective voltage according to the programming and create an «extremely high endurance against soft error[s]» after [12]. This

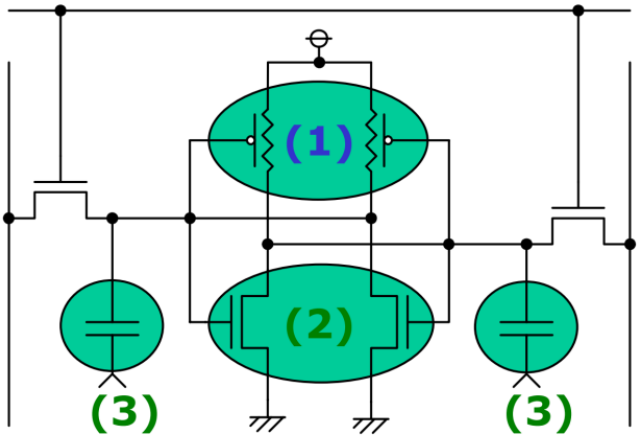


Figure 2-1 : Six transistor SRAM cell [12]

means, that an impact that normally causes a soft error by shifting charges is, in most cases, recuperated by the load of the respective capacitor. This fact has been a big factor when pre-choosing the Renesas SRAM as a COTS component with considering its probable radiation performance and qualification. Another even more important factor is the companies' designation «latch-up free» [12]. With the polysilicon thin film PMOS transistors stacked on top of the silicon substrate and therefore only the N-channel transistors in the substrate, it is ensured that no parasitic thyristor can be generated by a particle strike, what would cause an SEL.

For choosing the component the electrical reliability point of view is one of the things that need to be considered. The Renesas SRAM has a Failure In Time (FIT) value of 8.4 failures per 10^9 hours at a confidence level of 60 % and an operating temperature of 55 °C [13]. The FIT-value describes the average appearance of component failures per time, also designated as the Failure Rate. It is always given in failures per one billion device hours (fpbh) The FIT is the reciprocal value of the above mentioned MTTF. It is used to make reliability predictions of components, assemblies or whole systems. For predicting electronic systems, like here the FGClite, FIT-values are commonly calculated by performing accelerated life tests of the single components. These tests are performed in conditions above the normal specifications to make the component fail sooner than during normal operational conditions. With this test data the FIT-value can be calculated after certain standards, e.g. the Japanese JIS C5003, by mainly taking the number of tested devices and the test duration into account. The resulting FIT-value is always indicated for a predetermined operating temperature, like the 55 °C mentioned above, and a confidence level, which states that with a minimum probability of a certain percentage, like the 60 % of above, all measured FIT-data of the calculated confidence intervals are containing a true value. For a specific application these values can be adapted by using the so-called Arrhenius equation for the temperature- and the Chi-Square Distribution for the confidence level conversion.

In table 2-2 a minor market comparison for the electrical reliability is shown surveying the Renesas SRAM and four other potentially possible 16 Mbit or 18 Mbit SRAMs for the FGClite. Three of the components are asynchronous SRAMs and only the 18 Mbit device is a synchronous memory like the Renesas SRAM. Synchronous means in this context that the device is controlled synchronously to an external clock signal while asynchronous SRAMs are not using a clock, which limits the maximum data rate. Concerning the memory size, the requirement of the FGClite is a data storage with a minimum capacity of 10 Mbit. The FIT-values in the table are converted to the assumed maximum ambient temperature in the LHC

tunnel of 40 °C and the confidence level is converted to the higher value of 90 %, which is defined by default for all FGClite components. The prices in US-Dollar in the fourth column are from the online parts distributor Digi-Key Corporation [14], accessed in March 2015. For additional information the last row displays an 8 Mbit SRAM of the Cypress Semiconductor Corporation («Cypress SRAM» in the following) in context to the insertion in the next subchapter.

Table 2-2 : Comparison of possible SRAMs for the FGClite

Device	Manufacturer	FIT (fpbh)	Price ($)	Comments	Source
R1LV1616R	Renesas Electronics Corp.	12.7	15.95	- Synchronous	[13]
CY62168DV30LL-55BVI	Cypress Semiconductor Corp.	9.98	9.53	- Asynchronous	[15]
AS6C1616-55TIN	Alliance Memory Inc.	1.6	7.18	- Asynchronous	[16]
IDT71T75602	Integrated Device Technology	3.07	11.86	- Synchronous, 18 Mbit	[17]
SMV512K32-SP	Texas Instruments Incorp.	0.614	308.25	- Asynchronous - Not COTS (Rad-hardened)	[18]
CY62157EV30LL-45ZSXI	Cypress Semiconductor Corp.	8.45	9.90	- Asynchronous, 8 Mbit - see chapter 2.2	[19]

As it can be seen the FIT-values of the first four rows are within a small range and are likewise the prices when regarding for both the absolute target values of the FGClite. For the whole system the goal for the budget per unit is 1500 CHF and for the FIT-value of one controller it is 1000 fpbh, which is equal to the above mentioned MTTF value of 1 million hours. Therefore the FIT-value of the Renesas SRAM influences the envisaged MTTF of the FGClite with a weighting of 1.27 %. This is not much and acceptable by taking the function and complexity of the memory into account, however all the other SRAMS have a better value. The next fact that the Renesas SRAM is the most expensive out of the first four rows is most probably caused by the above described different and more complex technology that is implemented avoiding SELs. The second last row of the table shows the data of a special radiation-hardened device. When comparing to the other SRAMs, the extraordinary high price of this non-COTS component illustrates the design strategy of using primarily COTS components, in the first chapter described, by regarding the budget restrictions. The following two subchapters are further executing this reliability approach with also covering the radiation tolerance and availability in the special environment of the LHC.

2.2 The Renesas SRAM in the FGClite project

In the FGClite module, the Renesas SRAM is mounted on the so-called Communications Board (CB) plugged into the Main Board (MB), over which all backplane in- and outputs are directed. These two boards form together with four other boards the FGClite module when regarding the current status of development. In the LHC several of these modules will be connected to a field

bus where one power converter gateway computer is connected. At maximum 30 controllers are on one field bus. The sum of the gateway computers is connected via a network to the CERN Control Center (CCC). This allows the CCC to analyse the performance of the power converters and the FGClite itself to detect errors and to carry out actions.

On the CB the Renesas SRAM fulfils the function of storing operational data from the power converters generated over a Field Programmable Gate Array, the so-called Critical FPGA. This FPGA hasn't got the possibility and capacity to store this information wherefore an additional memory is needed. Therefore the stored information is transferred by the Critical FPGA into the SRAM, where it is kept and provided when the gateway needs and requests it. A second reason why the memory is needed is the fact that the communication bandwidth on the field bus between the FGClite, respectively the Critical FPGA and the gateway, is not sufficient enough to send the data permanently there. In figure 2-2 the reduced communication principle of the FGClite is shown by just displaying the communication which is relevant for the integration of the Renesas SRAM. One additional thing in the diagram is the integration of the Cypress SRAM which is communicating with the Auxiliary FPGA, see insertion below.

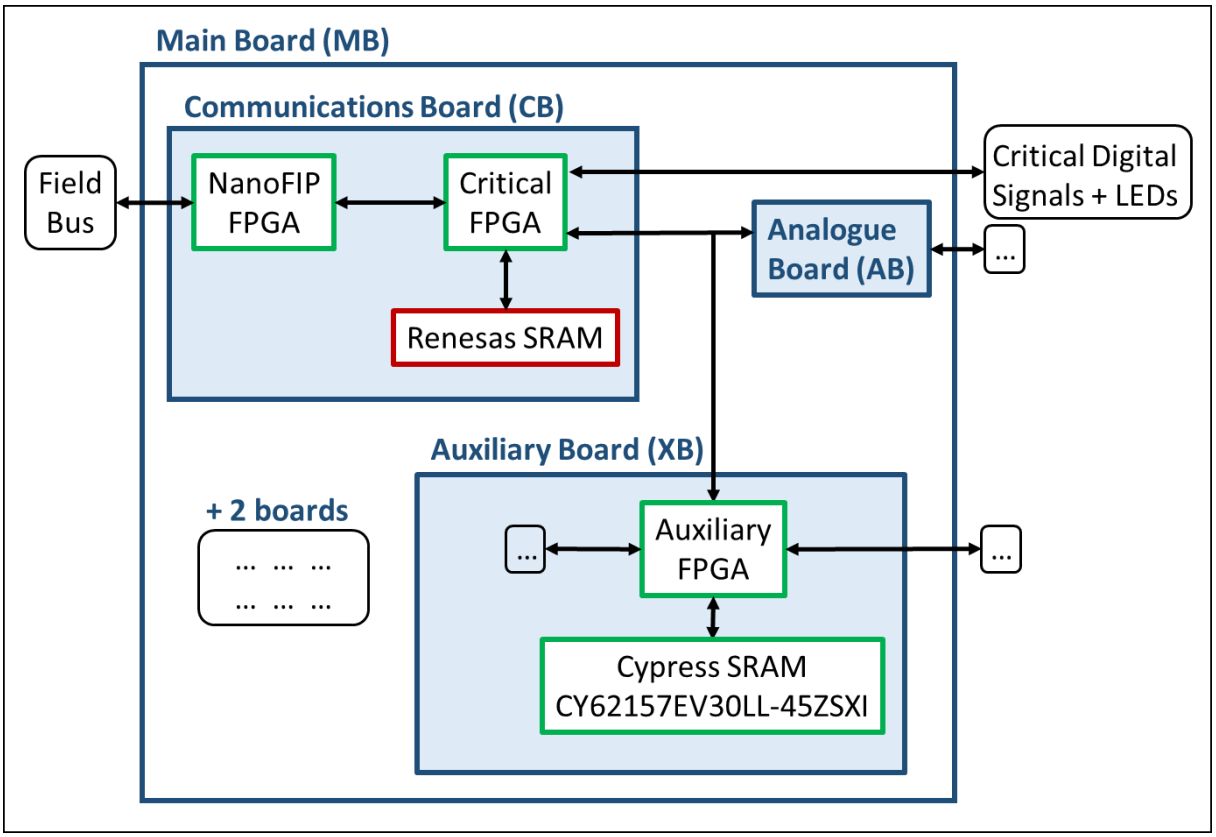


Figure 2-2 : Functional Implementation of the Renesas SRAM

By tying up to the reliability approach of the chapter above the Renesas SRAM has mostly been chosen due to radiation qualification reasons. When looking towards the year 2024 with the continually increase of the radiation levels in the LHC, and then in 2024 the upcoming high luminosity environment of the HL-LHC, radiation tolerance is, for semiconductor devices, of more importance than electrical reliability given that the electrical reliability of a single

component is within an acceptable range. Of course the electrical reliability becomes more and more important with an aging device, which might lead to prematurely replacements, nonetheless SEEs appear constantly from the time of first operation. Thus, the characteristic with only the NMOS transistors being placed in the substrate, making no SEL possible, has been really interesting. Another reason has been the availability of a radiation test report about two different irradiation test campaigns that have been performed in June and October of the year 2007 by the National Aeronautics and Space Administration (NASA) of the United States (US). The results have been published in 2008 during the IEEE Radiation Effects Data Workshop in Tucson (US) [20]. During one of these campaigns a very low occurrence of SEUs has been measured with proton beam energies up to 198 MeV. This confirms the designation of an «extremely high endurance against soft error[s]» [12]. A further description of these irradiation tests is following in the next subchapter. In the end, the two radiation qualifying facts concerning SELs and SEUs, together with the acceptable electrical reliability of the component, have been leading to the decision of considering the Renesas SRAM for a possible use in the FGClite project and to perform further tests with the memory.

The Cypress SRAM in the FGClite

The «CY6157EV30LL-45ZSXI» SRAM from the Cypress Semiconductor Corporation has been added to the FGClite design in the late development phase. Together with the Renesas SRAM these two memories are the only SRAMs which are used within the FGClite controller. In contrary to the Renesas SRAM, the Cypress SRAM has a relatively high cross section of 1.94E-13 cm^2 per bit [21] at a proton beam energy of 480 MeV. This is around 5000 times higher than the cross section of the Renesas SRAM (3.85E-17 cm^2/bit, see chapter 2.3.3) at this energy. For the specific use in the FGClite this high error rate has been chosen on purpose because with this sensitivity to radiation the Cypress SRAM functions as a radiation monitor device in the controller. With the connection to the Auxiliary FPGA it is possible to read out SEUs constantly and to access and analyse the error data over the gateway. In addition the Cypress SRAM is a well-known and tested device which is also used for the CERN «RadMon V6 HEH detector» [21]. Both this gives the opportunity to monitor the received radiation of each FGClite during the later operation and to predict the future radiation performance of the module, what also gives valuable data to predict and analyse the performance of the Renesas SRAM.

2.3 Previous irradiations of the Renesas SRAM

With the decision of most probably using the Renesas SRAM in the FGClite it has become necessary to generate irradiation test data to qualify it for its later operation. The data is needed to predict how it will perform and how many and which failures may appear and, of course, if it can actually fit the requirements and be used. Prior to the test that is presented later in this work, four irradiation campaigns have been performed with the SRAM, including the two by NASA. At first, the NASA test campaigns and their results are described and then two by CERN

performed campaigns at the Paul Scherrer Institute (PSI) in Villigen, Switzerland and at the Tri University Meson Facility (TRIUMF) in Vancouver, Canada are presented. In this part of the work it is not always explicitly described how the tests are set up and how they are performed. A detailed description for a similar test setup and execution follows for the CERN internal testing in the main part of this work in chapter 3. Furthermore the results of the three following proton beam tests are not presented explicitly in detail. Further details and the comprehensive analysis of these results also follows in chapter 3 for all the generated data.

2.3.1 Heavy ion tests and up to 198 MeV proton beam tests by NASA

The NASA heavy ion irradiation test of the Renesas SRAM has been performed in June 2007 at the Single Event Effects Test Facility (SEETF) of the Texas A&M University Cyclotron. Even though heavy ion radiation is not considered for the radiation requirements of the Renesas SRAM in the FGClite and the accelerator environment, the results are presented in this work. In fact cross section results of heavy ion irradiation can indicate a certain range where the proton cross section might be located.

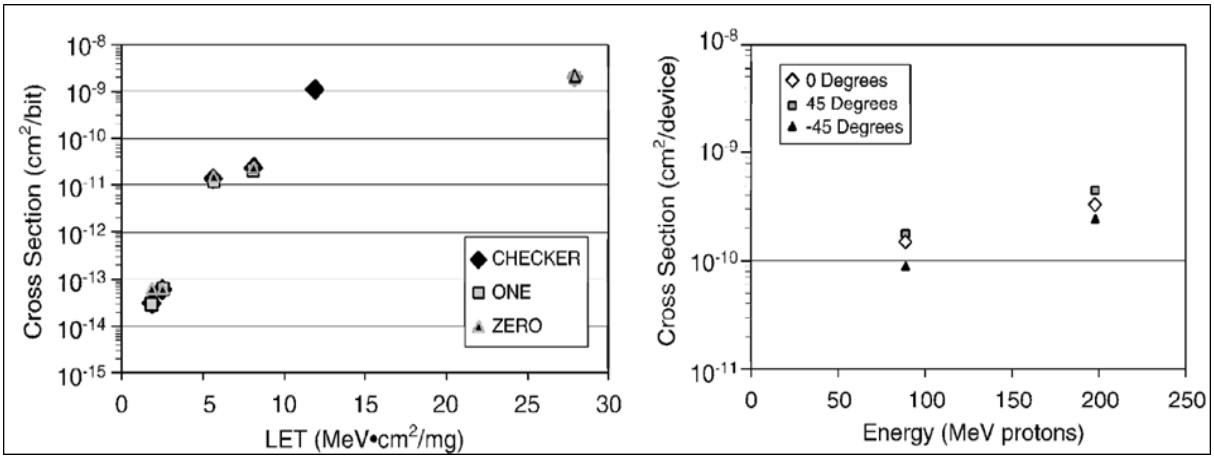


Figure 2-3 : Heavy ion beam- (left) and proton beam (right) SEE cross section results for NASA testing [20]

For heavy ion SEL-testing eight Devices Under Test (DUT) have been tested at a supply voltage of 3.3 V for SEU-testing and 3.6 V for SEL-testing. For SEL-testing no effect occurred up to the threshold LET_{th} of 55 MeV*cm^2/mg and a temperature of 74 °C. The used particle fluences have been up to 10^7 p/cm^2. That confirms the designation «latch-up free» for both high load and high energy particles, which are affecting semiconductor devices stronger than lighter particles, e.g. protons. The SEE cross section per bit for the heavy ion testing is displayed in the left diagram of figure 2-3 for six different LET levels. For each level three different test patterns have been written to the transistor cells of the memory: a complete static '0', a complete static '1' and a 'checkerboard' pattern. A «checkerboard» pattern means that the transistors in each row of the memory are written with the alternating values of a logical '1' and a logical '0'. As it can be seen, the different patterns don't have an effect on the test results, which is

noteworthy. To convert the values into the SEU cross section per device, the results must be divided by the factor 16 Mbit/device. Additionally there has been no SEFI during the heavy ion test up to the used LET_{th}.

The NASA proton beam tests have been taking place at the Indiana University Cyclotron Facility (IUCF) in Bloomington (US) in October 2007. A supply voltage of 3.3 V and also a sample size of eight DUTs has been used. The results are shown in the right hand diagram of figure 2-3 for the two different beam energies of 83 and 198 MeV with the SEU cross sections per 16 Mbit device scaled on the ordinate. At each energy always three irradiations have been performed with differing angles of 0, 45 and - 45° to the regular right angle position between the device's upper surface and the beam direction. Therefore the respective cross sections values are slightly, however not considerable different to each other. The resulting cross sections for the 0°-position used in the following documentation and analysis in chapter 3, are 9.0×10^{-18} cm^2/bit for the beam energy of 83 MeV and 2.0×10^{-17} cm^2/bit for 198 MeV. Also during this test no SEFI has been observed. One destructive event has occurred on one device at the dose of 40.5 krad (405 Gy).

2.3.2 Up to 230 MeV proton beam tests at PSI

The irradiation tests at the Proton Irradiation Facility (PIF) of the PSI have been performed in October 2013 by the TE-EPC-CCE section of CERN. The goal of the campaign and the later analysis has been to obtain SEUs and Multiple-Cell Upsets (MCU) at different energies up to the maximum of 230 MeV and compare the results with the proton beam test results from NASA. Here it needs to be distinguished between an SEU, where a particle strike is just causing one bit error in a single word and an MCU, where a single particle strike causes several bit upsets in at least two words, respectively two physical or logical lines. An analysis for Multiple-Bit Upsets (MBU) has not been done. A further execution of this follows in chapter 3.3.4. In addition the TID degradation has been measured by monitoring the power consumption of the memories during the test. The tests have been performed with several randomly preselected DUTs of a batch of 1536 Renesas SRAMs received at CERN. The remaining parts of the batch will be used for the further tests and the later FGClite production as well as prototype manufacturing. Just like during the NASA campaign the three test patterns 'all 0', 'all 1' and 'checkerboard' have been written to the memories. Eight DUT cards aligned in the beam line have been tested at once for the proton energies of 60, 100 and 230 MeV. The concerning beam fluxes have been 7.55×10^7, 1.02×10^8 and 1.73×10^8 p/cm^2*s. Table 2-3 shows the results of the irradiation with table 2-4 adding them up and summarizing them for the three different beam energies. A little misleading in the tables is the fact that the columns counting the SEUs only count single bit-flips caused by one particle strike. It is better to refer to them as Single Bit Upsets (SBU), see chapter 3.3.4. In contrary to this, the columns counting the total SEUs take single upsets as well as the concerning number of MCU upsets into account.

Table 2-3 : Test results for the proton beam tests at PSI (Oct, 2013) [22]

Run	Energy (MeV)	#DUT	SEU	MCU (2)	MCU (3)	MCU (4)	MCU (5)	…
2	230	7	0	0	0	0	0	…
3	230	7	6	2	0	0	0	…
4	230	7	82	18	5	2	0	…
5	230	7	87	28	0	0	0	…
6	230	7	95	25	3	0	2	…
7	230	7	94	17	1	1	0	…
8	100	7	19	1	1	0	0	…
9	100	7	146	8	2	0	0	…
10	100	6	29	1	0	0	0	…
11	60	6	4	0	0	0	0	…
12	60	6	9	0	0	0	0	…

…	Total SEU	Fluence (/cm2)	#Bits (/dev)	XS (cm2/bit)	XS 90% UL (cm2/bit)	XS 90% LL (cm2/bit)
…	0	1.00E+10	1.68E+07		1.96E-18	
…	10	1.00E+10	1.68E+07	8.51E-18	1.44E-17	5.25E-18
…	141	1.00E+11	1.68E+07	1.20E-17	1.38E-17	1.05E-17
…	143	1.00E+11	1.68E+07	1.22E-17	1.40E-17	1.06E-17
…	164	1.00E+11	1.68E+07	1.40E-17	1.59E-17	1.23E-17
…	135	1.00E+11	1.68E+07	1.15E-17	1.33E-17	1.00E-17
…	24	1.00E+11	1.68E+07	2.04E-18	2.87E-18	1.48E-18
…	168	2.11E+11	1.68E+07	TID failure		
…	31	1.00E+11	1.68E+07	3.08E-18	4.16E-18	2.31E-18
…	4	1.00E+11	1.68E+07	3.97E-19	9.09E-19	1.96E-19
…	9	1.00E+11	1.68E+07	8.94E-19	1.56E-18	5.39E-19

Table 2-4 : Summarized test results of table 2-3 [22]

Energy (MeV)	#DUT	SEU	MCU (2)	MCU (3)	MCU (4)	MCU (5)	…
60	6	13	0	0	0	0	…
100	6.5	48	2	1	0	0	…
230	7	364	90	9	3	2	…

…	Total SEU	Fluence (/cm2)	#Bits (/dev)	XS (cm2/bit)	XS 90% UL (cm2/bit)	XS 90% LL (cm2/bit)	SEU ratio in XS
…	13	2.00E+11	1.68E+07	6.46E-19	1.03E-18	4.20E-19	100.00%
…	55	2.00E+11	1.68E+07	2.52E-18	3.16E-18	2.03E-18	87.27%
…	593	4.20E+11	1.68E+07	1.20E-17	1.29E-17	1.12E-17	61.38%

Unfortunately one DUT has failed in Run 1, which could have been due to an issue in the powering circuit. This has affected the test data and therefore the upper table starts with run 2 and with only seven DUTs running the tests. During the 9th run three out of seven DUTs have been failing due to reaching the TID limit between an absorbed dose of 480 and 670 Gy. A second set of seven DUT cards has been used for the further test, where again one card has not been functional, wherefore only six DUTs have been finishing these second runs. The columns of the tables which are counting the appearance of different MCUs are displaying the number of affected cells in brackets. They have been read out by analysing the addresses of the errors and writing down errors which occur on the same position in at least two logical lines, which

means within at least two written words. It needs to be added, that there is the possibility that by using this methodology some MCUs might have appeared as two or even several SEUs which incidentally changed the bit-values of two or more bits physically adjacent within two or more lines. But by taking the amount of occurred errors and the total number of 16777216 bits (2^{24}) in the memory, the probability for this is far below a percentage of 0.0001 % and can be excluded by demonstrating a high probability. One much bigger point to consider is that with this methodology MCUs are only counted when they appear in the written address lines in the respective writing direction or, in other words, in the logical implementation. When they appear in other physical directions without having any logical correspondence to this, they cannot be detected with this methodology. Concerning this, the Renesas Electronics Corporation unfortunately does not provide any data about the correspondence between the logical and physical memory organization. For this reason the counting of MCUs during this test campaign must only be considered as an attempt without using the data for an analysis. The last three columns of table 2-3 and 2-4 calculate the error bars for the measured SEU cross section with the 90 % upper and lower limits of it, by using the Chi-Square-Distribution. The measured cross sections by PSI for the three different beam energies are between 6.46×10^{-19} and 1.2×10^{-17} cm^2/bit, however according to these results it needs to be added that an ESA SEU Monitor has been used to measure and calibrate the cross sections for the different proton beam energies and to compare the results with the data that has been provided by the PSI measurement system. The results of the ESA SEU Monitor have not always, especially at lower energies, been consonant with the PSI data, wherefore three correction factors (Table 2-5) have been used for each energy. The corrected values of 1.2×10^{-18}, 4.21×10^{-18} and 1.21×10^{-17} cm^2/bit for 60, 100 and 230 MeV are used for the further documentation and analysis. The reason for these big corrections has most probably been a small offset in the alignment of the PSI measurement system. Further documentation about the ESA SEU Monitor and the measurement can be found in the appendix. For the TID degradation no significant increase of the power consumption has been measured.

Table 2-5 : Corrected XS (PSI)

Energy (MeV)	Correction Factor	Corrected Cross Section (cm^2/bit)
60	1.86	1.20×10^{-18}
100	1.67	4.21×10^{-18}
230	1.01	1.21×10^{-17}

2.3.3 Up to 480 MeV proton beam tests at TRIUMF

The proton beam tests of the Renesas SRAM at the TRIUMF facility of Canada's national laboratory for particle and nuclear physics have been performed in December 2013 by the TE-EPC-CCE section and the EN-STI group of CERN. The test setup and the measurements have been the same to the above described tests at PSI. As only differences just three DUT boards have been performing the tests at once at the provided beam energies of 230, 355 and 480 MeV and the power consumption for TID degradation has not been measured during the campaign. Also no MCU-analysis has been performed. In total six DUTs have been used. Table 2-6 shows the results and circumstances of the irradiations.

Table 2-6 : Test results for the proton beam tests at TRIUMF (Dec, 2013)

Run	#DUT	Sum #DUT	Pattern	Energy (MeV)	#SEU	Fluence (p/cm²)	Dose (Gy)	XS (cm²/bit)	Corrected XS (cm²/bit)	Comments
1	1,2,3	3	Chkbrd	480	139	8.37E+10	30.5	3.30E-17	3.79E-17	
2	1,2,3	3	Chkbrd	480	175	8.36E+10	30.5	4.16E-17	4.78E-17	
3	1,2,3	3	Chkbrd	480	132	8.36E+10	30.5	3.14E-17	3.61E-17	
4	1,2,3	3	All'0'	480	165	8.36E+10	30.5	3.92E-17	4.51E-17	
5	1,2,3	3	All'0'	480	142	8.36E+10	30.5	3.37E-17	3.88E-17	
6	1,2,3	3	All'1'	480	116	8.37E+10	30.5	2.75E-17	3.17E-17	
7	1,2,3	3	All'1'	480	118	8.36E+10	30.5	2.80E-17	3.23E-17	
(8')	1,2,3	3	All'1'	~~355~~	~~17~~	1.30E+10	7	~~2.60E-17~~	~~2.99E-17~~	20% run
(8'')	1,2,3	3	All'1'	~~355~~	~~36~~	3.25E+10	17.5	~~2.20E-17~~	~~2.53E-17~~	50% run
8	1,2,3	3	All'1'	355	91	6.44E+10	34.7	2.81E-17	3.23E-17	
(9')	1,2,4	3	Chkbrd	~~355~~	~~29~~	3.25E+10	17.5	~~1.77E-17~~	~~2.04E-17~~	50% run
9	1,2,3	3	Chkbrd	355	60	6.44E+10	34.7	1.85E-17	2.13E-17	
10	1,2,3	2	Chkbrd	230	35	1.21E+11	64.6	8.62E-18	9.91E-18	Acc. Dose 324.9 Gy
DUT1 TID failure										
11	2,3,4	1	Chkbrd	230	33	1.21E+11	64.5	1.63E-17	1.87E-17	Acc. Dose 389.5 Gy
DUT2/DUT3 TID failure										
12	4,5,6	3	Chkbrd	230	46	8.07E+10	43.1	1.13E-17	1.3E-17	Acc. Dose 454 Gy
13	4,6	2	All'0'	230	41	8.07E+10	43.1	1.51E-17	1.74E-17	
14	4,6	2	All'1'	230	21	8.06E+10	43	7.76E-18	8.93E-18	
					1396					
*Bits/DUT=16777216; XS Correction Factor = 1.15										

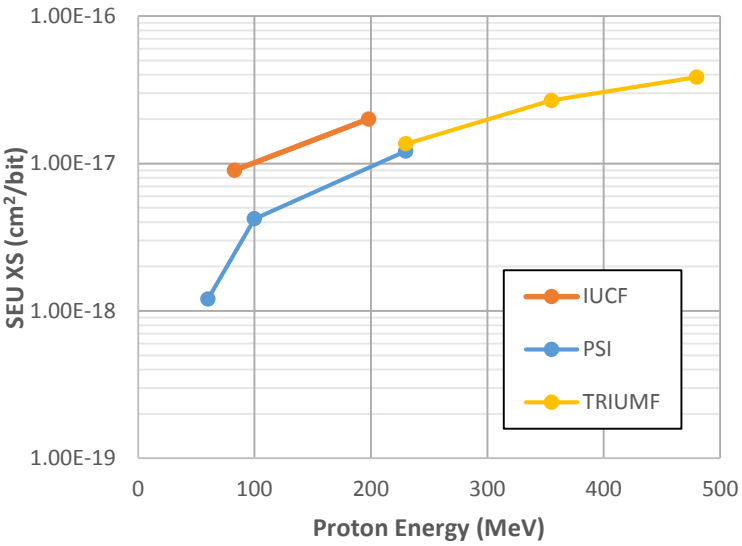
During 14 main tests at the energies of 230, 355 and 480 MeV plus three additional irradiations at 20 and 50 % of the concerning energy 1396 SEUs have been observed in total. By taking the number of SEUs together with the respective fluences and the number of bits of the devices the measured SEU cross sections are calculated in the ninth column of the table. The tenth column shows again corrected cross sections by multiplying the measured cross section value with the factor of 1.15, because during the TRIUMF tests the ESA SEU monitor has also been used and has been showing deviations to the PSI data at the beam energy of 230 MeV. By comparing the monitor results of the two campaigns at this energy the absolute SEU cross section at TRIUMF is around 15 % lower than the one at PSI. Therefore the factor is applied to all test results at the different energies, making the results consistent to each other for the later analysis. Table 2-7 is showing the average cross sections for the different energies with the corrected numbers of 1.36×10^{-17}, 2.68×10^{-17} and 3.85×10^{-17} cm²/bit for 230, 355 and 480 MeV. Here it needs to be added, that three runs at 355 MeV are not taken into account, because they have been performed at either 20 or 50 % of the fluence. For the total dose calculation they are of course considered, where the first three DUTs have been failing between accumulated doses of 324.9 and 454 Gy due to TID.

Table 2-7 : Average XS (TRIUMF)

Energy (MeV)	XS (cm²/bit)	Corrected XS (cm²/bit)
480	3.35E-17	3.85E-17
355	2.33E-17	2.68E-17
230	1.18E-17	1.36E-17

2.3.4 Summary of the previous proton irradiations

With three different test campaigns for proton beam irradiation at seven different energies by CERN and NASA a lot of data has been generated within a wide beam energy range. This chapter shortly summarizes this data of these previous irradiations to lead to the main part of this work in the following. Also here it needs to be mentioned again that a more detailed elaboration and analysis is described together with the irradiation campaign in the next chapter wherefore the data is mostly just presented and pre-analysed in this part.



Facility	Energy (MeV)	Cross Section (cm^2/bit)
IUCF	83	9.00E-18
	198	2.00E-17
PSI	60	1.20E-18
	100	4.21E-18
	230	1.21E-17
TRIUMF	230	1.36E-17
	355	2.68E-17
	480	3.85E-17

Figure 2-4 : Summarized XS results for the IUCF, PSI and TRIUMF tests

As it can be seen in figure 2-4, the results are presented for each campaign in the diagram with the SEU cross section on a logarithmic ordinate and the beam energy on the abscissa. The data of the three campaigns is very consistent to each other with a slight deviation of the IUCF values. It can be seen that the SEU cross section is increasing with higher energies. On top, even the slope of a graph, which is using the points, increases constantly for these higher energies. For better displaying this circumstance the following figure 2-5 uses trendlines and additionally the diagram is shown again in the appendix using two linear scales. Due to this fact of a still increasing slope an expected saturation of the SEU cross section over the proton energy, further explained in the following chapter, cannot be generated yet using an extrapolation. Figure 2-5 displays the trendline for the data points in black which has been generated using the automatic function of Microsoft Excel. The additional green dashed line only takes the CERN tests at PSI and TRIUMF into account. The still present slope for the extrapolation of the lines is also illustrating that a saturation (compare chapter 3.1) is not yet reached at the maximum tested energy of 480 MeV with the SEU cross section of 3.85×10^{-17} cm^2/bit. The green trendline relativizes the deviation of the IUCF data to the CERN measurements, however it does not create significantly differences to the black trendline at higher energies. The deviation of the IUCF data can be explained with two different approaches, although the effect in relation to the FGClite test result needs is negligible, because it appears

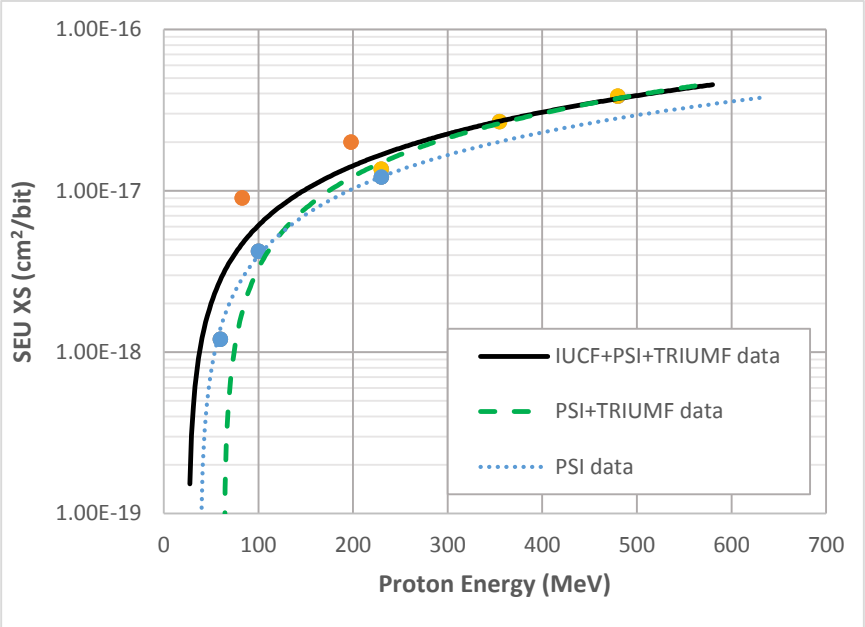


Figure 2-5 : Trendlines associated with figure 2-4

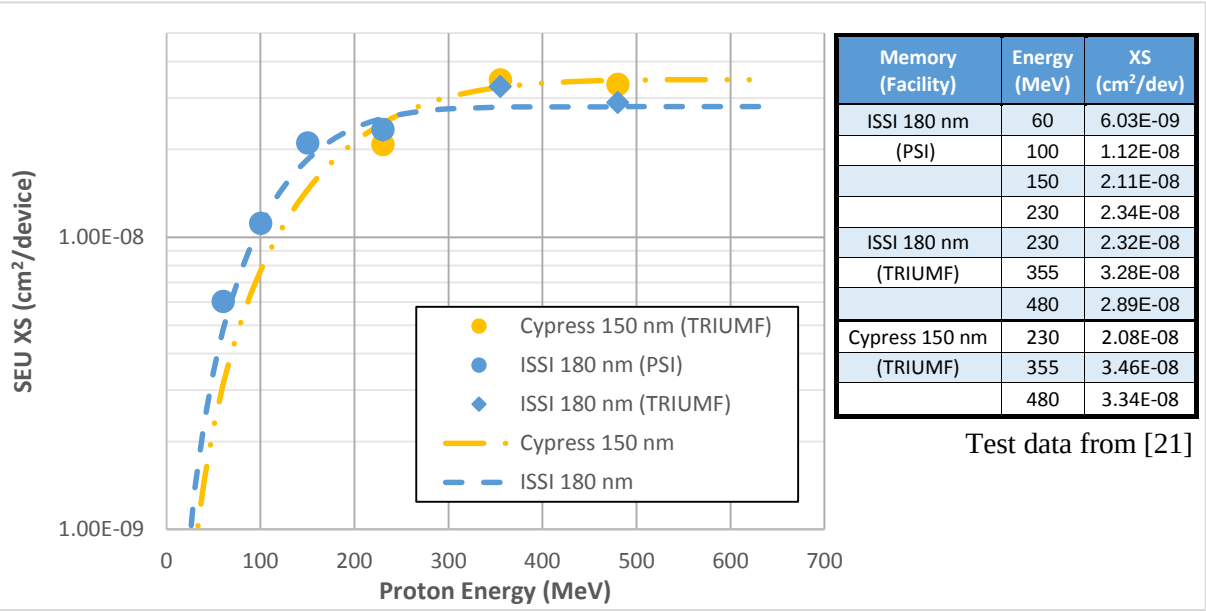
at lower energies and also the PSI and TRIUMF data are proving a different curve progression with their consistency. The first, most likely, reason could be the fact, that the irradiations have been taking place in 2007, six years prior to the other two campaigns. Due to possible changes in the technology or manufacturing process of the components, e.g. different silicon wafers, this deviation would not be surprising. Unfortunately the Renesas Electronics Corporation is not providing data about that, assumed that there has been at least one change. The minor second reason could maybe be a systematic offset in the measurement of the fluence at IUCF. Even though this has happened during the PSI measurement it should be unlikely that it happened to the NASA testing. Also a failure in the ESA SEU monitor measurement for the PSI- and TRIUMF campaigns is very unlikely. Previous results of the monitor are very consistent.

3 Irradiation testing at CHARM and data analysis

This main part of the work describes an irradiation test campaign of the Renesas SRAM which has been executed on the 6th and the 17th and 18th of November 2014 at the Cern High energy AcceleRator Mixed field facility, short CHARM [23]. This chapter starts with a short introduction of why the test is needed, then describes the new CHARM facility, following then with the test setup and its implementation and afterwards the execution of the irradiation campaign. It finishes with presenting the results of the test and analysing the data containing the results of the above described previous irradiations.

3.1 Needs for testing at higher energies

The presented fact that the SEU cross section of the Renesas SRAM is not saturating at the prior tested higher beam energies up to 480 MeV leads to the question of how the cross section behaves at even higher energies. In the environment of the LHC this can be up to several tens of GeVs. By comparing the Renesas memory to other commercial SRAMs it is conspicuous that some other memories show a cross section saturation at a certain energy. Two examples that saturate below an energy of 480 MeV have been tested at PSI and/or TRIUMF and are displayed in figure 3-1.



Memory (Facility)	Energy (MeV)	XS (cm²/dev)
ISSI 180 nm	60	6.03E-09
(PSI)	100	1.12E-08
	150	2.11E-08
	230	2.34E-08
ISSI 180 nm	230	2.32E-08
(TRIUMF)	355	3.28E-08
	480	2.89E-08
Cypress 150 nm	230	2.08E-08
(TRIUMF)	355	3.46E-08
	480	3.34E-08

Test data from [21]

Figure 3-1 : XS saturation of the Cypress 150 nm and the ISSI 180 nm SRAMs

The cross sections of the 16 Mbit «CY7C1069AV33» SRAM from the Cypress Semiconductor Corporation and the 4 Mbit «IS61LV5128AL» SRAM from Integrated Silicon Solution Incorporated (ISSI) saturate at 3.47 x 10^{-8} respectively 2.80 x 10^{-8} cm^2 per device. This results into the cross sections per bit of 2.07×10^{-15} cm^2/bit for the 16 Mbit device and 6.68×10^{-15} cm^2/bit for the 4 Mbit device.

However there are also the «K6R4016V1D» from Samsung and the «AS7C34098A» from Alliance Memory Incorporated SRAMs that have been tested which are not saturating up to an energy of 480 MeV, compare test data in [21]. In addition to this it is unique for the Renesas SRAM that an extrapolation of the PSI test data at lower energies shows a lower curve than the extrapolation for all the test data which reflects the above mentioned increase of the slope. This is the opposite for any other out of three SRAMs tested during a campaign at TRIUMF in December 2013 [21], where data from PSI has been available. The PSI extrapolation for the Renesas SRAM is displayed with the blue pointed line in figure 2-5. Associated to the above mentioned increasing slope, the curve is extraordinary because it shows with the green line having higher cross section values than the blue line, that the relative increase of the cross section is even higher for the higher energies at TRIUMF. Again, this does not yet indicate that it soon leads to a saturation. Two effects can explain this increase at the higher energies. The first and most probable reason can be the presence of 58 % tungsten in the M1 metal layer and tungsten silicide in the active region as well as tungsten in certain via-connections of the memory. Figure 3-2 is showing the transverse section of the different regions and layers of the Renesas SRAM. It is known that tungsten and other high-Z materials can increase the SEU cross section at energies above 100 MeV up to GeV-energies, when a proton starting from this certain energy hits these heavy ions, wherefore the ion can cause an SEU. A saturation value for this effect should be reached at an energy of 3 GeV according to FLUKA Monte Carlo («FLUKA» in the following) simulations [24, 25]. The other reason can probably be a higher contribution of MCUs, because the probability of affecting more than one cell increases when the particles are at higher energies. This higher probability of an MCU appearance at the higher energies increases the SEU cross section, because an MCU is caused by a single particle strike but affects several words, wherefore, several SEUs could have been counted for the TRIUMF results. The crossing point of the green and the blue trendline at a proton energy of around 130 MeV can be interpreted as the point where the additional increase of the slope, and therefore most probably, the tungsten contribution to the increase of the cross section starts the latest.

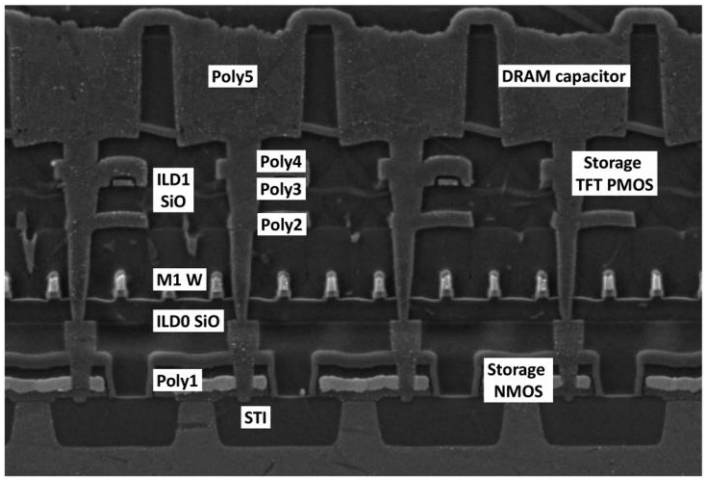


Figure 3-2 : Renesas SRAM cross section through metallization and active layers [24]

This all leads to the necessity of testing at higher energies to accurately predict the behaving of the SEU cross section for the Renesas SRAM and the FGClite during the LHC operation. A facility to test with a proton beam at higher energies has been and is not available outside of CERN, with the TRIUMF facility providing the highest beam energy apart from CERN facilities with its' energy of 480 MeV. But also at CERN there have been difficulties and restrictions for testing at existing facilities in the GeV-range. Therefore the new designed CHARM facility started its operation in the autumn of 2014 providing most of the unfulfilled needs.

3.2 The CHARM facility

CHARM [23] is an irradiation testing facility for various environments in the East Area of CERN's Meyrin site. It is designed by the CERN project «Radiation to Electronics» (R2E) and has started its operation in the autumn of 2014 with the purpose of performing irradiation tests for electronic components and equipment which is situated in a radiated environment, e.g. in space or in an accelerator environment. The following two subchapters first describe the facility itself and then how testing can be performed at CHARM.

3.2.1 Planning and technical description

The planning of the CHARM facility began in 2007 with the aim of providing a high-energy irradiation testing facility. The further aims have been a slow extraction of the beam and to fulfil demands for an adjustable radiation environment, a wide spectrum of this and to provide enough space to test larger systems in a mixed-field, like for example testing the whole FGClite module or even the module plus the concerning power converter. Here, slow extraction means that the particle beam is slowly extracted within many thousands of turns within the PS. At each turn just a small amount of the beam is extracted. A mixed-field means that the environment in the radiation chamber consists of mixed particles which are at mixed energies.

With the maximum beam energy of 24 GeV, CHARM is one of CERN's irradiation test facilities in the GeV-range. Its purpose is also to replace some testing at the existing H4IRRAD facility, located at an extraction line of the SPS accelerator, and to especially compensate disadvantages of it. CERN is the only place around the world to provide proton irradiations in this GeV-energy region. Table 3-1 displays a selection of proton beam irradiation test facilities all around the world and illustrates the beam energy differences of these facilities. For example the 24 GeV of CHARM are exactly 50 times higher than the 480 MeV of the TRIUMF facility in Vancouver, Canada. Thus advantages of CHARM in contrast to lower energy facilities are the simulations of representative accelerator environments, especially LHC environments, high intensities, high-energy radiation fields and particularly reduced testing time due to the accelerated testing.

Table 3-1 : Comparison of existing proton irradiation facilities

Facility	Maximum Beam Energy (MeV/c)	Location	Characteristics/Comments	Reference
H4IRRAD	400 000	CERN	- Also mixed-field	[26]
CNRAD (Neutrons)	400 000	CERN	- Neutron-induced mixed-field - No longer in operation	
CHARM	24 000	CERN	- Also mixed-field	[23]
IRRAD	24 000	CERN	- In the same complex than CHARM	[27]
TRIUMF	480	Vancouver, Canada		[28]
PIF	230	Zurich, Switzerland		[29]
IUCF	205	Bloomington, Indiana, USA		[30]
PAULA	180	Uppsala, Sweden		[31]
RADEF	55	Jyväskylä, Finland		[32]
KAZ	23	Karlsruhe, Germany		[33]
…	…	…	…	…

With being meant as a sort of replacement of CERN's H4IRRAD and also the CNRAD facility, while CNRAD already stopped its operation, CHARM has a lot of advantages compared to these higher energy facilities, such as a larger irradiation chamber as indicated above. This also differentiates it from the IRRAD facility which is located in the same complex than CHARM on the same extraction line of the PS. Four other advantages to the H4IRRAD facility are a lower activation level of the area, respectively a lower residual radiation dose due to the lower energy, a higher beam availability and a much easier access to the equipment. The higher beam availability results from the extraction of the PS- instead of the SPS accelerator, where the beam is simply not so limited than for the SPS. The easier access results on one hand from the lower doses and, therefore, less needed time for the irradiation chamber to recover to acceptable radiation values with additionally an electric shuttle system that drives the devices out of the high radiated area, and on the other hand, from an independent access to the area where there is no need to stop the PS operation. By summarizing all the above presented table 3-2 shows the relevant technical parameters of the CHARM facility. The maximum beam energy is unfortunately also the minimum beam energy for an in-beam position and in theory the number of different test position is infinite. For the measuring of the beam profile a Multi-Wire Proportional Chamber (MWPC) is installed. Its functionality is described in chapter 3.4.2.

Table 3-2 : CHARM - Technical parameters

Parameter	Value
Proton beam momentum	24 GeV/c
Maximum number of protons per second	$6.7*10^{10}$
Number of shielding configurations	8 (15)
Number of test positions	28 defined + 1 in beam
Minimum spot size	5 x 5 mm
Beam availability	Max. 200 days/year
Beam profile measurement	Yes (MWPC)

3.2.2 Infrastructure and testing

In figure 3-3 the layout of the CHARM facility is displayed. By getting the proton beam of a slow PS extraction, the beam leads into the CHARM irradiation chamber where it can directly irradiate a DUT that is mounted in a test box on the so-called Montrack Shuttle. The shuttle creates, together with cable rails on the ceiling, the possibility to drive the connected DUT into and out of the direct irradiation chamber to a low radiation zone. There the different DUTs can be mounted and dismounted. It is also possible to align them into the later beam position by using reference points and a laser alignment. Over the rails several moveable and extendable cable-loops with different lengths can be connected to a patch panel in the low radiation zone. This ensures the power supply of the DUT and the signal transmission with the test equipment. The connections on the patch panel lead over 15 m long cables to another same patch panel in the non-radiated test control room, where the test equipment can be installed and the irradiation can be executed and controlled. It is also possible to observe the irradiation zone over several cameras and to control the shuttle. For mixed-field tests CHARM has a moveable target and four moveable and adjustable shielding walls. The target, either a copper or an aluminium cylinder, creates the mixed field by interacting with the proton beam. The copper or the aluminium interact differently with the protons giving the opportunity to create different fields. Another adjustment can be achieved with the availability of cylinders with holes to reduce the surface in the beam and therefore the interaction. With two shielding walls made of concrete and two other made of iron, the opportunity to modulate the field in a calibrated way is given. In the mixed-field, the DUT can then be placed in any position on the shuttle rail, where the field has different intensities. Bigger and heavier equipment can of course be placed in any position in the chamber. This all allows to simulate the different locations in the mixed field in and around the LHC tunnel. It is possible to simulate the received dose of a whole year of LHC operation within only a few days. Because the CHARM facility will also be high frequented and the human access to the irradiation chamber should be minimized to the least possible, CHARM also has a normal control room. Its purpose is to perform dry runs with the later test equipment to exclude possible failures and delays in the later irradiation testing. Therefore the control room has two exact same patch panels like in the real installation, connected with also 15 m long cables. With providing additional cables to simulate the cables on the ceiling, a dry run under the exact same conditions is possible, when excluding the radiation environment of course. It can especially be tested if the signal transmission and powering works over this long cable lengths. For the later described Renesas SRAM test the cable length between the DUT and the first patch panel has been 24 m with two 12 m cables.

For the CHARM facility the irradiations for the FGClite project are the first executed tests and also have high priority due to the time pressure of the project. They are scheduled over a planned time period between November 2014 and July 2015 with the test of the whole module in the autumn of 2015. As additional information, at this point it is most likely that there will be small delays in the development process and thus, the testing will be probably a little delayed. The test of the Renesas SRAM in November 2014, which is described in the next subchapters, has been together with a test of an Analogue to Digital Converter (ADC) and a test of several

SRAMs in the peripheral area of the beam, the first component test at CHARM. The test has additionally been used to commission the facility in a lot of ways on one hand and on the other hand to commission for the further FGClite tests of other components. Because the Renesas SRAM is a well-known and tested device it thereby serves as a more or less calibration device for the following component tests.

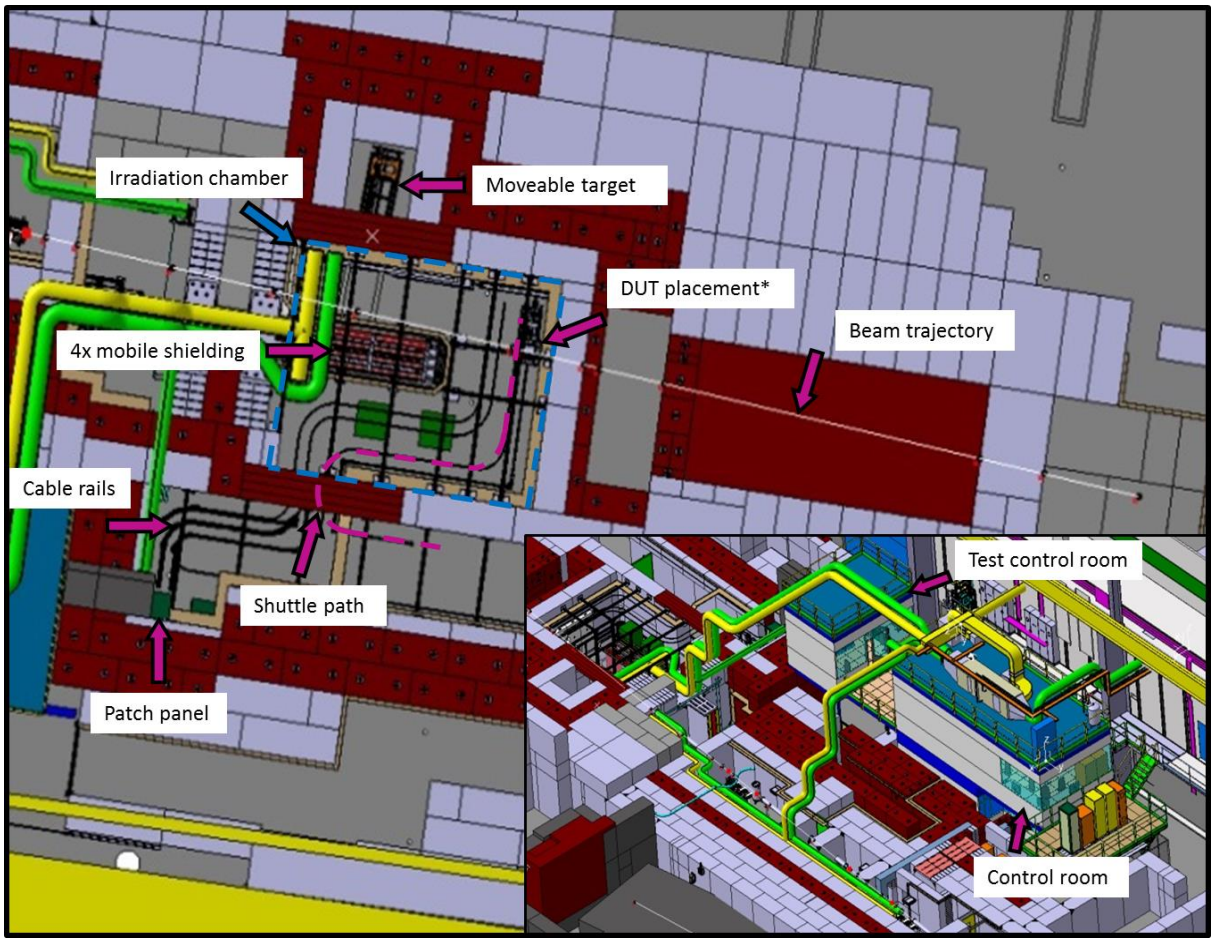


Figure 3-3 : CHARM Layout (drawings from [23])

3.3 Hardware test setup and strategy

The hardware test setup which is used for the Renesas SRAM testing is arranged to power the memory, to expose it to irradiation and to detect and document errors. For the setup, three PCBs have been developed and are described in the next subchapters. The hard- and firmware of the boards has been developed by the following persons of the TE-EPC-CCE section.

Table 3-3 : Hard- and firmware developers of the Renesas SRAM test setup

Board	Hardware - Developer	Firmware - Developer
DUT	Benjamin Todd	Andrea Vilar Villanueva
TCC	Karol Motala	Benjamin Todd and Andrea Vilar Villanueva
NCC	Slawosz Uznanski	

The following subchapters describe how everything is set up and installed and how the error detection is implemented and read out.

3.3.1 Test setup

The test setup for the CHARM irradiation has already been designed for previous irradiation campaigns of different components and DUT cards. A universal hardware setup for different and various testing has been used and then modified and extended. Therefore the setup has already been utilised during the PSI and TRIUMF campaigns and at CHARM it is just slightly adapted. In this CHARM configuration it is composed of three electronic boards, one laptop, two power supply units (PSU), the cabling and an additional device to measure the radiation dose. The boards have been designed and assembled at CERN and manufactured by an external company. The simplified block diagram in figure 3-4 overviews the setup and the connection of the individual components. Figure 3-5 specifies this by showing more detailed the connection between the different boards and devices. Also figure 3-6 in the next subchapter later explains how the communication principle is executed.

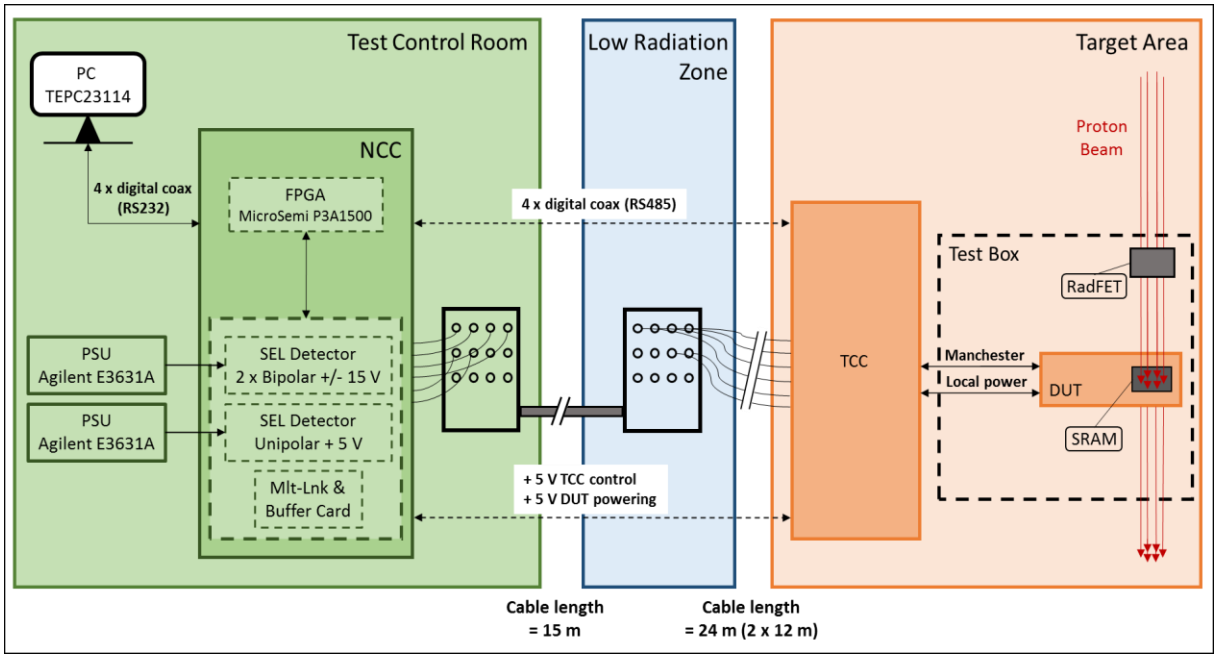


Figure 3-4 : Simplified block diagram of the test setup for the CHARM irradiation test

The DUT card on the right, where the Renesas SRAM is mounted, is fixed and aligned in the test box where it can be exposed to the proton beam. In the target area, or alternatively the high radiation zone, the DUT board gets connected to the Test Control Card (TCC) which powers the board with a voltage of + 5 V and communicates with it to read out the generated radiation-induced events of the DUT FPGA. With the configuration of the TCC up to eight DUT boards can be plugged in at once and exposed to the beam in a straight alignment. The TCC is then connected to the first patch panel in the low radiated zone behind the shielding walls. From there the connection leads over the other patch panel to the test control room and

connects the New Control Card (NCC) from there. With the connection to two PSUs the NCC receives two times the voltage of + 5 V. These two power lines get transferred to the TCC, where one line is for the TCC itself and the other for the powering of the DUT board. In this test setup for the Renesas SRAM, the functional part of the NCC with the latch up detectors has been used just to transfer the power to the TCC, because no SEL measurement has been performed. This has been the same during the tests at PSI and TRIUMF because the appearance of an SEL has been excluded prior to the tests. Concerning the further data transmission the NCC connects to a laptop PC in the test control room to transmit the error data of the TCC to the PC. The software on this laptop, called «Docklight», reads out and saves this data for the later analysis in a text document file. After each reading out the Renesas SRAM also gets rewritten to the required values from there by using the communication chain in the opposite direction. The other block diagram in figure 3-5 shows more detailed the serial communication between the PC and the NCC FPGA after the RS232- and from there to the TCC FPGA after the RS485 standard, where four lemo cables are connected between the two boards. Between the TCC and the DUT 12-pin straight connectors, that can either be plugged or connected over short cables, are used. The next subchapter describes this communication principle and the later installation is described in chapter 3.4.1.

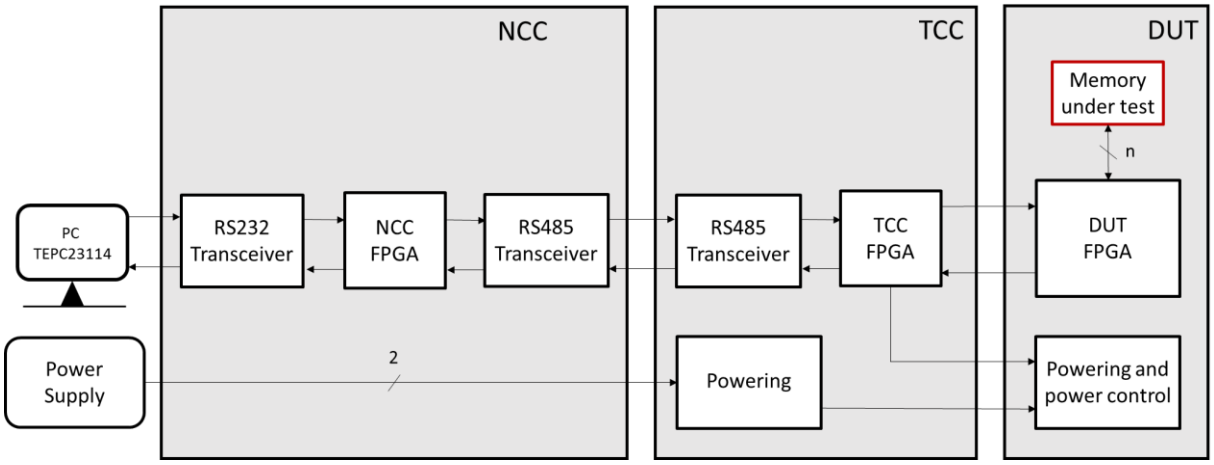


Figure 3-5 : Principle elements of the test apparatus

For the measurement of the dose a so-called Radiation sensing Field-Effect Transistor (RadFET) dose sensor is foreseen. It gets installed in front of the DUT upstream the beam. A description of this device follows in chapter 3.3.4.

3.3.2 Communication principle

The communication chain between the DUT, with the Renesas SRAM mounted, and the laptop PC to store the test data is illustrated in the simplified block diagram in figure 3-6.

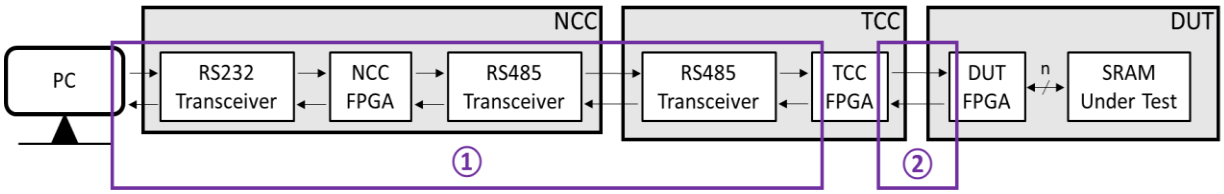


Figure 3-6 : Communication principle

The principle is established by using two different levels of communication. On one hand the communication between the PC and the FPGA of the TCC (1) is executed over the NCC board by using 8-N-1 encoded data with a data rate of 128 kbit/s. For the firmware programming the American Standard Code for Information Interchange (ASCII) has been used. The transmission standards of RS232 between the PC and the NCC and RS485 between the NCC and the TCC are used together with the corresponding transceivers on the boards. It needs to be considered, that during the CHARM test the total cable length between the NCC and the TCC has been 39 m. The communication between the FPGA of the TCC and the FPGA of the DUT (2) on the other hand is executed by using 32-bit Manchester encoded data frames with a data rate of 1 Mbit/s, by keeping in mind, that up to eight DUT boards can be connected to the TCC, respectively to the TCC FPGA.

The communication starts with the PC sending commands to the TCC FPGA through the NCC to establish the test conditions. In the other direction, the TCC responds, also through the NCC, with the test and error data to the PC, what gets recorded there over the «Docklight» software. The TCC FPGA carries out some test execution and data processing because the transmission path between the PC and the TCC has a very limited capacity for the large data sizes that are involved. The commands being sent by the PC get translated in the TCC FPGA into commands for the DUT FPGA, which sets the memory to the required value. In the other direction the responses from the DUT FPGA get also translated in the TCC FPGA before they get sent back to the PC and recorded. These responses include the number of radiation-induced events plus the address of the memory cell and the written and read values.

3.3.3 Test procedure

The firmware for the FPGAs of the TCC and the DUT card to implement the test procedure has been written by Ms. Andrea Vilar Villanueva and Mr. Benjamin Todd of the TE-EPC-CCE section. With the ASCII encoding for the communication between the PC and the TCC and the Manchester encoding between the TCC and the DUT, this subchapter describes how these communications are executed.

The test procedure starts with the user sending a write command from the PC to set the Renesas memory to the required values. This command gets transferred to the TCC FPGA requesting that the DUT FPGA initialises the memory. Afterwards a read command needs to be sent to run the memory verification. Followed by this read command the location of the error(s) gets recorded if at least one error has been found. The TCC FPGA only reports the locations of the

errors to the PC. When the scan of the intended memory area is complete the TCC sends an acknowledgement to the PC containing the last memory location and the last data that have been read. In the following subchapters the communication between each of the devices is explained by starting with the PC sending commands to the TCC and the TCC responding to the PC and then an equal procedure with commands being sent from the TCC and responses of the DUT card. At the end an example for a typical test sequence is shown.

Commands from the PC to the TCC

The PC sends commands to the TCC by using a single 28-character string. This string contains the following characteristics by using the ASCII encoding where one character refers to 1 x 8 bits:

S,P,R,C,W,FFFFF,TTTTT,DDDD<CR><LF>

The commands are sent to the TCC in the hexadecimal encoding, where one character refers to 1 x 4 bits. For hexadecimal encoding the prefix ‘x’ and for ASCII encoding the prefix ‘0x’ is used. The function of each character is described after the following scheme:

- 1st character: **S**

  The first character is used for the utilisation of several TCCs and indicates which TCC should be switched to the output lines for monitoring. One out of eight TCCs can be selected with the ASCII characters ‘0’ to ‘7’ and no TCC is selected with an ‘8’. This refers to the hexadecimal values ‘x30’ to ‘x38’. For the CHARM test only one TCC is used, therefore just the ‘0’ (x30) has been set for the TCC selection.

- 2nd, 4th, 6th, 8th, 10th, 16th and 22nd character: **,**

  The ASCII character ‘,’, which is ‘x2C’ in the hexadecimal system, has been used as an interim space to separate the code line for better reading.

- 3rd character: **P**

  The third character indicates which TCC should be power cycled or if no TCC should be power cycled at all. The ASCII characters ‘0’ to ‘8’ (x30 to x38) are used again with just the ‘0’ selecting the one TCC of the CHARM test. A power cycle enables the pin of each relevant voltage regulator of the TCC to be pulled low until a new command indicates the end of the power cycle.

- 5th character: **R**

  This position indicates with the characters ‘0’ to ‘8’ which TCC should be soft-reset or if no TCC should be soft-reset. The reset line gets pulled low until a new command indicates the end of the reset.

- 7th character: **C**

  With this character the certain TCC the command is directed to gets selected using ‘0’ to ‘7’. With an ‘8’ all TCCs get selected.

- 9th character: **W**

This character indicates the type of operation, what can be ‘W’ (x57) for write, ‘R’ (x52) for read or ‘N’ (x4E) for none.

- 11th to 15th character: **FFFFF**

  These characters select the address of the memory where reading or writing should start. The memory address contains 20 bits. With five characters the validity ranges from the ASCII encoding ‘0x00000’ to ‘0xFFFFF’ (x3030303030 to x4646464646). For example for the original hexadecimal SRAM 20 bit address ‘x023B5’, which is sent to the TCC, the ASCII encoding ‘0x023B5’ that refers to the hexadecimal ‘x3032334235’ is used.

- 17th to 21th character: **TTTTT**

  These five characters select the address of the memory where reading or writing should finish similarly to the 11th to 15th characters above.

- 23th to 26th character: **DDDD**

  These four characters indicate the data that is going to be written. To write the 16 bit binary data ‘0011 1011 1100 1101’ for example, that refers to the hexadecimal data ‘x3BCD’, the ASCII encoding ‘0x3BCD’ is used, referring in this encoding to the hexadecimal ‘x33424344’.

- 27th and 28th character: **<CR><LF>**

  These ASCII control characters perform a carriage return and a line feed for better clarity of displaying the results.

The following line shows an example for a PC command to the TCC:

0,8,8,0,R,00000,FFFFF,5555<CR><LF>

DUT 0 should be switched to the output lines and no DUT should be power-cycled. No DUT should be reset and the command is directed towards DUT 0. Reading should be performed from row ‘x00000’ to ‘xFFFFF’ and it should be checked whether the data is conform to ‘x5555’ corresponding to ‘0101 0101 0101 0101’ in the binary code.

Response from the TCC to the PC

The TCC responds to the PC with a 24-character string with the following characteristics:

S,P,R,C,W,AAAAA,DDDD,F<CR><LF>

- The characters ‘S’, ‘P’, ‘R’, ‘C’, ‘W’, ‘<CR>’, ‘<LF>’ and the commas are identical to the characters described above.

- 11th to 15th character: **AAAAA**

  These five characters select the 20-bit memory address after the same encoding as above.

- 16th to 20th character: **DDDD**

These four characters represent the read out data of the values that have been written before. If at minimum one bit-flip has occurred the values are different to the written ones above.

- 22nd character: **F**

  This character indicates the status of the reading from the memory. If the four 'DDDD' characters being read out comply with the written values, a 'P' (x50) gets displayed for a passed reading. If they are different and it failed, an 'F' (x46) gets displayed. The later used «Docklight» software only displays the error lines (F) and the last address line for the end of the reading (P or F).

The following line shows an example for a TCC response to the PC checking for the original written value of 'x5555':

0,8,8,0,R,0496E,5455,F<CR><LF>

DUT 0 has been switched to the output lines, no DUT has been power cycled and no DUT has been reset. The command has been directed towards DUT 0 and the reading of row x0496E has been performed. The read value is 'x5455' and the test has been failing because the original written value has been the checkerboard pattern 'x5555'.

Commands from the TCC to the DUT

The Manchester encoded commands from the TCC to the DUT use two 32-bit strings after the following division:

0	W	F_{19}	F_{18}	F_{17}	F_{16}	F_{15}	F_{14}	F_{13}	F_{12}	F_{11}	F_{10}	F_9	F_8	F_7	F_6
F_5	F_4	F_3	F_2	F_1	F_0	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}
1	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}
D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	X	X	X	X	X

Herein the TCC only sends the type of operation, the addresses and the data to the DUT. The two first bits in violet identify the 32-bit frames. The '0' indicates the first frame and the '1' the second frame. The 'W' identifies the type of operation with a '0' for 'read' and a '1' for 'write'. The blue F_{19} to F_0 are defined for the first address to apply the command and the green T_{19} to T_0 for the last address. The orange D_{15} to D_0 sends the data that needs to be written to the memory.

Response from the DUT to the TCC

The also Manchester encoded responses from the DUT to the TCC use the following 32-bit strings:

0	W	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6
A_5	A_4	A_3	A_2	A_1	A_0	X	X	X	X	X	X	X	X	X	X

1	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
D_0	F	X	X	X	X	X	X	X	X	X	X	X	X	X	X

The two first bits identify again the two frames and the ‘W’ the type of the operation. The blue A_{19} to A_0 represent on one hand for a write operation the last address that has been written and, on the other hand, for a read operation the address that has been containing the wrong data or the last address that has been read which means that the read operation is complete. During a write operation the D_{15} to D_0 sends the data that have been written and during a read operation it sends the wrong data that have been read from the memory. The last bit ‘F’ represents a ‘1’ during a write or a read operation and a ‘0’ during a read operation when wrong data is read from the memory.

Example for a typical test sequence

To illustrate the above this subchapter shows an example. A typical test sequence can start with the user command, respectively the PC command, to set the memory of DUT 0 to the value ‘xAAAA’. The communication between the TCC and the DUT is constituted in the hexadecimal code.

PC to TCC: **0,8,8,0,W,00000,FFFFF,AAAA<CR><LF>**
TCC to DUT0: **x 400003FF**
x FFF55540

DUT0 to TCC: **x 7FFFFC00**
x D5554000
TCC to PC: **0,8,8,0,W,FFFFF,AAAA,P<CR><LF>**

The memory of DUT 0 is now written to the requested value. The next user command reads out the memory of DUT 0 for possible errors:

PC to TCC: **0,8,8,0,R,00000,FFFFF,AAAA<CR><LF>**
TCC to DUT0: **x 000003FF**
x FFF55540

DUT0 to TCC: **x 3FFFFC00**
x 80000000
TCC to PC: **0,8,8,0,R,FFFFF,0000,F<CR><LF>**

For this response at least one error has been found in the last memory address ‘xFFFFF’. The read out data in this address is ‘x0000’. By comparing the binary encoding of ‘xAAAA’ (1010 1010 1010 1010) and ‘x0000’ (0000 0000 0000 0000) a number of 8 bit-flips or 8 errors appeared in this address.

An example for a test sequence of the actual CHARM test is shown in the following chapter 3.4.3.

3.3.4 Test strategy

With the needs for testing the Renesas SRAM at higher energies, described in chapter 3.1, the main goal of the testing strategy at CHARM has been to determine the SEU cross section of the memory at the proton energy of 24 GeV provided by the PS. This includes to observe, on one hand, the appearance of Single Bit Upsets (SBU) and, on the other hand, the appearance of Multiple-Bit Upsets (MBU) to get the concerning cross sections, while also getting the SEU cross section in total. An SBU is a single bit-flip which is caused by a single particle strike and an MBU sums up bit-flips of at least two bits which are also caused by one single particle strike. In contrary to an MCU, the MBU only affects two or more bits in a single word in one physical line, while an MCU is affecting at least two words (compare chapter 2.3.2). An analysis for MCUs has not been foreseen for this testing due to the difficulties described in the mentioned chapter 2.3.2. Without the Renesas Electronics Corporation providing information of the correspondence between the physical and logical memory organization, it does not make sense to analyse MCUs by only comparing bit-flips of different words in adjacent lines when analysing the addresses. In this case, the uncertainty and the missing of data is so high that it would produce wrong data. By multiplying MBUs with the number of affected cells and counting the results together, the number of the concerning SEUs can be calculated. By additionally adding the number of SBUs to that, the total number of SEUs with the concerning cross section can be calculated. This is done in chapter 3.5.1.

To achieve this, enough error-data results are necessary. To get sufficient of this data and to exclude the possibility of a device or test setup failure, the strategy defines the testing of at least three DUT boards during two or, if possible, three irradiations depending on the available beam time and the possible access to the facility. For these three boards it is planned to load each with one of the three test patterns ‘all 1’, ‘all 0’ and ‘checkerboard’, what refers to ‘x1111’, ‘x0000’ and ‘x5555’ in the hexadecimal system. Despite these requirements, it has ultimately only been possible to test one board during the test campaign due to certain circumstances described in the next subchapter. This tested memory has been loaded with the ‘checkerboard’ test pattern.

As secondary goal of the test strategy, the measurement of the TID being received during the whole irradiation is defined. Therefore a RadFET radiation dose sensor [34] (see figure 3-8), which uses a field-effect transistor with a gate oxide thickness of 100 nm, is foreseen to be placed in the particle beam. To measure the radiation dose a RadFET sensor uses the source-drain-resistance of a p-type MOSFET with a very thick gate oxide which has been 100 nm thick for the used one. This resistance changes proportional to the radiation dose with particle strikes whilst producing electron-hole pairs in the gate region. The holes enrich positive flaws in the substrate. Therefore an increase of the radiation dose is proportional to an increase of the voltage drop of the source-drain voltage.

3.4 Irradiation test and results

The irradiation test campaign of the Renesas SRAM at CHARM has been performed by Mr. Karol Motala, Mr. Slawosz Uznanski, Mr. Volker Schramm (all TE-EPC-CCE), Mr. Ruben Garcia Alia (EN-STI-EET) and Mr. Julien Mekki (EN-STI-ECE) with the dry run on November 6th and the execution of the irradiation on the 18th November 2014. The whole campaign including preparations and the setting up of the facility lasted from the 17th to the 18th November. This includes the testing of 16 ADCs which are also for the FGClite project.

3.4.1 Performing the test

Installation

In preparation for the irradiation, the whole test equipment has been installed in the CHARM control room for a dry run by Mr. Uznanski, Mr. Motala and Mr. Schramm. The dry run has successfully been performed on the 6th November 2014. All writing and reading out has worked as expected without the long cable lengths being a problem.

For the irradiation, the test equipment has been installed by Mr. Motala, Mr. Garcia Alia, Mr. Mekki and Mr. Schramm on the 18th November 2014. Figure 3-7 documents the installation of the DUT card in the irradiation test box. The used memory belongs to the Renesas' component batch with the lot date code «1328» and has been out of the MSC batch «2013280001». The central in-beam position of the Renesas SRAM is aligned by a laser cross which is using reference markings on the test box. Over a twelve cable harness, the DUT card is connected to the TCC, which is placed on top of the test box (compare figure 3-4). During the previous tests at PSI and TRIUMF the DUT card has

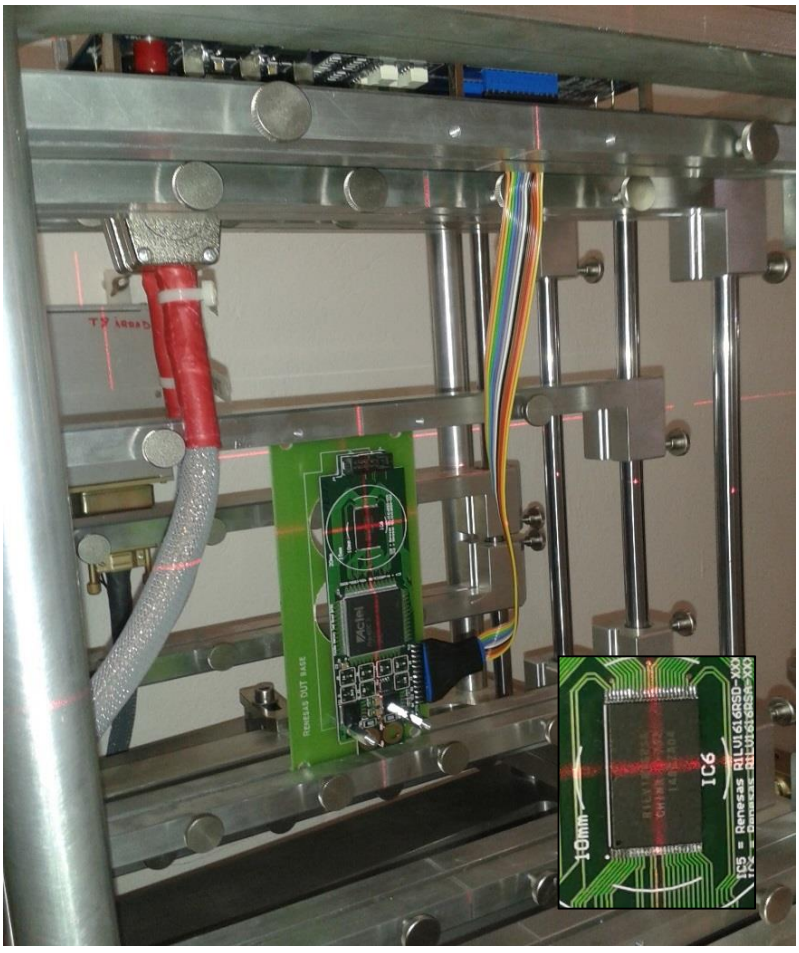


Figure 3-7 : Aligned Renesas SRAM DUT in the test box

been plugged directly into the TCC, this however has not been possible at CHARM. Out of the TCC, the 24 m long ceiling cables to the first patch panel are plugged with two DB25-connectors plus four single lemo push-pull connectors. After driving the shuttle to the in-beam position, the alignment has been checked again and slightly adjusted, where a precise centred irradiation has been guaranteed. This has been possible because of the still low radiation level in the chamber with the CHARM operation having just been started. In this final position the additional 100 nm RadFET dose sensor has been installed in the test box. It has been aligned in front of the DUT in the upstream position of the beam trajectory, see figure 3-8. The connection has been executed using a separate cable provided by the CHARM facility. The issue of a minor influence of the RadFET on the Renesas SRAM results is executed in chapter 3.5.1. After this being done, the six cables of the TCC have been connected to the patch panel in the low radiation zone and everything got connected to the NCC board in the test control room using the connectors of the transferred lines of the upper patch panel. There the NCC has been connected to the two PSUs and the laptop. After running a test to check the communication everything worked as planned and thus the test could start. As it has been mentioned above, it has not been possible to irradiate and test three Renesas SRAMs like originally planned. Due to geometrical reasons of the test box, it has not been possible to plug three DUT boards into the TCC and to align the TCC parallel to the beam making possible an alignment of the memories. Due to the short access time to the chamber and the facility, it also has not been possible to align two or more DUTs in several layers of the test box, neither has it been possible to perform another irradiation.

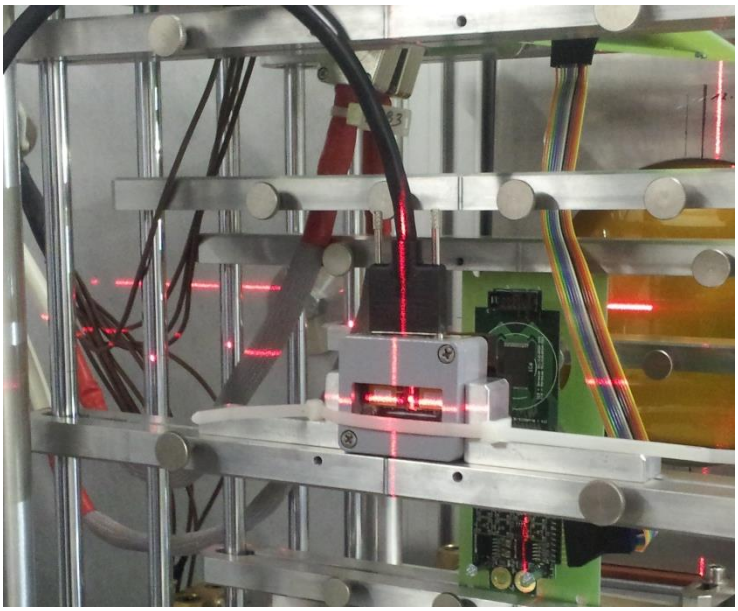


Figure 3-8 : Installation of the RadFET dose sensor

Irradiation

The irradiation has started then at 1:43 pm on the 18th November 2014 with the PS providing two slow extracted beam-spills per super cycle. The exact beam conditions are described in the next subchapter. A super cycle is a combination of different elementary cycles with a total time length of 38.4 s for the PS accelerator. At the PS, a super cycle consists of 32 individual cycles, where two have been available for the CHARM facility. The reading and writing of the memory has been performed manually from the laptop because the automatic function of the software has not been working. Due to the fact that the two spills have been the 8th and the 12th spill of the super cycle (Figure 3-10) and therefore they have been too close together to perform a save

read- and write command, the commands have always been performed after both spills of the super cycle. It has not been guaranteed that, on one side, the reading and writing would have been finished in this short interim time frame and, on the other side, that a save manual execution would have been possible each time. A problem due to this might be that too many errors that cannot all be saved in the DUT FPGA have appeared. The written values have been conform to the indicated checkerboard test pattern in chapter 3.3.4. The hexadecimal value '5555' has been written corresponding to the binary '0101' for each '5' and therefore 16 bit (compare below).

After 13 minutes at 1:56 pm several reading commands have been executed without any error responses, thus it can be assumed that the communication with the DUT has been lost. The section of the text document file for this sequence generated by the «Docklight» software is shown below.

```
[…]
18/11/2014 13:56:01.282 [TX] - 0,8,8,0,W,00000,FFFFF,5555<CR><LF>
18/11/2014 13:56:01.291 [RX] - 0,8,8,0,W,FFFFF,5555,P<CR><LF>
18/11/2014 13:56:34.241 [TX] - 0,8,8,0,R,00000,FFFFF,5555<CR><LF>
18/11/2014 13:56:34.251 [RX] - 0,8,8,0,W,FFFFF,5555,P<CR><LF>
18/11/2014 13:56:38.091 [TX] - 0,8,8,0,R,00000,FFFFF,5555<CR><LF>
18/11/2014 13:56:45.250 [TX] - 0,8,8,0,R,00000,FFFFF,5555<CR><LF>
[…]
```

Due to the fact that the TCC and the DUT card have been subjected to irradiation, they stayed at CHARM after the campaign. As they remain radioactive, the CHARM facility is disposing them.

3.4.2 Beam conditions

At the CHARM facility the proton beam is delivered from the PS accelerator at slow extraction. The beam energy for the Renesas SRAM test has been 24 GeV with the DUT card being placed in the primary beam. The diameter of the beam has taken an area of 90 cm^2, where the whole surface of the Renesas SRAM of 2.208 cm^2 has been directly irradiated by the beam. During the test the beam profile has been monitored by using the multi-wire proportion chamber at CHARM, being located directly downstream of the beam to the test setup. The MWPC, which has been developed at CERN in 1968 by Georges Charpak, detects the protons and charged particles in general by using several wires. These wires are placed in a chamber filled with gas, like an argon-methane mix for example. The wires are arranged in parallel and set under a positive high voltage. If a charged particle passes the chamber it ionizes the gas around its trajectory, where a current flow between the closest wire and the cathode is generated. By analysing these current impulses of each different wire, a two dimensional profile of the particle intensity can be generated over the distance. For the recorded beam profile during the CHARM measurements, shown in figure 3-9, two parallel arrays of wires have been used to measure the horizontal and the vertical beam profile. With such an array it is possible to determine the

position of the particle flying past up to a preciseness of a tenth of a millimetre. The MWPC being used at CHARM uses a preciseness with one pixel taking an area of 0.6 x 0.6 cm^2.

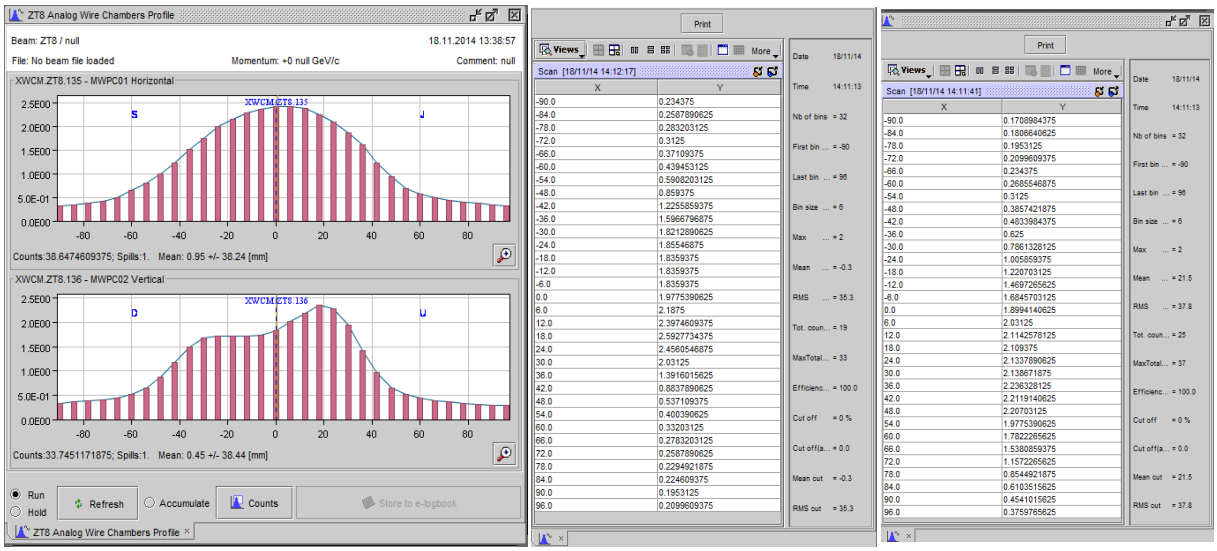


Figure 3-9 : Beam profile during the CHARM test

The measurement during the irradiation test showed a really stable beam profile. In the upper diagram on the left side of figure 3-9 it can be seen that the horizontal beam profile is very homogenous over the distance on the abscissa. On the ordinate the beam intensity is scaled. With a horizontal broadening of the Renesas SRAM of 12 mm and therefore 6 mm to each side of the beam centre, a very homogenous irradiation can be guaranteed. The beam profile in the vertical direction in the lower diagram is a little different to this, but by taking into account the vertical expansion of the Renesas SRAM of only 9.2 mm to each side, a homogenous irradiation has also been the case for this direction. The data of the beam profile in real time can be accessed over the web tool in [35].

Table 3-4 : Beam intensity per spill during the test

Timestamp (local time)	Value	#POT
18/11/2014 13:43:35	16097	3.22E+11
18/11/2014 13:43:40	16274	3.25E+11
18/11/2014 13:44:14	15223	3.04E+11
18/11/2014 13:44:19	16171	3.23E+11
18/11/2014 13:44:52	15433	3.09E+11
18/11/2014 13:44:57	15645	3.13E+11
18/11/2014 13:45:31	15908	3.18E+11
18/11/2014 13:45:36	15463	3.09E+11
18/11/2014 13:46:09	16121	3.22E+11
18/11/2014 13:46:14	15244	3.05E+11
18/11/2014 13:46:47	16297	3.26E+11
18/11/2014 13:46:52	15431	3.09E+11
18/11/2014 13:47:26	16273	3.25E+11
18/11/2014 13:47:31	16489	3.30E+11

Timestamp (local time)	Value	#POT
18/11/2014 13:48:04	16203	3.24E+11
18/11/2014 13:48:09	16852	3.37E+11
18/11/2014 13:48:43	16213	3.24E+11
18/11/2014 13:48:47	16368	3.27E+11
18/11/2014 13:49:21	15385	3.08E+11
18/11/2014 13:49:26	16364	3.27E+11
18/11/2014 13:49:59	15337	3.07E+11
18/11/2014 13:50:04	15776	3.16E+11
18/11/2014 13:50:38	16286	3.26E+11
18/11/2014 13:50:43	15686	3.14E+11
18/11/2014 13:51:16	16335	3.27E+11
18/11/2014 13:51:21	16214	3.24E+11
18/11/2014 13:51:55	16465	3.29E+11
18/11/2014 13:51:59	15857	3.17E+11

Timestamp (local time)	Value	#POT
18/11/2014 13:52:33	16192	3.24E+11
18/11/2014 13:52:38	15990	3.20E+11
18/11/2014 13:53:11	15710	3.14E+11
18/11/2014 13:53:16	16464	3.29E+11
18/11/2014 13:53:50	15555	3.11E+11
18/11/2014 13:53:55	15900	3.18E+11
18/11/2014 13:54:28	15736	3.15E+11
18/11/2014 13:54:33	15554	3.11E+11
18/11/2014 13:55:07	15965	3.19E+11
18/11/2014 13:55:11	15712	3.14E+11
18/11/2014 13:55:45	15909	3.18E+11
18/11/2014 13:55:50	15031	3.01E+11

To analyse the particle fluence during the test the table 3-4 has been generated. Here it shows the number of Particles On Target (POT), respectively protons, measured by instruments of the CHARM facility for each of the 40 received spills until the communication has been lost. This results in a total number of 1.27×10^{13} POTs received during all these spills and, in average, a beam intensity of 3.19×10^{11} POTs per spill. By taking into account the cross section area of 90 cm^2 taken by the beam a fluence of 1.42×10^{11} p/cm^2 during the irradiation time can be computed.

The infoscreen in figure 3-10 shows the CERN «VISTAR» tool. A section being recorded during the test is displayed. In the first column on the bottom left the spills are shown with spill number 8 being extracted to the CHARM facility. The abbreviation «EAST_Irrad» is used for an extraction to the complex in CERNs «East Area», where CHARM is located. The fifth column describes the type of particle. The displayed «P+» stands for protons (positive charge) with the green colour additionally indicating that everything is fine. The graph in white on top of the figure over the whole width displays the magnetic pulses being received by the particles with a time scale on the abscissa.

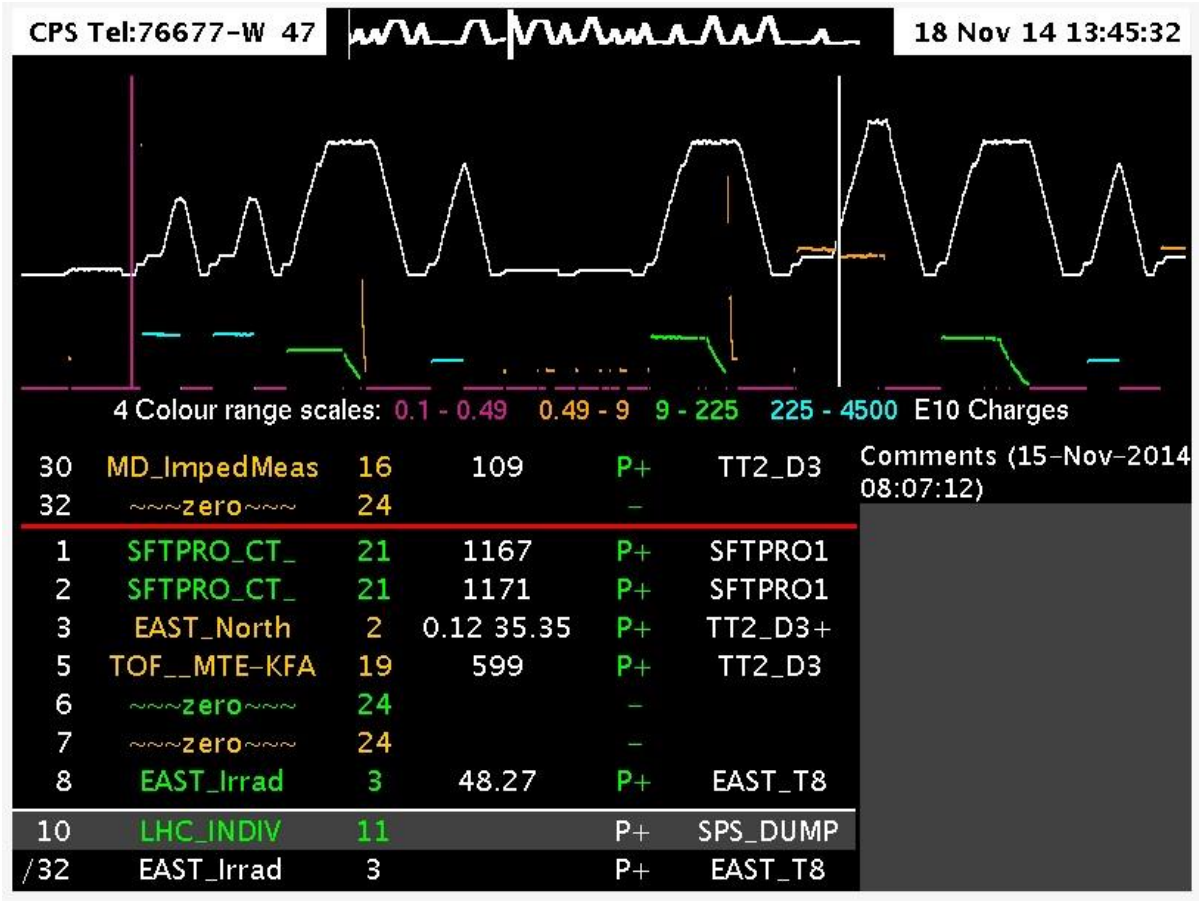


Figure 3-10 : VISTAR during the Renesas test

The VISTAR for the current operation of the PS accelerator in real time can be accessed over the web tool in [36] by selecting «CPS» from the pulldown-menu on the top left of the webpage.

3.4.3 Results

The generated text document file containing the results of the test revealed that up to the loss of communication at 1:56 pm it has been possible to read out data for in total 20 super cycles or respectively 40 spills during the test. In total 1018 error events have been observed and saved in a text document file. An example of one read-out at 1:54:02 pm with 26 occurred effects is shown below. It has been the reading with the smallest amount of error events.

```
[…]
18/11/2014 13:54:02.187 [RX] - 0,8,8,0,R,0103A,5554,F<CR><LF>
0,8,8,0,R,0848C,5545,F<CR><LF>
0,8,8,0,R,0850C,5545,F<CR><LF>
0,8,8,0,R,2CDB2,5535,F<CR><LF>
0,8,8,0,R,2CE32,5515,F<CR><LF>
0,8,8,0,R,2EB7E,5554,F<CR><LF>
0,8,8,0,R,3C945,1555,F<CR><LF>
0,8,8,0,R,5E4FB,5515,F<CR><LF>
0,8,8,0,R,6E082,5554,F<CR><LF>
0,8,8,0,R,88EE5,555D,F<CR><LF>
0,8,8,0,R,A086A,5755,F<CR><LF>
0,8,8,0,R,A5F75,5755,F<CR><LF>
0,8,8,0,R,A5F76,5455,F<CR><LF>
0,8,8,0,R,B9C59,7555,F<CR><LF>
0,8,8,0,R,BBC85,5455,F<CR><LF>
0,8,8,0,R,BD9FC,5515,F<CR><LF>
0,8,8,0,R,BDA7C,5515,F<CR><LF>
0,8,8,0,R,BDAFC,55D5,F<CR><LF>
0,8,8,0,R,BDB7C,55D5,F<CR><LF>
0,8,8,0,R,BDC7D,55D5,F<CR><LF>
0,8,8,0,R,BDCFD,55C5,F<CR><LF>
0,8,8,0,R,DA557,5545,F<CR><LF>
0,8,8,0,R,EB20D,4555,F<CR><LF>
0,8,8,0,R,FB6BA,5755,F<CR><LF>
0,8,8,0,R,FE72D,7555,F<CR><LF>
0,8,8,0,R,FFA72,5755,F<CR><LF>
0,8,8,0,R,FFFFF,5555,P<CR><LF>

18/11/2014 13:54:03.997 [TX] - 0,8,8,0,W,00000,FFFFF,5555<CR><LF>
[…]
```

A conspicuousness has been that during the second reading out of the data the reading has not completed its operation. Instead of finishing with the last memory address ‘FFFFF’, the last error line which has been read out belongs to the address ‘CE2A9’.

```
[…]
0,8,8,0,R,CD9AF,5655,F<CR><LF>
0,8,8,0,R,CE2A9,0,8,8,0,
18/11/2014 13:44:13.291 [TX] - 0,8,8,0,W,00000,FFFFF,5555<CR><LF>
[…]
```

It is also conspicuous that the line is not containing the usual end. After the displayed address, the characters of a new line continue instead of displaying the error data. In addition the reading out has been the one with, by far, the most errors by comparing it to the other read cycles. In total 127 errors occurred. An explanation for this could be that the buffer of the FPGA has been overwritten. By counting the addresses which are not displayed up to the last address of the memory a missing value of around 19 % reveals. By also taking the 19 % of the 127 errors

which occurred in this reading a missing value of around 25 events after probability calculation can be stated for this read out. The following chapter deals with this circumstance and summarizes as well as analyses the results of the measurement.

3.5 Data analysis

By taking the data and the results of the CHARM test campaign from the chapters above, a data analysis follows in this subchapter. It starts with two, more extensive, subchapters containing the SEU cross section analysis and afterwards the comparison of this analysis to results of the FLUKA simulation and finishes with a shorter subchapter, dealing with the generated results for TID effects.

3.5.1 SEU cross section analysis

The analysis of the «Docklight» file, where a small section is shown in chapter 3.4.3, revealed 1018 error events in total. Analysing the failure data and the addresses, which have been read out, resulted in the following table 3-5.

Table 3-5 : Events statistics for the CHARM irradiation

# Events	# SEU	# SBU	# MBU(2)	# MBU(3)	# MBU(4)	# MBU(>4)
1018	1159	900	97	19	2	0

Events XS	SEU XS	SBU XS	MBU(2) XS	MBU(3) XS	MBU(4) XS
4.29E-16	4.88E-16	3.79E-16	4.08E-17	8.00E-18	8.42E-19

Table 3-6 : Events statistics for the CHARM irradiation with correction factor

# Events	# SEU	# SBU	# MBU(2)	# MBU(3)	# MBU(4)	# MBU(>4)
1043	1187	922	99	19	2	0

Events XS	SEU XS	SBU XS	MBU(2) XS	MBU(3) XS	MBU(4) XS	Corr. Factor
4.39E-16	5.00E-16	3.88E-16	4.18E-17	8.19E-18	8.62E-19	**1.024**

The table shows the occurrence of error events in total and their division into SEUs, SBUs and MBUs with a different amount of bits affected. To get the amount of the different MBUs the read out data has been compared to the written ‘x5555’, if more than one bit-flip occurred. The missing errors of the second reading of around 25 events, mentioned above, are taken into account in the second table 3-6 by applying a correction factor for the missed events during the second reading. With a number of 1018 error events in total, the missing of around 25 events leads to a correcting value of around 2.4 %. This derives to a correction factor of around 1.024 which is applied in the second table by multiplying it with the results of the first table, using rounded values. The second parts of both tables are showing the concerning cross sections of

the different error events in cm^2 per bit by dividing the value of the first row with the average fluence of 1.42×10^{11} p/cm^2 (chapter 3.4.2) and the total number of 16777216 bits per memory.

In addition it needs to be mentioned, that the influence of the RadFET device which has been placed upstream the beam is neglected. By referring to experiences during previous measurements performed by the TE-EPC-CCE section at PSI, it can be stated that an influence of the beam flux by an additional card placed upstream the beam becomes insignificant at a certain energy [22]. For these measurements the flux has not significantly changed starting from energies of 230 MeV and higher for a card placed on the first upstream position and a card placed behind. At lower energies than 230 MeV an influence has been measured for different positions.

By taking the corrected SEU cross section of the CHARM data the following diagram in figure 3-11 has been generated with a value of 5.00×10^{-16} cm^2/bit at a beam energy of 24 GeV.

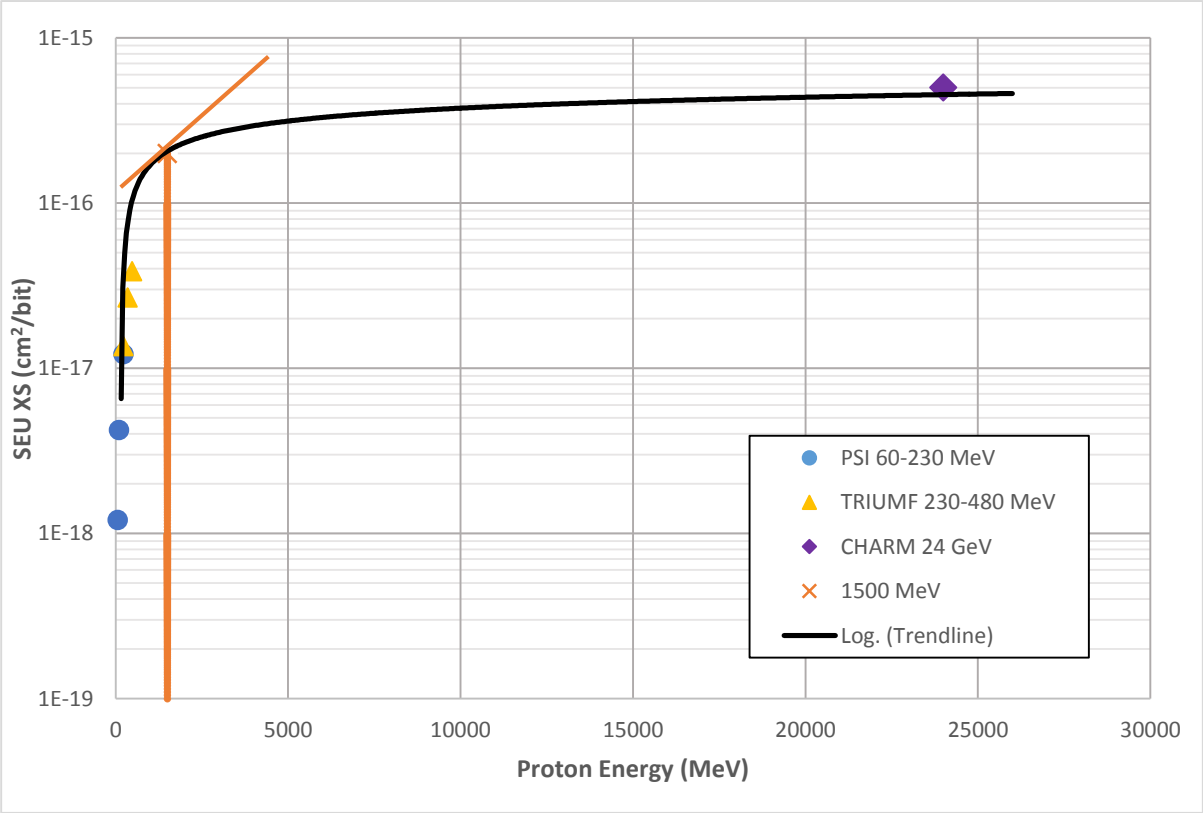


Figure 3-11 : Summarized XS results for the PSI, TRIUMF and CHARM tests – Logarithmic trendline

In compliance to figure 2-4, the data of the CHARM testing has been added. The data of the IUCF campaign by NASA has not been taken into account because data generated by the TE-EPC-CCE section is available for this energy region. Additionally the SRAMs tested by CERN have all been produced in 2013 out of two batches. It is not very likely that any process changes in the production of the SRAM have been executed in this short timeframe. For the CHARM and PSI testing the batch with the lot date code «1328» has been used and during the

TRIUMF test campaign the lot date codes «1328» and «1343» have been used. For the first analysis a logarithmic trendline in black has been added using the automatic function of Microsoft Excel. The line roughly shows a possible curve progression for the cross section development of the Renesas SRAM up to higher energies. By carefully interpreting this trendline it can be seen that the turning point of the slope is reached a little below the proton energy of 1500 MeV. This means that from this point the relative increase of the cross section in proportion to the energy is reducing, which also means that the angle of a tangent on the trendline to the horizontal line is less than 45° from this point. In addition it can be seen that around the energy of 5 GeV the slope starts getting close to a horizontal progression for the higher energies. Between 5 and 24 GeV the cross section of this specific curve increases from around 3×10^{-16} to 5×10^{-16} cm^2/bit. Compared to the big energy range and keeping a logarithmic trendline in mind this is not much, which indicates saturation in this region. A further execution of this assumption follows together with figure 3-12 in the following. For the diagram in figure 3-11 it needs to be mentioned that all this interpretation is made under the assumption that the logarithmic trendline reflects the behaviour of the memory in reality.

The following diagram in figure 3-12 displays the same data like the previous diagram with the addition that the abscissa also uses a logarithmic scale which makes it easier to display.

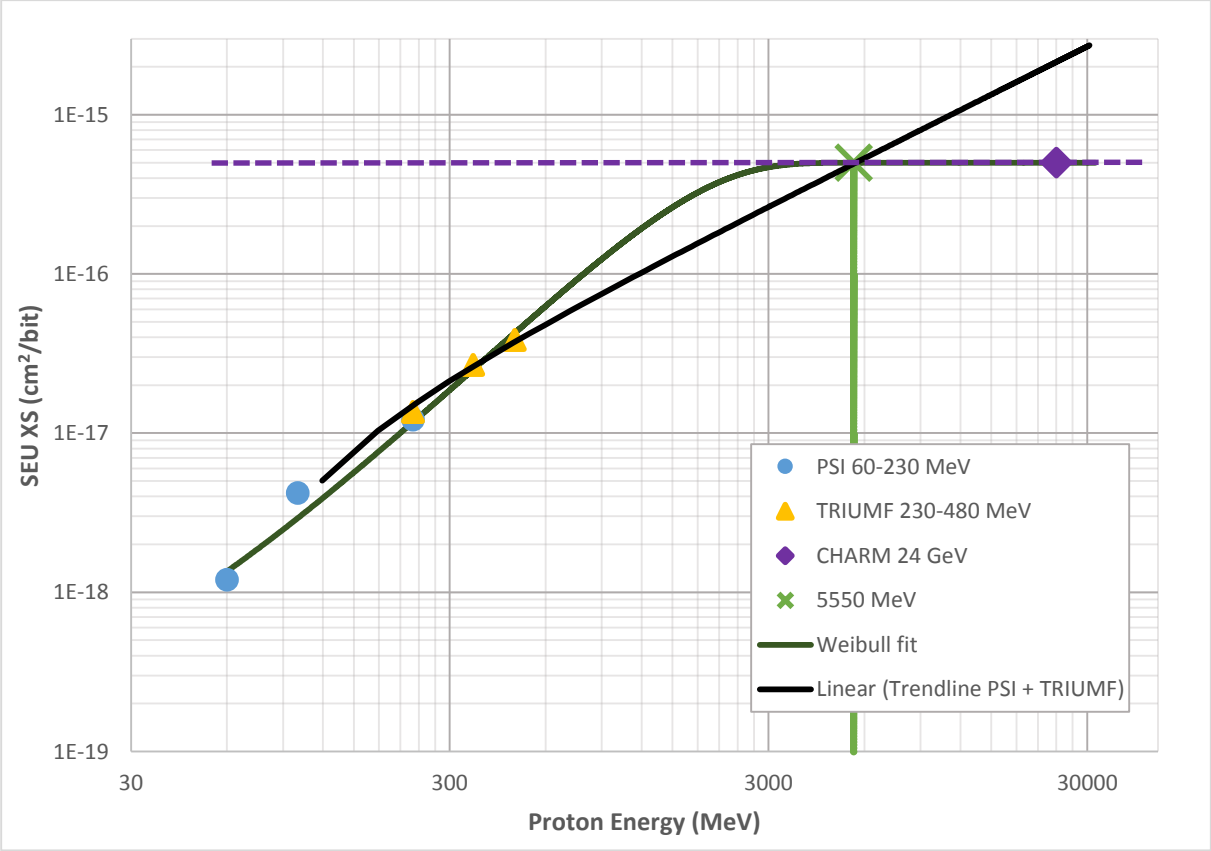


Figure 3-12 : Summarized XS results for the PSI, TRIUMF and CHARM tests – Linear trendline, Weibull fit

With this axis configuration the increase of the cross section and the approximation towards saturation at higher energies can be easily displayed. By assuming the turning point of the relative cross section increase at a beam energy of 1500 MeV, a linear trendline (black), which only uses the PSI and TRIUMF data, has been generated by using the automatic function of Microsoft Excel. Due to the fact that the cross section slope is still increasing at energies higher than 480 MeV up to approximately 1500 MeV, it can be stated that the real progression of the cross section graph must be above this linear continuation. Taking this fact into account while also considering the fact that the measurement point of the CHARM testing is below and right of the linear continuation, it can be demonstrated that at the cross section of the CHARM measurement saturation must have been reached under the assumption that no other unexpected cross section increasing effects other than the tungsten contribution appear. It can also be said that the full saturation, meaning the graph has fully approached to the cross section value of 5.00×10^{-16} cm^2/bit, is reached at latest at an energy of 5550 MeV (bright green) where the trendline crosses the saturation value, displayed by a horizontal dashed line in violet. This is matching the results of the FLUKA simulation, mentioned in chapter 3.1 and further executed in the next subchapter. By further executing the analysis of figure 3-12, the crossing point in the diagram must be interpreted as the point where the tangent to the graph has a slope of zero and thus the saturation is fully reached. The real graph to display the cross section increase over the energy should approach at much lower energies to the saturating value of the cross section, without having a significant increase at energies close to the 5550 MeV. The additional graph in the diagram named «Weibull fit» illustrates a possible progression of such a graph with a saturating cross section. It takes the PSI and the TRIUMF data, continues this data for higher energies and approaches the graph to the assumed maximum cross section of 5.0×10^{-16} cm^2/bit using the Weibull function. For this approximation it can be seen that the start of the saturating region is around the proton energy of 3 GeV without taking into account an insignificant increase after 3 GeV, keeping in mind that the FLUKA simulation predicts an end of the cross section increasing tungsten effect in this energy range (see next subchapter).

To better display the above mentioned turning point in association with the Weibull function, the diagram of figure 3-12 is shown again in the appendix using a linear scale on the ordinate and illustrating that the turning point of the Weibull approximation also appears around the energy of 1500 MeV. This is compliant with the interpretation of the logarithmic trendline in figure 3-11. And to mention once more at the end of this first analysis, it has unfortunately not been possible to produce several points at energies around 24 GeV, which would have proofed all the assumptions from above.

Another and last thing noteworthy mentioning in this subchapter is the error polarity of the 1159 SEUs in total, which have been read out by the «Docklight» software. As displayed in table 3-7 bit-flips from a logical ‘0’ to a logical ‘1’ occurred 528 times, and bit-flips in the other direction appeared 631 times. With a deviation of less than 20 % it can be said that there is most probably no specific polarity towards a flipping into a certain direction.

Table 3-7 : SEU error polarity

Error polarity	
0->1	528
1->0	631

3.5.2 Comparison of the SEU cross section analysis to FLUKA Monte Carlo results

In the diagram of figure 3-13 the results of the FLUKA simulation are integrated into the previous diagram of figure 3-12. The simulation has been prepared before the start of this work by Mr. Ruben Garcia Alia from the EN-STI-EET section of CERN and published during the NSREC conference in the year 2014 [25]. By modelling the nuclear interaction between the accelerated particles and the matter, the geometry of the Renesas SRAM has been built in FLUKA. By additionally using the real measurements of the different regions in the component and the material composition corresponding to the reality, the FLUKA model represents a very powerful tool simulating very close to the reality as the FLUKA simulation is using physical models and the best data available.

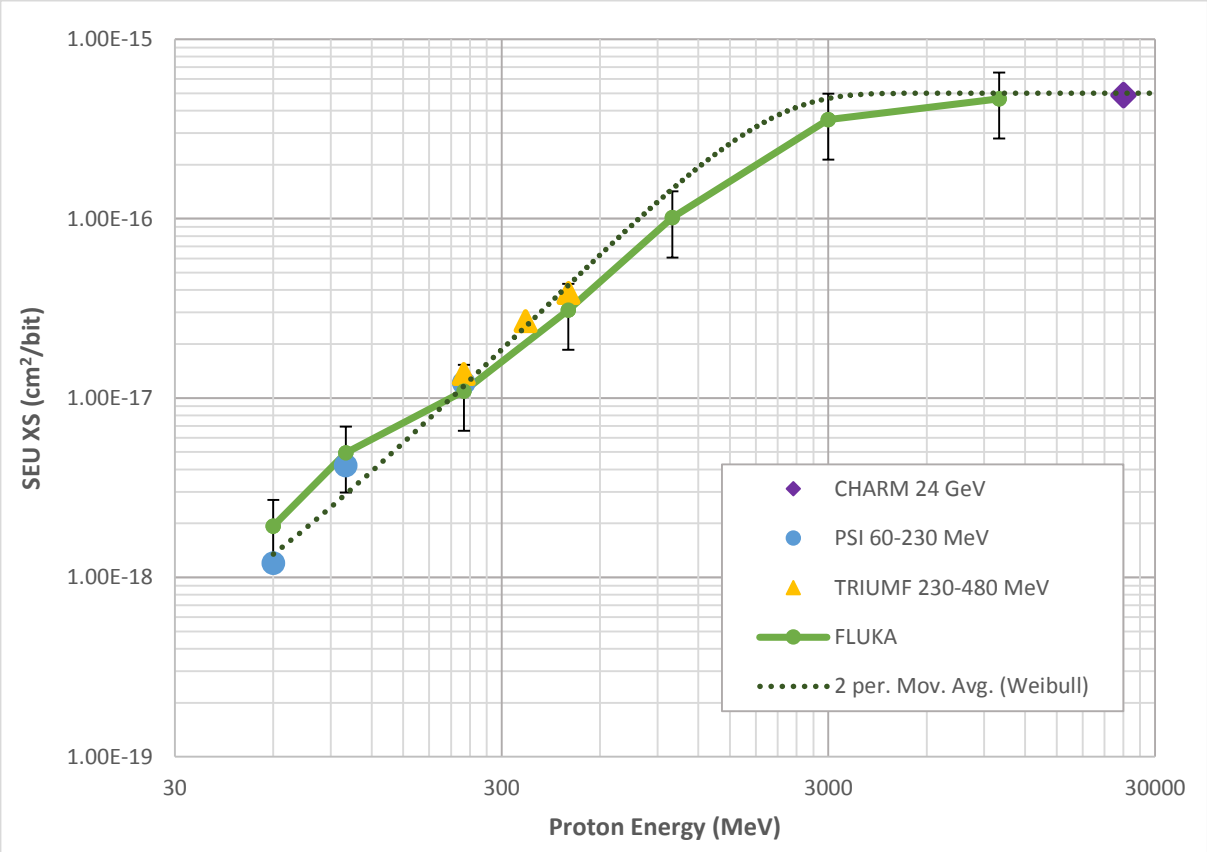


Figure 3-13 : Summarized XS results for the PSI, TRIUMF and CHARM tests – FLUKA simulation

The graph in bright green uses the simulated cross section data of table 3-8 and connects the data points. The table displays the results of the simulation for seven different beam energies from 60 MeV to 10 GeV. Due to limited processing power the cross sections have just been simulated for the beam energies of certain PSI and TRIUMF measurements, for 1 and 10 GeV and for the 3 GeV, where it is predicted that the influence of the tungsten stops increasing the cross section. However, these simulated energies match very well the measured points at PSI and TRIUMF and especially the measured point at CHARM, displayed in violet, when

presuming an imaginary continuation of the progression. As already mentioned the results of the FLUKA simulation have a very strong weighting in the analysis due to the fact of integrating a lot of real measured data. Therefore FLUKA produces very solid data in the energy regions where no measurement is available and gives a model to rely on.

To compare the FLUKA data points to the Weibull approximation of the previous analysis the Weibull graph is added in figure 3-12 represented by a dashed line in dark green. In addition, error bars for each FLUKA point are shown with a percentile deviation of 40 % of the value. As it can be seen, the Weibull graph is very close to the FLUKA simulation and within this deviation. The percentile deviation of 40 % is not much regarding the absolute range of the numbers on the ordinate with the logarithmic scale. It can be concluded that the Weibull approximation matches the values of the FLUKA model very well under the assumption that the Weibull graph can approximate the real progression of the SEU cross section and beam energy. This is especially important between the energies of 480 MeV and 24 GeV where only FLUKA data is available. As it can be seen in the diagram both graphs confirm the predicted effect of the tungsten contribution to the cross section with a predicted saturation at an energy around 3 GeV.

Table 3-8 : FLUKA Monte Carlo cross section simulation

E (MeV)	FLUKA (cm^2/bit)
60	1.93E-18
100	4.96E-18
230	1.09E-17
480	3.10E-17
1000	1.01E-16
3000	3.56E-16
10000	4.66E-16

3.5.3 TID analysis

To analyse the received Total Ionizing Dose during the CHARM testing, the loss of communication after 13 minutes of irradiation needs to be regarded. During this time, the Reneses SRAM and the DUT board have received a radiation dose of 65 Gy as measured by the RadFET monitor. Due to the fact that no TID failure during the previous measurements at PSI and TRIUMF appeared in such an exceptional low energy region it can be concluded that the loss of communication must have occurred due to other reasons. Therefore still the lower TID failure value of the PSI and TRIUMF measurements needs to be considered as the TID limit for the LHC requirements. With a minimum bearable dose of 324.9 Gy, measured at these facilities, the LHC minimum TID requirement of 200 Gy until 2035 (chapter 1.3.2) is still satisfied.

3.5.4 Result and conclusion of the analyses

To finish and summarize the data analysis of the three subchapters above, it can be concluded that a maximum SEU cross section of around 5.00×10^{-16} cm^2/bit can be stated for the Renesas SRAM when exposed to proton radiation. By comparing this result with the cross sections of four other SRAMs, which have been measured by the EN-STI group of CERN in October 2013 at the much lower beam energy of 480 MeV [21], it can also be stated that the maximum cross section of the Renesas SRAM is around factor 70 and 390 lower than these results at much lower energies. At the energy of 480 MeV with the measured cross section of 3.85×10^{-17} cm^2/bit for the Renesas SRAM (chapter 2.3.3) this error-reducing factor even lies between an order of magnitude of around 1000 and 5000. Table 3-9 shows the average measured cross sections at a beam energy of 480 MeV for these four SRAMs which are the 4 Mbit Samsung «K6R4016V1D», the 4 Mbit Alliance «AS7C34098A», the 16 Mbit ISSI «IS62WV20488ALL» and the 16 Mbit Cypress «CY6157EV30LL-45ZSXI», which is also installed in the FGClite (chapter 2.2). The third column displays the cross section reducing factor for the Renesas measurement at the energy of 24 GeV.

Table 3-9 : Cross sections at 480 MeV for different SRAMs compared to 24 GeV Renesas SRAM cross section [21]

Device	XS (cm^2/bit)	XS/5.0E-16cm^2/bit
K6R4016V1D	4.04E-14	80.8
AS7C34098A	3.48E-14	69.6
IS62WV20488ALL	8.06E-14	161.2
CY6157EV30LL-45ZSXI	1.94E-13	388

To shortly mention the TID analysis, it needs to be said that, unfortunately, no further results could have been presented with the test at CHARM.

4 Conclusion and outlook

Conclusion

A maximum Single Event Upset cross section of around 5.0×10^{-16} cm^2 per bit can be stated for the Renesas SRAM, where its SEU reliability in the radiation of the LHC can be predicted for the environmental circumstances in the installed regions while also considering the electrical reliability with the acceptable Failure In Time value of 12.7 FIT (Table 2-2). The reason for this low cross section is the use of two additional capacitors per 6-transistor cell of the memory (Figure 2-1), mentioned in chapter 2.1. These two capacitors increase the nodal charge inside the cell, what also increases the resistance against particle strikes. Thus the ionization of atoms induced by a particle strike needs to be much higher than without using the capacitors. To display a probable progression of the cross section over the proton energy, a graph has been generated using the Weibull function (Figure 3-12) to display the possible beginning of a cross section saturation and the progression in the wide energy range between 480 MeV and 24 GeV. Even more dependable results for parts of this energy region have been generated prior to this work using a FLUKA Monte Carlo simulation integrating data from previous measurements [25]. These results have been used and analysed in chapter 3.5.2. Another big reduction of the Renesas SRAM failure rate due to radiation results from the fact that the memory does not have a classical CMOS structure with its two thin film PMOS transistors placed on the silicon substrate (chapter 2.1). For this reason the occurrence of any Single Event Latch-up can be excluded. As third point to mention in this conclusion, adding up to the SEU cross section analysis, the Renesas SRAM shows an increasing growth of the cross section at proton energies higher than 230 MeV in contrary to standard SRAMs, which tend to saturate in this energy region. According to FLUKA Monte Carlo simulations this effect is most probably caused by the presence of Tungsten in several regions of the memory of which the heavy ions interact with the proton radiation at higher energies (chapter 3.1). A second explanation for this effect could be an increasing contribution of Multiple Bit- respectively Multiple Cell Upsets to the SEU rate for proton radiation at these energies. Here it can also be stated that the FLUKA simulation matches the measured reality fairly well.

Unfortunately, for a Total Ionizing Dose analysis, no further results have been generated during the irradiation at CHARM as well as a testing for Displacement Damage has not been executed for the Renesas SRAM yet. Nevertheless, previous TID tests confirm a sufficient reliability for the specified lifetime in the LHC and Displacement Damage is not regarded to appear in a considerable amount in the radiation and at the energies of the accelerator.

Outlook

To give a broad outlook of what can further be done to investigate and specify the radiation performance of the Renesas SRAM, it can be said that at least five test campaigns are planned with the memory for the near future. In addition to this, a Master thesis starts in June 2015 analysing the whole reliability of the FGClite module. One of the test campaigns is the testing of the complete FGClite module at the mixed-field energies of the CHARM facility, planned to be executed in the autumn of 2015. In addition, a test of a whole power converter, including the controller, is also planned. During these tests the Renesas SRAM needs to proof its predicted qualification for this environment in its later operating system and in a mixed-field environment similar to the one in the LHC complex. The complete proof will be of course the operation of the FGClite module starting from 2016 in the accelerator itself and in the HL-LHC from 2024 up till hopefully 2035 or maybe even longer. A lot of reliability data will then be generated with the mass of at minimum 1094 units installed and the, until now not known, high luminosity environment of the HL-LHC. As a third campaign there is, prior to the FGClite test at CHARM another mixed-field test planned at the facility by the EN-STI-EET section of CERN to investigate the energy dependence of the SRAM at different energy ranges, likewise to the environment of the LHC. By using a quantity of around 10 DUTs it should be ensured that enough errors will be produced by the memories in the relatively low dose environment to perform an analysis. As fourth campaign on the current schedule testing of the Renesas SRAM, with heavy ion irradiation, is planned in June 2015 at the «Kernfysisch Versneller Instituut» (KVI) in Groningen, Netherlands. This campaign, of which one main goal is to investigate the reliability of the Renesas SRAM for space applications, has already started in March 2015 with heavy ion irradiation tests at the UCL (Université Catholique de Louvain) facility in Louvaine-la-Neuve, Belgium. In 2016, in the scope of this campaign, it is further planned to perform tests at the GSI (Gesellschaft für SchwerIonenforschung) facility in Darmstadt, Germany.

To further execute and determine the results being presented during this work other measurements can be carried out with the memory at beam energies around 24 GeV to generate definitive proof for the saturation of the SEU cross section over the proton energy. Associated to this the suspected saturation region around a proton energy of 3 GeV and the still increasing growth of the cross section graph after 480 MeV can be further determined. Also in this context, the results of the FLUKA simulation can be verified by real test data. In addition different test patterns should be tested during such tests to investigate the error polarity.

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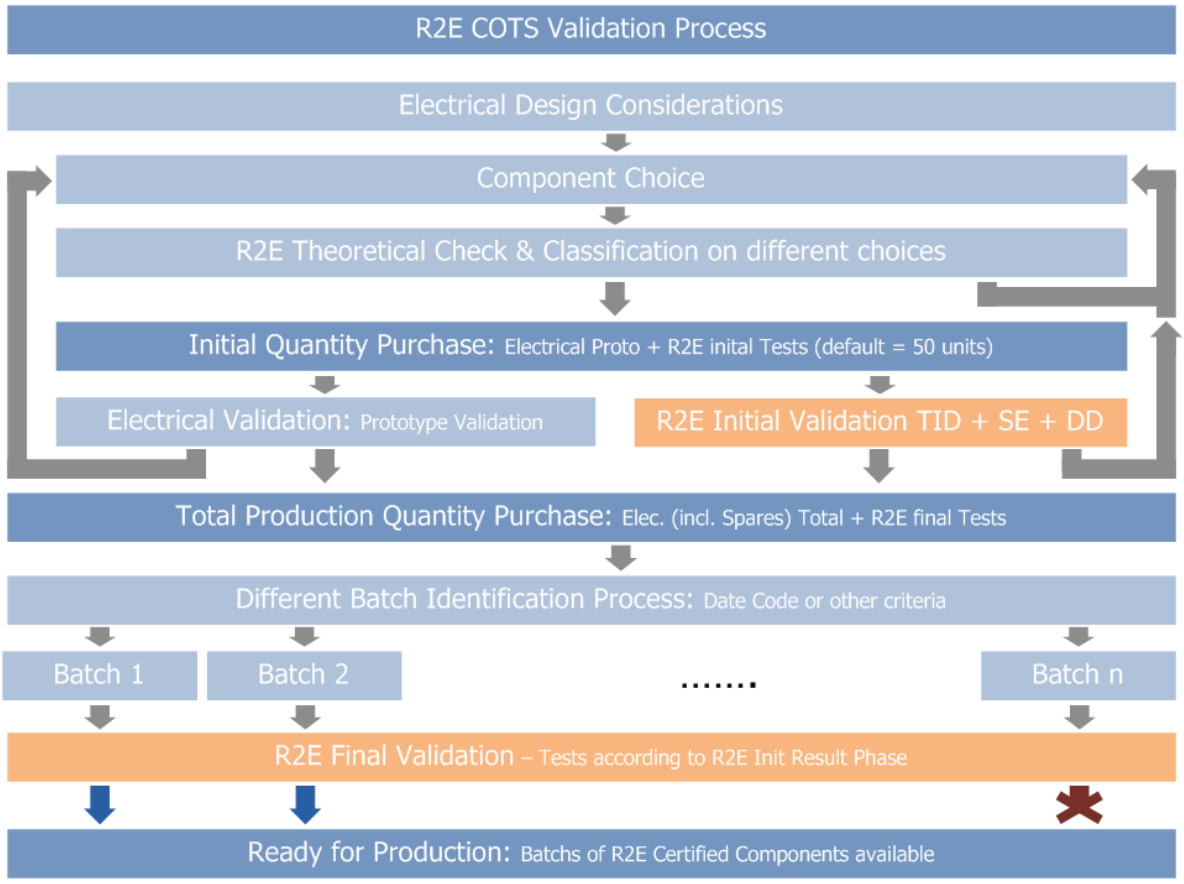
6 Appendix

Table of Contents

- **1.3.2 Reliability and availability requirements for the FGClite**

COTS management of the TE-EPC group:



(http://te-epc-lpc.web.cern.ch/te-epc-lpc/context/radiations/r2e_cots.stm)

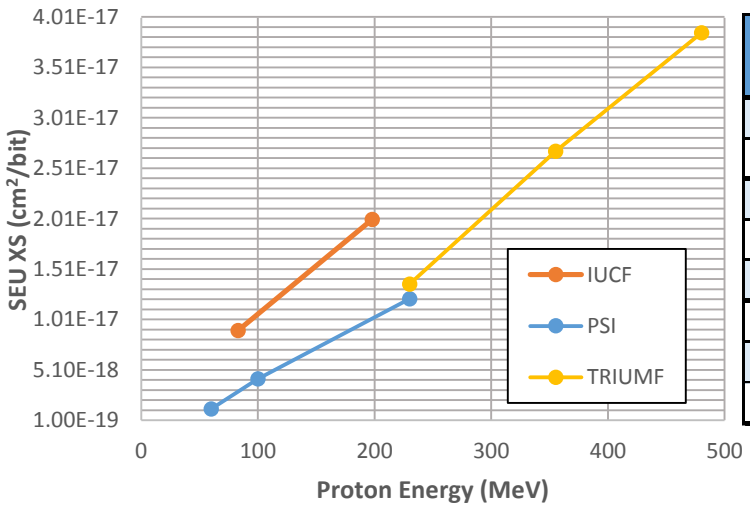
- **2.3.2 Up to 230 MeV proton beam tests at PSI**

The ESA SEU monitor is a device developed by the European Space Agency as a reference standard for the beam calibration for radiation induced errors. With a 4 Mbit SRAM memory mounted as reference it detects SEUs. This generated error data can be compared to other electronic components. During the PSI test in October 2013 the measured cross section of the monitor is displayed in the fourth row of the following table. The correction factor, which has been mentioned in table 2-5, is calculated with the PSI measurement data in the fifth row.

	run 2	run 4	run 5
Energy	**230**	**100**	**60**
SEUs	4337	2713	2684
Fluence	1.00E+10	1.00E+10	1.00E+10
Measured XS	2.59E-14	1.62E-14	1.60E-14
Golden data XS (Giovanni Oct 21, 2013)	2.60E-14	2.70E-14	2.97E-14
Correction factor	1.01E+00	1.67E+00	1.86E+00

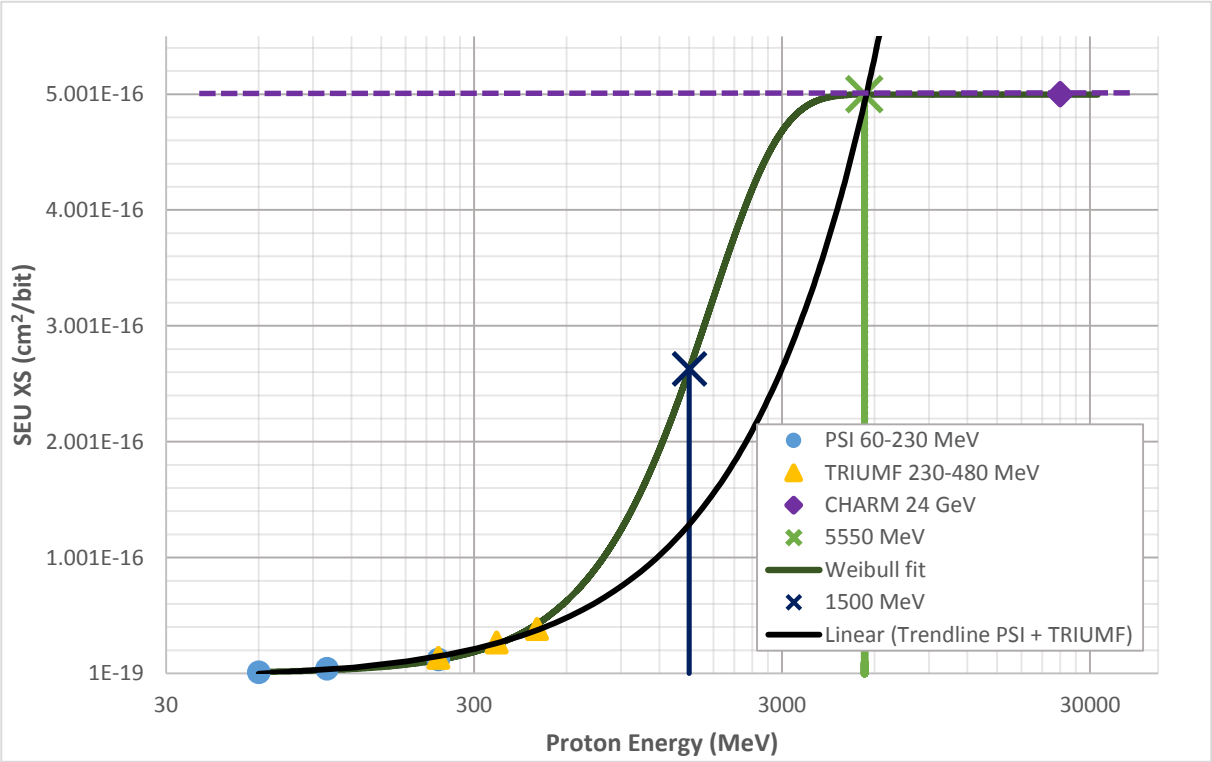
(Andrea Vilar Villanueva, Slawosz Uznanski (both TE-EPC-CCE) "Renesas LPSRAM: SEU/MCU cross section measurement", 2013, test report)

- **2.3.4 Summary of the previous proton irradiations**



Facility	Energy (MeV)	Cross Section (cm^2/bit)
IUCF	83	9.00E-18
	198	2.00E-17
PSI	60	1.20E-18
	100	4.21E-18
	230	1.21E-17
TRIUMF	230	1.36E-17
	355	2.68E-17
	480	3.85E-17

- **3.5.1 SEU cross section analysis**



- **Bibliography [13] :**

From: Birgit Pingel [mailto:birgit.pingel@renesas.com]
Sent: 13 April 2015 11:43
To: Volker Schramm
Subject: RE: [Technical Support Center] Re: RE: [Technical Support Center] Re: Technical Inquiry - R1LV1616RSA-7SI#B0

Dear Mr. Schramm,

I am sorry it seems that my colleague Jessica and I misunderstood each other, as I thought that she would reply to you.

There is no concern from our side to publish the FIT-value of our 16Mb advanced Low Power SRAM:
8.4 FIT (60%CL)

Best regards
Birgit Pingel

From: Volker Schramm [mailto:volker.schramm@cern.ch]
Sent: 13 April 2015 11:18
To: Birgit Pingel
Subject: FW: [Technical Support Center] Re: RE: [Technical Support Center] Re: Technical Inquiry - R1LV1616RSA-7SI#B0

Dear Ms. Pingel,

In March I sent Renesas a request that has been forwarded to you. It is displayed on the bottom of the thread below. I would kindly like to ask, if it's possible to publish the FIT-value of the attached document of your SRAM.

Thank you very much in advance,

Best regards,
Volker Schramm

- **Bibliography [16] :**

From: Volker Schramm [mailto:volker.schramm@cern.ch]
Sent: Wednesday, March 11, 2015 2:54 AM
To: app@alliancememory.com
Subject: Product inquiry - AS6C1616-55TIN

Dear ladies and gentlemen,

Here at CERN, the Central European Organization for Nuclear Research, we are considering using your Low Power SRAM "AS6C1616-55TIN". Due to a reliability analysis I would like to ask you if you have test data concerning that. If you could provide a Failure Rate, FIT- respectively MTTF-value it would help a lot.

Thank you very much in advance,

Best regards,
Volker Schramm

From: Sue Macedo [mailto:sue@alliancememory.com]
Sent: 12 March 2015 16:23
To: Volker Schramm
Cc: sue@alliancememory.com
Subject: RE: Product inquiry - AS6C1616-55TIN

Dear Volker
I have been forwarded your enquiry via our website.

I attach details as requested for the Alliance Memory part# AS6C1616-55TIN.

Please let me know if you need further information or any support.
Regards
Sue

ALLIANCE MEMORY
Sue Macedo
Director EMEA

Alliance Memory Inc.
EMEA HQ
NEW Address!
20 Grensell Close
Eversley
Hampshire RG27 0QQ
United Kingdom
m: +44 (0)787 634 4055 |
e: sue@alliancememory.com |
w: www.alliancememory.com
Twitter | Facebook
:sue.macedo-alliance

From: Volker Schramm [mailto:volker.schramm@cern.ch]
Sent: 10 April 2015 09:16
To: sue@alliancememory.com
Subject: RE: Product inquiry - AS6C1616-55TIN

Dear Sue,

Thank you very much for that information. I would kindly like to ask you one further thing:
I am writing a research project for my university (University of Stuttgart) for what your SRAMs performance has been tested under radiation, to evaluate a possible use in our machine. Due to an analysis of the electrical reliability I would kindly like to ask you if I could use the FIT-value of your SRAM (6.8) in my paper. It will only be used once in a table.

This would help a lot, thank you very much in advance,

Best regards,
Volker Schramm

From: Sue Macedo [mailto:sue@alliancememory.com]
Sent: 10 April 2015 12:33
To: Volker Schramm
Cc: sue@alliancememory.com; david@alliancememory.com
Subject: RE: Product inquiry - AS6C1616-55TIN

Volker
I confirm that Alliance Memory would be OK with you using the FIT value in your Research Project, as long as it reflects Alliance Memory in a favourable light, and not in any way is defamatory...

Would it be possible to have a copy of your paper for *internal use purposes only*...once you have completed..
Thanks and good luck.
Regards
Sue

ALLIANCE MEMORY
Sue Macedo
Director EMEA

Alliance Memory Inc.
EMEA HQ
NEW Address!
20 Grensell Close
Eversley
Hampshire RG27 0QQ
United Kingdom
m: +44 (0)787 634 4055 |
e: sue@alliancememory.com |
w: www.alliancememory.com
Twitter | Facebook
:sue.macedo-alliance

- **Bibliography [17]:**

From: IDT Technical Support [mailto:product-support@idt.com]
Sent: 16 March 2015 03:22
To: Volker Schramm
Cc: Markus.Koehne@idt.com; Ruben.Aszkenasy@idt.com
Subject: Issue 50088: IDT Support Request

Hello Volker,
Please refer below.

71T75602 - 4 FIT (MTBF = 25,862yrs)@ Tu = 55C, Ea =0.7eV, 60%C.L.

Thanks.....hblee

am/no. 24

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From: IDT Technical Support [mailto:product-support@idt.com]
Sent: 13 March 2015 09:28
To: Volker Schramm
Subject: Issue 50088: IDT Support Request

Thank you for your inquiry. Your request has been forwarded to the IDT Support Team. We make every effort to send an initial response to your request within one business day.

If you have an additional request regarding this issue, please reply to this email. If you have another request regarding a different issue, please submit a new request.

IDT Support Team

Name	Volker Schramm
Email	volker.schramm@cern.ch
Company	CERN
Address	Route de Meyrin 385
City	1217 Meyrin
State/Region	
Country	Switzerland
Phone	
Cat Tier 1	Memory & Logic
Cat Tier 2	SRAMs
Cat Tier 3	Zero Bus Turnaround (ZBT)
Cat Tier 4	
Product	71T75602 - 2.5V 512K X 36 ZBT Synchronous 2.5V I/O PipeLine SRAM
Issue Type	Technical
Support request detail:	
Dear ladies and gentlemen, Here at CERN, the Central European Organization for Nuclear Research, we are considering using your Low Power SRAM "71T75602". Due to a reliability analysis I would like to ask you if you have test data concerning that. If you could provide a Failure Rate, FIT- respectively MTTF-value it would help a lot. Thank you very much in advance, Best regards, Volker Schramm	

am/no. 08

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