

The PreProcessor Module for the ATLAS Tile Calorimeter at the HL-LHC

F. Carrió^{a,*}, A. Valero^a, on behalf of the ATLAS Tile Calorimeter Collaboration

^aInstituto de Física Corpuscular (CSIC-UV)
C/ Catedrático José Beltrán 2, 46980, Paterna, Spain

Abstract

The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider. In 2026, the LHC will be upgraded to the High Luminosity LHC (HL-LHC) allowing it to deliver up to 7 times the nominal instantaneous design luminosity. The Phase-II TileCal Upgrade will accommodate the detector and data acquisition system to the HL-LHC requirements. The on- and off-detector electronics will be completely redesigned, using a new readout architecture with a full-digital trigger system. The upgraded on-detector electronics will transfer digitized data for every bunch crossing (~ 25 ns) to the Tile PreProcessor system in the counting rooms, with a total data bandwidth of 40 Tbps. The TilePPr will store the detector data in pipeline memories to meet the new ATLAS Trigger and Data Acquisition architecture requirements, and will interface with the FELIX system and the first level trigger system.

Keywords: DAQ system, High Energy Physics, ATLAS, CERN, Field Programmable Gate Array, ATCA

1. Introduction

The Tile Calorimeter (TileCal) [1] is the hadronic calorimeter of the ATLAS experiment [2] at the Large Hadron Collider (LHC) at CERN. TileCal is a sampling detector made of steel plates as absorber and scintillator tiles as active medium. TileCal (Figure 1) is divided longitudinally into two central barrels (Long Barrel A and Long Barrel C) and two Extended Barrels (Extended Barrel A and Extended Barrel B) which are in turn staggered azimuthally into 64 modules each.

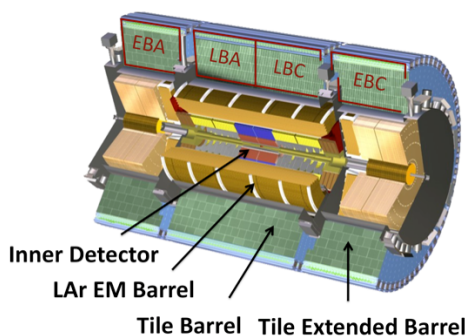


Figure 1: The Tile Calorimeter detector.

TileCal comprises a total of 4672 readout cells, each equipped with two PhotoMultipliers (PMT) that receive light

from opposite sides of every scintillator tile. Energy depositions by particles crossing the plastic scintillating tiles produce light which is conducted by wavelength shifting fibers to the on-detector electronics in the outermost part of the detector.

The current on-detector electronics shape and digitize the signals from the PMTs every ~ 25 ns with 10-bit Analog-to-Digital Converters (ADCs). Data is stored in pipeline memories until a first level trigger acceptance signal is received, upon which data from selected events is read out to the off-detector electronics. In parallel, the PMT signals are grouped and transmitted to the ATLAS trigger system for trigger decision.

In the back-end electronics, the main component is the Read-Out Driver (ROD) which performs preprocessing and gather the data coming from the front-end electronics at a maximum average trigger rate of 100 kHz. After performing the energy and time reconstruction for each channel, RODs transmit the processed data to the High Level Trigger system. A total of 32 RODs are required for the complete readout of the Tile Calorimeter.

2. Tile Calorimeter at the HL-LHC

The LHC was designed to collide protons at a centre of mass energy of 14 TeV with a luminosity of $1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ which allowed the discovery of the Higgs boson on July 2012. In order to fully exploit its potential, the LHC plans a series of upgrades towards the High Luminosity-LHC. After these upgrades the LHC will reach an instantaneous luminosity of $7.5 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ with an expected number of collisions per bunch crossing up to 200 collisions in average and providing a total integrated luminosity of 4000fb^{-1} in 10 years.

After the ATLAS Phase-II Upgrade in 2026, the readout electronics of TileCal will be completely replaced to cope with the

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*Corresponding author
Email addresses: fernando.carrio@cern.ch (F. Carrió),
alberto.valero@cern.ch (A. Valero)

new requirements in radiation levels of the HL-LHC and increased data bandwidths imposed by the full-digital ATLAS TDAQ system [3]. The upgraded readout electronics includes redundant power supplies and optical fibers between on- and off-detector electronics, radiation-tolerant electronics, and the use of communication protocols with error correction such as the GigaBit Transceiver (GBT) [4] protocol.

The upgraded on-detector readout electronics (Figure 2) transmits digitized data for every bunch crossing (~ 25 ns) to the PreProcessors (TilePPr) located off-detector. The TilePPr stores digitized data in large pipeline memories up to $60 \mu\text{s}$. Upon the reception of the trigger acceptance signal, the selected data is extracted from the pipeline memories and it is transmitted to the Front End LInk eXchange (FELIX) system [5].

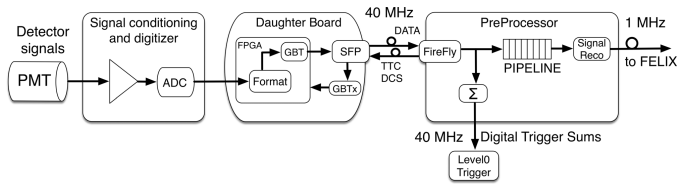


Figure 2: Block diagram of the TileCal readout architecture for the HL-LHC.

In addition, the TilePPr will process the detector data in real-time, transmitting calibrated energy and time per cell to the Trigger and DAQ interface module (TDAQi) which interfaces with to the ATLAS trigger system.

A total of 32 TilePPr and TDAQi modules will be installed in ATLAS keeping the current ratio between the number of channels and off-detector electronics boards. Table 1 shows a comparison between the data bandwidths and general requirements for the current and HL-LHC off-detector systems.

| | Current | Phase II Upgrade |
|------------|----------|------------------|
| Total BW | 165 Gbps | 40 Tbps |
| Nb. fibers | 256 | 4096 |
| BW/module | 800 Mbps | 160 Gbps |
| Nb. boards | 32 | 32 |
| Nb. crates | 4 (VME) | 4 (ATCA) |
| BW/board | 6.4 Gbps | 1.28 Tbps |

Table 1: Comparison between the off-detector requirements for the current and Phase-II Upgrade systems.

3. Upgraded TileCal electronics for the HL-LHC

3.1. On-detector electronics

For the HL-LHC, each TileCal module is divided into four identical and independent mini-drawers, which contain the on-detector electronics. Each mini-drawer contains the on-detector electronics required for the acquisition of the PMT signals, high-speed interface with the off-detector electronics and the high voltage distribution system for the PMTs. This new segmentation of the readout system improves the reliability of the on-detector acquisition system through an increased redundancy of the on-detector electronics and power supplies.

A picture of a mini-drawer populated with all the on-detector electronics is shown in Figure 3.

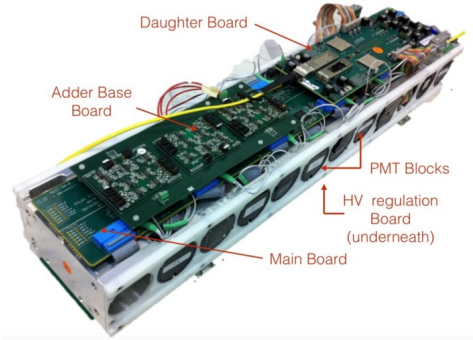


Figure 3: Picture of one Tile mini-drawer containing the upgraded on-detector electronics. The red line indicates the redundancy of the electronics system.

3.2. PreProcessor prototype

A first prototype of the TilePPr, called the TilePPr Demonstrator, has been designed and validated. This prototype (Figure 4) represents $1/8^{\text{th}}$ of a full-size PPr module for the HL-LHC, and it is capable of operating one complete TileCal module (4 mini-drawers) while providing compatibility with the current DAQ architecture.

The TilePPr Demonstrator is a double mid-size AMC form factor compliant with the AdvancedTCA standard [6] which can be operated in an ATCA carrier or in a μTCA crate. The TilePPr Demonstrator includes one Virtex 7 FPGA (Readout FPGA) connected to four QSFP modules and one Kintex 7 FPGA (Trigger FPGA). It also hosts two Texas Instruments CDCE62005 jitter cleaners, DDR3 memories and one Ethernet port in the front panel. The backplane provides power to the board, as well as a high number of high-speed ports for the communication to the ATCA backplane. The Readout FPGA implements all the firmware required for the readout and operation of one TileCal module, and the Trigger FPGA is devoted for the communication with the trigger system.

As part of the validation stage, BER tests have been performed using sixteen links running at 9.6 Gbps with a PRBS-31 data pattern over a period of 115 hours. Results showed a BER better than 5×10^{-17} with a confidence level of 95%.

3.3. Demonstrator module

The Tile Calorimeter collaboration has built a Demonstrator module to validate and qualify the upgraded readout electronics before its installation during Phase II.

The Demonstrator module was equipped with prototypes of the Phase-II Upgrade electronics. The performance of the upgraded electronics was tested and validated during seven test beam campaigns between 2015 and 2018 in the H8 beam line of the SPS accelerator at CERN. The test beam setup was composed of the Demonstrator module and two more TileCal modules instrumented with the legacy electronics.

During the test beams, the TilePPr Demonstrator was responsible for acquisition, processing of the detector data and clock distribution to the on-detector electronics.

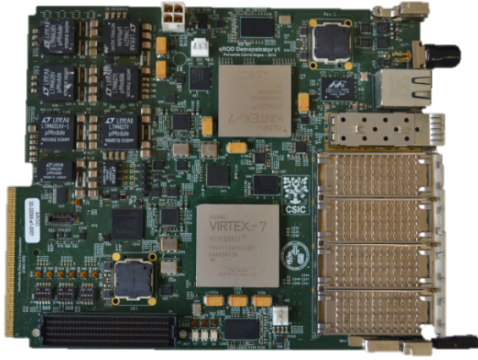


Figure 4: Picture of the Tile PreProcessor Demonstrator.

In order to continue studying the performance of the upgraded electronics, the Demonstrator module will be installed into ATLAS during the Long Shutdown 2 (end 2018-early 2021) replacing one of the current TileCal modules of the Long Barrel A.

4. Full-Size PreProcessor

The PreProcessor module envisaged for the HL-LHC is being designed as a full-size ATCA blade form factor. It is composed of an ATCA Carrier Blade Board (ACBB) and four FPGA-based Compact Processing Modules (CPM) with AMC form factor. The communication interfaces of the CPMs, TDAQi and the ATCA backplane, monitoring, configuration and power distribution are managed by the ACBB, while CPMs are populated with high-speed optical connections and FPGAs for the acquisition and processing of the data coming from the on-detector electronics. Each CPM can operate and read out up to two TileCal modules (8 mini-drawers).

4.1. ATCA Carrier Base Board

The ATCA Carrier Base Board (ACBB) is an ATCA cutaway carrier board which supports up to four single AMC boards. The high-speed communication with the on-detector electronics, data acquisition and core processing functionalities relies on the CPMs, while functionalities for power management, control and configuration of the boards are implemented in separated mezzanine cards. The use of separated boards allows the reduction of the complexity of the overall system and provides the ability to easily upgrade and replace them if necessary.

In addition to the 4 CPMs located at the AMC slots, the ACBB can host up to three mezzanine boards to extend its functionalities:

- **Tile Computer on Module (TileCoM):** This 204-pin SO-DIMM form factor board is equipped with a System-on-chip Xilinx ZYNQ FPGA running embedded Linux operating system. The main purpose of the TileCoM is the remote control and configuration of all the boards placed in

the ACBB, remote configuration of the on-detector electronics FPGAs and interface with the Detector Control System (DCS) for monitoring.

- **GbE Switch:** This mezzanine board is a 204-pin SO-DIMM form factor card populated with a Broadcom BCM5396 chip. The GbE Switch, shown in Figure 5, provides up to 16 port Gigabit Ethernet ports to provide communication between the CPM, TDAQi and TileCoM boards and with other systems in the ATCA shelf through the Fabric and Base interfaces.
- **Intelligent Platform Management Controller (IPMC):** The IPMC has been designed at CERN using a Very Low Profile DDR3-DIMM form factor and it is equipped with an Microsemi A2F200 FPGA which implements the IPMI functionalities.



Figure 5: Picture of the TileCal GbE Switch mezzanine card.

Figure 6 presents a block diagram of the ACBB showing the interconnections between the components of the ACBB and Zone 1, 2 and 3 connectors.

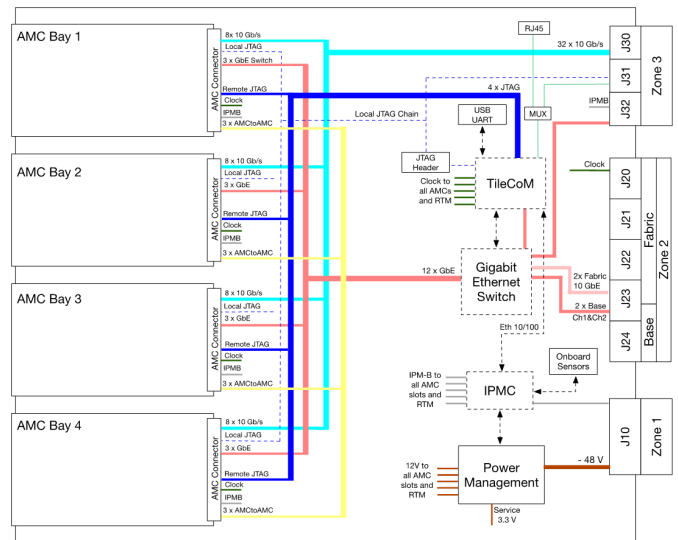


Figure 6: Block diagram of the ATCA Carrier Base Board.

The Zone 1 connector provides up to 400 W distributing -48 V to the on-board power supplies for the generation of 12 V, and it also interfaces the IPMC board with the SM. The Zone 2 connector is used to provide communication between the ATCA framework and the ACBB through two 10 GbE ports and two GbE ports connected to the GbE Switch board. Each CPM is connected to three GbE ports of the GbE Switch board and two JTAG chains controlled by the TileCoM. The first

JTAG chain is devoted for the remote or local configuration of the CPM FPGA, while the second one is used for remote programming the Daughter Board FPGAs over the fiber optic links. Finally, the Zone 3 connector provides up to 32 point-to-point connections to interface the CPMs and the TDAQi for the communication with the FELIX system and to the FPGAs in charge of the trigger processing.

4.2. Compact Processing Modules

The Compact Processing Modules is the core processing and high-speed interface of the Full-Size PPr. This single AMC board is equipped with a Xilinx UltraScale KU115 FPGA and eight Samtec FireFly optical modules connected through 32 GTH transceivers for a total bandwidth of 500 Gbps. Other 16 GTH transceivers provides a 260 Gbps interface through the backplane for the communication with the TDAQi and ACBB. A Xilinx Artix 7 35T FPGA is in charge of the slow control and monitoring of the clocking, optical modules, and power supplies of the CPM. In addition, this FPGA implements a phase monitoring module based on the OSUS circuit [7] which permits the detection of latency variations of the clock distributed towards the on-detector electronics with an accuracy of 30 ps_{RMS}.

The PCB stack-up counts 14 layers with Isola FR408HR as dielectric material which reduces the signal losses at high frequency and provides a low dielectric constant. Up to 6 layers of this PCB are used for ground and power distribution while 8 layers are dedicated to high-speed and control signals. Copper and dielectric material thicknesses has been selected to provide 100 Ohm differential impedance for signals and proper signal quality. Figure 7 shows the layout of the CPM.

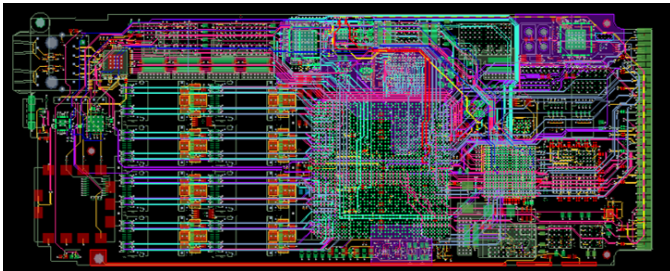


Figure 7: Layout of the Compact Processing Modules showing the internal high-speed layers.

Different studies have been done using ANSYS Electromagnetics Suite to design the high-speed lines and to improve the signal integrity of the overall design. These studies includes the optimization of differential via design to reduce the degradation of signal quality due to impedance discontinuities. Figure 8 shows the 3D via model and the Time Domain Reflectometry (TDR) results of the simulation performed for the differential via design.

The selection of the FPGA was a critical decision during the design process. The preliminary studies on the firmware resource occupancy indicates that the CPM FPGA contains enough resources to implement all the required functionalities, considering that twice number of links will be implemented.

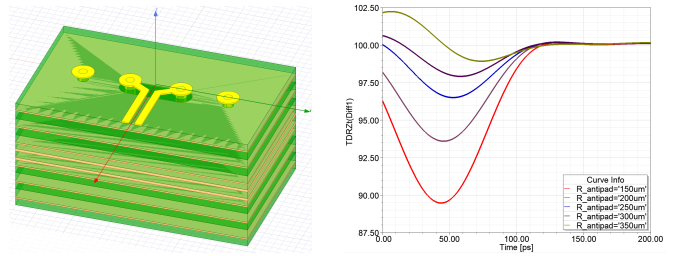


Figure 8: 3D via model and TDR results for different via anti pad radii.

Table 2 shows a comparison between the available and occupied resources of the Readout and CPM FPGAs.

| | PPr Demo VX485T | | CPM KU115 |
|-----------------|--------------------|-------|--------------|
| | Available | Used | Available |
| Slice registers | 607,200 | 17% | 1,326,720 |
| Slice LUTs | 303,600 | 29% | 663,360 |
| RAMB36E1 | 1,030 | 22.5% | 2,160 |
| CMT tiles | 14 | 28% | 24 |
| GTX/GTH | 56 | 33% | 48 |

Table 2: Comparison between the occupied and available resources for the PPr Demo and CPM FPGAs.

5. Conclusions

The new conditions of the HL-LHC motivates the complete redesign of the on- and off- detector electronics of the Tile Calorimeter.

The PreProcessors will be the core element of the off-detector electronics of TileCal after the Phase II Upgrade. The PPr system will be responsible for detector data acquisition, cell energy reconstruction and clock distribution towards the on-detector electronics. The full-size PreProcessor has been designed based on the experience gained with the design of the PPr Demonstrator and operation during test beams. The Preliminary and Final Design Review of this project are planned for Q3 2019 and Q2 2020 respectively, followed by the final production for its installation in ATLAS in 2024.

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