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# A Monolithic HV/HR-MAPS Detector with a Small Pixel Size of 50 µm x 50 µm for the ATLAS Inner Tracker Upgrade

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This paper presents a HV/HR-MAPS detector developed in the framework of the HV-CMOS collaboration for the ATLAS Inner Tracker update of the HL-LHC era. It was fabricated with a 150 nm HV-CMOS process which includes a layer to isolate the bulk of the PMOS transistors from the collecting node of the sensor. All the front-end electronics is integrated in the pixel, which is of only 50 µm x 50 µm, and include a preamplifier, shaper, discriminator and digital block with FEI3 column drain architecture.

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## 1. Introduction

The inner tracker of ATLAS will be upgraded for the High Luminosity-LHC (HL-LHC) to fulfil the requirements needed to cope with a 5-7 times increase of the luminosity with respect to the LHC phase 0 [1]. A new type of pixel detectors called High Voltage/High Resistivity-Monolithic Active Pixel Sensors (HV/HR-MAPS) is currently being considered for the outer-most (fifth) pixel layer, which at a radius of 28 cm, will have to sustain a fluence of $1.5 \times 10^{15}$ $n_{eq}/cm^2$. Several demonstrators are being developed in order to validate this technology [2].

This paper presents a small fully monolithic matrix of 3.9 mm x 2 mm in the 150 nm HV-CMOS process from LFoundry. The dies are fabricated on two wafers with different substrate resistivities of 500 Ω·cm and 1900 Ω·cm. The aim of this matrix is to demonstrate that it is possible to fabricate small pixels of only 50 µm x 50 µm with all the front-end electronics integrated inside the pixel. The electronics includes a pre-amplifier, discriminator and digital front-end stage similar to that of the FEI3 [3]. The chip is a prototype to study the LFoundry technology process, so the readout of the matrix is untriggered and unlike the FEI3 it does not include on-chip time-walk correction, buffering, and zero suppression.

## 2. Pixel cross section

The sensing diode of each pixel is the p-n junction between a deep buried n-layer (DNWELL) and the high resistivity p-substrate, see Figure 1.a. The junction is reversed biased from the top to a negative High Voltage (HV) with a p-well (PW) ring that surrounds the DNWELL. The DNWELL is connected to an n-well (NW) ring through an additional layer called NISO. A bias circuit sets the operating point of the n-well ring slightly below the bias voltage VDDA (1.8 V).

The electronics of the pixel is embedded in the DNWELL. PMOS and NMOS transistors lay in n-wells and p-wells, respectively. A buried p-type layer (PSUB) between the NW and the DNWELL avoids punch through between them. The PSUB layer allows the integration of comparators and digital gates in the pixel.These circuits generate peak currents caused by large voltage swings. If there is not the PSUB layer, these peaks may induce noise to the collecting electrode (DNWELL) and hence disturb the response of the sensor. The isolation layer is not required in analog circuits because the signals do not swing between the ground and the power supply, so no large peak currents are produced.

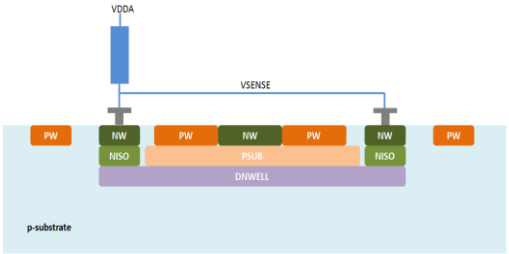


**Figure 1:** Cross-section diagram of a HV/HR-MAPS implemented with the LFoundry 150 nm HV-CMOS technology where PW is p-well, NW is n-well, DNWELL is deep n-well, and PSUB is deep p-well.

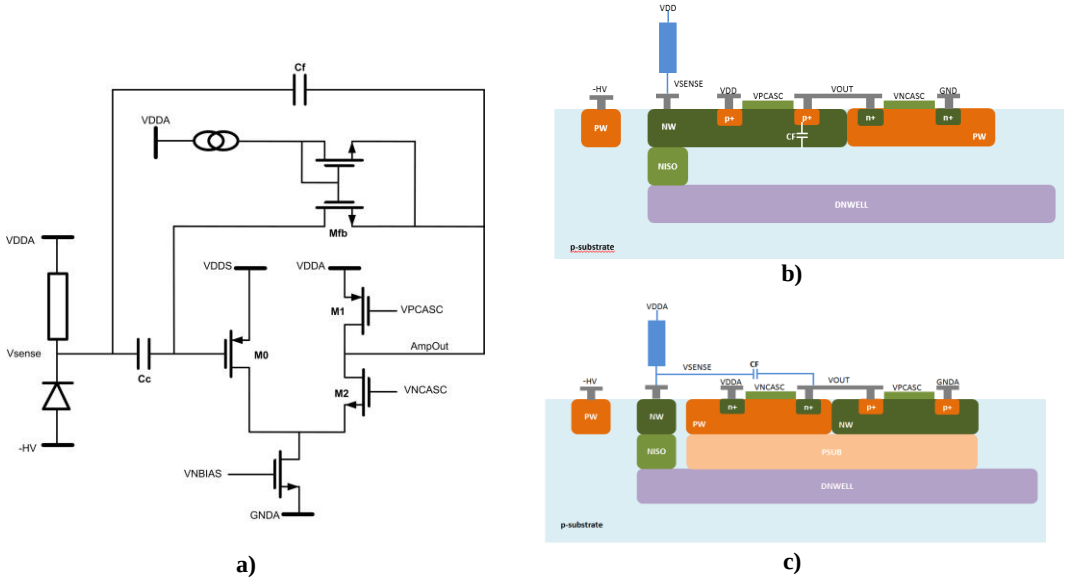


**Figure 2:** a) Schematic diagram of the preamplifier. Cross-section of transistors M1 and M0 and detector with b) a MIM feedback capacitor and c) a diffusion feedback capacitor.

The sensor is AC coupled to a Charge Sensitive Amplifier (CSA) formed by a single-ended folded cascode preamplifier, a feedback capacitor $C_f$ and an active discharging circuit as shown in Figure 2.a. Two versions of the CSA are implemented. In the first one, the bulks of the PMOS transistors of the analog front-end electronics are connected to the collecting node. The drain-bulk capacitance of the PMOS transistor of the cascode stage (M1) is the feedback capacitor $C_f$. A cross-section of the sensor with transistors M0 and M1 is shown in Figure 2.b. This is the typical approach used in HV/HR-MAPS with no isolation layer [4]. In the second version of the CSA, the bulks of the PMOS transistors of the analog front-end electronics are isolated from the DNWELL, Figure 2.c. In this case, $C_f$ is a Metal-Insulator-Metal (MIM) capacitor. Its value is chosen to be as close as possible to that of the feedback capacitor implemented via transistor diffusion to compare both approaches. This value is 1.8 fF. To make the analog front-end more radiation tolerant, an additional sub-version of each pixel flavour with enclosed NMOS transistors is implemented. The final matrix has 4 different pixel flavours.

## 3. Analog and digital on-pixel front end electronics

A block diagram of the in-pixel electronics is shown in Figure 3. The analog stage is composed of bias circuit, preamplifier, shaper and discriminator. The function of the shaper is not only to limit the noise of the signal, but also to set a different Base Line (*BL*) for the discriminator and reduce the threshold mismatch. The output of the shaper (*HpOut*) is continuously compared to a global reference threshold level *VTh*. A local 4-bit DAC allows to fine-tune the threshold level to compensate the input offset voltage of the discriminator. The pixel includes a 4-bit SRAM to store the trimming value. The output of the discriminator (*CompOut*) is processed by the digital stage. An edge detector monitors *CompOut*. When it detects a leading edge, it asserts the *LE* signal, and the Time-Stamp (*TS*) corresponding to this event is stored into an 8-bit DRAM memory. When the tailing edge is reached, it asserts the *TE* signal and the TS corresponding to that event is stored into a second 8-bit DRAM. Simultaneously, a hit flag is also asserted and any new event can be processed

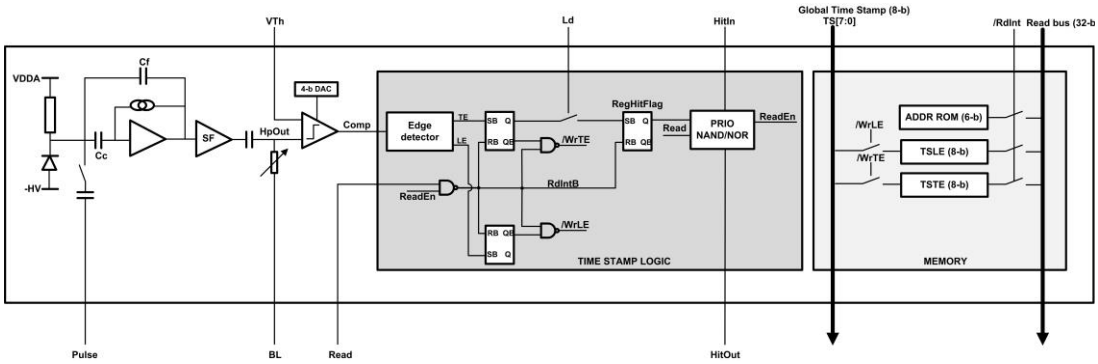


**Figure 3:** Block diagram of the in-pixel electronics.

until the pixel has been read out. The pixel has an 8-bit hardwired address. The data stored in these three memory elements is read through a 24-bit bus. The pixel receives an 8-bit gray-encoded TS generated at the periphery of the chip.

Each pixel has a hit flag *HitOut* that propagates to an End Of Column (EOC) circuit through a priority NAND-NOR chain. The value of this flag depends on the status of the hit register and the value of the hit flag from the previous pixel. *HitOut* is only deasserted when all the hit flags from the previous pixels are inactive and no hit is detected in the current pixel. This means that the pixel cannot be read out until the hit pixels in the same column with higher priority have already been read out.

## 4. Matrix

Figure 4 shows the floorplan of the matrix. Its size is 5 mm x 2.5 mm and most of its area is occupied by a matrix of HR/HV-MAPS pixels with 40 rows and 78 columns. The matrix has four different pixel flavours, which are arranged in 4 different sub-matrices with 40 rows x 20 columns of pixels in two of them and with 40 rows x 19 columns of pixels in the other two. Vertical and horizontal configuration registers to program the pixels are placed at the left and bottom of the pixel matrix. These registers are connected in series and accessed through a low speed serial interface. A control unit manages the readout of the matrix.

The architecture of the Read Out Cell (ROC) is column drain. The stored LE and TE time-stamp together with the address are accessed through a 24-bit bus shared by all the pixels in a

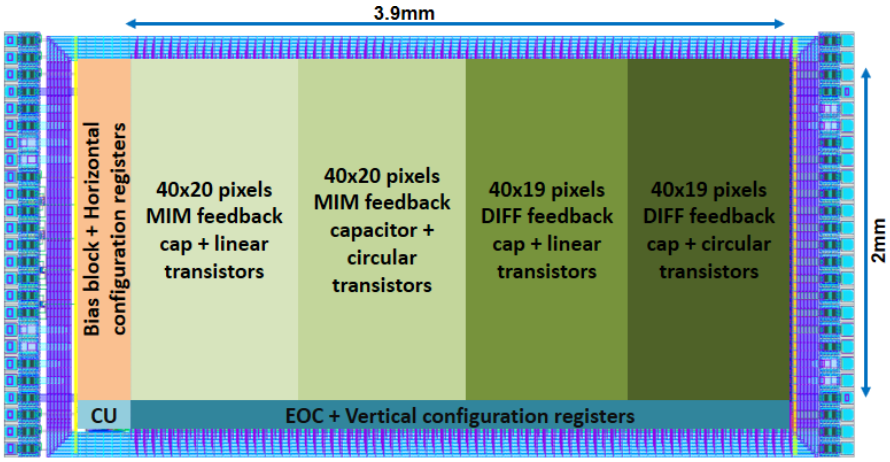


**Figure 4:** Layout of the chip.

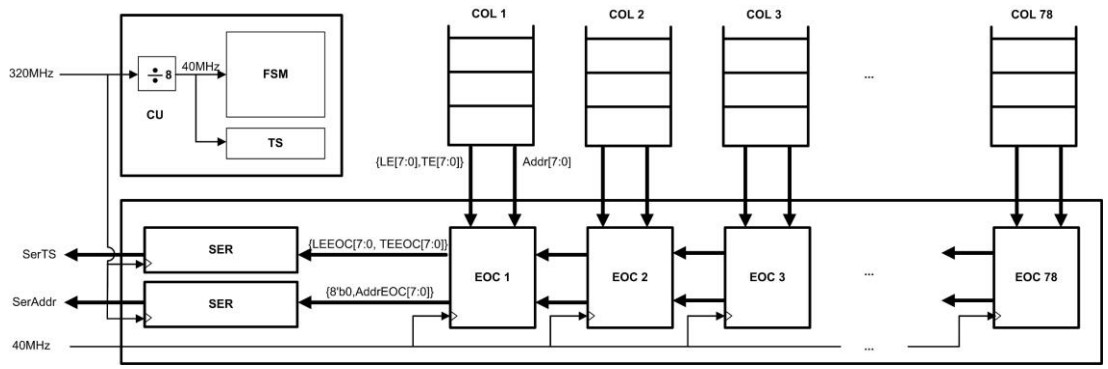


**Figure 5:** Block diagram of the readout electronics.

column. The bus lines are terminated with pull down transistors placed at the EOC cell. This stores the information into two 16-bit registers with parallel read/write capabilities. The EOCs are connected in such a way that form a 24-bit parallel shift register of 78 cells as show in Figure 5. The two 16-bit outputs of each shit register are connected to two serializers.

The readout process of the matrix is handled by a control unit. It receives a 320 MHz external clock which is fed to the two serializers and a clock divider. The latter generates a 40 MHz clock, which is used to read the matrix out. The control unit has an 8-bit time stamp generator and a finite state machine that produces all the control signals for the readout. It executes an infinite loop with two steps. In the first one, the address and time-stamp of the pixel with asserted hit flag and highest priority in the column are stored in the EOC. If there is no hit in the column, the EOC cell stores zeros. This step is carried out in one clock cycle (40 MHz). In the second step, the data stored in the EOC cells is shifted and serialized. When the content of the 78th EOC is being serialized, new data is stored in the EOC starting the loop again.

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