PROCEEDINGS OF SCIENCE

Investigations into the effect of gamma irradiation on the leakage current of 130-nm readout chips for the ATLAS ITk strip detector

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Central to the design of any detector system is a detailed understanding of the current and power dissipation due to the implications on power-supply design, thermal management and mechanical stability. It is well documented that certain 130-nm CMOS technologies exhibit an increase in the leakage current when exposed to ionising radiation. Such 130-nm technology is employed in the readout ASICs of the ATLAS ITk Strip Tracker Upgrade. Using the so-called *ABC130* prototype chipset, measurements are presented which allow the parametrisation of the increase in current as a function of dose rate in the region of phase space most applicable to High-Luminosity LHC conditions. Studies investigating the batch-by-batch, chip-by-chip and wafer-by-wafer variation of the total current increase are presented which demonstrate a significant batch-by-batch variation alongside non-negligible variations within wafers. Furthermore, studies are shown investigating the long-term annealing of irradiated chips (up to four months storing chips at 80 °C). Finally, the feasibility of pre-irradiating wafers to mitigate the current increase is demonstrated.

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1. Introduction

Starting in 2026, the CERN Large Hadron Collider (LHC) will enter a new phase called the High Luminosity LHC (HL-HLC), which will see its luminosity increased by an order of magnitude to $\mathscr{L} = 10^{35}$ cm^{-2}s^{-1}. To meet the challenges coming from a far busier environment during the proton-proton collisions, with a mean number of 200 collisions per bunch crossing [1], the ATLAS detector will receive upgrades to all of its sub-systems.

The innermost part of the ATLAS detector, currently called the *Inner Detector*, will be replaced by an all-silicon detector referred to as the *Inner Tracker* (ITk). The ITk will comprise five layers of pixel modules surrounded by four layers of strip modules [2].

The readout chips of the ITk strip detector are manufactured in a 130-nm process (*Global-Foundries CMOS 8RF*), and it is well known [3, 4, 5] that the transistors in such devices exhibit an increase in leakage current under ionising radiation. Understanding these *Total Ionising Dose* (TID) effects is crucial in planning the power-supply and thermal management, as well as the structural integrity of the ITk. Measurements of a prototype-chipset irradiation campaign are presented which will facilitate the parametrisation of these effects as a function of the dose rate of the ionising radiation.

2. Background

The silicon strip modules comprising the outer ITk layers are composed of individual *n-in-p* sensors of size 10×10 cm^2, and are each read out by a front-end *Application-Specific Integrated Circuit* (ASIC), a *Hybrid Controller Chip* (HCC), and an *End-of-Substructure* (EoS) card based on the *CERN LpGBT ASIC*. This work is concerned with a prototype version of the front-end ASICs known as *ATLAS Binary Chip 130* (ABC130). Charged particles ionise the silicon creating electron-hole pairs. These drift in the silicon's electric field creating a drift current that is read out by the front-end ASIC. The ABC130 is designed to simultaneously read out two rows of 128 strips each. The final upgrade will implement a version of the ASIC known as ABCStar [6].

Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits with manufacturing nodes below 250 nm generally employ a technique to reduce leakage current between adjacent device components known as *Shallow Trench Isolation* (STI). There are two radiation-damage effects which influence the leakage current in devices using STI: In the first effect, positive charges are trapped in the STI, and can form a *parasitic channel* allowing leakage current to flow, even in the absence of a gate voltage. In the second effect, which takes place more slowly, negative charges build up at the Si-SiO_2 interface, and act to reduce the leakage current. The combination of the two effects leads to a characteristic bump shape with a sharp increase followed by a slow decrease in leakage current.

The observable of interest is the *Current-Increase Ratio* (CIR) as a function of accumulated dose, which is defined as the ratio of the measured current during irradiation to the baseline current in the unirradiated device.

3. Experimental setup

The experimental setup at the Rutherford Appleton Laboratory (RAL) comprised an X-ray machine, single-chip test cards hosting the ABC130s, and a moveable stage on which an irradiation

box was mounted. The ABC130s were thermally coupled to an aluminium strip to which a *Negative Temperature Coefficient* (NTC) thermistor was attached.

Previous irradiations have been performed at dose rates and temperatures that are compatible with ITk conditions in an HL-LHC environment [2, 7, 8]. Here, higher-rate and higher-temperature measurements are performed to maximise the available statistics. The irradiations were performed using a *Seifert RP149*-type X-ray system equipped with a tungsten target. The tube was operated at a voltage 60 kV and a current of 3 to 50 mA to yield dose rates between 47 to 780 krad/h. It should be noted that the systematic uncertainty in dose rate of 15% across the chip area affects all measurements equally due to their identical placement in the beam spot.

4. Results

This section demonstrates variations in the TID effects between different batches, wafers, and chips. The *wafers* delivered by the semiconductor plant (*GlobalFoundries*) each contain 130 ABC130 *chips*. A *batch* refers to a series of wafers produced in the same manufacturing window. The batches considered here are called *batch 1, 2* and *3*, and comprised 6, 24 and 48 wafers, respectively.

In order to demonstrate an in-wafer variation, nine chips from a single batch-2 wafer were selected for irradiation so as to sample the wafer across its surface. An equivalent selection was made for two batch-3 wafers in order to assess the batch-by-batch variation. The wafer-by-wafer variation was investigated using central-wafer chips (chip no. `065`) from batches 1, 2 and 3. The irradiations performed to assess the batch-by-batch variation are summarised in Figure 1, and reveal a significant difference in the maximum CIR between batches. Batch 2 has an average maximum CIR of 6.8 ± 0.4 while that of batch 3 is 5.2 ± 0.4 (the single batch-1 measurement is batch 3-like).

The measurements assessing the chip-by-chip variation are presented in Figure 2. The position of each data point reflects its approximate location on the physical wafer. The agreement between wafers is high in the first two quadrants[1] of the wafers, whereas the third and fourth quadrants show stronger disagreement. It is noteworthy that while one batch-3 wafer shows a large variation of the magnitude of the effect (middle map in Figure 2), the distribution of maximum CIRs is much more uniform on another wafer from the same batch (rightmost map in Figure 2).

4.1 Basis for a global model

A major aspect of this study is to serve as input into a global[2] description of the TID effects. To this end, the results shown above for chip `065` (Figure 1) are combined with previous measurements performed at different dose rates and temperatures at Brookhaven National Laboratory (BNL) and CERN[3].

The simplest description of the physically relevant aspects of the TID effects only contains two parameters - the peak height and the peak position in accumulated dose. The peak position in dose was found to not depend significantly on dose rate and temperature, with a mean accumulated dose of 0.79 ± 0.04 Mrad at the maximum CIR. Figure 3 shows that the maximum CIR increases

[1] A Cartesian quadrant-numbering scheme is assumed, where the quadrant spanned by the positive x-axis and the positive y-axis is quadrant 1, and the labels increment in the anticlockwise direction.

[2] *Global* here refers to a description of the effect at arbitrary dose rates and temperatures.

[3] Carried out by collaborators from the University of Toronto.

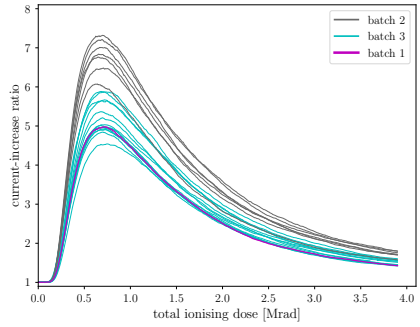

Figure 1: CIR as a function of dose for mid-wafer irradiations from batches 1, 2 and 3.

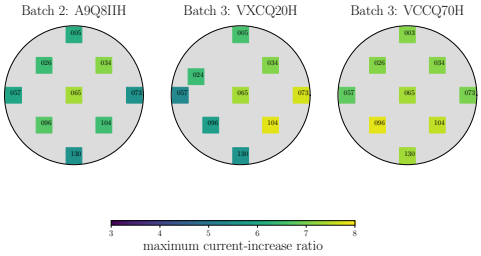

Figure 2: Wafer maps of TID peaks for batch 2 (left) and 3 (middle and right). The maps are normalised such that all central-wafer chips (`065`) are equal in magnitude.

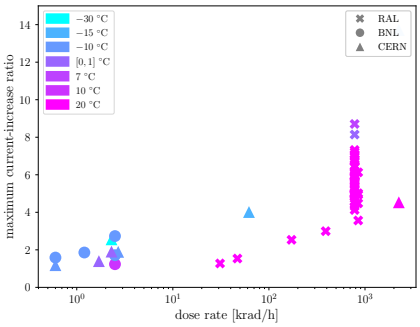

Figure 3: Maximum CIR as a function of dose rate for 48 irradiations.

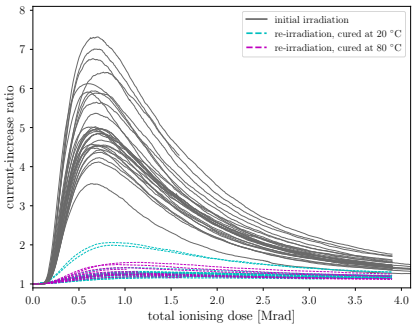

Figure 4: Current-increase ratio vs. dose for 29 initial ABC130 irradiations (solid), and their re-irradiations (dashed) after curing at 20 °C (cyan) and 80 °C (magenta).

with higher dose rates. Note that within these results there is significant variation in chip position, batch and wafer.

4.2 Annealing and pre-irradiation

Annealing denotes the recombination of silicon defects due to thermal diffusion. 29 chips previously irradiated were chosen for re-irradiation, 19 of which have been left, unpowered, at room temperature in a dry cupboard between 5 and 310 days, and 10 of which were left in an oven at 80 °C. The annealing studies in the two temperature regimes are summarised in Figure 4. The CIR curves at re-irradiation (dashed lines) do not vary noticeably as a function of annealing temperature, which leads to the assumption that long-term annealing is not significant on the time-scales and temperatures probed here. One hypothesis is that the maximum CIR at re-irradiation is similar to the value of the CIR at the end of the initial irradiation. The ratio of these two quantities, i.e. the *current-increase peak-tail ratio*, is plotted in Figure 5, which shows that after sufficient curing time, the maximum CIR at re-irradiation approaches the CIR at the end of the initial irradiation (indicated by a current-increase peak-tail ratio of 1). It is conceivable that instantaneous annealing during the irradiation leads to the dose-rate dependence of the maximum CIR (c.f. Figure 3), while long-term annealing is not measurable.

The feasibility of pre-irradiation is demonstrated in Figure 6, which shows that the TID effects after pre-irradiation to 8 Mrad[4] are significantly reduced as compared with an initial irradiation of a chip from the same wafer.

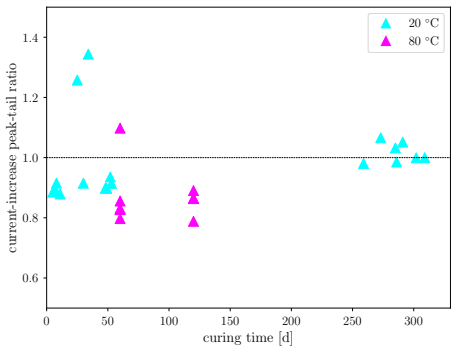

Figure 5: Ratio of the peak at re-irradiation to the value of the CIR at the end of the initial irradiation for the same 29 chips.

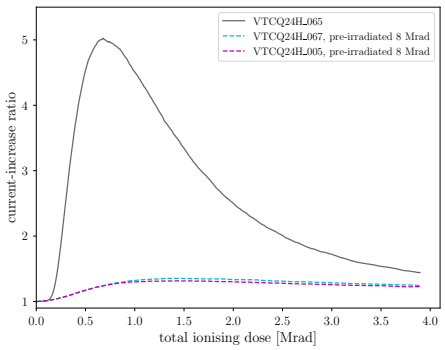

Figure 6: Two re-irradiations of chips that have been pre-irradiated to 8 Mrad (dashed), and an initial irradiation from the same wafer (solid).

5. Conclusion

Manufactured using 130-nm CMOS technology, the front-end readout ASICs for the ATLAS ITk exhibit TID effects characterised by an increase in leakage current, the understanding of which these proceedings aimed to further. There are significant variations in the magnitude of the effects between different batches, and non-negligible variations within batches and wafers. The effect of annealing at room temperature and at 80 °C is not significant. Pre-irradiation of wafers to 8 Mrad may be a feasible way of mitigating the TID effects, but further investigation is ongoing to ensure that long-term powering or storage does not lead to recurrence of the TID peak at full height.

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