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Effects of Ultra-High Total Ionizing Dose in Nanoscale Bulk CMOS Technologies

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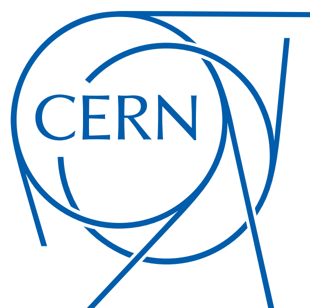

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Effects of Ultra-High Total Ionizing Dose in Nanoscale Bulk CMOS Technologies

Qualification of commercial CMOS technologies

Henri Koch

Abstract

Particle accelerators are an excellent instrument to investigate at the smallest scale in our universe. The last breakthrough was made by the Large Hadron Collider (LHC) with the observation of the Higgs boson (2012) at CERN. A future upgrade of the particle accelerator, called High-Luminosity Large Hadron Collider (HL-LHC), is planned to increase its potential for new discoveries in particle physics. The upgrade will produce a ten-fold increase in luminosity resulting in a significant increase in the number of collisions in the various detectors distributed along the particle accelerator. The higher number of collisions will increase the amount of interesting events for particle physicists. However, the important increase of particle collisions will result in an unprecedented level of radiation in the detectors. This high radiation level is a concern for the electronics in the detectors as radiation damages the transistors. The integrated energy deposited by ionizing radiation, called total ionizing dose (TID), exceeds by several orders of magnitude the typical requirements for the main concerned industry, space (hundreds of Mrad(SiO_2) vs. hundreds of krad(SiO_2)). CERN developed the tools and knowledge to design radiation hardened application specific integrated circuits (ASICs) by characterizing the radiation response of selected commercial technologies and using hardening-by-design (HBD) techniques.

The characterization to total ionizing dose (TID) of the 65 nm CMOS technology used in the development of ASICs for the High-Luminosity Large Hadron Collider (HL-LHC) was realized. The characterization was performed within the temperature range of interest (−30 °C, 0 °C and 25 °C) up to 500 Mrad(SiO_2). The different degradation mechanisms have been outlined. The data are used to create models that will allow integrated circuit (IC) designers to directly simulate the impact of total ionizing dose (TID) during the design of the ASICs. Four publications IEEE conference have been published based on the measurement performed during this work. In addition to these measurements, the radiation response of different foundries have been study in 65 nm. We showed that the effects known as Radiation-Induced Narrow Channel Effects (RINCEs) and Radiation-Induced Short Channel Effects (RISCEs) are also observed in at least three different foundries, which increases our confidence in the universality of the mechanisms.

The study of total ionizing dose effects in two smaller technological nodes began, namely 40 nm and 28 nm CMOS technologies, from different foundries in order to investigate the next viable technology.

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To the memory of Pierre Aubry

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List of Acronyms

ALICE A Large Ion Collider Experiment.

ASIC application specific integrated circuit.

ATLAS A Toroidal LHC ApparatuS.

BX bunch crossing.

CERN Conseil Européen pour la Recherche Nucléaire.

CLIC Compact Linear Collider.

CMOS complementary metal-oxide semiconductor.

CMS Compact Muon Solenoid.

CTRW continuous time random walk.

CVU capacitance voltage unit.

DD displacement damage.

DG Director-General.

DUT device under test.

ESD electrostatic discharge.

ESE Electronics Systems for Experiments.

FCC Future Cicular Collider.

FinFet fin field-effect transistor.

GaaFet gate all-around field-effect transistor.

HBD hardening-by-design.

HEP High Energy Physics.

HL-LHC High-Luminosity Large Hadron Collider.

IC integrated circuit.

ITRS International Technology Roadmap for Semiconductors.

LDD lightly doped drain.

LEP Large Electron-Positron Collider.

LHC Large Hadron Collider.

LHCb Large Hadron Collider beauty.

LOCOS LOCal Oxidation of Silicon.

MOS metal-oxide semiconductor.

MOSFET metal-oxide semiconductor field-effect transistor.

nMOS n-type metal-oxide semiconductor.

PIN positive intrinsic negative.

pMOS p-type metal-oxide semiconductor.

PS Proton Synchrotron.

RINCE Radiation-Induced Narrow Channel Effect.

RISCE Radiation-Induced Short Channel Effect.

SEB single event burnout.

SEE single event effect.

SEGR single event gate rupture.

SEL single event latchup.

SEU single event upset.

SMU source measure unit.

SPS Super Proton Synchrotron.

STI Shallow Trench Isolation.

TEM transmission electron microscopy.

TID total ionizing dose.

Introduction

In 1962, the United States of America conducted several high-altitude nuclear tests from Johnston Atoll near Hawaï known as the operation Starfish Prime [1]. The main and unwanted aftereffect of this operation was the creation of radiation belts of MeV electrons around the Earth [2] that caused the first loss of a spacecraft, the satellite Telstar 1 [Web1], due to ionizing radiation-induced effects in on board semiconductor devices [3].

Radiation jeopardizes the reliability of electronic components that are now used in many applications. The first-line industry is the space industry where satellites have to survive in a harsh environment, exposed to solar winds, cosmic rays or to the Van Allen radiation belt. When particles enter the atmosphere they generate new particles in cascades. The radiation level increases with altitude [Web2] and so the avionics industry also has to face electronics reliability. At terrestrial altitude, the radiation level was often neglected but it is no more the case in advanced technologies, e.g. used in the memories [4]. The nuclear industry has also to address this problem [5] but it is not deeply affected as limited number of electronic components are exposed to radioactive area. However, it will not be the case for future thermonuclear fusion reactors where the plasma needs to be monitored and will produce a very high level of radiation [6].

High Energy Physics (HEP) accelerators and in particular the Large Hadron Collider (LHC) at CERN are now using more and more electronics in their experiments that are subjected to unprecedented radiation level [7]. The harsh radiation environment is created by the high particle collisions rate inside the detectors in which the electronics must continue to operate correctly. The integrated energy deposited by ionizing particles, called total ionizing dose (TID), exceeds by several orders of magnitude the typical requirements for space applications (hundreds of Mrad(SiO_2)[1] vs. hundreds of krad(SiO_2)) [8].

The development of a qualified radiation-hard state-of-the-art semiconductor technology requires an investment in multi-billion-dollar range [Web3]. Therefore, CERN chose another strategy to develop application specific integrated circuits (ASICs) based on the use of commercial CMOS technologies. CERN developed the tools and knowledge to design radiation hardened ASICs by characterizing the radiation response of selected commercial technologies and using hardening-by-design (HBD) techniques.

Since its creation, CERN has been challenging the field of research in particle physics. The latest breakthrough was done in 2012 with the observation of the Higgs boson with the ATLAS and CMS detectors [9, 10]. Now CERN's scientists want to go beyond the Standard Model of particle physics (New Physics) [Web4], looking after dark matter [Web5] and extra dimensions [Web6]. These investigations at the smallest scale of our universe are possible thanks to particle accelerators.

[1]The rad is a unit to express the radiation absorbed dose still used by the semiconductor radiation community. The SI unit is the gray (Gy). The conversion is given by $1\,\text{rad} = 0.01\,\text{Gy} = 0.01\,\text{J}\,\text{kg}^{-1}$. We will see later also that we need to express TID in a given material, here silicon dioxide (SiO_2).

The Large Hadron Collider and its Experiments

The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator in the world with a ring of 27 km buried 100 m underground at the Franco-Swiss border [11]. The Large Hadron Collider (LHC) was launched in 2008 replacing the Large Electron-Positron Collider (LEP) accelerator and its development cost makes it the most expensive scientific experience in the world, around 9 billion euros [11].

Figure 1 illustrates the whole accelerator complex of CERN. There are several machines that accelerate particles with an increasing energy. The LHC is represented by the biggest red circle with the four main experiments (ATLAS, CMS, ALICE and LHCb) spread along its circumference. Two kinds of particles can be injected in the particle accelerators, protons and ions. Before being injected in the LHC, the particles are progressively accelerated through the two old, growing in size, accelerators: the Proton Synchrotron followed by the Super Proton Synchrotron. The particles are then injected in the Large Hadron Collider. Two beams of particles flow in opposite direction and are accelerated to reach 7 TeV and collided at different experiments with a total energy of 14 TeV. A strong magnetic field is applied (8.6 T) to generate a force in order to bend the trajectory of the particles in a circular motion. The particles are accelerated thanks to RF cavities placed along the LHC. When a bunch of particles crosses the cavities, the radio waves exchange with the bunch of particles some energy and push them forward [12].

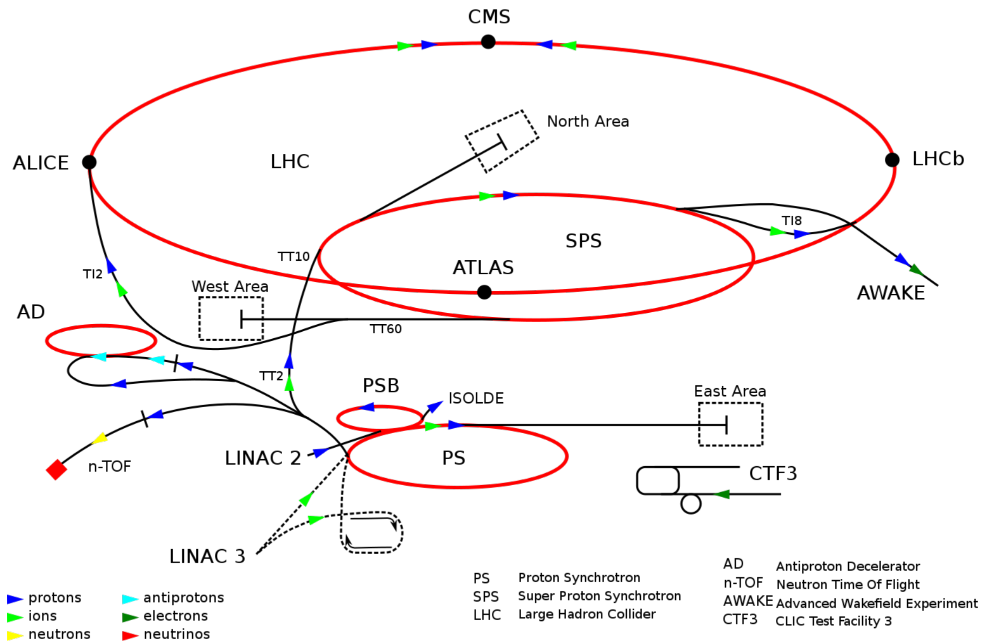


Figure 1: *Overview of the CERN accelerator complex. The Large Hadron Collider (LHC) corresponds to the largest red circle with the four experiments distributed around its contour (ATLAS, CMS, LHCb and ALICE) [Web7].*

While the experiments ALICE and LHCb are dedicated to the study of specific tasks, ATLAS and CMS are two experiments of the same type. They are both general purpose detectors built to search for supersymmetry and exotic particles and to study the Higgs boson.

A slice of the CMS detector is presented in Figure 2 [13]. The experiment is composed of several different layers dedicated to particle detection [14]. The innermost part is made up of a silicon tracker allowing to record particles trajectory. The calorimeters give the energy of the particles. Finally, the outermost part consists of the iron return yoke interspersed with the muon chambers. It consists of a thick layer of iron, filtering the particles by interacting except the muons which can penetrate several meters, and the chambers that are able to detect muons [14].

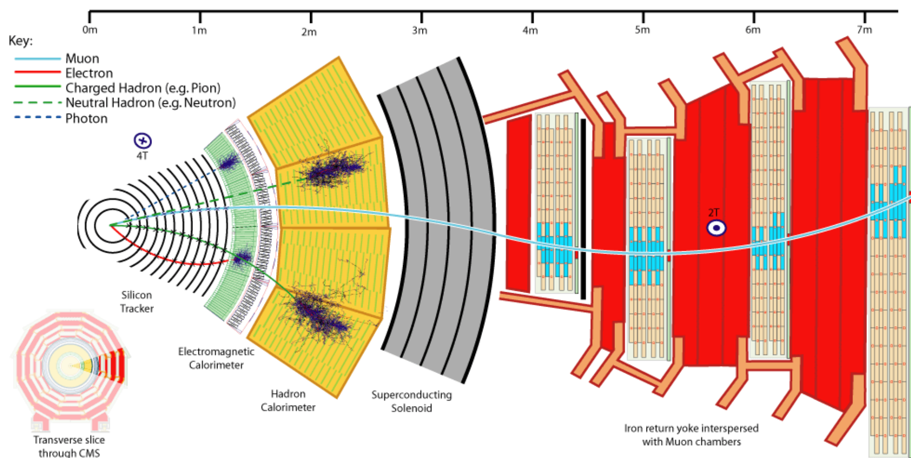


FIGURE 2: *Slice of the CMS detector [13]. Each layer of the experiment has a dedicated purpose for particle detection.*

High-Luminosity Large Hadron Collider (HL-LHC)

Two beams are injected inside the LHC, circulating in opposite direction, each beam contains approximately 2800 bunches of protons. There are 10^{11} protons per bunch. When the protons have reached the nominal energy, the bunch of protons are collided. This event is called bunch crossing (BX) and it happens at a 40 MHz rate in the detectors [15].

The luminosity $\mathcal{L}$ is a major parameter that characterizes particle accelerators. It is a measurement proportional to the number of collisions produced in a detector per cm^2 per second. Equation 1 yields some parameters showing its dependency on the number of protons in each bunch N, the collision rate f and the effective collision surface S_{eff}.

$$\mathcal{L} \approx \frac{f \cdot N^2}{S_{\text{eff}}} \tag{1}$$

Between each run of the LHC, the luminosity increases steadily and with it the quantity of interesting events to process. The instantaneous luminosity of the LHC has reached a new record at the value of $2.06 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$ in November 2017 [Web8]. The time-integration of the luminosity is hence proportional to the number of collisions and is usually expressed in inverse femtobarn ($\mathrm{fb^{-1}}$). The increase in the luminosity will increase the production of interesting events such as for example the Higgs boson which is now produced at about 20 000 per day [Web9]. The expected integrated-luminosity for the LHC is about $300\,\mathrm{fb^{-1}}$ while the value for HL-LHC will be of $3000\,\mathrm{fb^{-1}}$ [16].

This ten-fold increase in the number of collisions will create an unprecedented level of radiation, while the electronics inside the detectors must continue to operate properly. Therefore, radiation hard ASICs are designed to cope with this harsh environment. Two types of effects are present: cumulative effects (total ionizing dose and displacement damage) or transient effects (single event effects). The subject of this master's thesis focus on total ionizing dose whose accumulated level is several order of magnitude higher than in space applications. Figure 3 shows the simulation of the spatial TID distribution in the CMS detector for the HL-LHC ($3000\,\mathrm{fb^{-1}}$). The expected TID will be of 10 MGy (1 Grad).

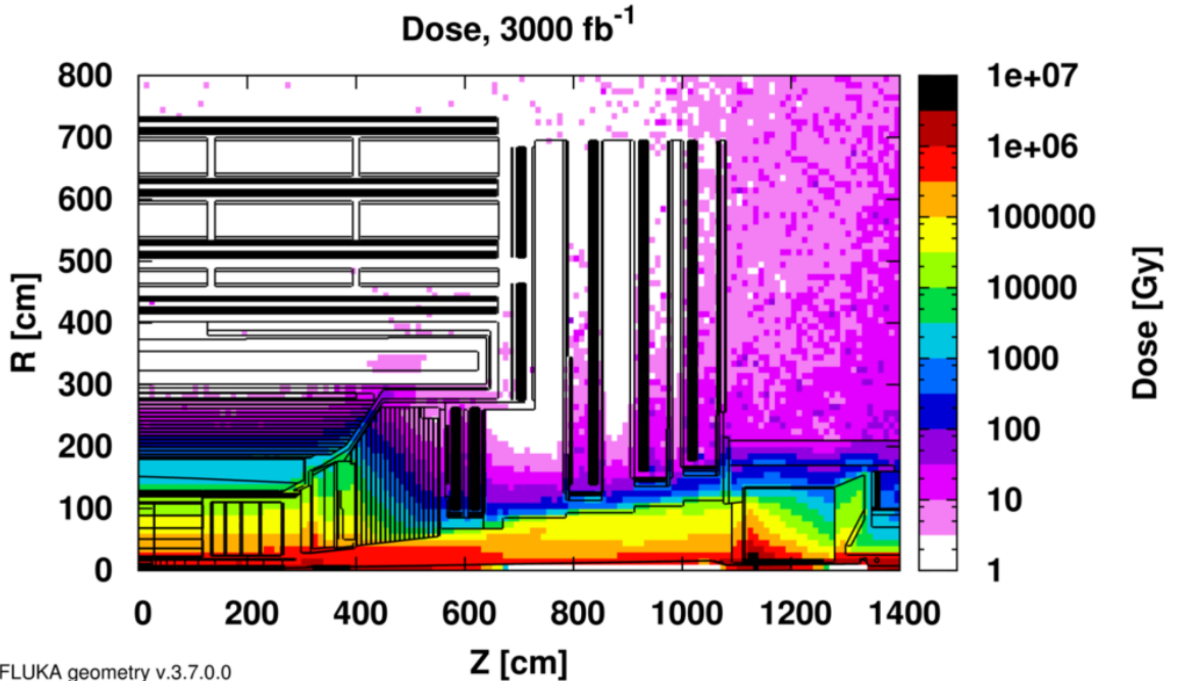


FIGURE 3: *Simulation of the total ionizing dose (TID) spatial distribution in CMS cavern expressed in* Gy *for a integrated luminosity of* $3000\,\mathrm{fb^{-1}}$ *[17, 18]. R is the transverse distance from the beam and Z is the distance alongside the beam from the collision point* ($Z = 0$ *and* $R = 0$)*.*

Master's Thesis Outline

The research work of this thesis focuses on the characterization of different commercial CMOS nodes with total ionizing dose (TID). Single transistors of different size, shape and type from the interested technologies are directly embedded on an ASIC in test structures and irradiated up to a relevant TID, typically between 200 Mrad(SiO_2) and 1 Grad(SiO_2), while measuring the evolution of transistors electrical properties. Measurements are typically current-voltage characteristics from which typical features are extracted, e.g. threshold voltage, subthreshold swing or maximum drain current. The results are compared to the current state-of-the-art knowledge to provide an interpretation of the physical mechanisms responsible for the observed degradation. Therefore, this research envisages a fundamental study of the physical mechanisms that govern the behavior of transistors exposed to ionizing radiation.

Figure 4 shows the impact of TID up to 1 Grad(SiO_2) in one of the transistor features, here it is the maximum current flowing through the transistor when it is turn on. The degradation is important and at 1 Grad(SiO_2): the p-channel transistor completely ceases to work while the n-channel transistor has reduced by more than half its current. The maximum drain current is only one parameter extracted from the whole characteristic. The complete behavior of the transistor is tremendously affected by the accumulation of ionizing radiation. Hence, the impact of TID in transistors is a major concern and the study of these effects helps the IC designers to anticipate and compensate the degradation.

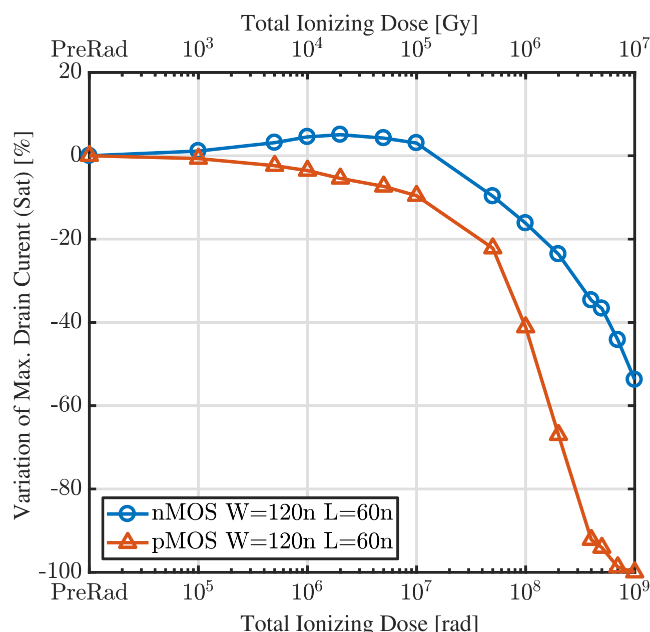


FIGURE 4: *Variation of the maximum drain current in minimum size transistors (p- and n-channels) for a* 65 nm *technology during an irradiation performed at* 25 °C *up to* 1 Grad*(SiO_2).*

The main contribution of this master's thesis is the characterization of the 65 nm technology currently used at CERN for the development of ASICs for the HL-LHC (a 130 nm technology is also used and already qualified [19]). The characterization involved the measurement of different transistors issued from the considered technology and the understanding of the underlying observed behavior. The measurements have been performed at CERN and lasted 6 months (November-April). The data obtained are used to model the degradation of the transistors electrical properties for three different TID values (100 Mrad, 200 Mrad and 500 Mrad). The creation of the models has been outsourced to the Technical University of Crete (TUC). So far, four publications in IEEE conference have been published based on the 65 nm measurements [20, 21, 22, 23]. The characterization of smaller technological CMOS processes has begun, namely 28 nm and 40 nm technologies, to investigate a potential replacement for the currently used technologies.

In chapter 1 (*CMOS Technology*), we will briefly review the basics of semiconductor physics applied to metal-oxide semiconductor field-effect transistors (MOSFETs), required to understand the content of this master's thesis.

The chapter 2, *Total Ionizing Dose Effects in MOS*, gives a detailed view of the physical mechanisms responsible for the degradation of the electrical properties of transistors caused by ionizing radiation in oxides. Before going into the detail of ionizing radiation effects, we will discuss the different radiation-induced effects, non-related in particular to ionizing radiation, that affect electronic component in general.

The chapter 3 called *Experimental Setup* provides the information about the experimental details, the irradiation facilities, the way the experiment parameters are controlled such as temperature and the equipment used to perform measurements.

The chapter 4 (65 nm *Bulk CMOS Technology Qualification to Total Ionizing Dose*) presents the data measured for the creation of the model in the 65 nm technology. We outline the different effects that take place in modern technologies in the range of TID expected for the particle accelerator upgrade.

In chapter 5 (*Study of TID Effects in Advanced Nodes*), we show the first measurement performed in smaller technologies (28 nm and 40 nm). We will present the performance against ionizing radiation in terms of degradation.

Finally, a conclusion reviews the work accomplished during the master's thesis and establishes a short and long term perspective for the future of CMOS technologies exposed to ultra-high total ionizing dose.

In addition to the main subject of this thesis, the interested reader can find in appendices a detailed chapter of interesting historical details about CERN (Appendix A). In appendix B, some radiation effects which are not yet fully understood are described.

Chapter 1

CMOS Technology

The complementary metal-oxide semiconductor (CMOS) technology is composed by two different transistors differentiated by the type of carriers flowing in their channel. The operating principle of transistors is based on semiconductor physics where the main material is silicon (Si). We will briefly review some basics of semiconductor physics as well as some important parameters of MOSFETs.

1.1 Semiconductor Physics

The current flowing in semiconductors can be created by two types of carriers: electrons (negatively charged) and holes (positively charged). In an intrinsic semiconductor, the number of electrons and holes are equal. In a extrinsic semiconductor, the process of implantation of impurities, called doping, allows to modify the balance between both carriers. In n-doped silicon, we have more electrons in the valance band due to the presence of electron donors (5 electrons in the valence band) as impurities. In p-doped silicon, the impurities are acceptors of electrons (3 electrons in the valance band) and therefore leave an empty place in the valance band called hole (absence of electron). This empty place in the valance band should normally balanced the positive charge of the nuclei, the absence of an electron leaves therefore a positive net charge at the hole location. The electrons surrounding the valence band can move to this empty position, leaving behind a positive charge, this process moves the hole in the valence band in the same way that electrons move in the conductive band. Thus, the holes can be considered as positive moving charges. Transistors are build thanks to n- and p-doped silicon.

For n-channel MOSFETs (Figure 1.1 left), also called n-type metal-oxide semiconductor (nMOS), there are three main terminals: the gate (G), the source (S) and the drain (D). The gate is a piece on metal build on top of an oxide which is in most of the commercial technologies silicon dioxide SiO_2. The gate allows to control the flow of charges from the source to the drain. When the gate voltage increases, the holes contains in the p-substrate are repelled leaving an area underneath the gate called depletion region where no mobile charge are present. A further increase of the gate voltage starts to attract electrons close to the gate forming a conductive path between the source and the drain called inversion layer. This inversion layer forms what is called the channel of the transistor. If a difference of potential is applied between source and drain, a current flows. As we will see later, the current flowing in the transistor depends on many parameters. These explanations picture in a very simplified way the behavior of a nMOS transistor because many complex phenomena are left out for the sake of simplicity.

In p-channel MOSFETs or p-type metal-oxide semiconductor (pMOS), the principle is the same but the carriers are holes. We apply a negative voltage to the gate of the pMOS which will repelled the electrons of the n-well and when the gate voltage becomes sufficiently negative, holes start to be attracted near the gate

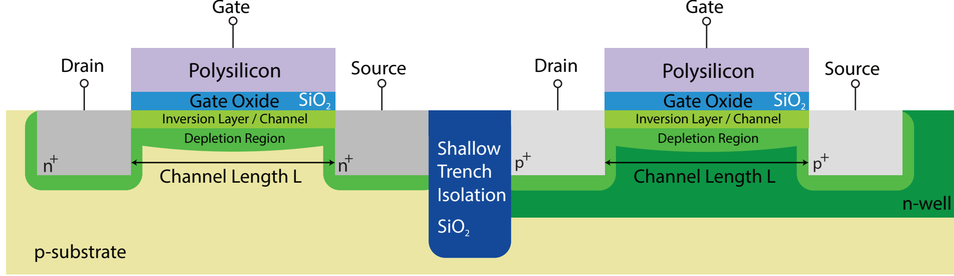


FIGURE 1.1: *Cross-section of a nMOS and pMOS in a CMOS technology where the different doping concentration are outlined (p- or n-doped).*

1.2 Current-voltage Characteristic

For a fixed drain to source voltage (V_{DS}), the increase of the gate voltage will lead to an increase of the drain current flowing in the transistor. Figure 1.2 pictures the extraction of common parameters from the current-voltage $I_D - V_G$ characteristic that will be continuously used in this work (leakage current, threshold voltage and maximum drain current). The evolution of these parameters during the exposition of the transistor to ionizing radiation have a major importance for IC designers. For digital electronics, the degradation of current driving capability linked to the maximum drain current and threshold voltage slow down the speed of the transistors. For analog electronics, each parameter variation is important and depends on the component under consideration (e.g., the decrease in transconductance reduces the gain in operational amplifiers).

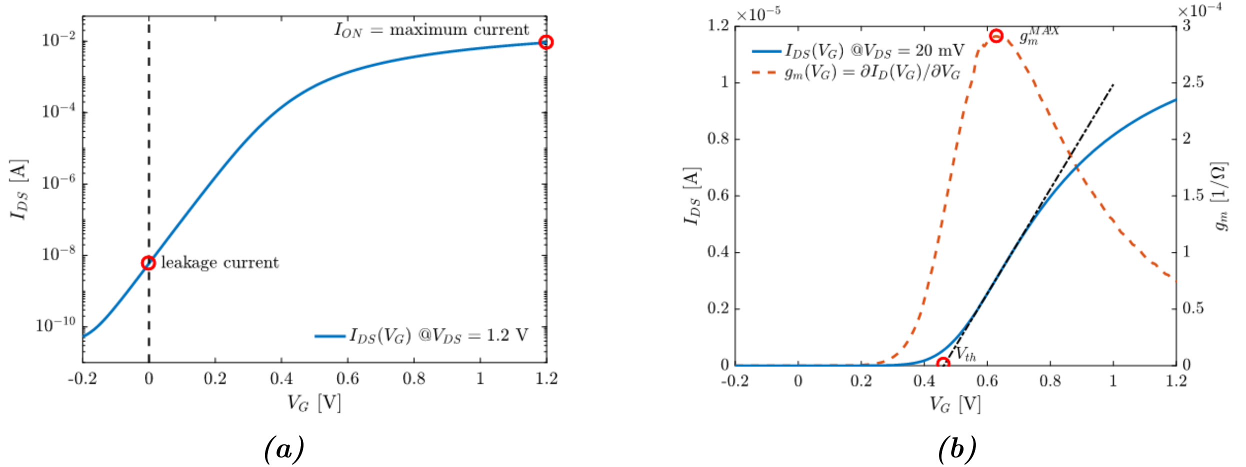


FIGURE 1.2: *Current-voltage ($I_D - V_G$) characteristic of a nMOS transistor with the main parameter extracted: leakage current, threshold voltage, maximum drain current and maximum of transconductance.*

Chapter 2

Total Ionizing Dose Effects in MOSFETs

In this chapter, we will detail the physical mechanisms involved in the degradation of the electrical parameters of MOSFETs with accumulation of ionizing radiation. The most sensitive part of MOSFETs is the oxide layer, namely silicon dioxide (SiO_2). In the first place because the electrons and holes generated by radiation have a significant difference in their mobility. Thus, the recombination of charges is not complete. Secondly because of the presence of defects in the structure: trapped charges begin to interfere with the normal behavior of the device. The way charges move inside SiO_2 and the way they interact with it have been studied intensively and mainly in the transistor gate oxide [24]. As we will see later, other oxides compromise the radiation hardness in modern technologies, but the physical mechanisms described in this chapter remain valid. We will start by giving a general overview of the different effects induced by radiation. We will then discuss in greater depth the processes involved with ionizing radiation.

2.1 Overview of Radiation Effects

Semiconductor devices are subject to three radiation-induced effects [25]: single event effects (SEEs), total ionizing dose (TID) and displacement damage (DD) (Table 2.1).

Table 2.1: *Summary of the radiation effects in MOSFETs.*

Radiation Effects	Ionizing	Non-Ionizing
Cumulative	Total ionizing dose (TID)	Displacement damage (DD)
Probabilistic	Single event effect (SEE)	

Displacement damage (DD) is created by energetic particles such as neutrons, protons, alpha particles, heavy ions and very energetic photons which disrupt the lattice structure of semiconductor materials. CMOS technology is mostly immune to displacement damage (DD) unlike other semiconductor devices such as bipolar transistors and optoelectronics [25].

Single event effects (SEEs) are due to the energy deposited by particles in the device and can have an impact on the device at any time since its exposition to radiation (probabilistic effect). The most relevant example is in digital electronics: the signal inside the device can change due to the energy deposited creating a transient error which can become static if it propagates to a latch and therefore stored by the circuit. These types of events are called single event upset (SEU). Nevertheless, this type of error can be corrected by HBD techniques (e.g. replication [26]). The most critical kinds of problems are called hard errors that corresponds to destructive events. One of these destructive events is called single event latchup (SEL) which is caused by parasitic structure inside the layout of the IC, the energy provided by the particles triggers a shortcut between the supply voltage and the ground, destroying the IC. Other types of destructive events exist such as single event burnout (SEB) or single event gate rupture (SEGR) [25].

The total ionizing dose (TID) called also total dose represents the quantity of energy that participates in the electron-hole (e-h) pairs generation (ionization). It is a cumulative effect that takes place during the whole operating time of the electronics device in the radioactive environment. The IC will continue to operate up to a critical TID value after which it will cease functioning. The SI unit of TID is the gray (Gy) which denotes the energy absorbed per unit of mass of a specific material. The radiation effects community prefers the rad unit ($1\,\mathrm{Gy} = 100\,\mathrm{rad}$) and the TID will be expressed in the silicon dioxide (SiO_2) which is the oxide used in CMOS technologies. Thus, all the TID value provided in this report will be expressed in silicon dioxide (SiO_2).

2.2 Impact of Ionizing Radiation in Oxides

The basic radiation problem related to total ionizing dose is pictured in Figure 2.1. Figure 2.1.A shows a classical n-channel MOSFET in normal operation where, by applying a sufficient positive voltage to the gate ($V_G > V_{TH}$), the channel turns into inversion creating a conductive path underneath the gate oxide: the transistor is turned on. When a MOSFET is exposed to ionizing radiation (Figure 2.1.B), there is an accumulation of trapped charges at the Si/SiO_2 interface and in SiO_2. In this case, the accumulation of positive trapped charges in the gate oxide inverts the channel even if no gate voltage is applied ($V_G = 0$). In general, the charge build up modifies the electrical properties of the transistor such as the transconductance, the leakage current, the subthreshold swing and the threshold voltage. The accumulation of charges in the oxide is the combination result of several physical mechanisms with different time dependence but also electric field and temperature dependence [27].

Figure 2.2 shows a schematic energy band diagram between SiO_2 and Si located in the gate layer with a positive bias applied on the gate and presents the whole process of charge build up in the gate oxide. By definition, an ionizing radiation is a radiation that carries enough energy to liberate electrons from the valence band and therefore ionizing the

atoms [28]. When an ionizing radiation is passing through the oxide (SiO_2), electron-hole pairs are generated by the radiation energy deposited [29]. The mobility of the electrons and holes are different in SiO_2. The holes are relatively immobile to the contrary of the electrons which are swept out of the oxide in picosecond [30, 31]. This is due to the possible presence of an electric field in the oxide which will drift both electrons and holes in the opposite direction with their respective mobility. The total ionizing dose effect happens in the oxide because the electron-hole pairs do not completely recombine and therefore each part of the transistor composed of oxide starts to accumulate charges. The holes hence generated will start to drift in the direction of the applied field [27]. When the holes reach the Si/SiO_2 interface they get trapped in deep energetic defects and behave as a fixed positive charge. During the drift of the hole through the silicon dioxide, the hole can cause the liberation of protons. The protons hence released will also drift in the same direction as the holes to form another type of defect: interface traps [32, 33, 34].

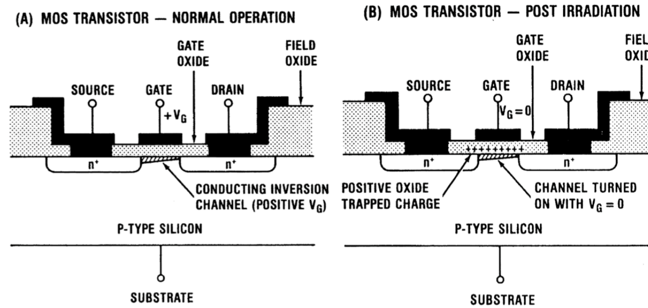


FIGURE 2.1: *Charge build-up (A) n-channel MOSFET in normal operation, positive voltage application ($V_G > V_{TH}$) creates an inversion layer underneath the gate oxide turning on the transistor. (B) n-channel MOSFET post irradiation, the accumulation of charge from ionizing phenomena in the oxide maintains an inverted layer while no gate voltage is applied ($V_G = 0$). (After Oldham [29]).*

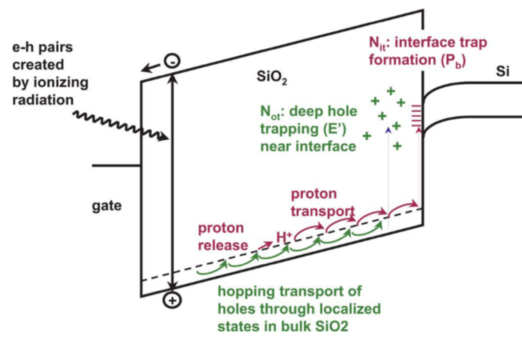


FIGURE 2.2: *Schematic of energy band diagram describing the creation of oxide traps and interface traps in the oxide and its interface with silicon induced by ionizing radiation. (After Schwank et al. [35])*

We will now review in greater depth the generation of the electron-hole pair and the formation of the two types of charges (oxide traps and interface traps).

2.2.1 Electron-Hole Pairs Generation

The starting point of the accumulation of charges is the generation of electron-hole pairs by ionizing radiation. Radiation refers to the transport of energy through electromagnetic waves (photons) or particles such as neutrons, electrons, protons and other subatomic particles (e.g. pions) as summarized in Table 2.2. Radiation is also classified in terms of ionization, that is, the ability to remove an electron from an atom or molecule *in which the radiation is propagated* [28]. Ionization can be itself direct or indirect depending if the radiation directly ionize the atom or molecule without intermediary steps.

TABLE 2.2: *Classification of the different types of radiation according to their ionization ability.*

<table>
<tr><td rowspan="7">Electromagnetic radiation</td><td rowspan="4">Non-ionizing</td><td>Radio wave</td></tr>
<tr><td>Infrared</td></tr>
<tr><td>Visible spectrum</td></tr>
<tr><td>Ultraviolet</td></tr>
<tr><td rowspan="4">Indirectly ionizing</td><td>Far-ultraviolet</td></tr>
<tr><td>X-ray</td></tr>
<tr><td>γ-ray</td></tr>
<tr><td rowspan="7">Particle radiation</td><td>Neutron</td></tr>
<tr><td rowspan="6">Directly ionizing</td><td>Electron/ β^- particle</td></tr>
<tr><td>Positron / β^+ particle</td></tr>
<tr><td>Muon</td></tr>
<tr><td>Proton</td></tr>
<tr><td>Ion ^{4}He / α particle</td></tr>
<tr><td>Other ions</td></tr>
</table>

In the present thesis, all experiments have been conducted with a 10 keV X-ray generated by a tungsten target and hence, the energy of the photons ranges from 5 keV to 50 keV [36, 37, 38, 39, 40]. Figure 2.3 outlines the effect that dominates in the interaction between the photon at a given energy and for a given material depending on its atomic number (Z). For the constituent of silicon dioxide (SiO_2), oxygen (Z $=$ 8) and silicon (Z $=$ 14), the photoelectric effect is the dominant one in the given energy range: the X-ray photon is absorbed by the atom which generates an high energy electron and a low energy photon. It is the emitted high energy electron that will generate electron-hole pairs through direct ionization. The electron-hole pair creation energy E_{EHP} was measured at the value of $17 \pm 1\,\mathrm{eV}$ [41]. From this value, one can compute the charge pair volume density per rad $g_0 = 8.05 \times 10^{12}$ pairs/cm^3/rad from equation 2.1 where $\rho_{\mathrm{SiO_2}}$ is the density of silicon dioxide.

$$g_0 = \frac{1\,\mathrm{rad}}{E_{\mathrm{EHP}}} \cdot \rho_{\mathrm{SiO_2}} = \frac{1\,\mathrm{rad} \cdot 10\,\mathrm{J\,g^{-1}} \cdot \frac{\mathrm{eV}}{1.6 \times 10^{-19}\,\mathrm{J}}}{17\,\mathrm{eV}} \cdot 2.19\,\mathrm{g\,cm^{-3}} = 8.05 \times 10^{12}\,\mathrm{pairs/cm^3/rad} \tag{2.1}$$

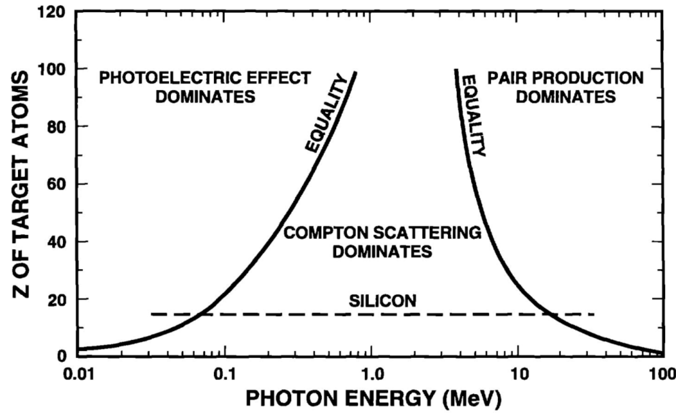


FIGURE 2.3: *Dominant effect in the photon interaction based on the energy of the incident photon and on the atomic number of the material. (After Evans [42]).*

All electron-hole pairs generated do not contribute to the accumulation of charges in the oxide because a fraction of them recombine immediately after their creation. The charge yield corresponds to the part of the holes that escape the initial recombination process. The initial recombination depends on both the amplitude of the electric field applied in the oxide (E_{OX}) and the type and energy of ionizing radiation. These dependencies are explained by the two analytically resolved recombination models: columnar [43, 44, 45] and geminate [46, 47]. In most cases of interest, the recombination process is a combination of both recombination models. Figure 2.4 shows the experimental results of the charge yield as a function of the applied electric field for different incident particles in silicon dioxide: it is important to take this information into account when comparing two different experiments irradiated by different radiation sources. It also indicates that charge yield increases with increasing electric field.

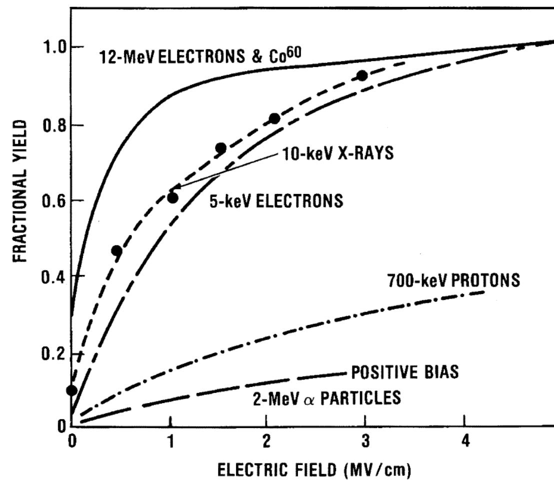


FIGURE 2.4: *Charge yield as a function of the electric field for different radiation source. (After Oldham [29]).*

2.2.2 Oxide Traps

When the hole escapes the initial recombination, the second process involves the hopping transport of the hole, called polaron hopping, through localized states in the SiO_2 oxide close to the Si/SiO_2 interface according to the applied field in MOSFETs (Figure 2.5). This process is several order of magnitude slower than the electrons swept out and is strongly influenced by temperature, biasing, oxide thickness and defect densities [48]. The investigation of the temperature dependence of the hole transport has been performed by Boesch et al. [49]. They show that an higher temperature leads to a faster hopping process and similar dependence is observed with the applied electric field: the higher is the electric field, the faster the holes move towards the interface [50]. The thickness of the oxide plays as well a role in the transport process. It has been shown that the transport time increases with the thickness following $\sim t_{\mathrm{OX}}^4$ dependency [48]. In particular, all these experiments show that this transport is universal and these parameters only modify the kinetic observed and not the behavior [51]. This transport can be accurately modeled by the continuous time random walk (CTRW) model [52].

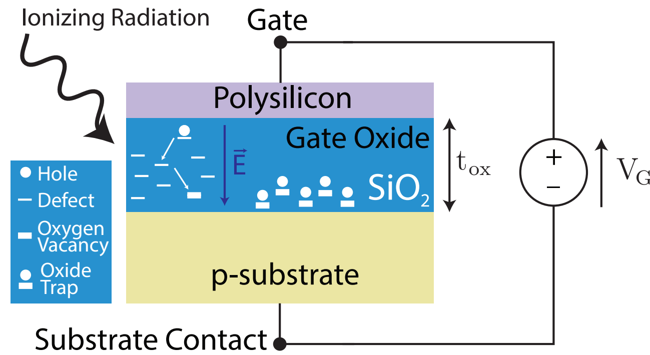


FIGURE 2.5: *Schematic view of the formation of oxide traps, the applied electric field causes the hole to drift towards the SiO_2/Si interface through defects. When they reach the interface, they get trapped in deeper energetic defects and formed fixed positive charges called oxide traps.*

Once the holes approach the Si/SiO_2 interface, they get trapped in another energetically deeper defects (oxygen vacancies) which is more present close to the interface. A portion of the holes stay trapped and the resulting positive charge is called oxide trap [29] (Figure 2.5). The holes trapped at the Si/SiO_2 interface can exchange with the Si through electrons tunnelling when they are close enough to the interface (typically 2 nm) and thereby recombine (annealing) while for distance greater than 3 nm this probability becomes quite low [53]. The thermal emission of electrons from the oxide valence band into oxide traps also participates in the annealing. The holes which remain deeply trapped constitute a fixed positive charge (N_{OT}). The formalization proposed by Fleetwood [54] is that as a general rule, the holes trapped in the silicon within 3 nm from the interface are called *border traps* and the more distant ones are called *oxide traps* but usually we refer to oxide traps to describe both.

If the oxide traps are located in the direct vicinity of the channel of the transistor, it will generate a threshold voltage shift ΔV_{TH} which can be calculated using equation 2.2 [55] where $\varepsilon_{\mathrm{ox}}$ and ε_0 represent respectively the oxide and vacuum permittivity, t_{ox} the oxide thickness, q the elementary charge of the electron and N_{OT} the charge of the build up of positive oxide charge.

$$-\Delta V_{\mathrm{TH}} = -\frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}} \cdot \varepsilon_0} q N_{\mathrm{OT}} \tag{2.2}$$

Equation 2.2 stresses that the thickness of the oxide has a huge impact on the threshold voltage shift ($\propto t_{ox}^2$) because N_{OT} is also proportional to t_{ox}. Therefore, the thickness of the oxide plays a key role in the radiation response and we can therefore expect a decrease in the contribution of the oxide traps for very thin oxides. This behavior will be discussed in chapter 4.

We can summarize the formation of oxide traps as follows:

1. Ionizing particles generate electron-hole pairs, increasing the total ionizing dose.
2. In the SiO_2, electrons have a higher mobility than the holes. Thus, the portion of recombination is much lower than in silicon. Under the application of an electric field, the recombination probability is even lower.
3. The electrons are swept out of the oxide while the holes start to drift towards the Si/SiO_2 interface hopping through localized states (defects) in the oxide.
4. Near the Si/SiO_2 interface, the holes get trapped in deeper energetic defects (oxygen vacancies) creating fixed positive charges named oxide trapped charge.
5. The distance from the interface (spatial distribution) impacts the tunnelling effect with carriers from the channel and thereby their neutralization. The energy levels of the oxide traps must be close to the valence band to anneal with electron thermal emissions.
6. The whole process is strongly influenced by temperature, applied electric field due to polarization (applied bias), oxide thickness and defects density (process fabrication). The process itself remains universal and these parameters only change its kinetic.

2.2.3 Interface Traps

As far as oxide traps are already changing the electrical properties of the MOSFETs, it is not the only charge build up mechanism arising from exposition to ionizing radiation. The drift of the holes (h^+) through the oxide towards the interface releases also hydrogen ions

(protons) (Equation 2.3) which will also drift towards the Si/SiO_2 interface where they will react to form what is called interface traps. The interface traps (Θ^+) are created by the drifted protons at the interface by equation 2.4 as shown in Figure 2.6.

$$h^+ + H \text{ (in oxide)} \longrightarrow H^+ \tag{2.3}$$

$$H^+ + SiH \longrightarrow \Theta^+ + H_2 \tag{2.4}$$

The time constant associated with this mechanism is much bigger than with oxide traps [24]. The interface traps find their origins in defects located at the interface between silicon dioxide and silicon. In fact, the density of defects and the sign of the charge they are trapping are a function of the Fermi (E_F) and midgap (E_M) level which depends on the applied bias (electric field). The defects capture a hole under negative bias, an electron under positive bias and is neutral at zero bias [24]. They have therefore a different sign for p-channel and n-channel MOSFETs: Figure 2.7 shows the filling of interface traps at the interface between the gate oxide and the silicon channel for both transistor type in inversion. The impact on the transistor proprieties are multiple depending on localization of the interface traps. If the interface traps are situated on the interface between the channel silicon and the gate oxide, there is an increase of the subthreshold swing as well as a threshold voltage shift and carrier mobility degradation.

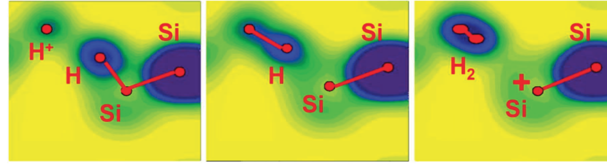
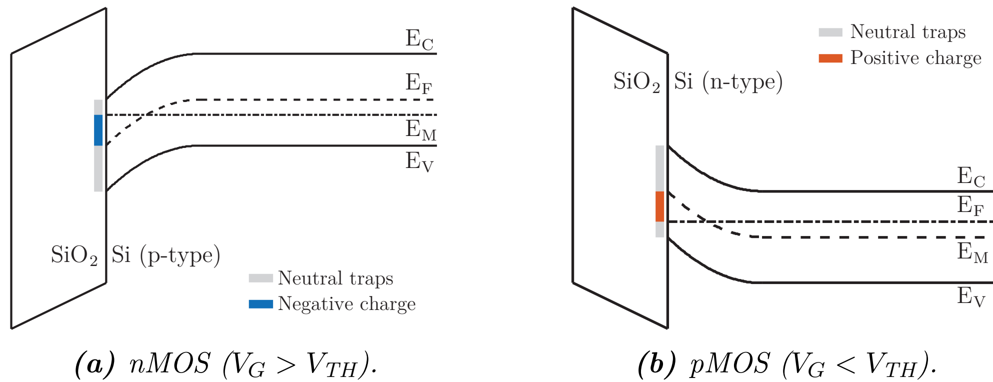


FIGURE 2.6: *Reaction of the hydrogen ions with SiH to form interface traps.*



(a) nMOS ($V_G > V_{TH}$). *(b) pMOS ($V_G < V_{TH}$).*

FIGURE 2.7: *Filling of interface traps in both transistor type when the gate voltage is higher than the threshold voltage. pMOS interface traps are filled with holes (positive charges) and nMOS with electrons (negative charges). Courtesy of Giulio Borghello.*

Chapter 3

Experimental Setup

The radiation response of transistors with total ionizing dose (TID) is very sensitive to many parameters and therefore very complex to study. Fortunately, the influence of these parameters can be controlled with an acceptable degree of confidence. In this chapter, we will give an overview of the experimental details. First, we will present the irradiation facilities operated during this work. Secondly, the measurement procedure will be described.

3.1 Irradiation and Measurements Facilities

The CERN Electronics Systems for Experiments (ESE) group holds two X-ray irradiation system (Seifert RP149) [Web10]. The outside part from one of both is pictured in Figure 3.1. The X-Ray beam and the device under test (DUT), placed inside the irradiation cabinet, are shown in Figure 3.2.

The irradiation cabinet shields the radiation scattered in all direction during irradiation. It also allows to perform experiments at low temperature down to −50 °C by injecting dry air inside which decreases the dew point value in order to avoid the formation of ice.

Temperature is controlled by a thermal chuck (Figure 3.2) whose temperature setting can vary from −50 °C to 200 °C. The position of the thermal chuck inside the cabinet can be controlled using the manual controller. Thermal control ensures that the temperature is constant and is not subject to variation even at room temperature (25 °C). The DUT is placed on a large copper block whose contact is made using a thermal paste that ensures an efficient heat exchange. Temperature control is important not only because the properties of the semiconductors themselves are highly dependent on it, but also because the mechanisms involved in the degradation by ionizing radiation are also strongly affected by temperature variation. It is important to note that some measurements are performed at low temperature because the ASICs inside the detectors are cooled down to −30 °C, we can thus place the DUT in the same temperature range.

The transistors to be measured are on a piece of silicon fabricated as an ASICs or an ICs, the probe card (Figure 3.3b) is used to reach the metal pad on the IC with needles (Figure 3.3a). The electrical contact point is made by scrubbing the surface of the metal pad to remove the thin layer of oxide as described in Figure 3.4b. The scratched metal pad after probing are shown in the top-right of Figure 3.4a.

FIGURE 3.1: *CERN EP-ESE group X-ray irradiation facility: the control station (computer) is used to automate measurements and is connected to the switching matrix and semiconductor analyzer via a GPIB cable. The X-ray machine is also remotely controlled from the control station. The temperature controller regulates the temperature of the thermal chuck inside the irradiation cabinet and its position can be adjusted by the manual controller.*

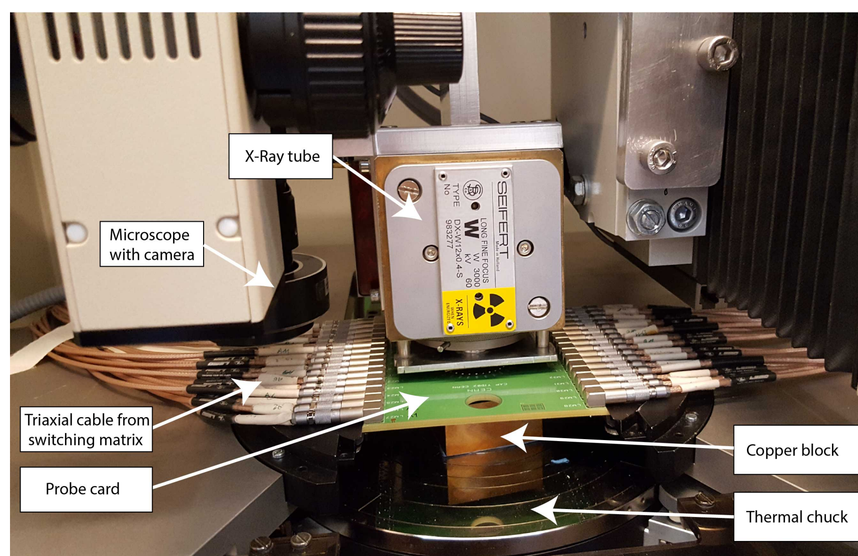
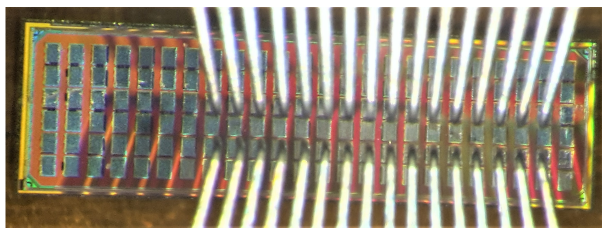
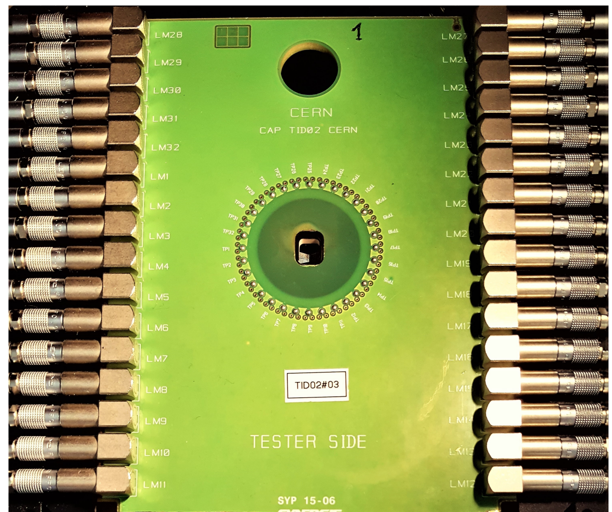


FIGURE 3.2: *Inside the irradiation cabinet: the X-ray beam is located above the probe card, which is connected to the switching matrix via Lemo cables. The device under test (DUT) is placed on the copper block and the thermal chuck is moved manually to reach contact with the DUT while monitoring through the microscope incorporating a camera.*

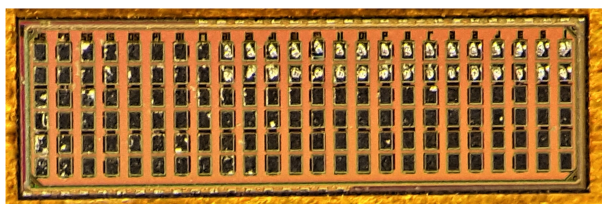


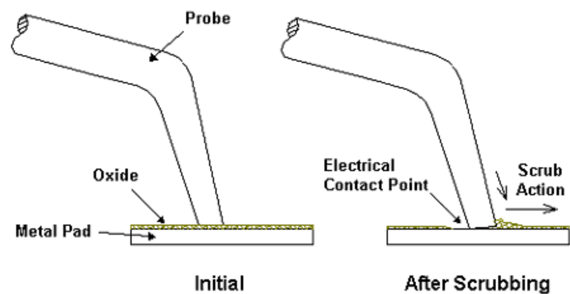


(a) Microscope view of the needles of the probe card (2×16*) are just above the metal pads of the ASIC. Each metal pad has a size of* $70\,\mu\text{m}$ *by* $100\,\mu\text{m}$*.*

(b) Probe card with 2×16 *Lemo cable connectors. The needles are situated in the center of the probe card.*

FIGURE 3.3: *Probe card and needles for contacting the custom test structures.*





(a) Microscope view of an ASIC embedding test structures of transistors in 28 nm technology. The dark rectangle corresponds to the metal pad (covered by oxide) allowing to probe the ASIC.

(b) Once the contact is established with the probe, the friction removes the oxide allowing the creation of an electrical contact point [56]. This can be seen in the microscope view (Figure 3.4a) on the top right scratched metal pad of the IC where the metal is now visible.

FIGURE 3.4: *Creation of an electrical contact point with the ASIC.*

The measurements are performed using a semiconductor parameter analyzer, the Keithley 4200A-SCS presented in Figure 3.1. The current version embeds six source measure units (SMUs) and one capacitance voltage unit (CVU). The SMU allows to both sourcing and measuring at the same time (e.g. biasing a voltage node while measuring the current at this node) and is a powerful electronic instrument for characterization. The CVU is simply an impedance meter. The semiconductor parameter analyzer is then connected to a switching matrix which allows to route each SMU through 32 triaxial[1] outputs wired to the probe card. Figure 3.5 gives an overview of the whole setup while Figure 3.6 outlines the use of both equipment for measuring several devices. Both the semiconductor parameter analyzer and the switching matrix are key equipment used in the characterization of semiconductor devices.

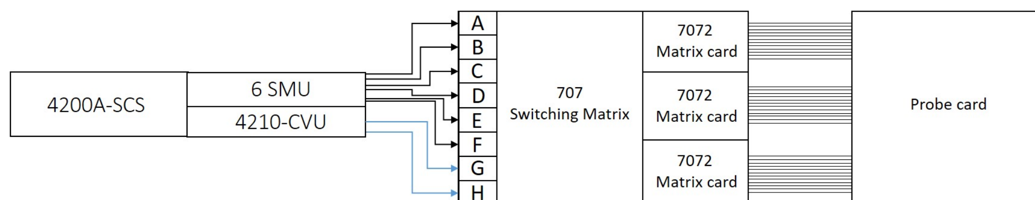


FIGURE 3.5: *Overview of the experimental setup from the instruments point of view. A semiconductor parameter analyzer 4200A-SCS has 6 SMUs and 1 CVU. The measuring probe of the 4200A-SCS is connected to the 707 Switching Matrix embedding 3 7072 Matrix card with a total of 36 outputs (only 32 are used) which are then connected to the probe card.*

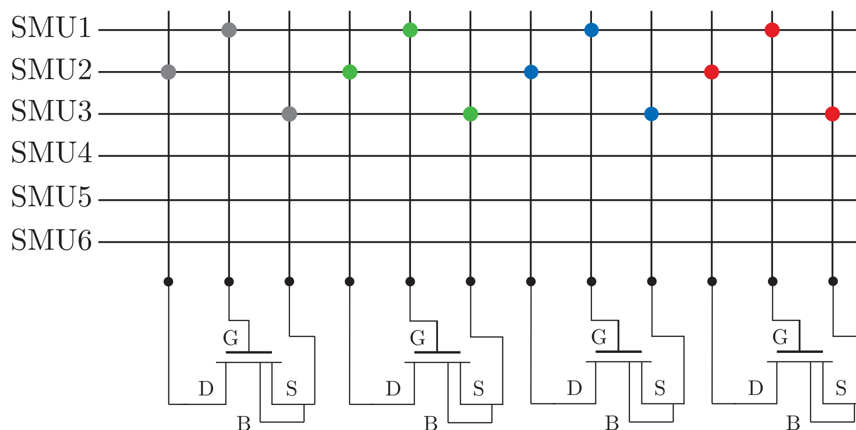


FIGURE 3.6: *The semiconductor parameter analyzer provides 6 SMUs, the switching matrix allows to measure different transistors by commuting the contact inside the matrix. Each colored dot corresponds to one connection during measurement while the others are not connected. Complex polarization configuration may require up to 6 SMUs (not detailed).*

[1]Triaxial cables contain an additional layer of insulation and conducting sheath than coaxial cables. It provides more shielding and bandwidth and is used for low current measurements to suppress leakage current between the core and the guard. However, connectors and cables are much more expensive.

3.1.1 Generation of Ionizing Radiation and Dose Rate

The ionizing radiation used to irradiate the ASICs are 10 keV X-rays generated by electrical energy using a Crookes tube. X-ray machines are convenient tools for performing irradiation because the dose rate is high and can be easily adapted to the needs. X-rays can also be generated using radioactive materials such as ^{55}Fe, ^{29}Cu, ^{241}Am but the dose rate is lower than the one provided by an X-ray tube. Another common source of ionizing radiation are γ-rays radiated by ^{60}Co but they are handled in appropriate facilities because of their high energy.

Calibrations are performed each time the X-ray tube is changed because the dose rate varies from tube to tube. The beam is calibrated using pre-calibrated positive intrinsic negative (PIN) photo-diodes [57, 58]. The current flowing through the diode is proportional to the deposited energy by photons that contribute to the electron-hole pair generation in the depletion region of the diode (Equation 3.1). The conversion coefficient β is given and pre-calibrated to express the dose rate D in silicon dioxide. By subtracting the dark current of the diode $I_{\text{Dark Current}}$ (mask the photon source from the diode and measure the current) to the measured photo-current I_{Exposed} (the photon source is exposed to the diode) we can retrieve the exact photo-current $I_{\text{Photo-current}}$. We upgraded the program controlling the beam position to perform an automatic calibration map of the X-ray intensity. A PIN diode is placed at the centre of the beam and a selected area is chosen to sweep around. The program controls a SMU to measure the current passing through the diode which depends on the photons intensity. Figure 3.7 shows the X-ray beam intensity when the beam is positioned at an altitude of 2 cm from the diode.

$$D = \beta \cdot (I_{\text{Exposed}} - I_{\text{Dark Current}}) = \beta \cdot I_{\text{Photo-current}} \tag{3.1}$$

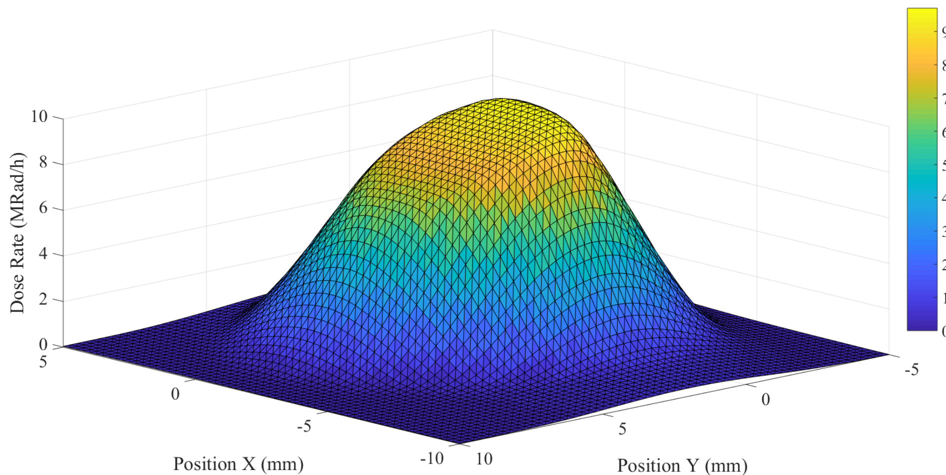


FIGURE 3.7: *Calibration map of an X-ray tube at* 2 cm *from the target for the operation mode of* 40 kV *and* 50 mA*. The measured maximum dose rate is* 10 Mrad h^{-1} *(SiO$_2$).*

The dose rate used to irradiate the transistors is relatively high ($10\,\mathrm{Mrad\,h^{-1}(SiO_2)}$) compared to the actual real condition in the particle accelerator ($\sim 11.4\,\mathrm{krad\,h^{-1}}$ for HL-LHC) but it allows irradiation to be performed within a reasonable time. For example, 500 Mrad will be reached in 5 years in the HL-LHC while an irradiation performed with an X-ray machine will only take 50 hours. Dose rate in the CMOS technology has never been a major concern because no dose rate dependence in degradation has been observed hitherto [59, 60]. However, Borghello et al. discovered recently a dose rate sensitivity in 65 nm and 130 nm technologies [61]. This dose rate sensitivity will be further investigated once the new X-ray machine will be operational.

3.1.2 Measurement Procedure

The DUT is placed in the irradiation cabinet at 2 cm from the X-ray beam and the instrument is configured on the control station to automatize the measurement. Prior, pre-irradiation measurements are performed to verify that the DUT is presenting an expected behavior (PreRad measurement in Figure 3.8). ASICs are sensitive to electrostatic discharge (ESD) which can damage the transistors (e.g. gate breakdown [62]). Once the DUT is validated, the full measurement procedure can start.

The measurement procedure is divided into two parts. The first one is the irradiation, several irradiation steps are prepared at which the irradiation stops and each transistors is measured one after the other. When the measurements are over, the irradiation continues to the next step. The measurements are fully automated and work continuously. During the irradiation, the transistors are kept under bias. The last step of the irradiation is usually set between 200 Mrad to 1 Grad depending on the type of measurements needed. Once the irradiation has reached the expected total ionizing dose, the irradiation is stopped and the second part of measurement procedure, the annealing, begins. During annealing, the DUT is placed at constant temperature and is kept under bias. The annealing is generally performed at high temperature to accelerate physical mechanisms.

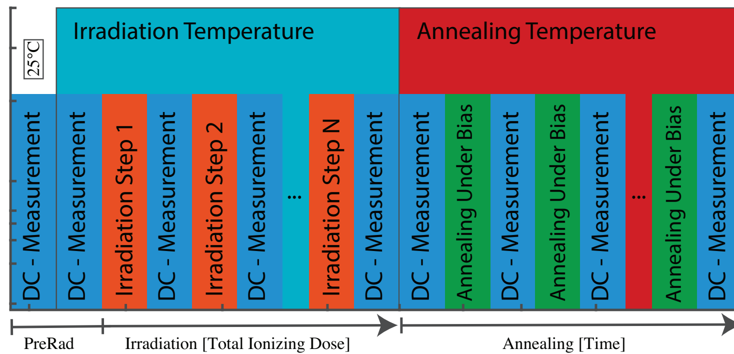


FIGURE 3.8: *Typical qualification procedure used during TID experiments [63]. The transistors are irradiated to specific TID level and the irradiation is stopped to measure the transistor characteristic (e.g. $I_D - V_G$ measurements). Once the irradiation reaches the last TID step, the measurement continues during the annealing phase.*

Chapter 4

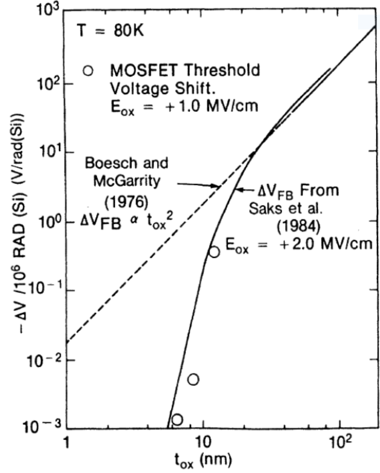
65 nm Bulk CMOS Technology Qualification to Total Ionizing Dose

The future upgrade of the Large Hadron Collider aims to increase the luminosity of the particle accelerator. As a result, the total ionizing dose perceived from the electronics in the detectors will also increase, foreseen to reach 1 Grad(SiO_2) over a period of 10 years. The upgrade requires the development of new ASICs to withstand this extreme radiation environment. In this chapter, we present the response to total ionizing dose for the 65 nm bulk CMOS technology used in the ASICs for the High-Luminosity Large Hadron Collider upgrade. We will outline how the different oxides present in the structure of transistors pose a threat to the radiation hardness of modern technologies.

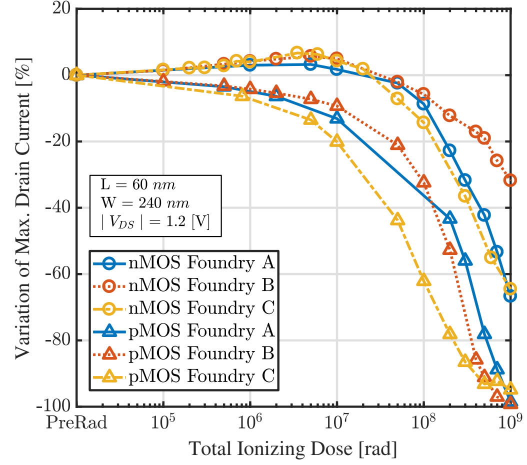
4.1 Impact of Ionizing Radiation in Nanoscale Technologies

The mechanisms involved in the degradation of MOS transistors with ionizing radiation, namely the charge build-up of oxide and interface traps in oxides, have been described in chapter 2. The presence of oxide in CMOS technologies is therefore the weak point when exposed to ionizing radiation. These phenomena have been intensively studied in the last decades mainly for the gate oxide of the transistors [24, 29, 35]. It has been predicted very soon (1980s) that the reduction in thickness of the gate oxide will increase its radiation hardness: Figure 4.1a shows the important decrease in the variation of the flatband voltage for a MOS capacitor (linked to the threshold voltage of a MOSFET) due to the increase of the tunneling effect and its ability to neutralize trapped charges [64]. This prediction has been confirmed experimentally on commercial technologies [65, 66] whose dimensions continue to scale down following the Moore's law trend (the number of transistors in a ICs doubles about every two years).

The gate thickness of modern deep nanoscale processes allows to the gate oxide to withstand very high levels of total ionizing dose and has been observed to be insensitive up to several Mrad from the 130 nm technology [65] where the gate becomes thinner than 3 nm. The aggressive scaling of CMOS technology carried out by the semiconductor industry has therefore improved the overall TID tolerance. However, Figure 4.1b shows a significant degradation of the maximum drain current for n- and p-channel MOSFETs of three different foundries in the 65 nm commercial node where the gate thickness is in the order of 2 nm (e.g. see [Web11]). The degradation observed cannot therefore be directly attributed to the gate oxide: the limitation in the radiation hardness are caused by other oxides present in the structure of modern transistors.



(a) Flatband voltage variation per Mrad *dose for MOS capacitors as a function of the oxide thickness. From Saks, et al. [67].*



(b) Maximum drain current variation for transistors of the same size from three different foundries.

FIGURE 4.1

Figure 4.2 presents a schematic representation of the architecture of modern submicron CMOS transistors, here an n-channel MOSFET. Since its introduction near the 0.25 µm technology node [68], in order to replace the LOCal Oxidation of Silicon (LOCOS), each transistor is enclosed by the Shallow Trench Isolation (STI) oxide to avoid leakage paths between devices. Other oxides, the spacers, have been introduced near the gate to allow the formation of the LDD extensions which are used to reduce the hot-carrier effects. These oxides are the main responsible for the weakness of the TID tolerance of modern CMOS architecture because of their thickness ($\gtrsim$ 100 nm [69] for STI) and lower quality compared to the gate oxide (rich in defects and much more process dependent). Figure 4.3 shows transmission electron microscopy (TEM) images of real transistor where the spacers, the STI and the gate oxide are outlined.

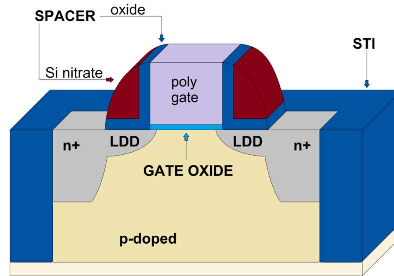
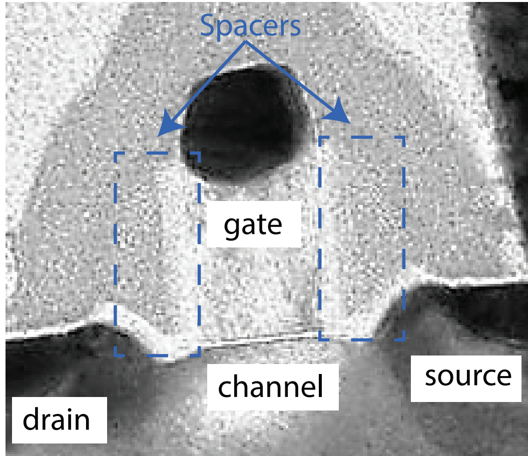
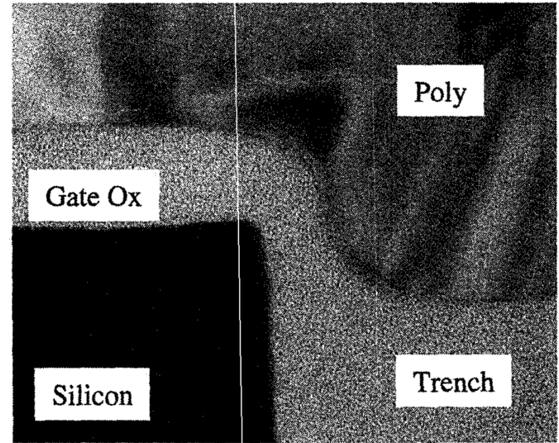


FIGURE 4.2: *Structure of modern submicron n-channel MOSFET. The spacer oxides allows the implantation of the LDD extensions needed to reduce the hot-carrier effect while the Shallow Trench Isolation (STI) is used to decrease the inter-device leakage current. Courtesy of Giulio Borghello [70].*



(a) TEM image of a transistor in 65 nm *commercial technology. The spacers are outlined [Web12].*



(b) TEM image of the region close to the channel of the transistor (Silicon) with the gate oxide (Gate Ox) and the STI (Trench) [71].

FIGURE 4.3: *Example of typical real transistors structure.*

4.2 Experimental Details

The radiation response of MOS transistors is strongly dependent on biasing and temperature conditions. These radiation effects also behave quite differently with respect to the size of the transistors. The spacer-related effects have a particular dependence on the channel length called RISCE [72] while STI-related effects have a channel width dependence known as RINCE [65]. The STI is also responsible of the increase in leakage current in n-channel MOSFETs. The following sections present both spacer and STI related effects from the 65 nm technology qualification. The qualification includes the influence of bias, geometry and temperature [22].

In addition to the 65 nm foundry used for the next generation of ASICs for the HL-LHC upgrade, designated by Foundry A in the following sections, two other foundries (foundry B and C) have been tested to increase confidence that the phenomena are general to the whole commercial node and not only related to one foundry in particular.

The irradiation was performed with the measurement and irradiation setup described in chapter 3. Custom test structures were used to perform the qualification with different transistor geometries, including a test structure containing enclosed layout transistors that we will describe later. Each test structure makes it possible to study the different effects induced by radiation. The standard qualification is performed at three different irradiation temperatures (−30 °C, 0 °C and 25 °C) and up to a total ionizing dose of 500 Mrad. Other measurements at different temperatures are also included.

The polarization of the transistors during irradiation has a major influence in the

degradation. If not stated otherwise the configuration used is the so-called diode configuration [73] where the gate and the drain are polarized ($| V_{DS} |= V_{DD} = 1.2\,\mathrm{V}$ and $| V_{GS} |= V_{DD} = 1.2\,\mathrm{V}$) where V_{DD} is the supply voltage of the technology (e.g. $V_{DD} = 1.2\,\mathrm{V}$ in 65 nm. This configuration is used for the qualification because it provides the largest degradation as we will see later.

Unirradiated devices were kept under bias for a period of time identical to an irradiation up to 1 Grad, both at room temperature and at high temperature (data not shown). These devices have shown less than 2 % of maximum drain current degradation. These control experiments ensure that the degradation observed during irradiation is actually due to radiation and not to other mechanisms that can affect MOSFETs performances such as negative bias temperature instability [74, 75] or hot-carrier effects [76, 77].

4.3 STI-related Effects

The Shallow Trench Isolation (STI) is a feature of integrated circuits (ICs) to prevent current leakage between adjacent devices. The STI are made in dielectric materials and mainly silicon dioxide (SiO_2) is used. As we will see, the STI introduces several radiation-induced mechanisms in the transistor.

4.3.1 Radiation-Induced Narrow Channel Effects (RINCEs)

The Radiation-Induced Narrow Channel Effects (RINCEs) is linked to the STI oxide present in modern devices. The STI encloses the transistor in order to avoid leakage paths between adjacent devices in integrated circuits but its important thickness presents one of the weaknesses of modern technology against TID. Indeed, the scaling of the CMOS technology concerns mainly the gate oxide and the STI thickness is not reduced accordingly [73].

Figure 4.4 illustrates the STI surrounding an n-channel MOSFET before (top) and after irradiation (bottom) for a narrow (left) and wide transistor (right). Before irradiation, the STI facing the channel contains a negligible amount of charges and the current simply flows through the channel without any influence. During and after irradiation, the accumulation of oxide and interface traps occurred and charges begin to accumulate in the area facing the channel. The trapped charges create an electric field that affects the current flowing through the transistor channel. The width W of the transistor plays a key role in this effect. As shown in Figure 4.4, the smaller the W, the larger the part of the channel impacted by the generated electric field.

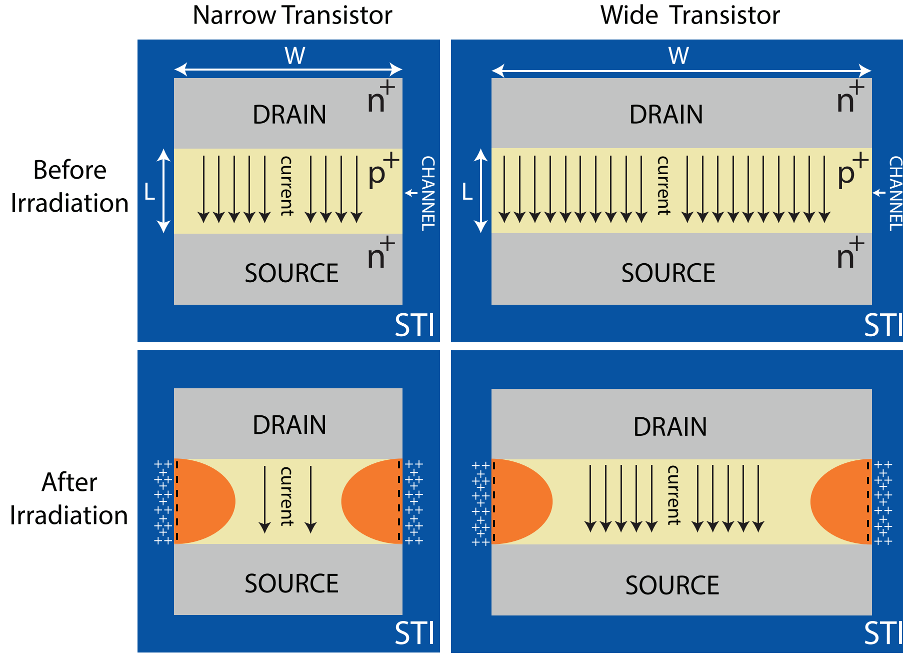
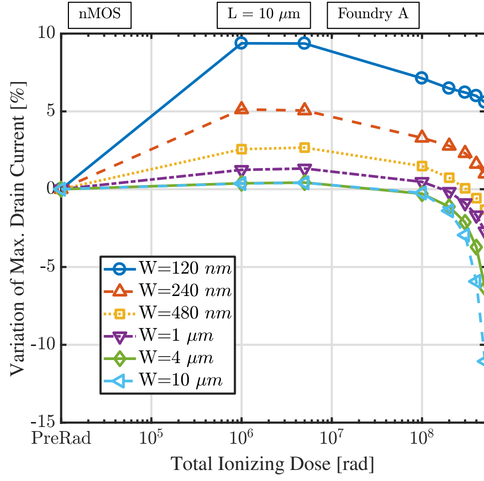


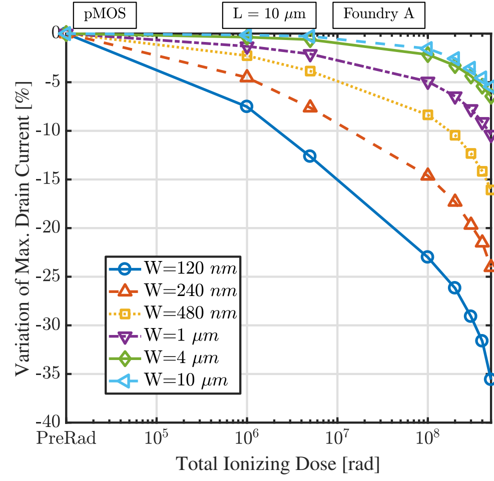
FIGURE 4.4: *Radiation-Induced Narrow Channel Effect related to the presence of the Shallow Trench Isolation. The top left and right n-channel MOSFETs are non irradiated with two different widths while the two bottom left and right n-channel are irradiated. The charges build up at and near the Si/SiO_2 interface (oxide traps and interface traps).*

The channel width dependence is outlined in Figure 4.5 where the maximum drain current and threshold voltage shift features are extracted from the $I_D - V_G$ characteristic of transistors irradiated up to 500 Mrad at room temperature. The channel width W of the transistors varies from 120 nm to 10 µm and the channel length L is fixed at 10 µm, since, as we will see later, the effects associated with spacers (RISCEs) are less important with greater channel length.

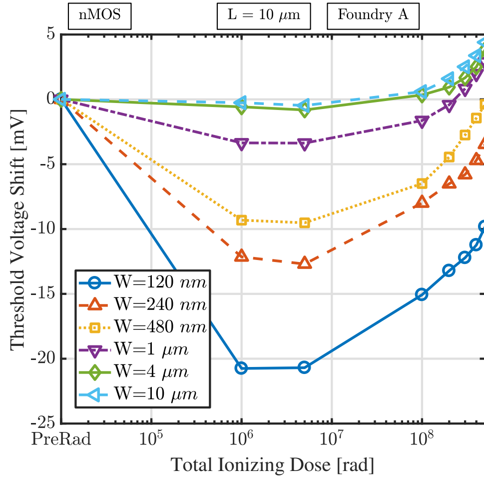
The consequences of this charge build-up are different for n-channel and p-channel MOSFETs. The generation of oxide traps is faster than interface traps and therefore in n-channel MOSFETs, where oxide and interface-trapped charges are opposite in sign, two different trends are observed. First, the accumulation of positive trapped charges in the STI produces a negative threshold voltage shift of the transistors (Figure 4.5c) and, therefore, an increase in the maximum drain current (Figure 4.5a) with a peak around 1 Mrad. Second, the slower build up of interface traps gives rise to the so-called rebound in the evolution of the electrical parameters: an increase in the threshold voltage and hence a decrease in the maximum drain current. For p-channel MOSFETs, interface traps carry a positive charge and thus both oxide and interface traps are positively charged. The maximum drain current and the threshold voltage are both monotonically decreasing during irradiation (Figure 4.5b and 4.5d). We can observe that in both n- and p-channel MOSFETs the threshold voltage shift and the maximum drain current variation are inversely proportional to the width of the transistor.



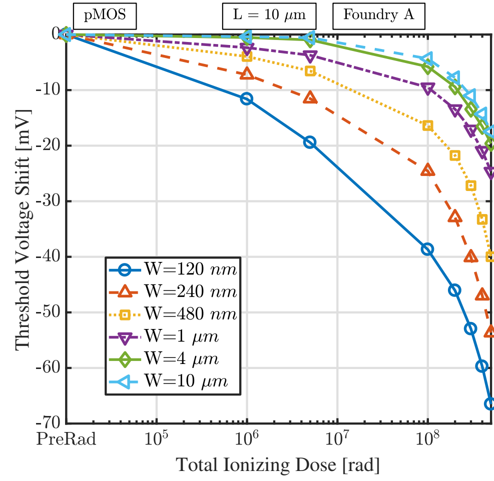
(a) *Maximum drain current variation in n-channel MOSFETs*



(b) *Maximum drain current variation in p-channel MOSFETs*



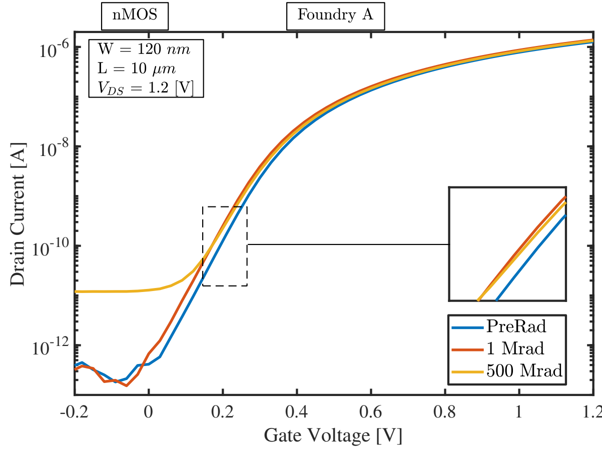
(c) *Threshold voltage shift in n-channel MOSFETs*



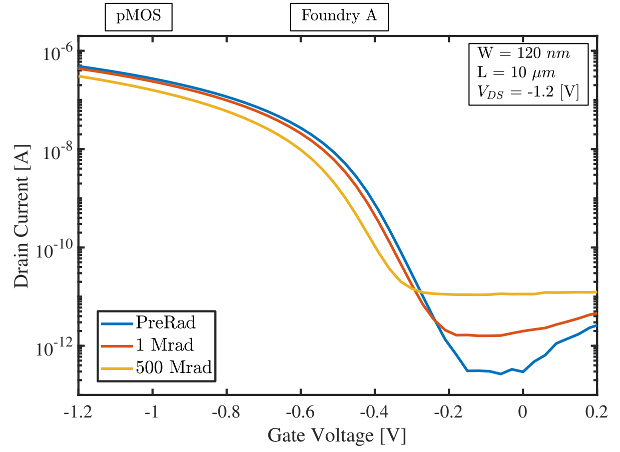
(d) *Threshold voltage shift in p-channel MOSFETs*

FIGURE 4.5: *Variation in the maximum drain current in saturation ($|V_{DS}| = 1.2V$) and threshold voltage shift for n-channel MOSFETs (a and c) and p-channel MOSFETs (b and d) during irradiation up to 500 Mrad at 25 °C. The variation is strongly dependent on the channel width. The channel length of the transistor is fixed and very large to mitigate the spacer-related effects. The transistors were biased during irradiation in diode configuration ($|V_{DS}| = 1.2V$ and $|V_{GS}| = 1.2V$).*

The $I_D - V_G$ characteristics of the narrowest n- and p-channel MOSFETs transistors are respectively shown in Figure 4.6a and 4.6b. For the n-channel MOSFET, we can observe between 1 Mrad and 500 Mrad the increase in the subthreshold swing related to the build-up of interface traps (zoom in Figure 4.6a).



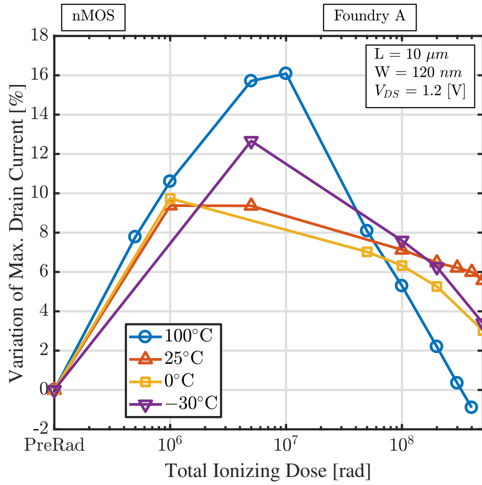
(a) *n-channel MOSFET*



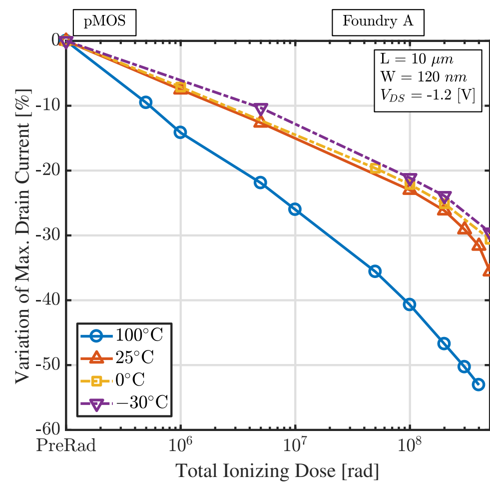
(b) *p-channel MOSFET*

FIGURE 4.6: *$I_D - V_G$ characteristics before irradiation, after* 1 Mrad *and* 500 Mrad.

Irradiation at different temperature have been performed from −30 °C to 100 °C (Figure 4.7). In n-channel MOSFETs, the influence of temperature is difficult to interpret. Indeed, holes trapping is enhanced at low temperature but the transport of both holes and protons near the interface Si/SiO_2 is slowed down and thus the observed degradation is difficult to interpret. We can conclude that temperature increases the magnitude of the change as we observed sharpest variation at 100 °C. The interpretation for the p-channel MOSFETs is straightforward as both mechanisms are participating to the degradation: the higher temperature leads to a higher degradation.



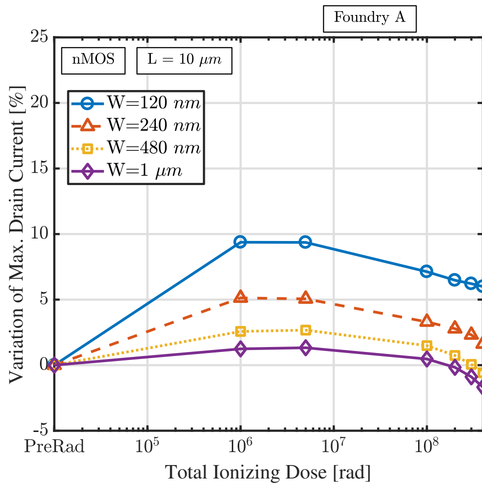
(a) *n-channel MOSFET*



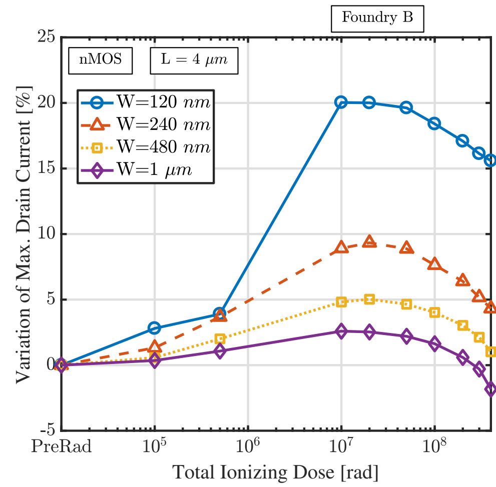
(b) *p-channel MOSFET*

FIGURE 4.7: *Influence of the temperature on the Radiation-Induced Narrow Channel Effect (RINCE) in n- and p-channel MOSFETs.*

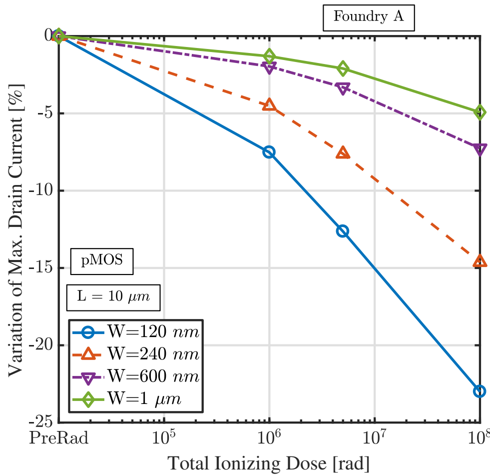
A comparison is performed between foundry A and B (Figure 4.8). The increase in the maximum drain current due to RINCEs is happening at the same range of TID in both foundries and is due to the same threshold voltage shift but the magnitude is more important in foundry B. This difference can be explained by the fact that more oxygen vacancies are present close to the interface and therefore more oxide traps are accumulated in the region close to the channel of the transistors. Nevertheless, the impact of the interface traps is similar in both foundries. For the narrowest transistor we can observe a decrease of 2 % just after the peak. For pMOS transistors similar degradation is observed in both foundry. Foundry C is left out from the comparison due to the lack of adequate transistor dimensions but have shown qualitatively similar dependence.



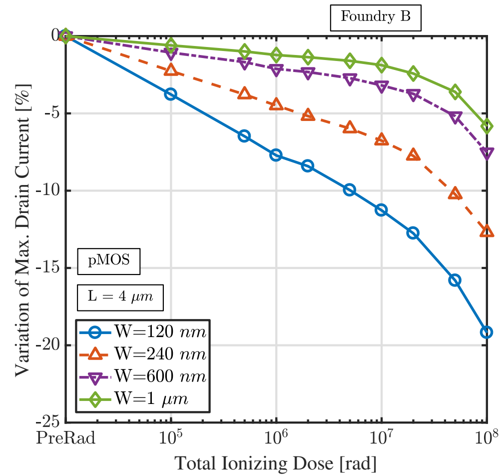
(a) Foundry A nMOS



(b) Foundry B nMOS



(c) Foundry A pMOS



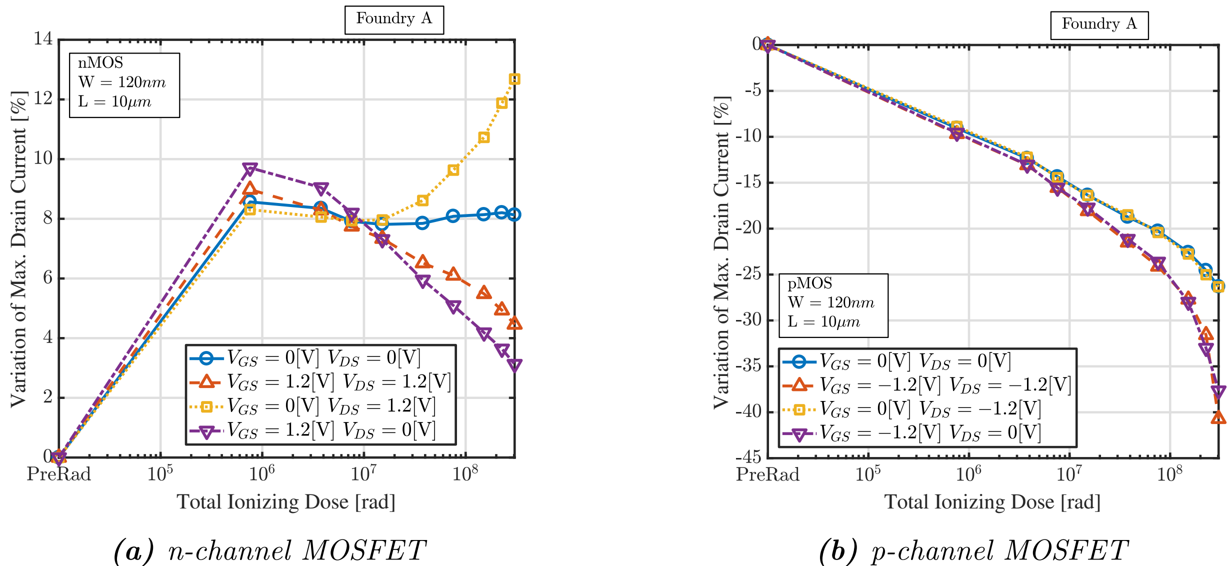
(d) Foundry B pMOS

FIGURE 4.8: *Radiation-Induced Narrow Channel Effects (RINCEs) for two different foundries with transistors of the same channel width and a large fixed channel length to alleviate the effects of the spacers.*

The electric field applied to the transistor during irradiation has a major influence on the behavior of the device because it is responsible for the drift of charges in oxides. Figure 4.9 presents the influence of the polarization of the RINCEs in a narrow and long device. nMOS and pMOS transistors have been kept under bias during irradiation with different bias possibilities for drain and gate.

In pMOS transistor (Figure 4.9b), the degradation is higher when the gate bias is applied, no matter the applied bias of the drain. The difference observed between the two degradations is due to a further increase of the threshold voltage due to oxide traps because no major change in the subthreshold swing is observed between the different configurations (not shown).

The effect of polarization is more important and complex in the nMOS transistor (Figure 4.9a). The first increase in maximum drain current at 1 Mrad due to oxide traps is not dependent on bias but the behavior after 10 Mrad is strongly bias dependent and both gate and drain bias influence the evolution. After 10 Mrad, the presence of the gate bias induces a decrease of the maximum drain current due to the accumulation of interface traps observed by the increase of the subthreshold swing (with and without drain voltage). Without gate bias, there is no build-up of interface traps and two different trends are observed. First, if no bias is applied at all (both gate and drain are at 0 V), we observed no significant change in the transistor characteristic up to 300 Mrad. However, when drain bias is applied, a second accumulation of oxide traps is observed, leading to a second increase in maximum drain current. This second increase is mainly due to an increase in transistor transconductance, which means that an increase in gate voltage induces a higher current than before. To the best of our knowledge, this behavior has not yet been observed.



***(a)** n-channel MOSFET*

***(b)** p-channel MOSFET*

FIGURE 4.9: *Influence of the transistor bias during irradiation for RINCEs.*

4.3.2 Radiation-Induced Leakage Current

Another consequence of charge generation in the STI is the increase in leakage current during irradiation. This effect can only appear in the n-channel MOSFETs because the positive oxide traps accumulated in the portion of the STI facing the channel can locally attract electrons from the p-substrate and thus create a parasitic conductive path between source and drain (Figure 4.10 (1)). Charges in the STI can also create a leakage path between two n-doped regions of different potential creating a parasitic leakage current between adjacent devices (Figure 4.10 (2)).

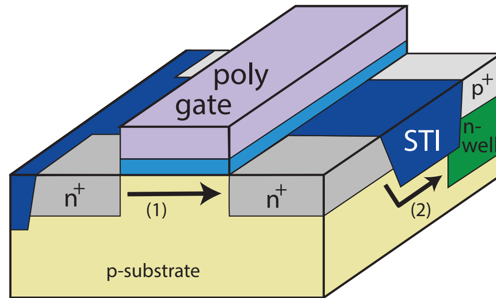


FIGURE 4.10: *Cross-section of an n-channel and p-channel MOSFETs. The build-up of oxide traps in the STI can create a parasitic path between the source and the drain in n-channel MOSFET (1) and between two n-doped silicon region of different potential (2).*

In the past history of studying the TID effects in transistors, the increase of the leakage current has been the major threat to the use of commercial technologies in radioactive environment [71, 78, 79, 80]. The most commonly used technique to eliminate leakage current between source and drain (Figure 4.11 left) is the enclosed layout transistor (Figure 4.11 right). Indeed, in enclosed transistors, the STI does not face the channel. The enclosed layout transistor as a HBD technique was used in the electronics developed for the LHC to eliminate the leakage current present in the 0.25 µm technology used at that time [81]. However, this type of transistor requires a considerable effort to be characterized and presents several drawbacks compared to standard layout transistor (e.g. larger dimensions, asymmetric, increased parasitic capacitance) [64, 82].

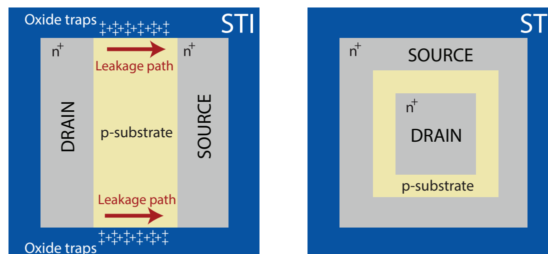
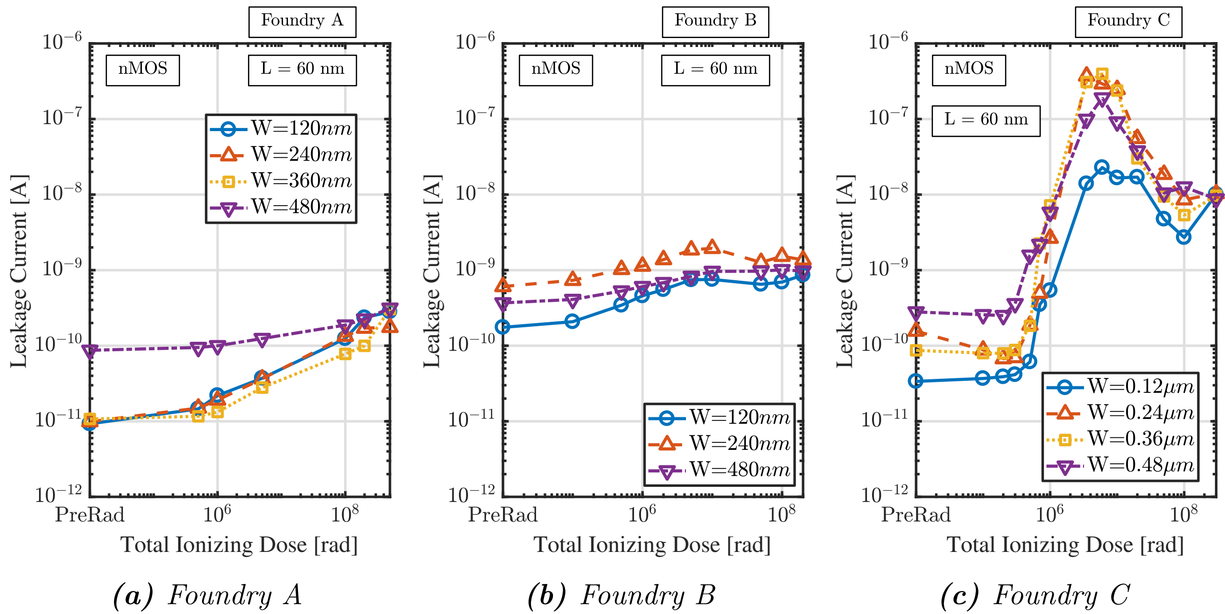


FIGURE 4.11: *Standard layout transistor (left) can present leakage current. Enclosed layout transistor (right) is a hardening-by-design (HBD) technique that eliminate the impact of the Shallow Trench Isolation (STI) [70].*

In the 65 nm technology used (foundry A), the radiation-induced increase in the leakage current observed is negligible even at very high TID (Figure 4.12a) and therefore the use of enclosed layout transistor can be avoided. Foundry B presents also a negligible variation of the leakage current (Figure 4.12b) but foundry C has an important increase by 3 orders of magnitude (Figure 4.12c). This strong foundry-to-foundry variation can be ascribed to the fabrication processes of the STI [83] as it has already been observed in 130 nm technology [19, 84, 85] but also maybe to the difference in the doping profile of the transistors.



(a) *Foundry A* ***(b)*** *Foundry B* ***(c)*** *Foundry C*

FIGURE 4.12: *Evolution of the leakage current in n-channel MOSFETs in foundry A, B and C. Foundry C has an important increase of the leakage current (3 orders of magnitude) while foundry A and B present a negligible increase.*

4.4 Radiation-Induced Short Channel Effects (RISCEs)

The Radiation-Induced Short Channel Effects (RISCEs) is related to the presence of spacer oxides in modern transistors [72]. The spacers are located near the gate and allow the implantation of the lightly doped drains (LDDs) (Figure 4.13) to mitige hot-carrier effects.

The hot-carrier effects are a major concern for modern technologies and are worsening due to the reduction in transistor size [86]. Indeed, the voltage supply is not scaled proportionally to the transistor dimensions, which leads to a significant increase in the electric field inside the transistor and saturates the velocity of the carriers. These carriers damage the transistor and lead to a degradation of the device's performance. The doping concentration of the LDDs allows to reduce the electric field in this region and alleviates the hot-carrier effects [87]. More details can be found in literature [88].

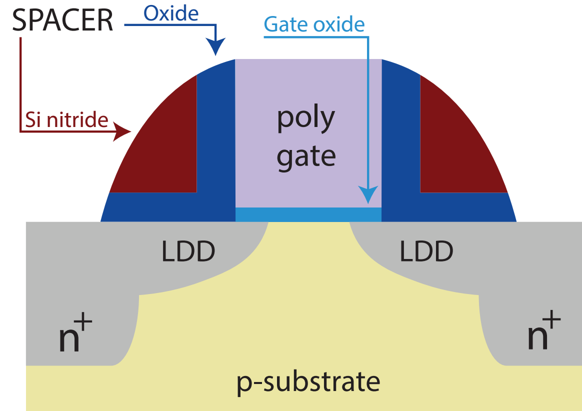
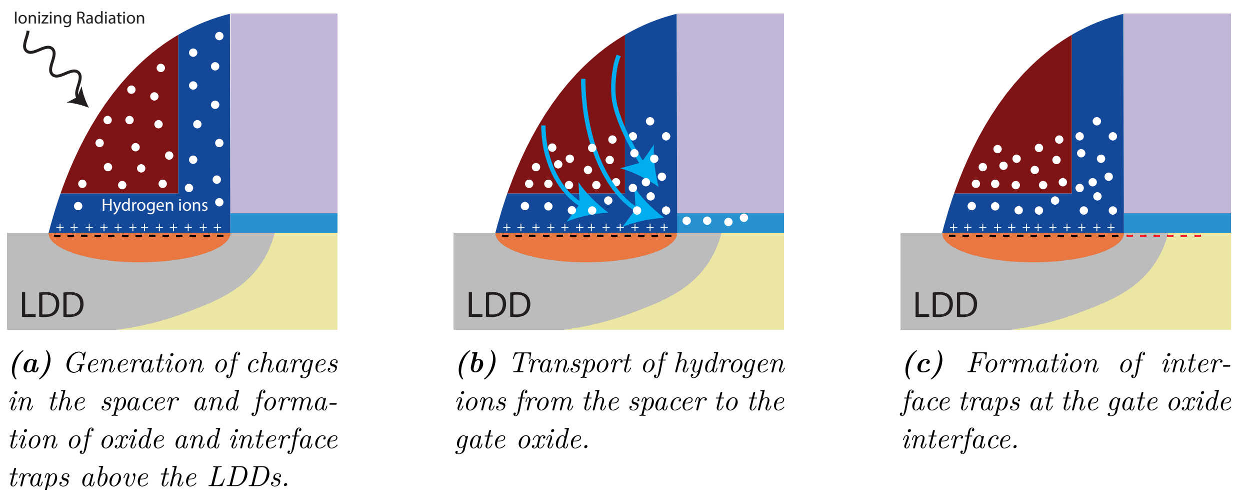


Figure 4.13: *Illustration of the spacers situated near the gate of the transistor and composed of silicon nitride (Si_3N_4) and silicon dioxide (SiO_2).*

The presence of the LDDs is crucial for modern technologies but since the spacers are constituted of oxides and silicon nitride, they are sensitive to ionizing radiation [72, 89]. In fact, they introduce two radiation-induced distinct mechanisms. Two test structures are available to investigate the RISCEs: transistors with a large channel width (20 µm) and enclosed layout transistors in order to strongly reduce or eliminate RINCEs.

The degradation observed due to the presence of the spacers is caused by to two different effects [72]: the first consists in an accumulation of charges just above the LDDs (Figure 4.14a) that lead to a an increase in the series resistance and a decrease of the maximum drain current. The second effect concerns the transport of hydrogen ions (protons) from the spacers to the gate oxide, which lead to the creation of interface traps directly in the gate oxide causing an important threshold voltage shift (Figure 4.14b and 4.14c).



(a) *Generation of charges in the spacer and formation of oxide and interface traps above the LDDs.*

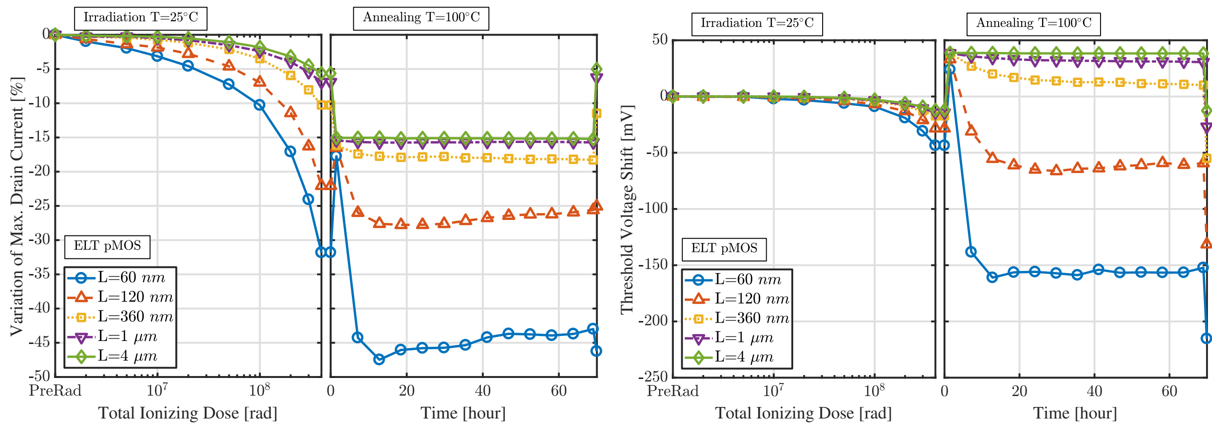
(b) *Transport of hydrogen ions from the spacer to the gate oxide.*

(c) *Formation of interface traps at the gate oxide interface.*

Figure 4.14: *Mechanisms involved in the Radiation-Induced Short Channel Effects (RISCEs).*

It has been observed in the considered technology (Foundry A) [72] that in n-channel MOSFETs both effects take place at the same time during irradiation and the flow of hydrogen ions from the spacers to the gate oxide continue during annealing. However, in the p-channel MOSFETs, the significant threshold voltage shift does not occur during irradiation because the kinetics of the phenomenon is only strongly accelerated above an approximate temperature of around 60 °C. Thus, if the irradiation is performed at room temperature followed by an high temperature annealing, both effects can be studied separately, one during irradiation and the other during annealing.

This behavior is shown in Figure 4.15, the first decrease of the maximum drain current is mainly due to the increase of the parasitic series resistance (resistivity perceived by the current flowing in the transistor [90]) during irradiation and is strongly channel length dependent (Figure 4.15a). During high temperature annealing, an important threshold voltage shift occurs that decreases again the maximum drain current (Figure 4.15b). The observed threshold voltage shift is also dependent on the channel length, indicating that a longer channel length attenuates these effects.

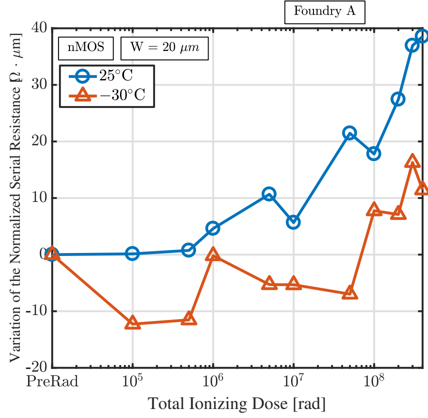


***(a)** Maximum drain current variation.*   ***(b)** Threshold voltage shift.*

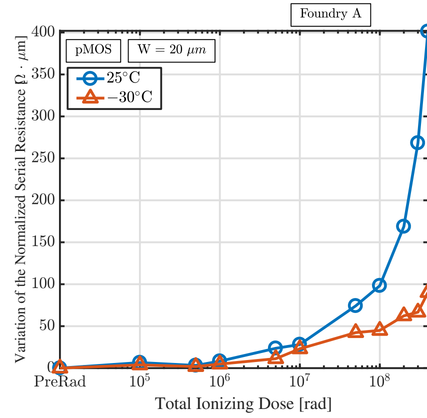
FIGURE 4.15: *RISCEs in enclosed layout p-channel MOSFETs in foundry A. The first and last point of the high temperature annealing are at room temperature indicating that the increases of the threshold voltage due to temperature is recover when cooled down.*

The transport of charges from the spacers to the gate oxide is strongly temperature dependent. The study of the time scale at which the effect unfolds was achieved by Borghello et al. [70]. The model proposed indicates that in the temperature range in which the ASICs are placed in the detectors of the particle accelerator (between −30 °C and −10 °C), the flow of hydrogen ions in n-channel MOSFETs gate oxide will take more than 400 years to halve the maximum drain current after irradiation. Therefore, this effect can be neglected in both n- and p-channel MOSFETs in foundry A, having regard that the ASICs must never be warmed up under bias. Thus, it is also not useful to model this effect for IC designers as they will not encounter it in the real application.

Figures 4.16a and 4.16b show the series resistance extracted with the method proposed by Fleury et al. [91] for both nMOS and pMOS transistors and for different temperatures. The degradation in p-channel MOSFETs is as usual larger than in n-channel MOSFETs and the degradation increases with higher temperature in both nMOS and pMOS. The increase of the series resistance correlates the location of the charges in the drain/source region and not directly in the channel.



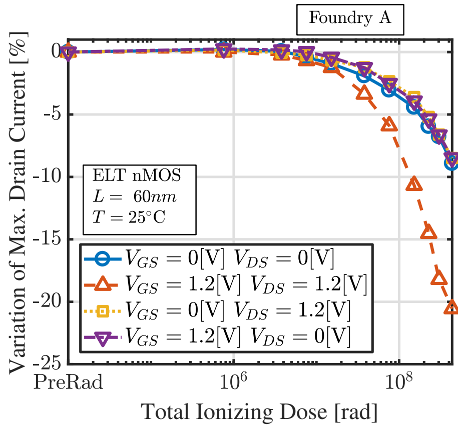
(a) n-channel MOSFET



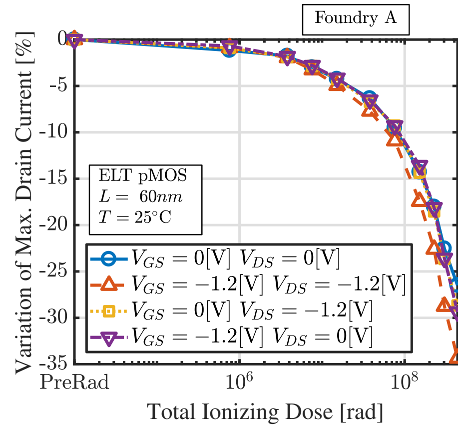
(b) p-channel MOSFET

FIGURE 4.16: *Increase of the series resistance of the transistors irradiated at different temperature [7].*

The bias during irradiation shows again an influence in the transistor degradation. The four different biases have been applied during irradiation to enclosed layout transistor. In nMOS transistor, the largest degradation has been observed with gate and drain biases applied (Figure 4.17a). In pMOS transistor, the diode configuration gives rise to the greatest degradation (Figure 4.17b).



(a) n-channel MOSFET



(b) p-channel MOSFET

FIGURE 4.17: *Influence of the polarization during irradiation for the Radiation-Induced Short Channel Effects (RISCEs).*

Figures 4.18 and 4.19 shows the evolution in maximum drain current and threshold voltage of, respectively, nMOS and pMOS transistors for different temperatures (−30 °C, 0 °C and 25 °C). The dependence with temperature is similar to the evolution of the series resistance, for both transistor types, the higher is the temperature, the higher the observed degradation in the maximum drain current. The threshold voltage shift increases as well with higher temperature but it is still very small compare to pMOS transistors.

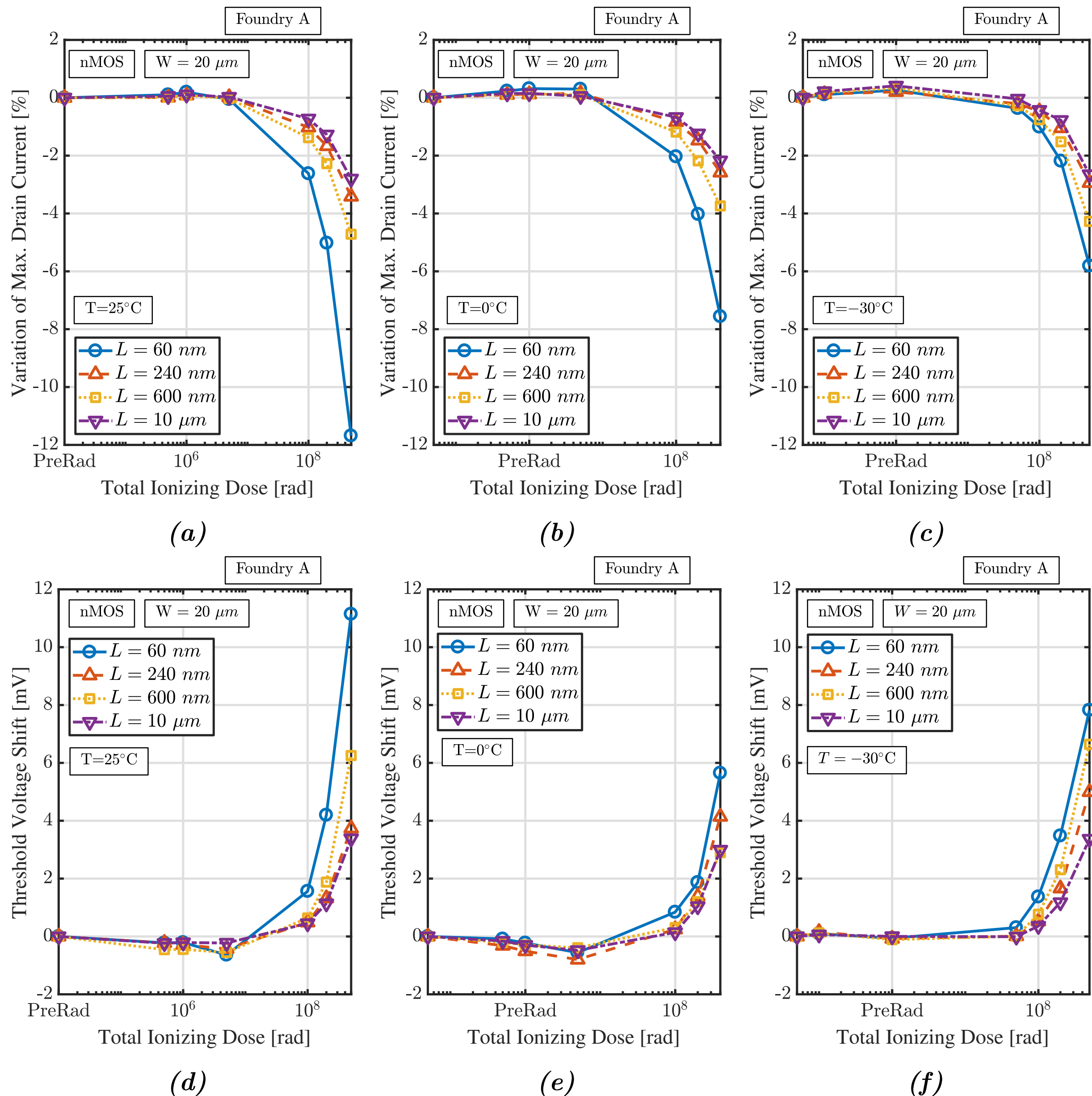


FIGURE 4.18: *Threshold voltage shift and maximum drain current degradation in standard layout nMOS transistors in due to Radiation-Induced Short Channel Effects (RISCEs).*

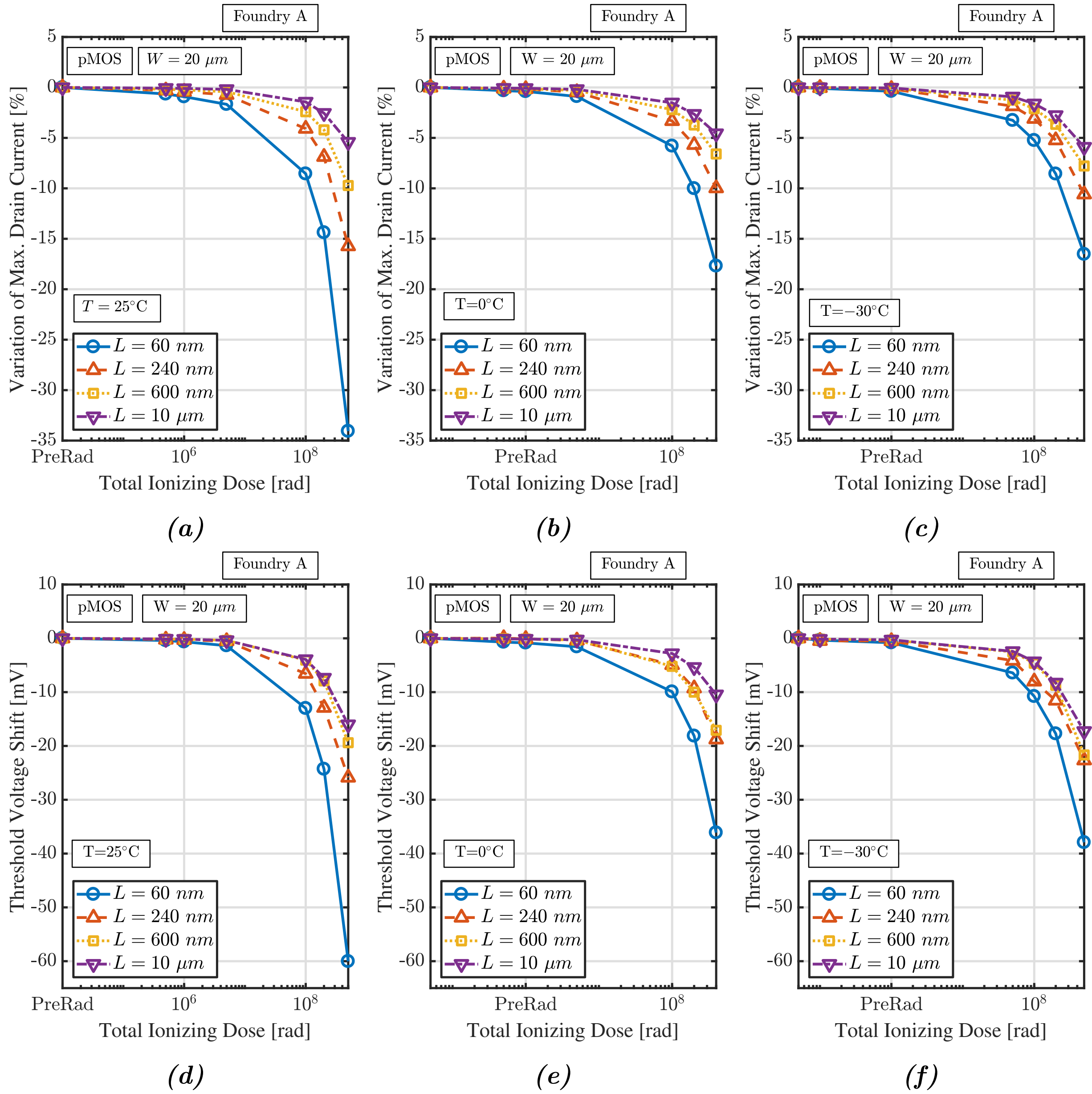
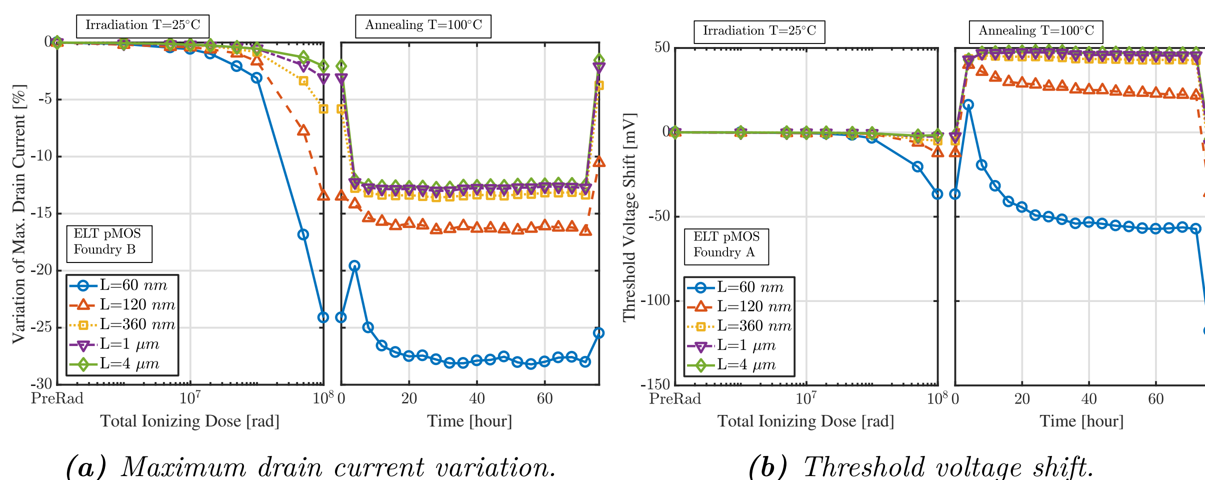


FIGURE 4.19: *Threshold voltage shift and maximum drain current degradation in standard layout pMOS transistors in due to Radiation-Induced Short Channel Effects (RISCEs).*

Radiation-Induced Short Channel Effects (RISCEs) have been recently explained by Faccio et al. [72] and they observed these effects in two technology, 65 nm and 130 nm, from foundry A. Figure 4.20 shows the irradiation at room temperature and the high temperature annealing of pMOS enclosed layout transistor issued from foundry B. We can observe a very similar behavior of the devices. During irradiation, there is a decrease of the maximum drain current and an important threshold voltage shift appears during high temperature annealing. In foundry C, the important threshold voltage shift happens already during irradiation at room temperature (data not shown). The irradiation performed in three different foundries indicates that Radiation-Induced Short Channel Effects (RISCEs) are a common degradation mechanism in the 65 nm node.



(a) Maximum drain current variation. *(b) Threshold voltage shift.*

FIGURE 4.20: *RISCEs in enclosed layout p-channel MOSFETs in foundry B. The first and last point of the high temperature annealing are at room temperature indicating that the increases of the threshold voltage due to temperature is recover when cooled down.*

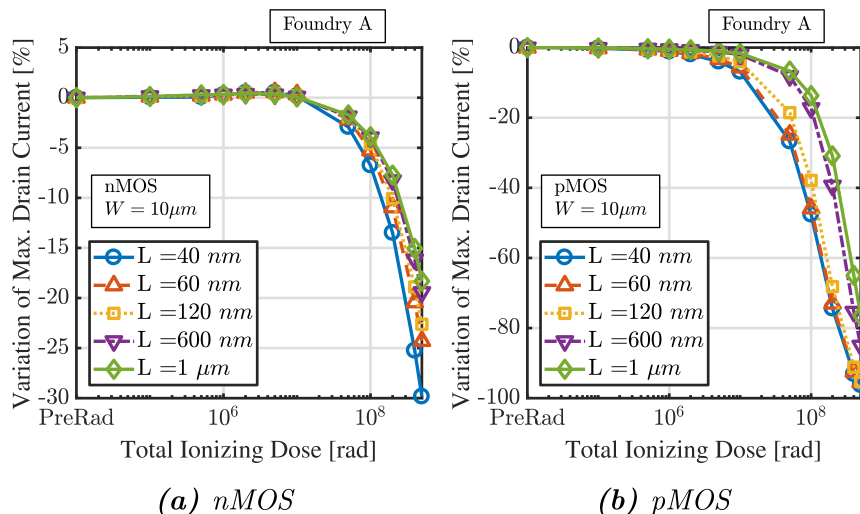
Chapter 5

Study of TID Effects in Advanced Nodes

In 65 nm technology, a reasonable understanding of the different radiation-induced effects has been achieved. The investigation of radiation response in smaller technological nodes has begun with the 28 nm and 40 nm for different foundries. The scale down to smaller dimensions leads to modifications of the traditional structure of the devices [55] but most of these modifications are not disclosed by the foundries. In this chapter, we will present preliminary results for the test of 28 nm and 40 nm technologies against ionizing radiation for foundry A.

5.1 40 nm Technology

To the best of our knowledge, the 40 nm of foundry A does not present major modification in the transistor structure (same gate oxide and no introduction of high-k material), the radiation response is worse than 65 nm. The degradation of the maximum drain current for nMOS and pMOS is shown in Figures 5.1 for different channel length and a large channel width, which should in principle alleviate RINCEs. The degradation in pMOS transistors is significant and already at 500 Mrad most of the transistors show a percentage decrease of the maximum drain current higher than 80%. In the previous technology, nMOS transistors have shown a better response than p-channel MOSFETs. The same behavior is observed but the degradation in n-channel MOSFETs is extremely high compared to 65 nm, around three times more.



(a) *nMOS* ***(b)*** *pMOS*

FIGURE 5.1: *Maximum drain current degradation for wide transistors with different channel length in foundry A for* 40 nm *technology irradiated up to* 500 Mrad *at room temperature in diode configuration.*

The higher degradation compared to 65 nm is again observed for transistors of different channel widths and long channel length, which should mitigate RISCEs. For n-channel MOSFETs (Figure 5.2a), the first increase of the maximum drain current is already higher than in 65 nm technology but the decrease observed just after is around 10 times higher. Moreover, we observed an increase in the leakage current during irradiation in nMOS (Figure 5.3). pMOS transistors show also a higher degradation (Figure 5.2b) (twofold degradation compared to 65 nm).

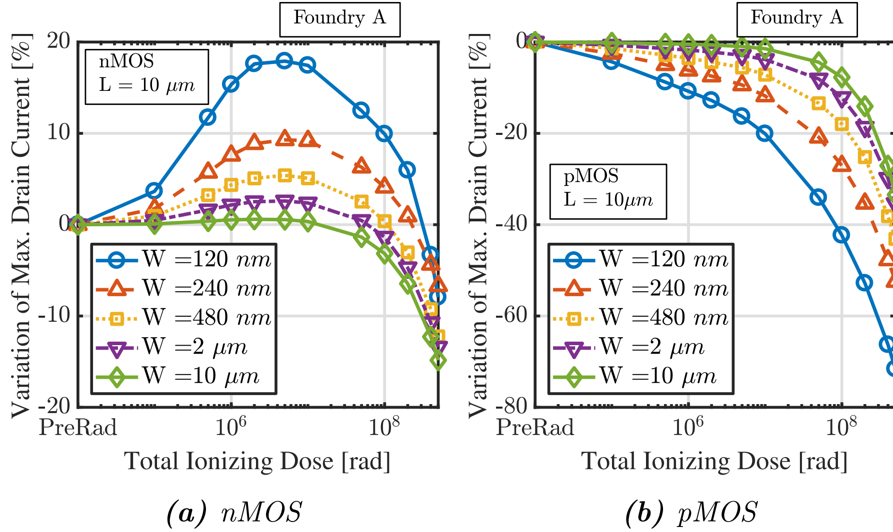


FIGURE 5.2: *Maximum drain current degradation for long transistors with different channel width in foundry A for* 40 nm *technology irradiated up to* 500 Mrad *at room temperature in diode configuration.*

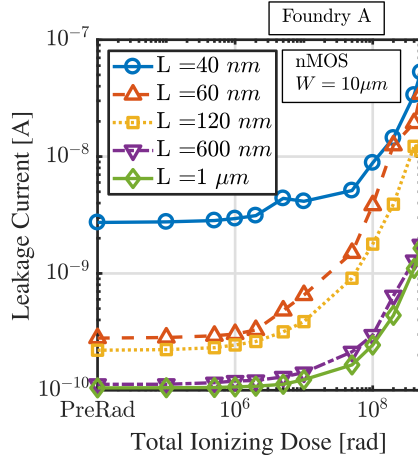


FIGURE 5.3: *Leakage current increases in foundry A for* 40 nm *technology.*

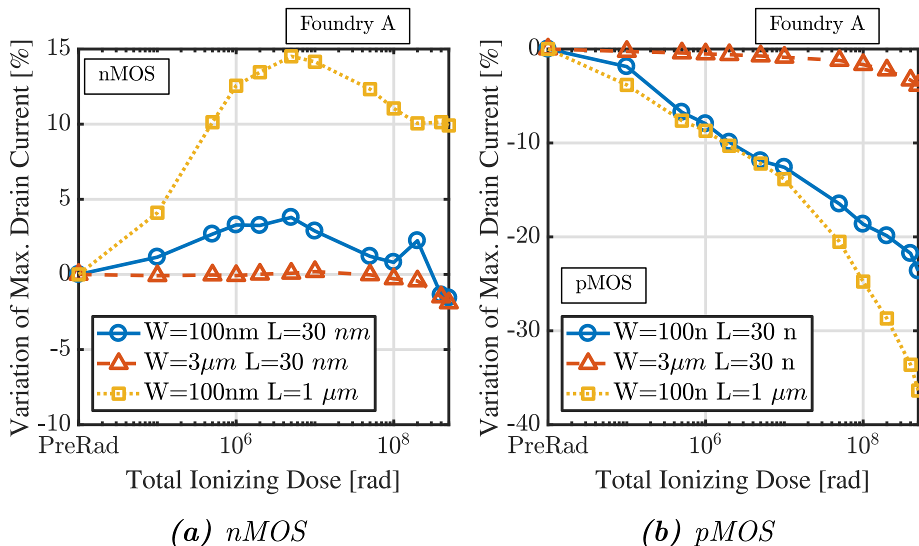
Preliminary exposure to ionizing radiation of the 40 nm technology in foundry A shows a worrisome behavior. The degradation in both type of transistors is strongly increased compared to the 65 nm technology and a significant increase in leakage current during irradiation occurres.

5.2 28 nm Technology

Irradiation of the 28 nm technology has already been performed in [92, 93, 94] and has shown an interesting radiation response. The technology studied in [92, 93, 94] is different from the one we will present in this section: it is the same technological node from the same foundry but with a different flavor and therefore we can not expect to have the same behavior (process dependence, variation in the doping profile).

In Figures 5.4, we can see the degradation of three devices, namely the narrowest and longest (minimum channel width and maximum channel length), the shortest and widest (minimum channel length and maximum channel width) and the minimum size transistors for both pMOS and nMOS transistors. In pMOS transistors (Figure 5.4b), the transistor with the largest width and minimum channel length presents a very low degradation (below 5%). Surprisingly, it is not the minimum size transistor which presents the largest degradation but the narrowest and longest as already seen in [92]. For nMOS transistors (Figure 5.4a), both minimum size and the transistor with the largest width and minimum channel length present a current variation below 5%. The transistor with the minimum channel width and maximum channel length shows the largest evolution. As well, nMOS transistors present an increase of the leakage current (Figure 5.5).

Preliminary measurements indicates that the 28 nm technology is a potential replacement for the 65 nm technology currently used. The technology shows a very robust behavior against ionizing radiation. Further measurements will allow to understand more deeply the radiation response of the devices which present some differences from the 65 nm technology.



***(a)** nMOS*   ***(b)** pMOS*

FIGURE 5.4: *Maximum drain current degradation for different transistors in foundry A for* 28 nm *technology irradiated up to* 500 Mrad *at room temperature in diode configuration.*

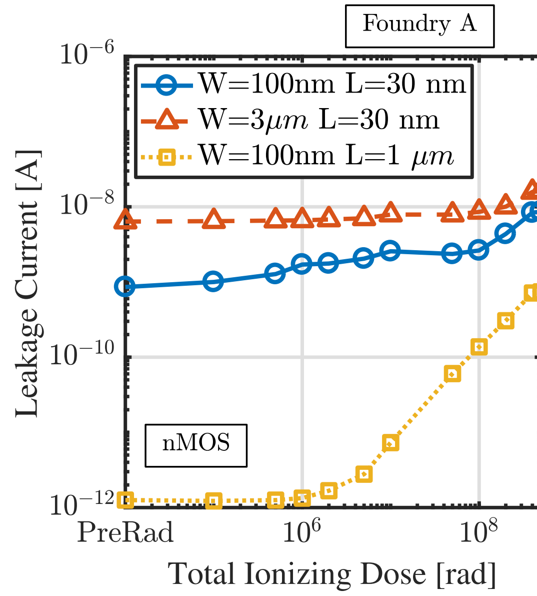


FIGURE 5.5: *Leakage current increases in foundry A for* 28 nm *technology.*

Conclusion and Future Perspectives

The ten-fold increase in luminosity in the future upgrade of the LHC results in a significant increase in the number of collisions in the various detectors distributed along the particle accelerator. The higher number of collisions will increase the amount of interesting events for particle physicists. However, the important increase in particle collisions will result in an unprecedented level of radiation in the detectors. This high radiation level is a concern for the electronics in the detectors as radiation damages the transistors. Such high level of ionizing radiation has never been reached before in practical applications.

The qualification to total ionizing dose (TID) of the 65 nm CMOS technology used in the development of ASICs for the High-Luminosity Large Hadron Collider (HL-LHC) was realized. The qualification was performed within the temperature range of interest (−30 °C, 0 °C and 25 °C) up to 500 Mrad(SiO_2). The different degradation mechanisms have been outlined. The data are used to create models that will allow IC designers to directly simulate the impact of TID during the design of the ASICs [20, 21, 22, 23]. In addition to these measurements, the radiation response of different foundries have been studied in 65 nm. We showed that the behavior known as RINCEs and RISCEs are also observed in at least three different foundries, which increases our confidence that what we observed are general behaviors in this commercial node.

The study of total ionizing dose effects of two new technological nodes began, namely 40 nm and 28 nm technologies, from different manufacturers. The continuous down scaling of the CMOS technology brings out numerous challenges as shown in the International Technology Roadmap for Semiconductors (ITRS) roadmap [55]. Because the scaling of CMOS transistors become increasingly difficult, it accelerates the introduction of new technologies into semiconductor structures. In fact, there have been more changes in the device structure in the past decade than in the previous forty years [55]. It is therefore interesting to study the TID tolerance of these more advanced commercial nodes whose development has different, and sometimes opposite, objectives than the radiation tolerance.

The down scaling of the planar bulk CMOS transistor studied during this work (Figure 5.6) is stopped near the 20 nm technological node [Web13] due to large increase of the leakage current and parasitic effects (e.g. short channel effects) and high variability during fabrication [95]. The foundries therefore opted for a different geometry, namely the FinFets (Figure 5.6) to continue the scaling down to 5 nm. In the literature, irradiation of such devices have been performed up to 1 Mrad [96, 97, 98, 99] and are showing mixed performances, particularly worrisome in terms of leakage current. The GaaFet (Figure 5.6) is another geometry planned below 5 nm and the pioneering works indicated an interesting radiation response [100, 101] because the channel of the transistors is not in contact with any isolating layer [102].

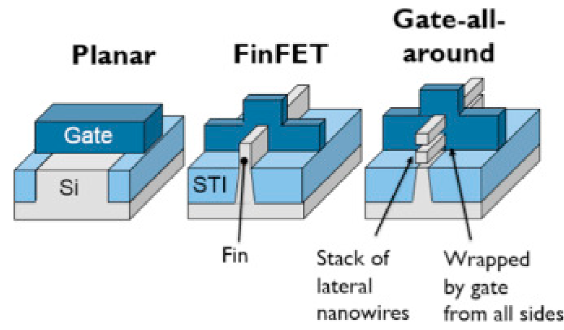


Figure 5.6: *Schematic illustration of different CMOS technologies. Planar corresponds to Bulk CMOS technology and two advanced node are shown, namely FinFet and GaaFet. (From [103]).*

The next big project for particle physics research will be defined in the next update of the European Strategy for Particle Physics (2018-2020) [Web14]. Two major projects are considered to replace the current particle accelerator, namely the Compact Linear Collider (CLIC) [104, 105] and the Future Cicular Collider (FCC) [106].

FCC is characterize by an important increase of the luminosity compared to HL-LHC and therefore of the level of radiation. The foreseen total ionizing dose (TID) in some part of the detectors in FCC reached value of 500 Grad [107]. The commercial technologies presented in this work are already significantly damaged at 1 Grad. Therefore, such high level of TID brings new challenges for the use of commercial technologies in a radioactive environment.

Appendix A

European Organization for Nuclear Research

European research has been the dominant movement in countless major discoveries and breakthroughs. These advances are associated with names like Albert Einstein, Erwin Schrödinger, Max Planck, Marie Curie or Niels Bohr in what it is now called Modern Physics (quantum physics, general theory of relativity). Indeed, the gathering of physicists at the Solvay conference of 1927 (Brussels, Belgium) laid the foundations of quantum theory which was mainly composed of European scientists (Figure A.1).

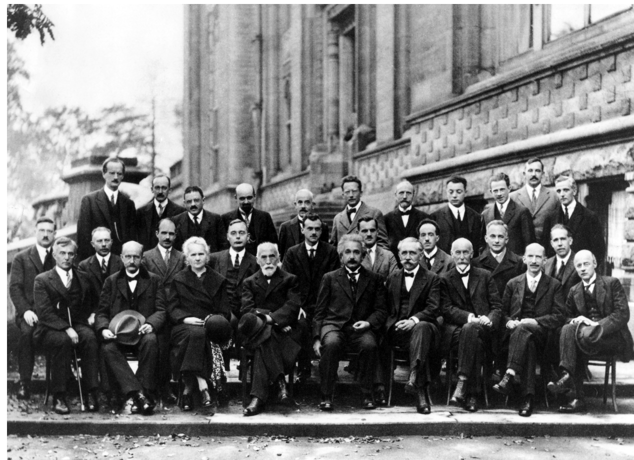


FIGURE A.1: *Solvay Conference in Brussels, 1927. In the picture can be found among others: P. Ehrenfest, E. Schrödinger, W. Pauli, W. Heisenberg, L. Brillouin, P. Debye, P.A.M. Dirac, L. de Broglie, N. Bohr, M. Planck, M. Curie, H.A. Lorentz, A. Einstein, P. Langevin. Photograph taken by Benjamin Couprie [Web15].*

At the end of World War II, most scientists end up in the United States of America due to the lack of subsidy while the cost of advanced research continued to rise due to increasingly expensive equipment and experimental dimensions that reached even higher industrial standards [108]. It left Europe on the second level.

French physicist Louis de Broglie was the first to put officially forward the need to create a European laboratory during the European Cultural Conference (Switzerland, Lausanne, 9 December 1949). This willingness has been intensified during the next UNESCO General Conference (Italy, Florence, June 1950) where a resolution was tabled to allow UNESCO

in assisting the development of regional research laboratories. The seeds of what will be the world's largest laboratory were there. During an intergovernmental meeting of UNESCO (France, Paris, December 1951), the first resolution was adopted for the creation of a European Council for Nuclear Research followed by the signature of 11 states to establish a provisional council under the acronym CERN (*Conseil Européen pour la Recherche Nucléaire*).

Several applications were submitted to host the new European laboratory. Geneva was selected in 1952 by the provisional council and a referendum was held on June 1953 in the canton of Geneva that authorized the establishment (16539 votes against 7332) [108]. The city had several arguments in its favour. Geneva has always been an international city and has a strong liberal tradition which strengthens the feeling of future total political independence. Furthermore, the association of Switzerland with the project has required guarantees in the post World War II context such as no secrecy and only scientific purpose for the new European laboratory. The construction began the next year in Meyrin located in the canton of Geneva.

Rutherford discovered in 1919 that it is possible to modify artificially the atomic structure but it was necessary to wait for the advent of quantum mechanics to understand that it is possible to cross the nuclear potential barrier with a non-zero probability, which was not the case in classical mechanics [109]. Scientists understood that it was possible to study the composition of matter by disintegrating it and that the energy of the particle plays a crucial role in this process. As soon as 1928 particle accelerators started to be built but slowed down by the highly technical requirements.

The first CERN accelerator is the 600 MeV Synchrocyclotron and was built in 1957 followed by the Proton Synchrotron (PS) which started for the first time on 24 November 1959 providing a beam energy of 28 GeV. In 1976, the Super Proton Synchrotron (SPS) was launched which was the first CERN underground rings and operates with beam energy of 400 GeV. A major discovery was made in 1983 during a proton-antiproton collision which highlighted the W and Z particles allowing for the key scientists behind the work to receive the Nobel Prize. The next accelerator was the LEP, a 27 km underground ring operating at the energy of 100 GeV to finally reach 207 GeV before the end of its operation. The LEP gave way to the current accelerator, the Large Hadron Collider (LHC), that reuses its underground facility.

A.1 CERN Structure

CERN is an international organization controlled by its member states. The number of member states at the present time is 22 and they are all situated in Europe except for Israël (Figure A.2).

The highest authority of CERN is the council which is responsible for the most important decisions. In particular, it decides about the scientific, technical and administrative domains, it approves the budget and regulates the expenditure. The council is formed by two official delegates from each of the 22-member states, one is a representative of the government's administration while the other represents the national scientific interests. Each member state has one vote and the decisions are subject to a vote which requires a simple majority. In general, discussions are engaged to be as close as possible to unanimity. The council is assisted and advised by the Finance Committee (as regards the budget and expenditure) and the Scientific Policy Committee (related to scientific activity).

The council is also responsible for the appointment of the Director-General (DG), usually for a period of 5 years. The DG proposes the members of the directorate which will assist the DG to manage CERN. The DG manages CERN through a structure of departments (Figure A.3). The current DG is Fabiola Gianotti, an Italian particle physicist. She is the first women to hold this position. Her mandate will last from 2016 to 2021.

There are 13 departments at CERN. Each of them is responsible for a specific task aggregated around the same objective of making knowledge evolve thanks to the LHC.

The Experimental Physics (EP) Department performed research in experimental particle physics. My master's thesis is done in the EP Department at the Electronic for Experiment group (ESE) in the Microelectronics (ME) section. The EP-ESE-ME is mainly responsible to develop ASICs able to meet expectations in terms of radiation hardness and functionalities for the experiment detectors. The ESE group is a support group that helps the main experiments of CERN. The EP Department is one of the largest at CERN (500 staff members and 300 members such as students, apprentices, associates or fellows) and is composed of many different groups with their respective sections.

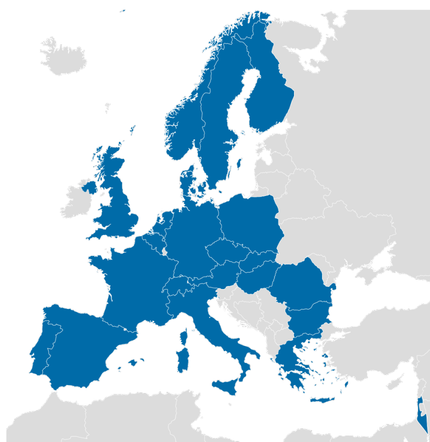


FIGURE A.2: *Map of member states of the European Organization for Nuclear Research (coloured in blue) [Web16].*

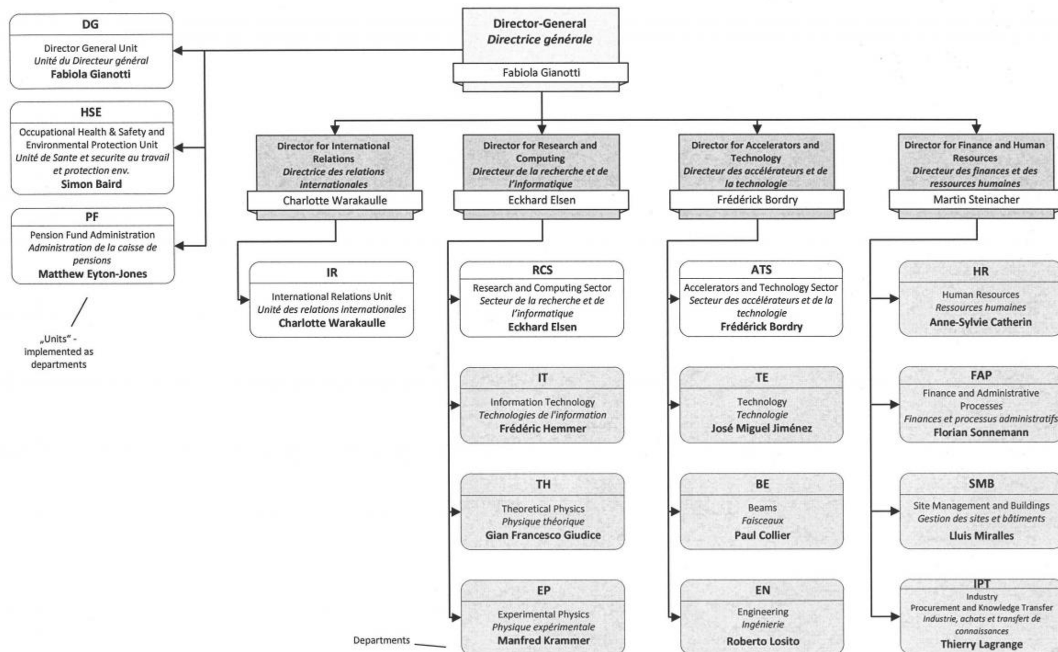


FIGURE A.3: *Management structure of CERN with the different departments [Web17].*

A.2 CERN Finance

CERN receives its subsidies from the 22-member states. It corresponds to the most important part of the budget (more than 90%). The Figure A.4 indicates the contribution of each member state. We can notice that Germany, United Kingdom, Italy and France contribute alone for more than 60 % of the total budget in 2018 while Belgium contributes to 2.7 %. The percentage of contributions is not strongly affected year after year.

The total budget from the years 2006 to 2018 is shown in Figure A.5. The mean budget for these years is 1104 million Swiss francs (CHF). The budget decreased after the commissioning of the LHC in 2008 and increased with the beginning of the research for the future upgrade of the LHC.

Figure A.6 shows a pie chart of planned spending for the year 2018. We note that 21.1% of the budget is allocated to the LHC and its operation but also to the detectors of the various experiments. 19.9% is for other scientific programs such as R&D for sensors, the two old particle accelerators and non-LHC physics. The projects of R&D corresponds to 21.7 % of the budget. It corresponds to the research for the future upgrade of the LHC as well as for the research for the future of particle accelerators. The rest of the budget is affected at various costs such as infrastructure and services, energy and water.

	Country	2018 Annual contribution in CHF 2017 prices	2018 Annual contribution in CHF 2018 prices	2018 Annual contribution in %
Member States	Austria	24 027 000	24 091 850	2.14546%
	Belgium	30 310 300	30 392 150	2.70652%
	Bulgaria	3 277 950	3 286 800	0.29270%
	Czech Republic	10 447 450	10 475 650	0.93289%
	Denmark	20 184 950	20 239 450	1.80239%
	Finland	14 906 100	14 946 350	1.33102%
	France	158 120 300	158 547 200	14.11914%
	Germany	230 134 900	230 756 250	20.54959%
	Greece	12 533 450	12 567 300	1.11916%
	Hungary	6 849 650	6 868 150	0.61163%
	Israel	18 080 550	18 129 350	1.61448%
	Italy	116 790 550	117 105 900	10.42866%
	Netherlands	51 611 950	51 751 300	4.60862%
	Norway	30 352 200	30 434 150	2.71026%
	Poland	31 568 950	31 654 200	2.81891%
	Portugal	12 334 000	12 367 300	1.10135%
	Romania	11 451 750	11 482 650	1.02257%
	Slovakia	5 467 250	5 482 000	0.48819%
	Spain	78 860 550	79 073 450	7.04175%
	Sweden	30 117 900	30 199 200	2.68934%
	Switzerland	45 071 600	45 193 300	4.02461%
	United Kingdom	177 400 750	177 879 750	15.84076%
Total Member States		**1 119 900 050**	**1 122 923 700**	**100.0000%**
Associate Member States in pre-stage	Cyprus	1 000 000	1 000 000	
	Serbia	1 914 950	1 920 100	
	Slovenia	1 000 000	1 000 000	
Total Associate Member States in the pre-stage to Membership		**3 914 950**	**3 920 100**	
Associate Member States	India	12 239 000	12 272 050	
	Pakistan	1 498 350	1 502 400	
	Turkey	5 603 900	5 619 000	
	Ukraine	1 000 000	1 000 000	
Total Associate Member States		**20 341 250**	**20 393 450**	
Grand TOTAL		**1 144 156 250**	**1 147 237 250**	

FIGURE A.4: *Contributions of the member states to the CERN budget for the financial year 2018 in million Swiss francs (CHF) [110].*

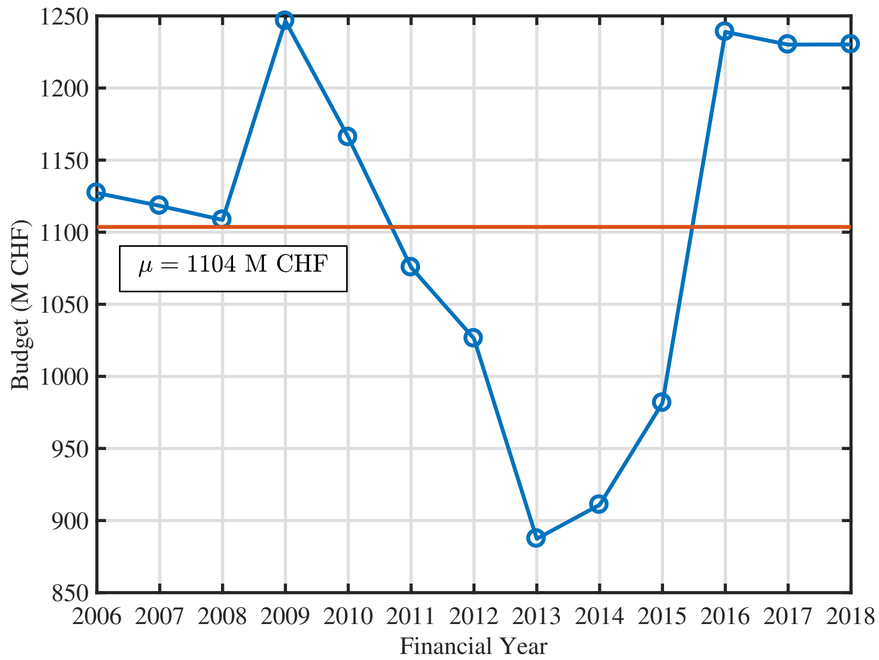


FIGURE A.5: *Evolution of the CERN budget from 2006 to 2018 (data extracted from [Web18]).*

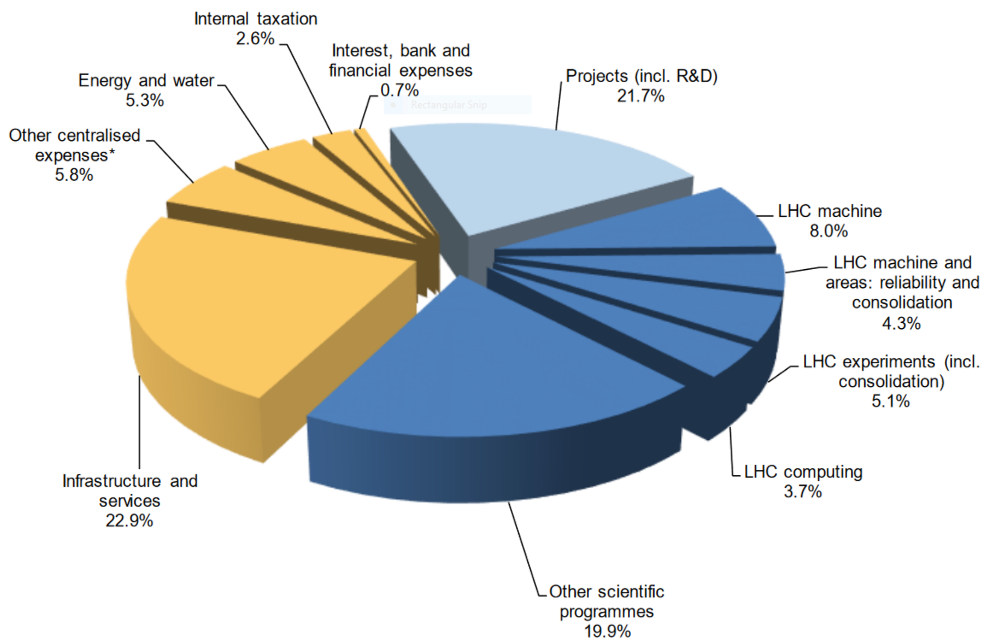


FIGURE A.6: *Breakdown of the budget for the financial year 2018 [110].*

Appendix B

Uncharted Radiation-Induced Effects

In this chapter, we will briefly describe some effects that have not yet been fully understood or that show counter-intuitive behavior. The simple principle of charge accumulation in different oxides and the underlying time difference between oxide trap generation and interface traps seems to be insufficient to explain these effects.

B.1 1-6 Mrad **Leakage Peak**

It is well known that some technologies irradiated above 1 Mrad face a significant increase in leakage current (several orders of magnitude). This behavior has been attributed to the presence of oxide traps in the STI [84]. The actual impact of this effect is extremely process dependent. For example in 130 nm technology, in the same manufacturer, the leak peak was observed in only one fabrication plant (Figure B.1) indicating a variation from fab to fab. The same increase in the leakage current has been observed in one 65 nm process (Figure B.2).

In the same range of TID and regardless of the considered process, one can observe an increase of the maximum drain current in both linear and saturation region (Figure B.4). This increase has also been attributed to oxide traps in the STI [73] that produce a negative threshold voltage shift in the $I_D - V_G$ characteristic (Figure B.3).

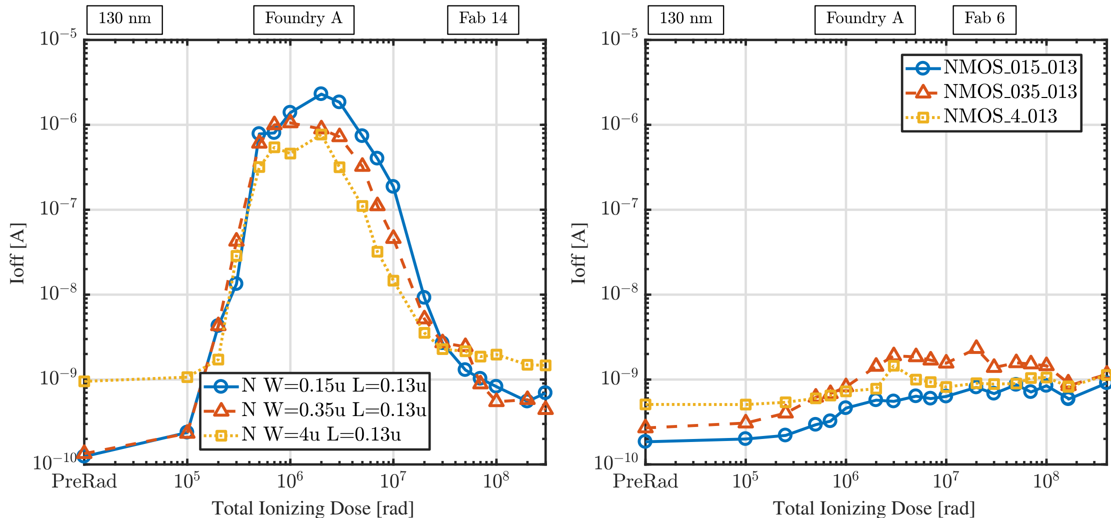


FIGURE B.1: *Leakage current measured during irradiation from the same commercial node (*130 nm*) but from two different fabrication plants (Fab). Left: the leakage current in the range of* 1-6 Mrad *increases by four order of magnitude. Right: the leakage current increases steadily during the irradiation but less than one order of magnitude.*

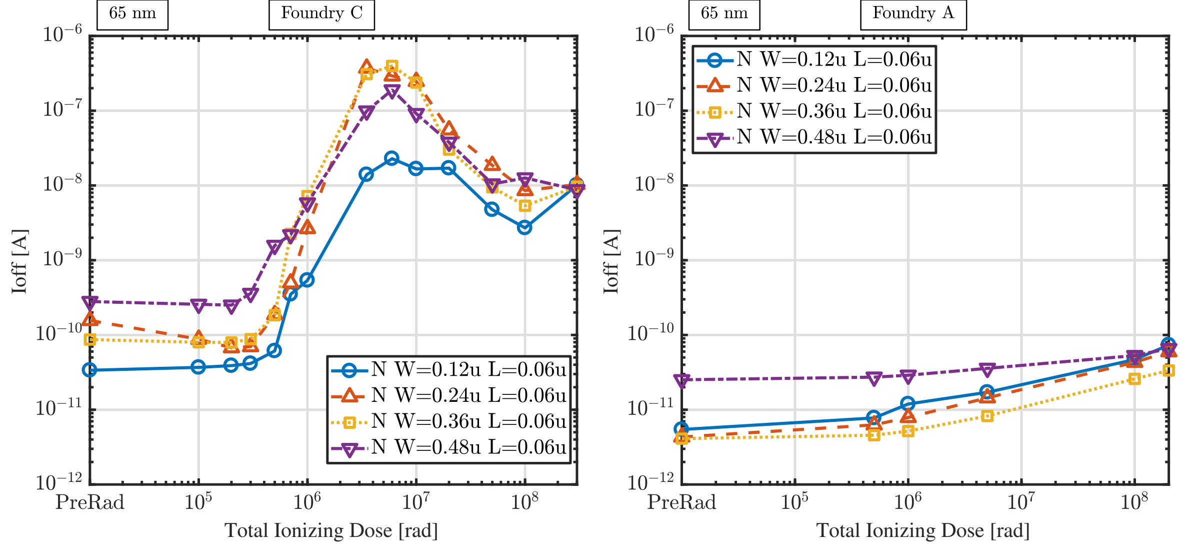


FIGURE B.2: *Leakage current measured during irradiation from the same commercial node (65 nm) but from two different foundries.*

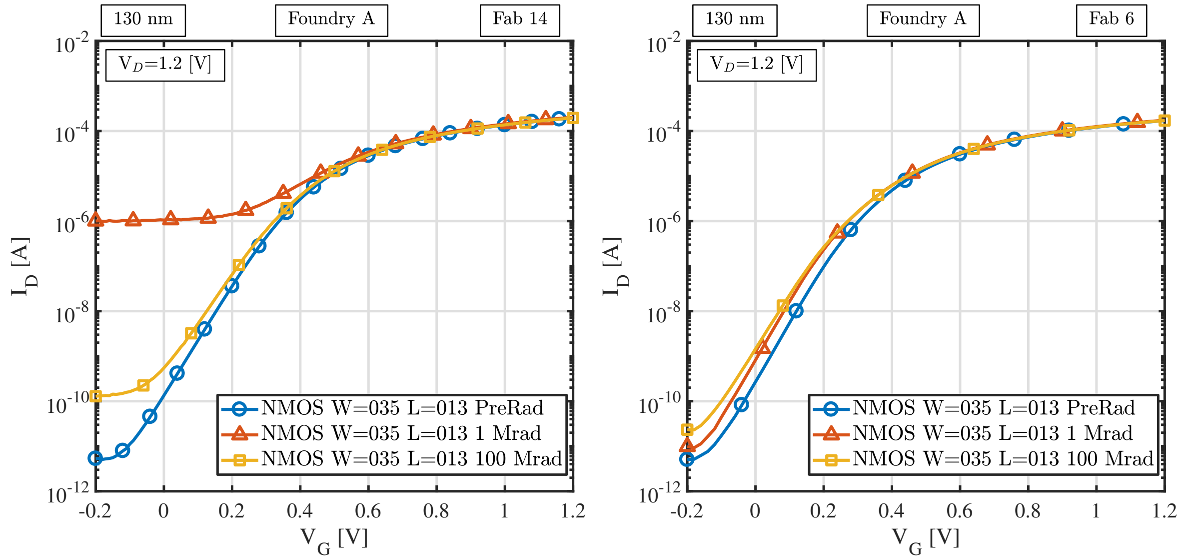


FIGURE B.3: $I_D - V_G$ *characteristic of two* 130 nm *processes from the same foundry but different fab. Left: with leakage peak. Right: without leakage peak. The threshold voltage shift is present in both cases while the increase of the leakage is only observe in one.*

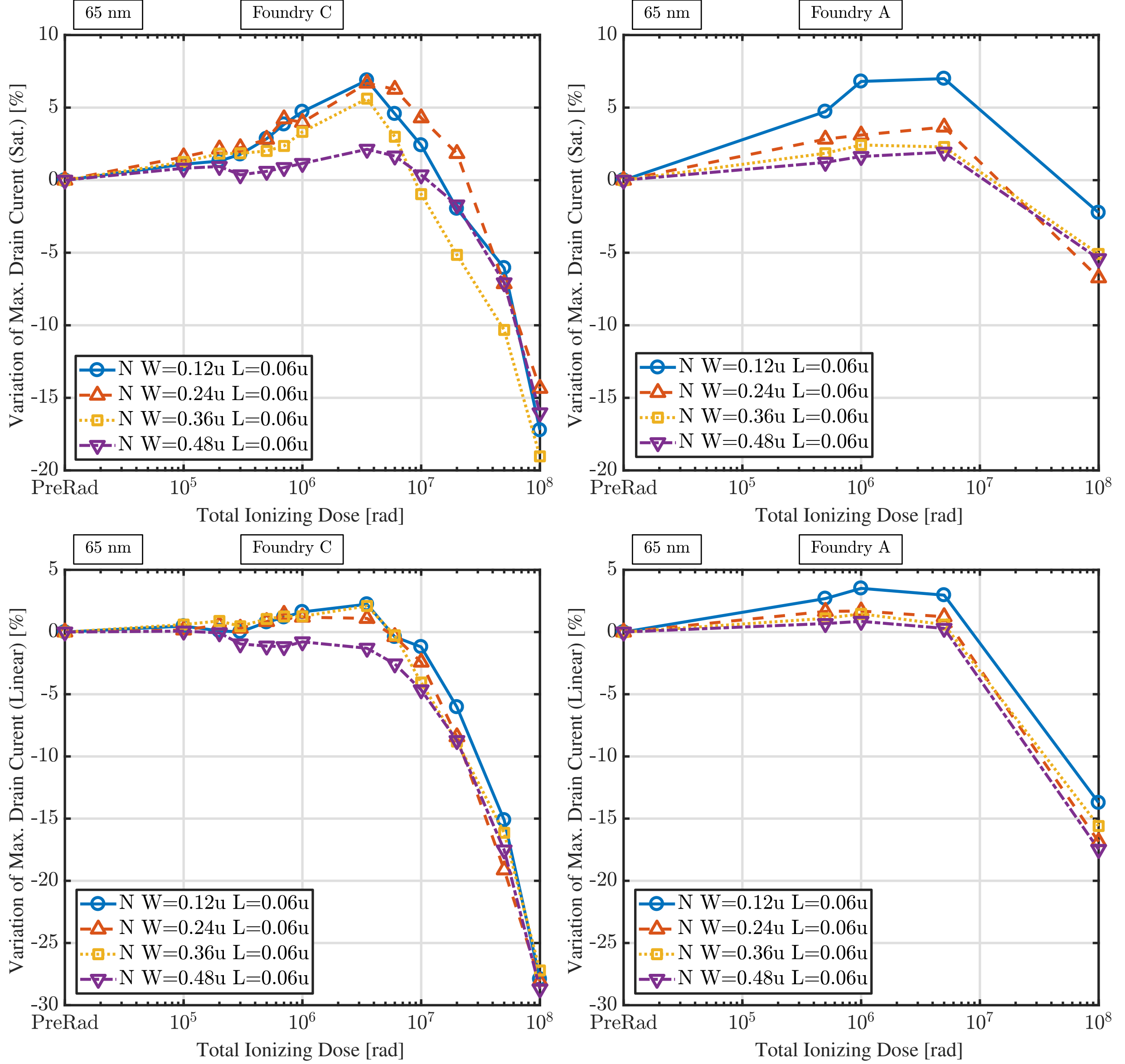


FIGURE B.4: *Evolution of the maximum drain current in both linear and saturation for two different foundry in* 65 nm *technology. Top left: foundry C, saturation region. Top right: foundry A, saturation region. Bottom left: foundry C, linear region. Bottom right: foundry A, linear region.*

The increase of the leakage and the threshold voltage shift are both related to the presence of oxide traps in the STI but we observe that in some process one is present while the other is absent. The physics behind these phenomena is not simple and the effect of the charge strongly depends on the applied electric field. This requires a more sophisticated model that has not yet been developed.

B.2 High Dose Induced Leakage

Some technologies that do not have a significant peak in leakage current at TID around 1-6 Mrad still show a steady increase of the leakage during irradiation as shown in Figure B.5. The increase of the leakage is very small and it is only possible to detect it at very high total doses. The same behavior was observed in two 65 nm processes as well as in 130 nm technology.

At very high doses, the radiation response of the maximum drain current becomes dominated by interface traps (Figure B.4) while the increase in the leakage indicate a continuous increase of the influence of oxide traps. This is different to the explanation of 1-6 Mrad leakage peak behavior where interface traps counterbalance the effect of oxide trapped charge. To some extent, the behavior of the leakage is more similar to what is observed in 28 nm process (Figure B.6) where the increase is much more significant but steady. Without a more detailed study we can not conclude about the origin of this leakage current compared to the 1-6 Mrad leakage.

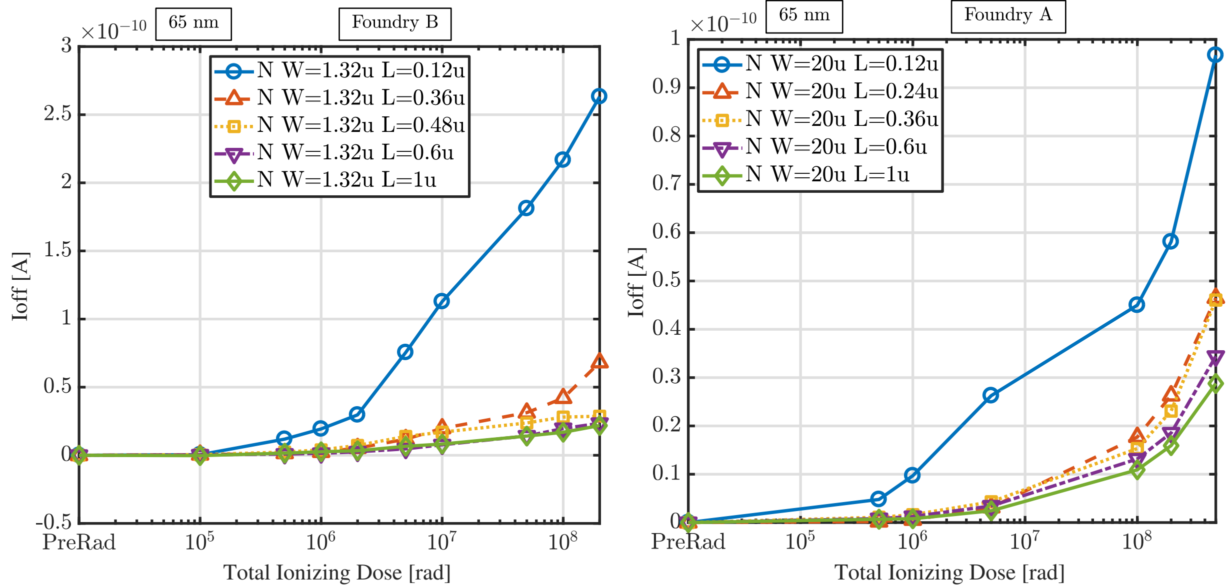


FIGURE B.5: *Increase of the leakage current at very high dose for two different* 65 nm *processes. Both show a channel length dependence.*

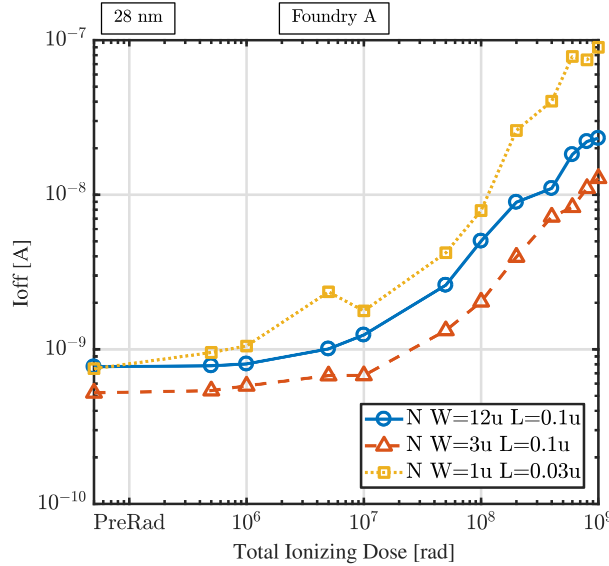


FIGURE B.6: *Increase of the leakage current at very high dose for a* 28 nm *process [92].*

B.3 Bias Dependence During Irradiation

Figure B.7 represents the classical irradiation performed to study the influence of polarization in the radiation response of transistors. Four devices of the same dimensions are integrated on the same structure, it is thus possible to irradiate the devices at the same time with four possibilities of drain and gate polarization. The worst cases irradiation are given when a gate bias is applied and produces the highest degradation. In the case of the bias with only drain voltage applied, the maximum drain current increases steadily with TID. The same behavior was observed in another foundry of the same technology (Figure B.8). The drain bias dependence is only observed in n-channel MOSFETs. In particular, it can be observed that the increase of the current occurred only in the saturation region for foundry A while in foundry B it is as well observed in linear region.

The irradiation was repeated with different drain biases up to 700 Mrad (Figure B.9), the increase in saturation current depends on the drain bias value. A second experiment was performed to study the impact of the channel length. The array contains transistors with minimum channel width and different channel length (Figure B.10). A smaller channel length should produce an higher electric field along the transistor. The results indicate that the effect appears only in long channel and not in short channel transistors.

The $I_D - V_G$ characteristic is first impacted by the negative threshold voltage shift increasing the current in both linear and saturation region (Figure B.11 bottom). After 10 Mrad, the second effect starts to take place and produces an increase of the current only in saturation region with a increase of the transconductance (Figure B.11 top).

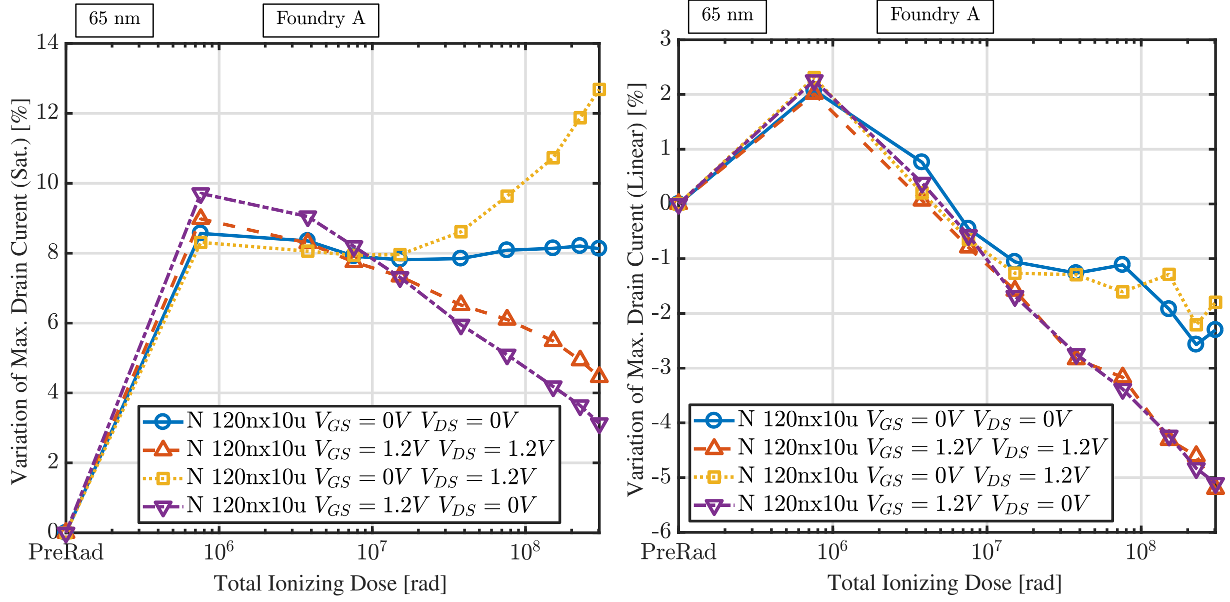


FIGURE B.7: *Irradiation of long and narrow nMOS transistors up to* 300 Mrad *with different biases in foundry A. Left: evolution of the maximum drain current in saturation region. Right: evolution of the maximum drain current in linear region.*

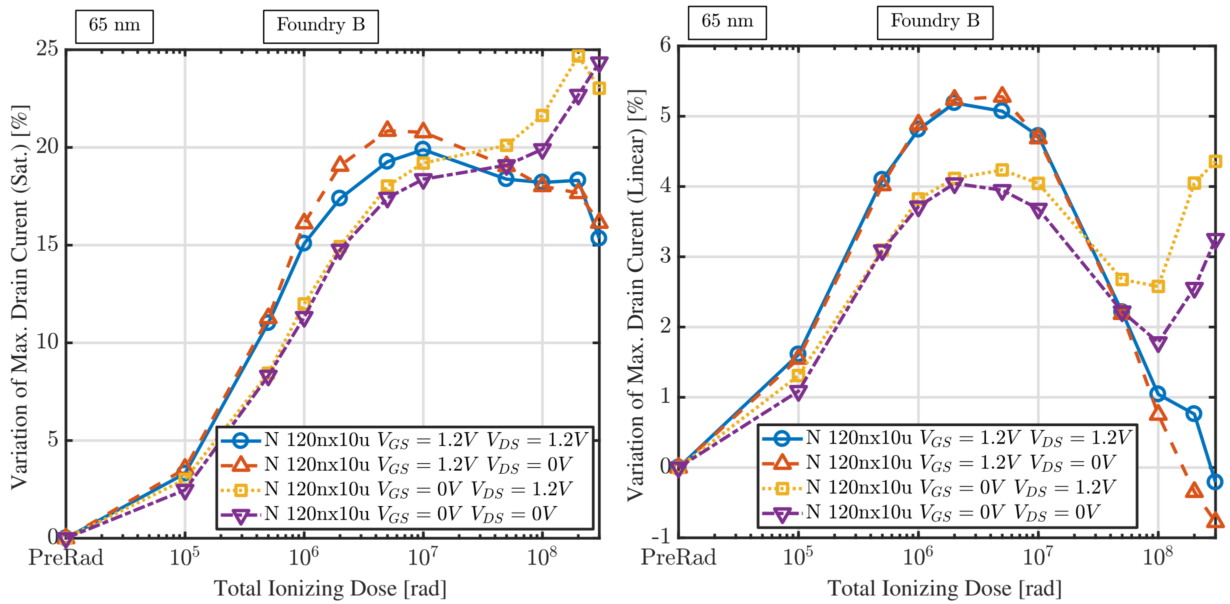


FIGURE B.8: *Irradiation of long and narrow nMOS transistors up to* 200 Mrad *with different biases in foundry B. Left: evolution of the maximum drain current in saturation region. Right: evolution of the maximum drain current in linear region.*

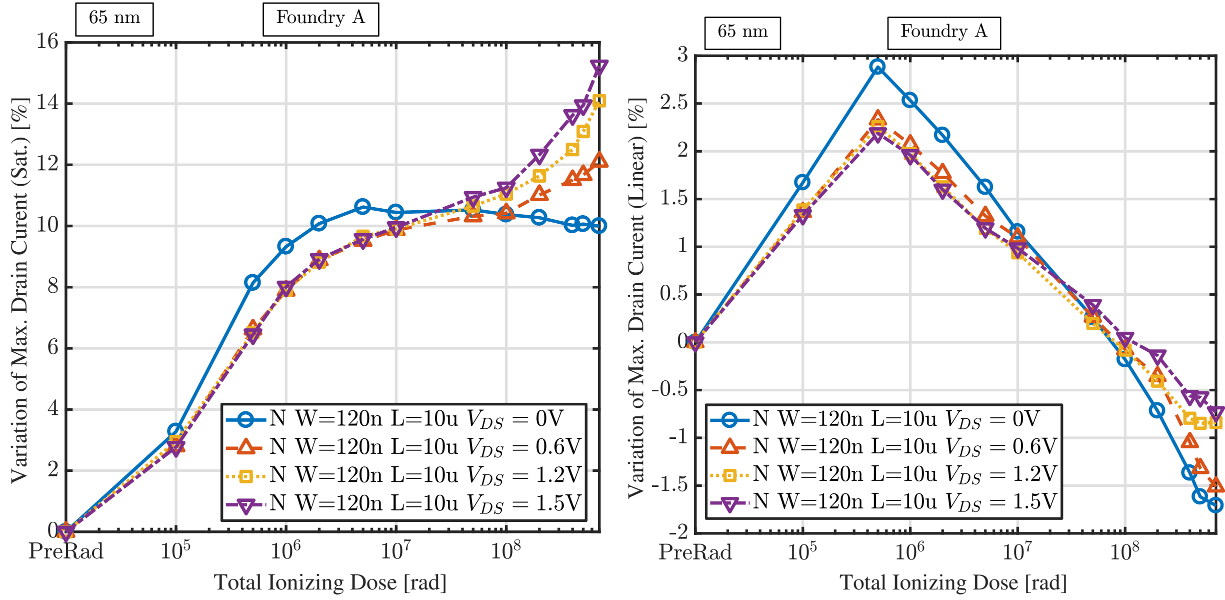


FIGURE B.9: *Influence of the drain bias during irradiation. Left: maximum drain current in saturation region. Right: maximum drain current in linear region.*

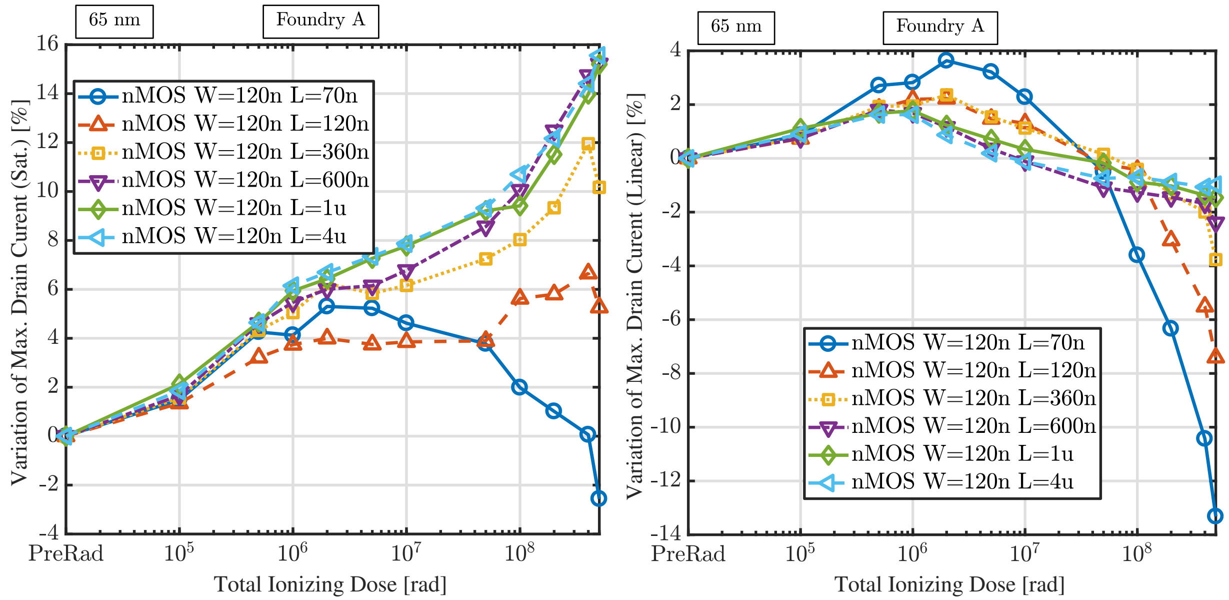


FIGURE B.10: *Influence of the channel length with narrow channel devices. The bias during irradiation was $V_{DS} = 1.2V$ and $V_{GS} = 1.2V$. Left: maximum drain current in saturation region. Right: maximum drain current in linear region.*

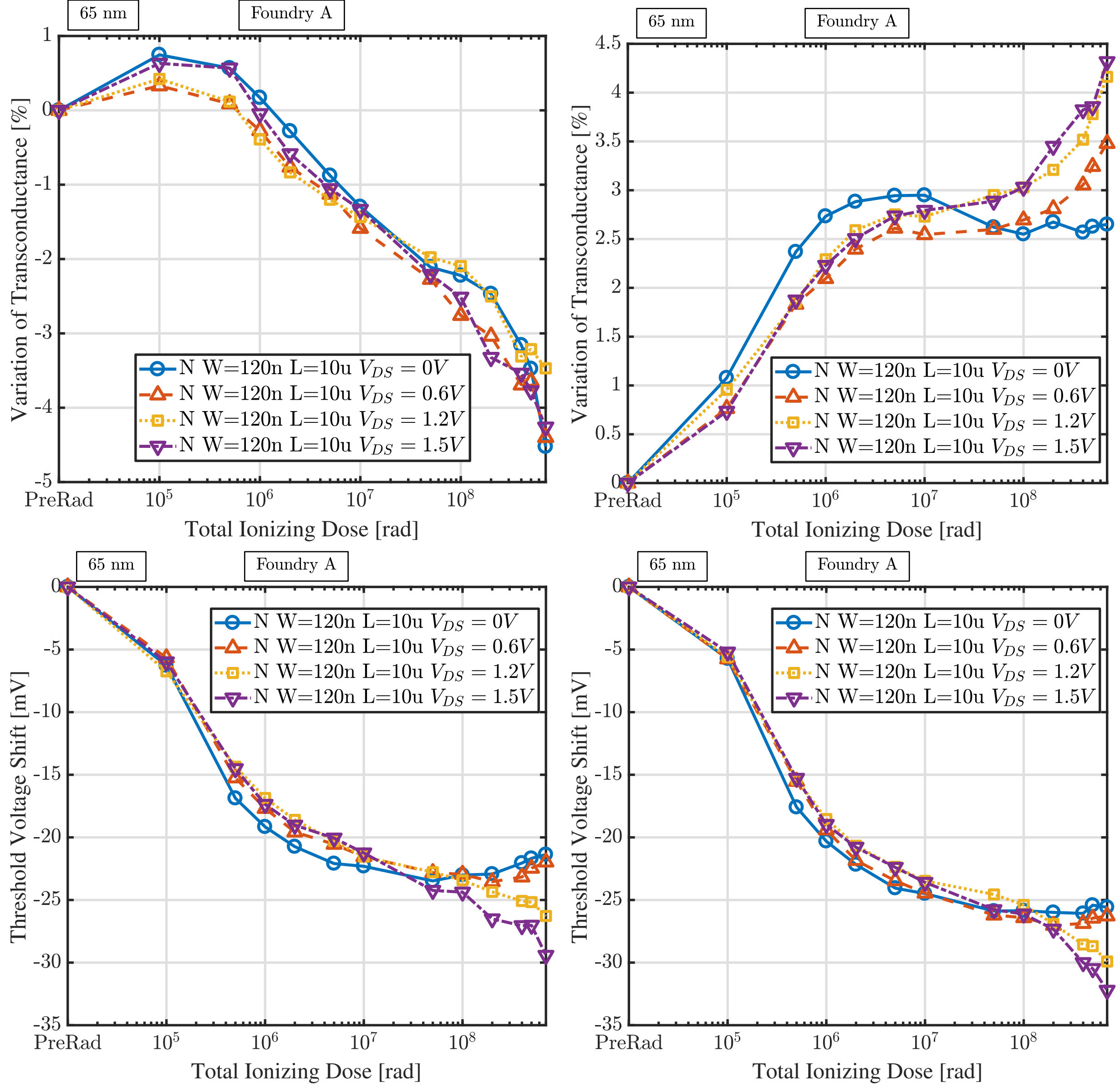


FIGURE B.11: *Variation of the transconductance and threshold voltage for different V_{DS} bias alone ($V_{GS} = 0V$) during irradiation. Top left: transconductance in linear region. Top right: transconductance in saturation region. Bottom left: threshold voltage shift computed in linear region. Bottom right: threshold voltage shift in saturation region.*

The polarization of the transistor during irradiation for long and narrow channel with V_{DS} alone seems to mitigate the influence of interface traps in the STI. Further experiments are needed to understand the influence of other parameters such as transistor width and to get a complete picture of this new effect.

B.4 Conclusion

Three radiation-induced effects are described. The first two effects are related to the increase of the leakage current during irradiation. The third effect presents a continuous increase of the maximum drain current in saturation and this even at extreme high dose. To the best of our knowledge and considering all the evidences accumulated, all this effect seems related to the STI. A more in-depth study of these effects must be undertaken to improve our knowledge of the role of STI in the radiation response of MOSFETs.

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