6 Sept. 2018

RD Collaboration Proposal: Extension of RD53

ABSTRACT: The RD53 Collaboration was established in 2013 to develop the next generation of pixel readout chips for the High Luminosity LHC detector upgrades. This proposal is to extend the scope of the collaboration to design the final pixel readout chip for the ATLAS and CMS upgrade detectors. A common design is proposed that can be fabricated with different pixel matrix sizes. The proposed work plan and resources are presented.

CERN-LHCC-2018-028 / LHCC-SR-008
07/09/2018

Contents

1. Introduction

The RD53 Collaboration was established in 2013 to develop the next generation of pixel readout chips for the High Luminosity LHC detector upgrades [1]. The collaboration was focused on building the technology foundation needed to produce large format readout chips with the basic characteristics needed by the experiments. This program culminated in the recent fabrication of the RD53A readout chip, which is working as designed and will be used by ATLAS and CMS to prototype hybrid modules for their pixel upgrades. With RD53A we can exercise all the required features: bump bonding with 300 mm wafers and 50 μm $\times$ 50 μm bump pitch, test beams and irradiations with final pixel geometry sensors, high hit rate operation, high speed I/O, serial powered module chains, etc. However, RD53A is a technology demonstrator and not a production chip. Finalization of requirements and further design work are needed to meet production requirements.

Following the success of the RD53A development, both ATLAS and CMS have requested that the RD53 Collaboration remain in place to deliver their production chip designs. The new mandate is to produce a common design, starting from a joint requirements document, but with the size of the pixel matrix as a parameter, such that different size versions of the same design can be produced. This common design framework is named RD53B. Two physical chips will be produced with the RD53B framework, an ATLAS version and a CMS version, differing only in the pixel matrix size. This is necessary to meet the incompatible geometrical constraints of the different detector layouts [3, 2]. However, a common design means that there will be one design team with a single set of tasks and milestones. Furthermore, in addition to design effort, significant

testing effort will be saved, as performance and radiation tolerance results from one size chip will be applicable also to the other.

Section 2 gives a brief introduction to the RD53A chip and design framework, as well as the RD53B design framework. Main changes from RD53A to RD53B are listed in Section 2.1. Section 3 summarizes the work plan leading up to production chip submissions. Section 4 discusses scenarios and needs beyond this work plan. Finally, the updated organization of the collaboration is described in Section 5, with a list of current collaborators and their areas of involvement given in Section 6. Section 7 discusses the requested CERN resources.

2. RD53A and RD53B Design Framework

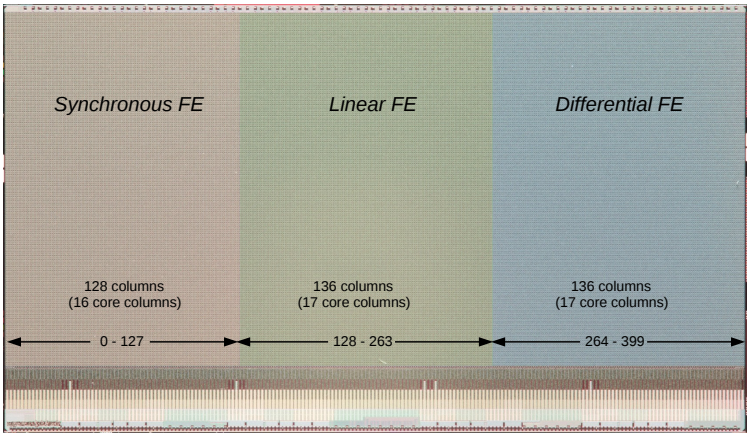

Figure 1: Photograph of RD53A chip with color shading added over each of the three front end designs in the pixel matrix.

The RD53A chip (Figure 1) was designed to meet prototype (not production) specifications [4] developed ahead of time and approved by ATLAS and CMS. The physical size is half of that desired for production in order to fit in a shared wafer run and lower prototyping cost. Nevertheless, this is large enough to validate "large chip" effects in both design and performance. RD53A is 20 mm wide by 12 mm tall, containing 76 800 pixels and 240 M transistors. It contains three different analog front end designs and two different pixel matrix read-out architecture implementations, to allow for detailed performance comparisons.

A detailed description of the RD53A design can be found in [5]. It was fabricated in a full wafer engineering run shared with CMS MPA in Sept.-Dec. 2017 and is currently under test. Bare chip (no sensor) test results showed RD53A to work essentially as designed, prompting a 25 wafer lot to be ordered in March 2018, to enable significant bump bonded module prototyping by ATLAS and CMS. A second 25 wafer lot has been ordered in August 2018 to ensure sufficient wafers for bump bonding market surveys. Public plots showing RD53A performance can be found on the RD53 Collaboration's public results web site [6]. Results have been presented at the Elba [7], ACES [8, 9, 10], FEE [11], and at a CERN instrumentation seminar [12]. Results will not be

reproduced here, as that is not the purpose of this document. A comprehensive technical publication is in preparation.

First bump bonded assemblies have been delivered in May 2018 and initial test results are equally promising. These assemblies were made with wafers from the engineering run and have only planar single chip sensors. A comprehensive testing program, including x-ray, beta, gamma, and proton high and low dose rate irradiations, source and test beam measurements of modules, and serial power system tests is under way with the aim of having mature results in the fourth quarter of 2018. These results are a very important ingredient to finalizing the RD53B design. This includes choosing one of the three analog front end variants as the common front end for both ATLAS and CMS chips (see Sec. 3).

An electronic design framework was developed for RD53A, including a *digital-on-top* integration flow and an industry standard verification environment [13, 14]. The successful testing of the very complex RD53A chip validates the framework and methodology used. Some lessons were learned from RD53A and these are being used to make incremental improvements that will benefit the ATLAS and CMS production chips. The RD53A chip does contain a few minor errors, which do not prevent detailed testing and are not difficult to correct, but more importantly, they point to areas of improvement in the digital design methodology. Broadly, the errors are in the categories of analog-digital interfaces, and in digital code of logic functions. The former call for added verification tools and for minimizing new interfaces for RD53B. The latter call for more precise specification of digital functionality and more involvement of the experiments in generating or validating behavioral models.

The RD53B design framework builds upon the RD53A framework with a number of technical improvements aimed at improving integration and verification of the final layouts. The 8x8 pixel core organization of RD53A is preserved. The core design is stepped and repeated to produce the pixel matrix, with the numbers in x and y being parameters of the integration flow. Generation of different size layouts is controlled by these parameters and is very fast. The plan is to contain all of the global chip functionality in the chip bottom analog and digital blocks, which will remain the same regardless of the chip size generated. Any different behavior between ATLAS and CMS will be addressed with configuration settings and modes, and not with design differences. Thus, the RD53B chip size produced for ATLAS will be capable of meeting the CMS functional requirements and vice-versa.

Work on RD53B has been in progress since January 2018, as there are many known tasks that do not need to wait for final requirements and specifications (see 2.1). As of this writing, the RD53B integration flow has already been implemented and generation of different size pixel arrays is working well.

2.1 Changes from RD53A to RD53B

A full list of changes can only be constructed once all final specifications are written. However, even before that point there are many known updates and improvements for which work is in progress. For each item we provide a status as of this writing.

- Update top level integration flow to apply lessons learned in RD53A (90% done).
- Update layouts of all 3 front ends and create models for improved integration (75% done).

- Increase the matrix number of rows from 192 to 328 (CMS) and 384 (ATLAS) (parameterization done).
- Increase the matrix number of columns from 400 to 440 for CMS (will be done in Jan. 2019).
- Update the serial power regulator design to include overcurrent protection and low current mode operation. (50% done. Complete by Dec. 2018).
- Update default configuration for low power startup (parametrized. Final values depend on FE choice).
- Adjust bias ranges to comply with specified maximum allowed current consumption (parametrized. Final values depend on FE choice).
- Reduce digital power through optimization where possible. (90% done).
- Add different, programmable bias settings for edge (left, right, and top) pixels for inter-chip gap spanning (design approach selected. Complete by Oct. 2018).
- Address known defects of RD53A design, such as higher than desired timing variation of charge injection pulses from column to column (50% done. Complete by Oct. 2018).
- Improve phase locked loop clock recovery circuit to reduce jitter and improve start-up reliability. (Design done. Test chip being submitted Aug. 2018).
- Add two level trigger functionality, including level 0 fast clear (done).
- Modify the command protocol to include a L0 fast clear (to be done Sept. 2018).
- Increase the latency range from 9 bits to 10 bits (done).
- Add capability to count ToT at 80 MHz and 6 bit dynamic range compressed to 4 bits (done).
- Add event truncation functionality to clear rare extremely high occupancy events (50% done. complete Oct. 2018).
- Add data compression functionality to optionally reduce output data volume (compression format studies in progress. Conclude and implement by Oct. 2018).
- Add boundary scans to all bottom of chip logic for structural testing and design for test features needed for production (started. Complete by Dec. 2018).
- Assess SEU hardening of bottom of chip logic and improve as needed (SEU simulation machinery developed. Complete by Nov. 2018).
- Potential functionality enhancements such as automation of threshold tuning, fast continuity testing of bump bonds, etc. (ongoing).

3. Work Plan

The execution of this work plan was already kicked off in December 2017 and continues to move ahead without delay. The design and measurement tasks are divided into the work packages shown in Table 1. A detailed schedule is maintained by the project engineer and reviewed at least monthly by the management board and with the ATLAS and CMS observers (see Sec. 5). A top level summary of the present schedule is shown in Fig. 2. This schedule shows two submissions for each experiment (labeled “V1” and “V2”) in accordance to their project schedules. The V1 submission dates are determined by the ongoing and planned RD53 work to finalize the RD53B design framework, and assembly and verify the two chip layouts. The tasks shown leading up to the V1 submissions are a roll-up of a detailed work breakdown schedule with 24 main tasks and 250

subtasks. The work for the V2 submissions is anticipated and cannot be defined in detail before. Further discussion the RD53 role beyond the V1 submissions is given in Sec. 4.

WP	Title	Scope
1	Integration	Floorplan, interfaces and assembly of full chip
2	Analog FE	Design of analog front ends and biases
3	Digital	Digital code management, synthesis and core
4	Digital Bottom	Code for chip-level functionality
5	IP blocks & monitoring	Circuit blocks such as DAC, ADC, temp. sens.
6	Pads, I/O, and Power	All functions included in wire bond pad frame
7	Verification & DFT	Development of execution of verification flow and Design For Test
8	Testing & Irradiation	Development of setups, testing of RD53A, radiation data and models

Table 1: Work Packages (WP) for extension of RD53 Collaboration.

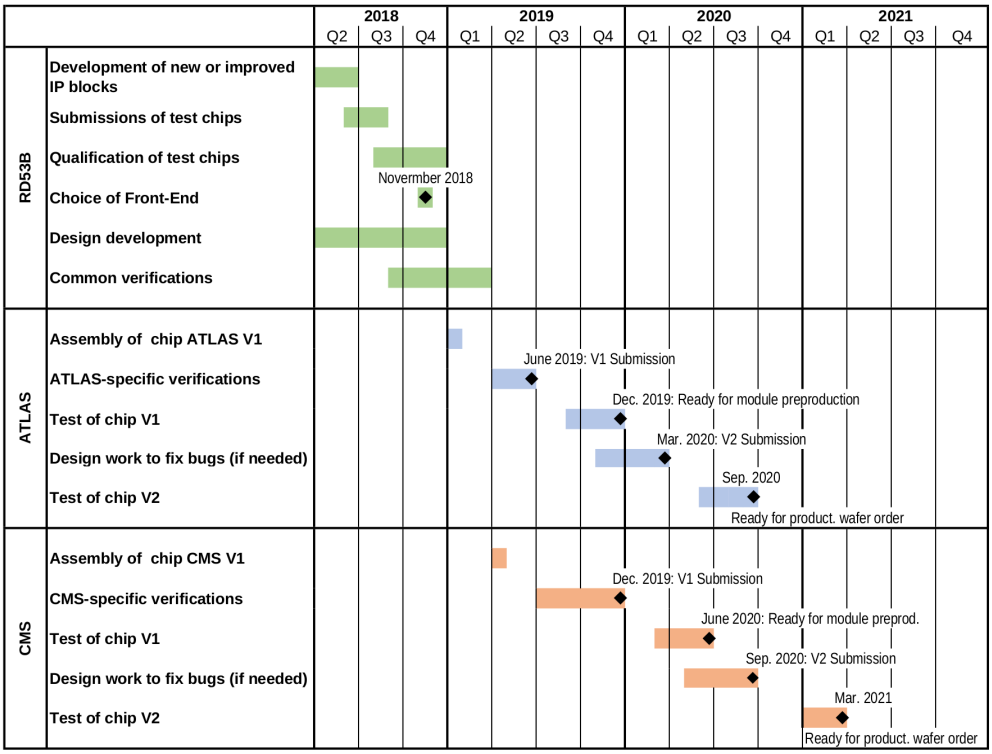

Figure 2: Summary view of RD53 master schedule showing ATLAS and CMS chip submissions.

A single RD53B requirements document has been prepared and is under review by both experiments, with approval to follow, much as was done for the RD53A specifications [4]. The RD53B requirements document has been circulated to ATLAS and CMS on Aug. 2, 2018, with a deadline for collecting comments on CDS of Aug. 31. The approval of a final version is planned for end of September. Detailed design specifications for RD53B, which spell out the circuit choices for meeting the requirements, will be captured in internal RD53 documents. The functions preserved

from RD53A are described in detail in the RD53A manual, so need no dedicated documents, while new functions not in RD53A, or those with significant changes, will have new specification notes as needed. An RD53B design manual will be produced to capture all the functional details in one public document.

The selection of an analog front end design is being carried out with the help of an external review committee, composed of two IC designers not on ATLAS, CMS, or RD53, plus two physicists from both ATLAS and CMS with experience on pixel sensors, modules, and operation. This committee is charged with evaluating the test results from RD53A, which contains three different front end designs, as well as simulations including any proposed updates, in order to recommend the best choice for meeting the RD53B requirements with minimal risk in terms of chip design and later detector operation. A Front End Review kick-off meeting was held with the full committee on July 24. An initial document assessing the RD53A measurements to be made is due in early September, and the committee conclusions are due in late November 2018. All three front ends conform to a generic template, and therefore the RD53B design progress does not depend on the final front end choice.

The plan is to submit an ATLAS V1 size chip first and a CMS size V1 chip second, in accordance with the difference in the construction schedules of the two experiments. Verification of a full design is the final critical task prior to each submission. The time allowed for this is estimated from the RD53A experience. Because the design framework is common, the majority of the verification for the ATLAS submission carries over to the CMS chip submission, and the same team will remain committed to both submissions. An overview of verification tasks is given in Sec 3.1. The main reason for the 6 month difference between the submissions in Fig. 2 is to take advantage of the opportunity to test the ATLAS chip as a final validation before submitting the CMS chip.

The work plan includes a series of small test chips with August 2018 submission date. These test chips and the front end choice time-line drive the ATLAS chip assembly date in Fig. 2. The test chips are needed to validate any blocks with analog modifications for a high confidence submission. This is analogous to RD53A where all analog blocks had been previously validated this way.

3.1 Verification Tasks

The verification process ensures that design functions as intended and that the final layout corresponds to the design and meets all fabrication requirements. The industry standard Universal Verification Methodology (UVM) is used to describe and verify the design functionality. Analog and mixed signal simulations are used to verify connectivity and function including analog elements. Most of the work is common for both ATLAS and CMS chips, while some specific steps need to be repeated for each new submission.

The common tasks include:

- Setup of UVM verification environment
- Develop functional golden models for automated tests
- Develop automated tests and validate on RD53B environment
- Develop directed tests and verify functionality of RD53B environment
- Incorporate ATLAS and CMS Monte Carlo hit files
- Perform power and hit loss simulations vs hit rate and trigger rate

- Validate timing extraction with corners, including radiation
- Update radiation models and corners from RD53A
- Analog simulation with full parasitics of all analog blocks
- Monte Carlo simulations of mismatch as appropriate
- Analog simulations of one full core (8 by 8 pixels) including all digital devices
- Generation of analog block models for mixed mode simulations
- Mixed mode simulation of one core column

For each submission the following tasks must be repeated:

- Layout vs. Schematic (LVS)
- Design Rule Check (DRC)
- Formal equivalence check for the logic
- Top level simulation for connectivity
- Timing back annotation and run all automated tests

4. Outlook Beyond RD53B Submissions

The two V1 chip submissions in the above plan are intended to meet all requirements and be suitable for production use by ATLAS and CMS. We anticipate that further testing support and design work will be needed beyond the actual submissions. Initial testing of each submission will be carried out by RD53 to validate that the chips work as designed and evaluate the success of the submission. After that point, shown as "ready for module production" in Fig. 2, testing and prototyping work is up to the experiments and the role of RD53 is to provide technical support and documentation as needed, for example to check with simulation any test results that deviate from expectations.

The decision of whether the V1 chips truly meet all requirements for production rests with the experiments, following module and system tests. If the experiments determine that a design revision is needed, then RD53 must be prepared to do it. Such a revision is shown as V2 in Fig. 2. The actual start of V2 design work, should it be needed, depends on the experiments and the dates shown are meant to illustrate the expected duration of this RD53 extension rather that do give a firm end date. The RD53 collaboration must remain in place and involved until module series production is under way for both experiments, which is expected to be 2021-2022.

5. Collaboration Organization

The RD53 collaboration organization is described in an MOU signed by the member institutes. Technical roles and responsibilities are described in MOU annexes, which have been updated in 2018 to address the new scope of designing and producing final chips for ATLAS and CMS.

The collaboration has an institute board with an elected chair, two elected co-spokespersons, an appointed project engineer, and a management board made up of the spokespersons, the project engineer, the appointed leaders of the work packages, plus one observer from ATLAS and one from CMS. All appointments are confirmed by the institute board. Close contact with bump bonding activities to sensors, needed for full chip characterization, is maintained with representatives from

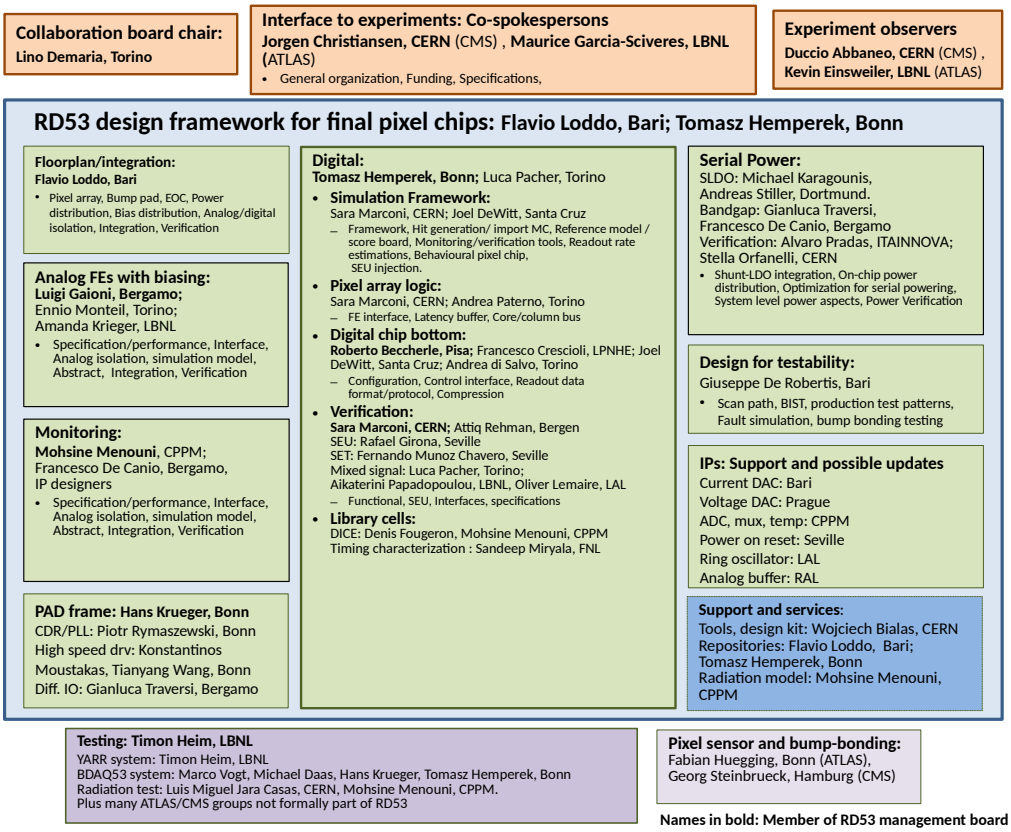

Figure 3: Organization chart of RD53 with RD53B framework core design team.

ATLAS and CMS, but they are not part of the management board. Fig. 3 summarizes the present organization.

The management board meets at least monthly to make decisions on resources, schedule, submissions, equipment, expenditures, etc.

6. Collaborators and Institutes

(D) Indicates IC designer.

- **Bergen University** (ATLAS group)
  M. Lauritzen, A. Ur Rehman (D), B. Stugu.

- **Bonn University** (ATLAS group)
  H. Krüger (D), M. Daas, Y. Dieter, T. Hemperek (D), F. Hügging, K. Moustakas (D), D. Pohl, P. Rymazewski (D), M. Vogt, T. Wang (D), N. Wermes.

- **CERN** (^{A}ATLAS, ^{C}CMS)
  D. Abbaneo^{C}, J. Christiansen^{C} (D), L. Jara Casas^{A,C}, D. Koukola^{C}, S. Marconi^{C} (D), S. Orfanelli^{C} (D), H. Pernegger^{A}.

- **CPPM Marseille** (ATLAS group)
  M. Barbero, P. Barrillon, P. Breugnon, D. Fougeron (D), S. Godiot-Basolo (D), A. Habib (D), M. Menouni (D), P. Pangaud (D), A. Rozanov.

- **Dortmund FH** (not on ATLAS or CMS)
  M. Karagounis (D), A. Stiller.

- **Fermilab** (CMS group)
  D. Christian, G. Deptuch (D), J. Hoff (D), T. Liu, S. Miryala (D).

- **FNSPE CTU, Prague/IP-ASCR** (ATLAS group)
  T. Benka, M. Havranek (D), Z. Janoska, M. Marcisovsky, G. Neue, L. Tomasek (D), V. Kafka, V. Vrba.

- **INFN Bari and Politecnico di Bari** (CMS group)
  F. Loddo (D), G. De Robertis (D), F. Licciulli (D), C. Marzocca (D).

- **INFN Milano and University of Milano (ATLAS group)**
  A. Andreazza, L. Frontini (D), V. Liberali (D), A. Stabile (D).

- **INFN Padova and University of Padova** (CMS group)
  D. Bisello, N. Bacchetta, M. Bagatin, M. Dall'Osso, S. Gerardin, A. Neviani (D), A. Paccagnella, D. Vogrig (D), J. Wyss.

- **INFN Pavia, University of Pavia and University of Bergamo** (CMS group)
  V. Re, F. De Canio (D), L. Gaioni (D), M. Manghisoni (D), L. Ratti (D), G. Traversi (D).

- **INFN Perugia and University of Perugia** (CMS group)
  G. Bilei, M. Menichelli, D. Passeri (D), P. Placidi (D).

- **INFN Pisa and University of Pisa** (CMS group)
  F. Palla, R. Beccherle (D), R. Dell'Orso, G. Magazzù (D), A. Messineo, F. Morsani (D).

- **INFN Torino and University of Torino** (CMS group)
  N.Demaria, G. DellaCasa, A. Di Salvo, G. Mazza (D), E. Migliore, E. Monteil (D), L. Pacher (D), A. Paterno' (D), A. Rivetti (D), M. Rolo (D).

- **Instituto Tecnológico de Aragón - ITAINNOVA** (CMS Group)
  A. Pradas (D), F. Arteche.

- **LAL Orsay -Université Paris-Saclay** (ATLAS group)
  D. Hohov , J. Jeglot, O. Lemaire (D), A. Lounis, M. Cohen Solal (D), C. Sylvia, P. Vallerand (D), D. Varouchas.

- **LAPP (Annecy)** (ATLAS group)
  R. Gaglione (D), S. Vilalte (D).

- **LBNL** (ATLAS group)
  A. Dimitrievska, M. Garcia-Sciveres, T. Heim, D. Gnani (D), A. Krieger (D), A. Papadoupoulou (D).
- **LPNHE Paris** (ATLAS group)
  G. Calderini, M. Bomben, F. Crescioli (D), O. Le Dortz (D), G. Marchiori.
- **NIKHEF**
  R. Kluit (D), A. Vitkovskiy (D).
- **U. of New Mexico** (ATLAS group)
  M. Hoeferkamp, S. Seidel.
- **RAL** (IC group serving both ATLAS and CMS)
  M. Prydderch (D), S. Bell (D).
- **U.C. Santa Cruz** (ATLAS group)
  J. DeWitt (D), H. Grabas (D), A. Grillo, J. Nielsen.
- **U. of Sevilla** (CMS group)
  R. Girona (D), F. Muñoz Chavero (D), R. Palomo (D).

6.1 Contributions

Table 2 gives a summary of the required total and committed effort, while Table 3 breaks down the contributions of the RD53 member institutes. The total effort is an integral from the start of the RD53B design (Jan. 2018) until submissions, given in FTE-Year. The committed effort is based on a survey of designer availability tracked per quarter. Some commitments are subject to uncertainties related to continuation of contracts, teaching and local administrative obligations, participation in conferences, and integration of new people (including students) that have joined the project. Certain tasks, like testing and verification, benefit from additional effort beyond the required minimum. The required effort is also not always constant for the entire project time and a larger commitment is generally needed in order to ramp up people for peak needs.

Effort	**WP1** Integr.	**WP2** FE's	**WP3** Digital	**WP4** Dig. Bot.	**WP5** IP blocks	**WP6** Pads, I/O, Pwr	**WP7** Verif, DFT	**WP8** Test. Rad.
FTE-YR required	3	3	3	3	3	4	6	20
FTE-YR committed	4.0	3.2	3.3	4.0	3.6	4.3	6.0	37.2

Table 2: Total effort required (integrated from start of RD53B work until submission) and committed effort.

Institute	**WP1** Integr.	**WP2** FE's	**WP3** Digital	**WP4** Dig. Bot.	**WP5** IP blocks	**WP6** Pads, I/O, Pwr	**WP7** Verif, DFT	**WP8** Test. Rad.
Bergen							B	B
Bonn	A	C	A	B	A	A	B	A
Dortmund FH						A		B
CERN	B		A	B	C	B	A	A
CPPM	B				A	B	C	A
Fermilab			B					B
FNSPE-CTU / IP-ASCR	C	C	C	C	A	C	C	B
INFN Bari	A	B	C	C	A	B	A	B
INFN Milano								B
INFN Padova	A				A			B
INFN Pavia-Bergamo	C	A			A	B		B
INFN Perugia			B	B				C
INFN Pisa			B	A	B			
INFN Torino	A	A	A	B		C	A	B
ITAINOVA						B	A	
LAL Orsay				C	A		B	
LAPP				B				B
LBNL	B	A	B	B			B	A
LPNHE Paris				A	B			B
NIKHEF							B	
New Mexico								B
RAL					C			C
UCSC			C	B			A	B
U. Sevilla				B	A		B	

Table 3: Matrix of institute involvement in Work Packages. "A" indicates a critical role, "B" significant contribution, and "C" minor involvement or ability to help if needed.

7. CERN Resources

The majority of the work takes place at the collaborators' respective institutes, including CERN for the work of the CERN group. For design reviews and for a few weeks during final integration, members of the core design team will maintain a physical presence at CERN. We anticipate temporary office space will be identified in or near the IC group (Bat. 14).

The design work is enabled by the CERN frame contract with TSMC already in place and the corresponding 65 nm design kit managed by the CERN IC group, including legal authorizations though letters of compliance. CERN computing resources are used to host the design repository, digital code, and verification environment. We do not anticipate an increase relative to what is already in use.

CERN Irradiation facilities and test beams are being used for RD53A characterization and will be used for the production designs as well. With the exception of the x-ray irradiators of the CERN IC group, all irradiation and test beam facilities are being booked and applied to RD53 chip tests by ATLAS and CMS users though the ATLAS and CMS beam test and irradiation programs. Many

facilities outside CERN are also used, both for irradiation and beam tests.

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