NATIONAL INSTITUTE FOR NUCLEAR AND HIGH ENERGY PHYSICS

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CTT-V2
Cosmics Trigger and Timing module for phase 2 of the L3 + Cosmic project. Technical Documentation

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Abstract: The CTT-V2 is a VME module to provide the triggers for phase 2 in the L3+Cosmics experiment at CERN. This module combines the scintillator signals and the majority signals from the L3 muon chambers, arriving via the CPC cards, and generates the cosmic trigger signal for the NIMRODs and the GPS module. In addition some external trigger signals can be accepted. The selection and prescaling of all triggers is controlled via the VME interface.

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Contents

1. CTT - Cosmics Trigger & Timing

The CTT-V2 is a VME module to provide the triggers for phase 2 in the L3+Cosmics experiment at CERN. This module combines the scintillator signals and the majority signals from the L3 muon chambers, arriving via the CPC cards, and generates the cosmic trigger signal for the NIMRODs and the GPS module. In addition some external trigger signals can be accepted. The selection and prescaling of all triggers is controlled via the VME interface.

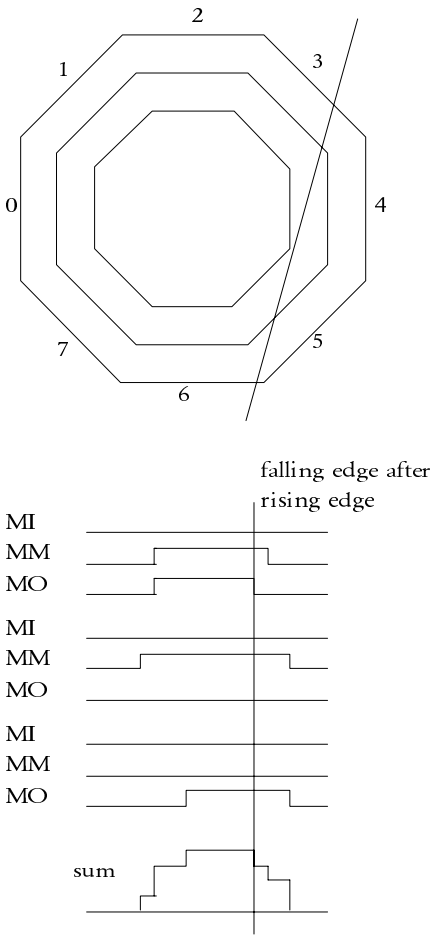
2. Trigger principle

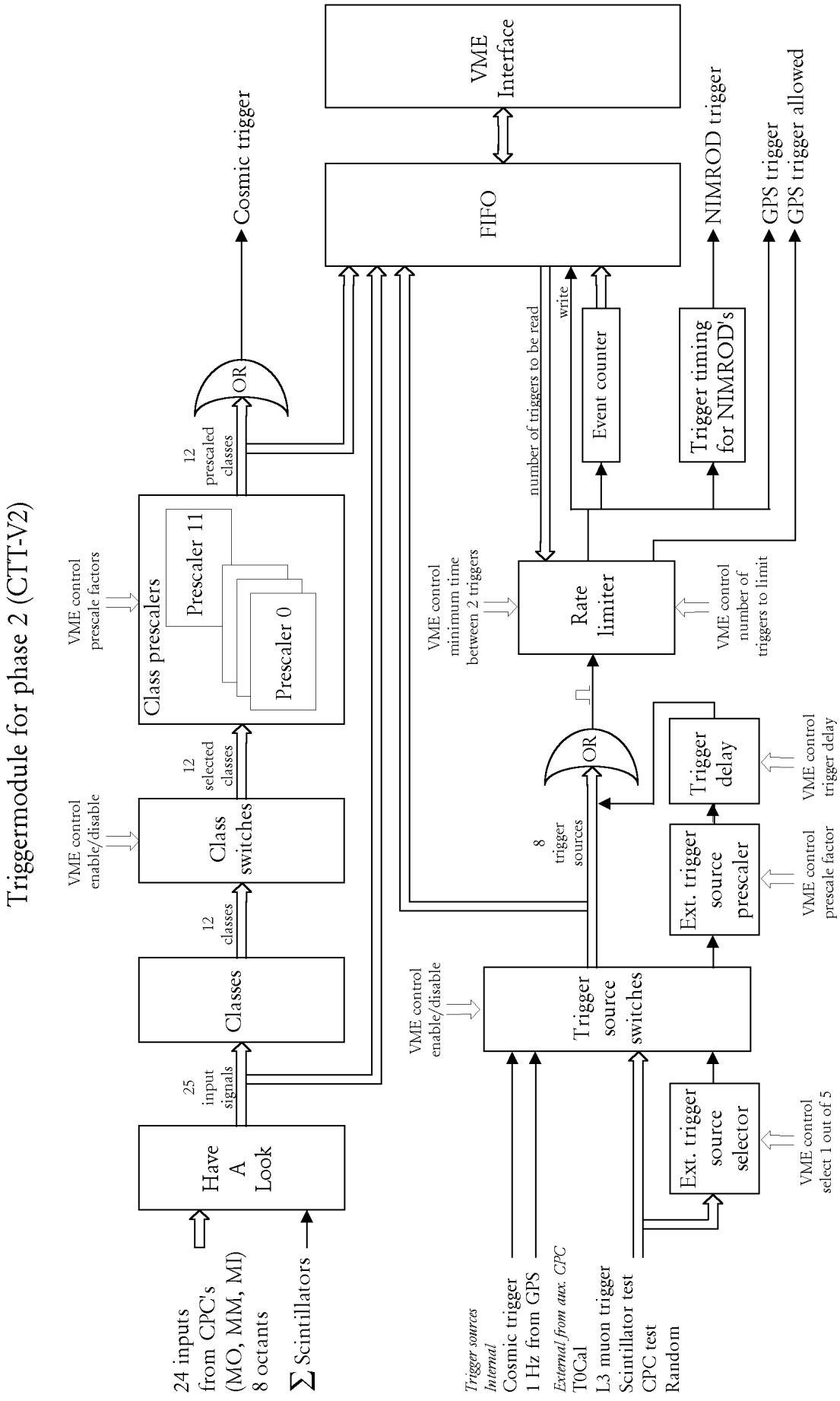
The trigger principle will be explained on the basis of a block diagram on the next page.

2.01 HAL - Have A Look

The first device on the diagram is called HAL, which looks at the input signals and determines a point when the data is valid. The input signals of this block are a logical OR of the P-cell majority signals in a P-layer. Every octant (8 in total) has 3 layers. So there are 24 layer signals (3 x 8 Majority Outer/ Middle/Inner signals) plus a scintillator signal. The signals from a track can arrive one drift time (1.2us) from each other. To determine a coincidence the CPC has to stretch these signals minimal one drift time. It appears that the coincidence can be made on the falling edge after a rising edge of these signals. This will be shown in the next drawing.

Principle of Have A Look




Triggermodule for phase 2 (CTT-V2)
24 inputs from CPC's (MO, MM, MI) 8 octants
Σ Scintillators
Have A Look
25 input signals
Classes
12 classes
Class switches
12 selected classes
Class prescalers
Prescaler 11
Prescaler 0
12 prescaled classes
OR
Cosmic trigger
VME control enable/disable
VME control prescale factors
FIFO
VME Interface
number of triggers to be read
write
Event counter
Trigger timing for NIMROD's
NIMROD trigger
GPS trigger
GPS trigger allowed
Rate limiter
VME control minimum time between 2 triggers
VME control number of triggers to limit
OR
8 trigger sources
Trigger delay
VME control trigger delay
Ext. trigger source prescaler
VME control prescale factor
Trigger source switches
VME control enable/disable
Ext. trigger source selector
VME control select 1 out of 5
Trigger sources
Internal
Cosmic trigger
1 Hz from GPS
External from aux. CPC
T0Cal
L3 muon trigger
Scintillator test
CPC test
Random

The input signals are added together. The sum is at a maximum when all the hit signals created by the track are present. The decision that the sum was at a maximum can only be made when the sum decreses. At that time the input signals are latched including the scintillator signal. The scintillator signal must be timed well by an auxillary CPC card. With this principle the hitpattern is determined on the fly without deadtime. The hitpattern is written into a FIFO if the decision is made that this hitpattern was used for a final trigger.

2.02 Classes

12 classes are defined. A class signal is made out of the latched data from HAL.
The class definitions are:
1) Triplet in any octant with a scintillator hit.
2) Triplet in octant 0 or 4 without a scintillator hit.
3) Triplet in octant 1 or 2 or 3 without a scintillator hit.
4) Triplet in octant 5 or 6 or 7 without a scintillator hit.
5) Three singlets in adjacent octants with scintillator hit.
6) Doublet and a doublet with a scintillator hit.
7) Doublet and 2 singlets with a scintillator hit.
8) Doublet and a singlet with a scintillator hit.
9) Doublet with scintillator hit.
The following classes are to identify the strange events and multiple muon events.
10) Triplet + at least 1 plane (no scintillator requirement).
    1) Multiple tracks (close together).
    2) Decay of a charged particle (the Kolar events).
11) 5 planes (no scintillator requirement).
    1) Multiple tracks (somewhat further apart).
    2) Decay. The opening angle is larger than in case a, and multiplicity low.
       Two charged tracks close together (Yunan event).
12) 6 or more planes (no scintillator requirement).
    1) Multiple muons towards the side of the detector.
    2) Decay originating outside the detector.

2.03 Class switches

In this device the selection can be made which classes may contribute to a final trigger. This selection is controlled via VME.

2.04 Class prescalers

Every selected class signal can be prescaled separately from 1 to 255. This is controlled via VME. The outputs of the prescalers are written into the FIFO.

2.05 Trigger source switches

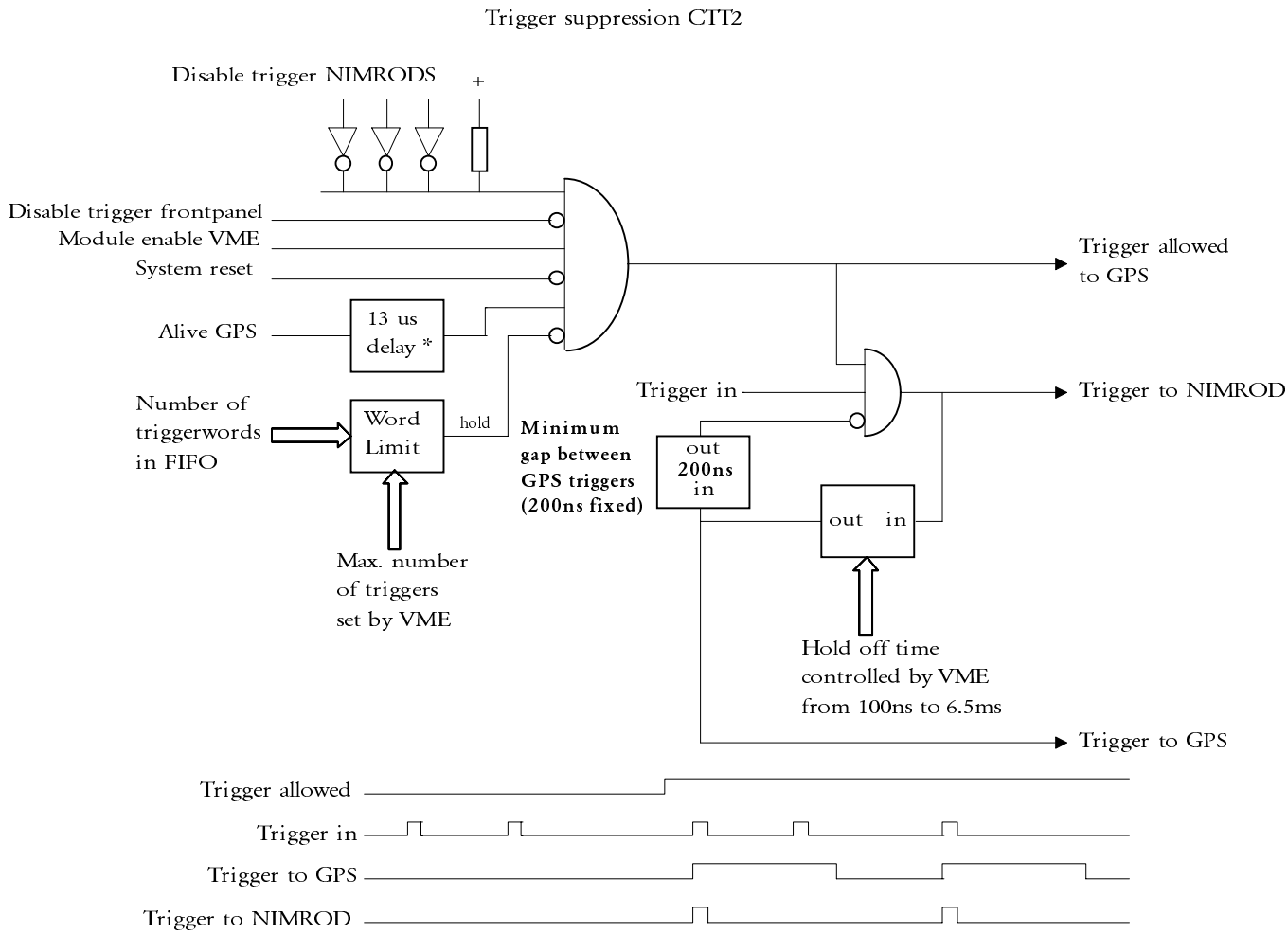
In this device the selection can be made which trigger source may contribute to a final trigger. This selection is controlled via VME.
The selectable trigger sources are:
1) Cosmic trigger
2) 1 Hz signal from GPS
3) Scint. Test Ref. Timing (external source)
4) T0cal Ref. Timing (external source)
5) CPC Test Ref. Timing (external source)
6) Random trigger (external source)
7) L3 Muon trigger (external source)
8) Selector external trigger sources
The output of this device (8 bit trigger source pattern) is written into the FIFO.

2.06 Selector external trigger sources
With this device one of the external trigger sources can be selected for prescaling later on. This option is made for trigger sources with a frequency which is too high.

2.07 Prescaler external trigger sources
This prescales scales the trigger rate of the selected external trigger source with a factor of 1 to 255.

2.08 Rate limiter
This device supresses the trigger rate depending of its input conditions.

The trigger can be stopped by the following signals:
1) Disable trigger from NIMRODs.
   All NIMRODs are connected on an "open collector" line. When one of the NIMRODs wants to stop the trigger, this line goes low.
2) Disable trigger from frontpanel.
   The trigger can be stopped with a NIM signal applied to a LEMO connector on the frontpanel.
3) Disable trigger by "module enable" bit.
   By clearing bit 4 of the status register the module is disabled and therefore the trigger stops.
4) Disable trigger by system reset.
   When system reset is active, the trigger stops. System reset can by made active by the VME master and by setting bit 7 of the status register.
5) Disable trigger from GPS.
   The CTT-V2 gets an "experiment alive" signal from the GPSTIM. The trigger stops when the GPSTIM makes this signal low (not alive).
6) Disable trigger by the word limiter.
   The word limiter compares the number of events in the FIFO which are not yet read out and a number set by VME. The trigger stops when the number of unread events is bigger than the setting. When the word limiter is set on zero, the triggers will not be stopped by this device.
7) Disable trigger by the hold off timer.
   The hold off timer limites the maximum trigger rate. The minimum time between two triggers can be set by VME from 100 ns to ~6.5 ms. The default value is 2.0 us. The output of the holdoff timer is the final "trigger to GPS" signal that triggers the GPS module and the NIMRODs (via the reset /trigger encoder).
   The signal "trigger allowed" (i.e. not trigger disabled) is sent to the GPS time recorder where it enables the life time counter.
   The signal "trigger to GPS" triggers the GPS time recorder and during the width of the signal it blocks the life time counter.
   The GPSTIM needs a gap between two triggers of at least 200ns to distinguish a trigger. Since the same signal blocks the life time counter, this gap is not taken into account. One has to subtract 200ns per event from the life time later on.



* This delay blocks the trigger for 13 us after the rising edge of the Alive-signal from GPS, because the system (CPCs etc) is cleared on this edge. The delay allowes the system to recover.

"Word limit" blocks the trigger if the number of triggerwords, which are not yet read out, exceeds a value which is set by VME. Except when the setting is zero, the limiter will not limit.

The Hold off time is the minimum time between two triggers.

2.09 Event counter

The event counter counts the number of triggers written into the FIFO. This means that every trigger gets its own number. The counter is 12 bit and can be reset by a VME command.

2.10 Trigger timing for NIMRODs

This device synchronizes the trigger and reset signals to the NIMRODs on a 40 MHz basis. These signals are combined and encoded and put on one wire (Front End Link). There are several patterns and ways to put something on this link.

1) Trigger.
   A trigger is a pulse of 25 ns and is generated every time a trigger is made in normal operation mode independent of a cosmic or external trigger. A second way is to force a cosmic trigger by setting bit 3 of the control register and make in the CTT-V2 the selection for cosmic triggers.
2) Global reset.
   A reset is a pulse of 75 ns (3 x 25) and is generated by the experiment alive signal from the GPSTIM. On the rising edge of this signal (at the beginning of a run) a reset is given. An other way is to force a reset (only on this link) by setting bit 2 of the control register.
3) Event Counter Reset (ECR).

This is a Atlas feature and not used for the L3 + cosmic project.
This signal has a bit pattern of 101 in steps of 25 ns and can be made by setting bit 1 of the control register. Do not confuse this signal with the event counter reset for the event counter of the CTT-V2.

4) Bunch Crossing Reset.
This is a Atlas feature and not used for the L3 + cosmic project.
This signal is a pulse of 50 ns (bit pattern = 110) and can be made by setting bit 0 of the control register.

2.11 FIFO

This device buffers the data that belongs with each trigger. The data consists of two words of 32 bits and described in the chapter "Format of FIFO output". The FIFO can store 128 events.

3. CTT-V2 VME Addresses

The Base Address of the CTT-V2 is defined by the Geographical Address pins on the backplane connector or by jumpers in case the backplane is not supporting geographical addressing. Default value is 0x3.

The A32 Base Address

31 24	23	22	21	20	19 16	12	8	4	0
0 0	Ga4	Ga3	Ga2	Ga1	Ga0 0	0	0	0	0

The A24 Base Address

23	22	21	20	19 16	12	8	4	0
Ga4	Ga3	Ga2	Ga1	Ga0 0	0	0	0	0

Valid AM Codes are 0x09, 0x0D, 0x39, 0x3D, 0x2F

Address Offsets:

0x0 to 0xFF	CR Prom	8 bit	Read only
0x100	Serial Number	8 bit	Read only
0x110	Interrupt Request Level	8 bit	Read/Write
0x114	Interrupt Vector	8 bit	Read/Write
0x200	Prescaler class 1	32 bit	Read/Write
0x204	Prescaler class 2	32 bit	Read/Write
0x208	Prescaler class 3	32 bit	Read/Write
0x20C	Prescaler class 4	32 bit	Read/Write
0x210	Prescaler class 5	32 bit	Read/Write
0x214	Prescaler class 6	32 bit	Read/Write
0x218	Prescaler class 7	32 bit	Read/Write
0x21C	Prescaler class 8	32 bit	Read/Write
0x220	Prescaler class 9	32 bit	Read/Write
0x224	Prescaler class 10	32 bit	Read/Write
0x228	Prescaler class 11	32 bit	Read/Write
0x22C	Prescaler class 12	32 bit	Read/Write
0x300	Enable classes	32 bit	Read/Write
0x304	Enable triggersources	32 bit	Read/Write
0x308	Select external triggersources	32 bit	Read/Write
0x30C	Prescaler triggersources	32 bit	Read/Write
0x310	Stretcher triggerpulse	32 bit	Read/Write
0x314	Word limiter	32 bit	Read/Write
0x318	Trigger delay	32 bit	Read/Write
0x400	FIFO	32 bit	Read only
0x7FFEC	Bit Clear Control Register	8 bit	Read/Write
0x7FFF0	Bit Set Control Register	8 bit	Read/Write
0x7FFF4	Bit Clear Status Register	8 bit	Read/Write
0x7FFF8	Bit Set Status Register	8 bit	Read/Write
0x7FFFC	Base Address	8 bit	Read only

Control Register:

Bit7	Don't look at GPS clock
Bit6	Don't look at GPS alive signal
Bit5	Reset event counter Module
Bit4	Reset FIFO Module
Bit3	Force Cosmic trigger
Bit2	Force global reset on FE-link
Bit1	Force event counter reset on FE-link
Bit0	Force bunch counter reset on FE-link

StatusRegister:

Bit7	Reset Module
Bit4	Enable Module
Bit3	VME Error
Bit2	Enable Interrupt
Bit1	FIFO Full Module
Bit0	FIFO Empty Module

All access must be performed using address modifier AM = 09h or 0Dh (32 bit address) or AM = 2Fh or 39h or 3Dh (24 bit address).

Only VME – D32 allowed.

Board base address: A31….A24 = 0x0, A23….A19 = selectable by jumpers (default = 0x3).

Device Assignments

Device Address	Content	R/W	Comments
Base + 0x00 to 0xFF	CR Prom	R	8 bits
Base + 0x100	Serial number	R	8 bits
Base + 0x110	Interrupt Request Level	R/W	8 bits
Base + 0x114	Interrupt Vector	R/W	8 bits
Base + 0x7FFEC	Bit Clear Control Register	R/W	8 bits B7 = Look at GPS clock (when set) B6 = Look at GPS alive signal (when set) B5 = Reset event counter module (no effect) B4 = Reset FIFO module (no effect) B3 = Force Cosmic trigger (no effect) B2 = Force global reset on FE-link (no effect) B1 = Force event counter reset on FE link (no effect) B0 = Force bunch counter reset on FE-link (no effect)
Base + 0x7FFF0	Bit Set Control Register	R/W	8 bits B7 = Do not look at GPS clock (when set) B6 = Do not look at GPS alive signal (when set) B5 = Reset event counter module (once by setting) B4 = Reset FIFO module (once by setting) B3 = Force Cosmic trigger (once by setting) B2 = Force global reset on FE-link (once by setting) B1 = Force event counter reset on FE link (once by setting) B0 = Force bunch counter reset on FE-link (once by setting)
Base + 0x7FFF4	Bit Clear Status Register	R/W	8 bits B7 = Reset Module B4 = Enable Module B3 = VME error B2 = Enable interrupt B1 = FIFO Full B0 = FIFO empty
Base + 0x7FFF8	Bit Set Status Register	R/W	Same as above
Base + 0x7FFFC	Base Address Register	R	8 bits B7 to B3 = BAR B2 to B0 = 0

Device Assignments

Device Address	Content	R/W	Comments
Base + 0x200	Prescaling factor Class 1	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x204	Prescaling factor Class 2	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x208	Prescaling factor Class 3	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x20C	Prescaling factor Class 4	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x210	Prescaling factor Class 5	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x214	Prescaling factor Class 6	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x218	Prescaling factor Class 7	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x21C	Prescaling factor Class 8	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x220	Prescaling factor Class 9	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x224	Prescaling factor Class 10	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x228	Prescaling factor Class 11	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x22C	Prescaling factor Class 12	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x300	Enable classes	R/W	12 bits enabled when set B0 = class 1 …… B11 = class 12
Base + 0x304	Enable triggersources	R/W	8 bits enabled when set B0 = Cosmics B1 = 1 Hz signal from GPS B2 = Scint. Test Ref. Timing B3 = T0cal Ref. Timing B4 = CPC Test Ref. Timing B5 = Random Trigger B6 = L3 Muon trigger B7 = Selector external triggersources
Base + 0x308	Triggersource selection in behalf of prescaling	R/W	5 bits enabled when set B0 = Scint. Test Ref. Timing B1 = T0cal Ref. Timing B2 = CPC Test Ref. Timing B3 = Random Trigger B4 = L3 Muon trigger
Base + 0x30C	Prescaling factor selected triggersource	R/W	8 bits data = 0 or 1 then divide by 1
Base + 0x310	Width of triggerpulse to GPS (holdoff time)	R/W	16 bits LSB :: 100 ns ; F.S. ~ 6.5 ms
Base + 0x314	Limit the number of unread words	R/W	7 bits number = 0 to 127
Base + 0x318	Trigger delay	R/W	8 bits LSB :: 100 ns ; F.S. 25.5 us
Base + 0x400	Output of FIFO	R	2 x 32 bits

4. Format of FIFO output

On every trigger two 32 bits words are written into the FIFO.
This data can be read out with two read cycles on address 'base + 0x400' (two times on the same address).

First word

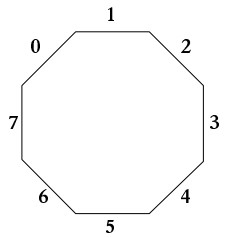
31 – 20	12 – 0	
Event counter (12 bit)	Trigger source (8 bit)	Prescaled classes (12 bit)

Second word

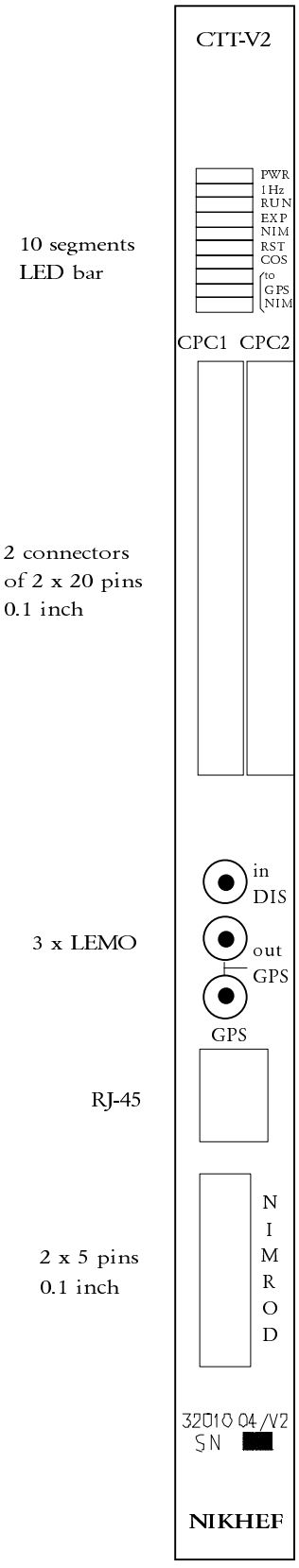
31 – 7	0
Majority and scintillator input (25 bit)	Events in FIFO (7 bit)

First word	**Second word**
B31 to B20 = Event counter B11 to B0 (B11 = msb) B19 to B12 = Trigger source B19 = Selector external trigger sources B18 = L3 Muon Trigger B17 = Random Trigger B16 = CPC Test Ref. Timing B15 = T0cal Ref. Timing B14 = Scint. Test Ref. Timing B13 = 1 Hz signal from GPS B12 = Cosmics B11 to B0 = Prescaled classes B11 = Hit from prescaled class 12 B10 = Hit from prescaled class 11 B9 = Hit from prescaled class 10 B8 = Hit from prescaled class 9 B7 = Hit from prescaled class 8 B6 = Hit from prescaled class 7 B5 = Hit from prescaled class 6 B4 = Hit from prescaled class 5 B3 = Hit from prescaled class 4 B2 = Hit from prescaled class 3 B1 = Hit from prescaled class 2 B0 = Hit from prescaled class 1	B31 to B7 = Majority and scintillator input B31 = Scintillator B30 = MI 7 B29 = MM 7 B28 = MO 7 B27 = MI 6 B26 = MM 6 B25 = MO 6 B24 = MI 5 B23 = MM 5 B22 = MO 5 B21 = MI 4 B20 = MM 4 B19 = MO 4 B18 = MI 3 B17 = MM 3 B16 = MO 3 B15 = MI 2 B14 = MM 2 B13 = MO 2 B12 = MI 1 B11 = MM 1 B10 = MO 1 B9 = MI 0 B8 = MM 0 B7 = MO 0 B6 to B0 = Number of events in FIFO at the moment the trigger arrived (not at read out time) (B6 = msb)

Configuration octant numbering in output word



5. View of frontpanel



Meaning of LEDs when ON
PWR - Power is present
1Hz - 1Hz signal from GPS is present
RUN - Run bit is set via VME
EXP - Experiment alive signal from GPSTIM is present
NIM - Trigger disable from NIMROD(s) is active
RST - System reset from VME or reset bit is set
COS - Cosmics trigger are present
to GPS NIM - Trigger to NIMRODs and GPSTIM
Word limiter is active
Valid VME cycle

6. List of frontpanel connectors

CPC1-2 x 20 pins 0.1 inch connector.
Connection between CTT and CPC.

Pin	Signal	Pin	Signal
1	Octant2-MO (+)	2	Octant2-MO (-)
3	Octant2-MM (+)	4	Octant2-MM (-)
5	Octant2-MI (+)	6	Octant2-MI (-)
7	Octant6-MO (+)	8	Octant6-MO (-)
9	Octant6-MM (+)	10	Octant6-MM (-)
11	Octant6-MI (+)	12	Octant6-MI (-)
13	Scintillator input (+)	14	Scintillator input (-)
15	Scintillator Test Ref. Timing (+)	16	Scintillator Test Ref. Timing (-)
17	T0CAL Ref. Timing (+)	18	T0CAL Ref. Timing (-)
19	CPC Test Ref. Timing (+)	20	CPC Test Ref. Timing (-)
21	Random (+)	22	Random (-)
23	L3 Muon Trigger (+)	24	L3 Muon Trigger (-)
25	Not Connected	26	Not Connected
27	Not Connected	28	Not Connected
29	Not Connected	30	Not Connected
31	Not Connected	32	Not Connected
33	Not Connected	34	Not Connected
35	Not Connected	36	Not Connected
37	Spare2 (+)	38	Spare2 (-)
39	GND	40	GND

CPC2-2 x 20 pins 0.1 inch connector.
Connection between CTT and CPC.

Pin	Signal	Pin	Signal
1	Octant3-MO (+)	2	Octant3-MO (-)
3	Octant3-MM (+)	4	Octant3-MM (-)
5	Octant3-MI (+)	6	Octant3-MI (-)
7	Octant7-MO (+)	8	Octant7-MO (-)
9	Octant7-MM (+)	10	Octant7-MM (-)
11	Octant7-MI (+)	12	Octant7-MI (-)
13	Octant4-MO (+)	14	Octant4-MO (-)
15	Octant4-MM (+)	16	Octant4-MM (-)
17	Octant4-MI (+)	18	Octant4-MI (-)
19	Octant8-MO (+)	20	Octant8-MO (-)
21	Octant8-MM (+)	22	Octant8-MM (-)
23	Octant8-MI (+)	24	Octant8-MI (-)
25	Octant1-MO (+)	26	Octant1-MO (-)
27	Octant1-MM (+)	28	Octant1-MM (-)
29	Octant1-MI (+)	30	Octant1-MI (-)
31	Octant5-MO (+)	32	Octant5-MO (-)
33	Octant5-MM (+)	34	Octant5-MM (-)
35	Octant5-MI (+)	36	Octant5-MI (-)
37	Spare 1 (+)	38	Spare 1 (-)
39	GND	40	GND

GPS1-RJ45 connector.
Connection between CTT and GPS.

Pin	Signal	Pin	Signal
1	40 MHz (+)	2	40 MHz (-)
3	1 Hz (+)	4	1 Hz (-)
5	Exp. Alive (+)	6	Exp. Alive (-)
7	Trigger Allowed (+)	8	Trigger Allowed (-)

LEMO connector
Connection between CTT and GPS.
Signal name: GPS-Trigger

LEMO connector
Signal name: Monitor GPS-Trigger

LEMO connector
Signal name: Monitor Cosmics Trigger

NIMROD1-2 x 5 pins 0.1 inch connector.
Connection between CTT and NIMRODS

Pin	Signal	Pin	Signal
1	Trigger Disable_L	2	GND
3	Clock 40 MHz (+)	4	Clock 40 MHz (-)
5	GND	6	GND
7	Reset/Trigger (+)	8	Reset/Trigger (-)
9	GND	10	Reset_N