An Innovative Radiation Hardened CAM Architecture

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Abstract

This article describes an innovative Content Addressable Memory (CAM) cell with radiation hardened (RH) architecture. The RH-CAM is designed using a commercial 28 nm CMOS technology. The circuit has been simulated in worst-case conditions, and the effects due to single particles have been analyzed by injecting a current pulse into a circuit node. The proposed architecture is suitable for on-time pattern recognition tasks in harsh environments, such as front-end electronics in ATLAS experiment at Large Hadron Collider (LHC) and in space applications.

Keywords: radiation hardening, CMOS technology, integrated circuits

1. Introduction

The "Associative Memory" (AM) chip used in the Fast TracKer (FTK) system of the ATLAS experiment at CERN [1] is a large digital chip based on Content Addressable Memory (CAM) architecture and dedicated to real-time pattern recognition. It has been designed using different technologies; the last version (AM06) contains 421 million transistors [2]. The AM06 employs a CAM cell called XORAM, made with a conventional 6T SRAM and a XOR gate [3].

The AM chip designed for FTK is not radiation hard, since it does not operate close to the particle beam.

Standard electronic circuits have high sensitivity to hard and soft effects of radiation and they are not suitable for harsh environments such as space and front-end of high energy physics experiments. High radiation levels produce critical effects on electronic devices. The radiation effects can be divided into two main categories: (1) total dose effects, i.e., cumulative effects from long-term exposure, and (2) single event effects that are due to the interaction with a single particle.

The 28 nm CMOS technology is intrinsically tolerant to total dose effects. **Single event effects (SEE)** produce "soft errors", which do not cause permanent damage to the circuit; however, they may change the logic value stored in a memory cell, thus causing a **Single Event Upset (SEU)**.

2. Radiation Hardened CAM architecture

To avoid SEU effects on CAM cells in harsh environments, a novel radiation hardened architecture is presented in this article. The proposed solution is based on Radiation Hardening

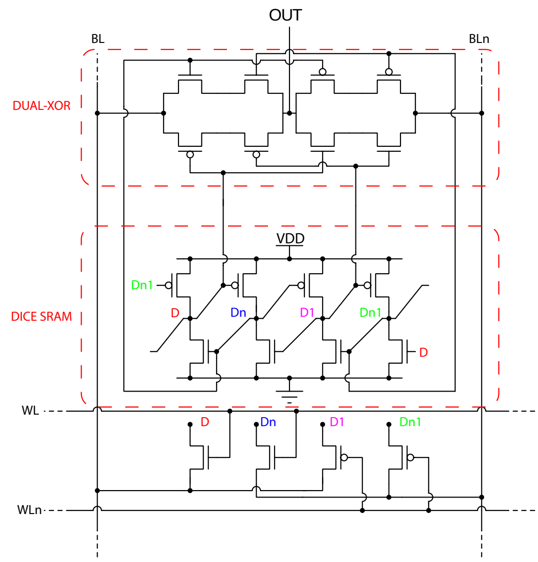

Figure 1: Schematic of the Radiation Hardened CAM (RH-CAM)

By Design methodology (RHBD), i.e., it employs circuit-level design techniques to prevent SEU, without requiring modifications to the fabrication process. Figure 1 shows the schematic diagram of the cell, which is composed of two main parts.

1. *Single bit memory cell*: As the standard SRAM is sensitive to SEU effects, the **Dual Interlocked Storage Cell (DICE)** architecture is employed to increase the tolerance to SEU [4]. The DICE contains duplicated data. Nodes D and D1 in Figure 1 are *'homologous'* nodes, as they have the same logic value (nodes Dn and Dn1 are the homologous pair at the opposite logic value). The simultaneous change of both identical bits is required to change the stored data. Therefore, if a single particle affects the voltage of one of the homologous nodes in a DICE, then the

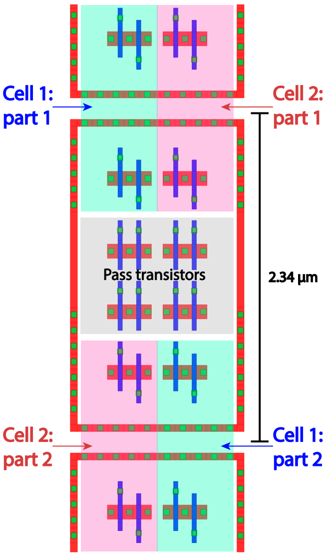

Figure 2: Layout of the Radiation Hardened CAM (RH-CAM) in 28 nm CMOS

cell should not exhibit an SEU.

2. *Dual-XOR logic*: In the original CAM cell, if a particle affects one of the four transistors of the XOR gate, the OUT signal will show an incorrect comparison result. Instead, in the proposed architecture, the dual-XOR gate compares the input logic value that comes from BL and BLn with the duplicated bits, and the output goes to 0 only if the input data matches both the homologous bits.

Therefore, any transient effect on the dual-XOR logic and on the DICE SRAM is mitigated and can not affect the result of the comparison. In the design of the cell layout, the homologous nodes of the DICE have been separated, to prevent a SEE from affecting both of them simultaneously (Figure 2).

3. Simulation of Single Event Effects

Current injection is employed to simulate the Single Event Effects on the sensitive nodes of the circuit. The energy required to generate a Electron-Hole Pair (EHP) in silicon is 3.6 eV; thus the collision of a 18 MeV proton generates $5 \cdot 10^6$ EHPs, corresponding to a total charge of $Q = 8 \cdot 10^{-13}$ C. The area affected by charge generation has a diameter equal to 1.94 µm, and the charge density is modelled as a discrete triangular distribution.

The area of a transistor only intersects a small fraction of the area of the generated charge, hence only a fraction of the total current will be injected into a node. By taking the ratio of transistor active area to the area affected by the interacting particle, we obtain that the maximum charge collected by a single node is 2.8×10^{-15} C. We assume a triangular current pulse, with duration $\Delta t = 50$ ps. The current peak I_{max} is calculated as:

$$Q = \int i\,dt = \frac{I_{max} \cdot \Delta t}{2} \qquad \Rightarrow \qquad I_{max} = 112\,\mu\text{A}$$

Simulations were performed by injecting the triangular current pulse into each one of the four DICE nodes, with both possible stored bit values. Figure 3 shows the DICE with the generator used to inject the current pulse into the node Dn.

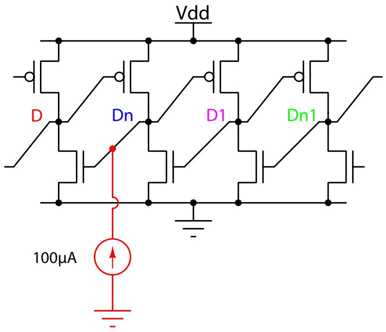

Figure 3: Current injection simulation

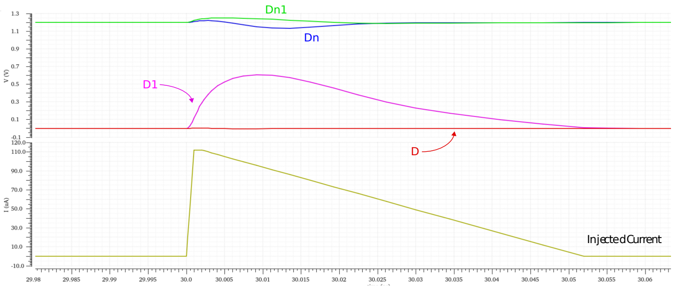

Figure 4: DICE simulation injecting 100 µA on node D1

Nodes with a logic value set to 1 exhibit a voltage spike with recovery proportional to the fall time. However, nodes storing a logic value equal to 0, exhibit a permanent logic value change, which propagates to all nodes of the DICE SRAM, thus resulting in a SEU, with the loss of the stored data.

The RH-CAM has been modified by increasing the width of MOS transistors. According to simulation results, to avoid the SEU, the optimal solution (at the cost of increased cell size) is to use 400 nm as the width for both P- and N-type MOS transistors, instead of the minimum width of 100 nm (Figure 4).

4. Conclusion

A novel Radiation Hardened CAM (RH-CAM) architecture is presented. It employs RHBD to achieve high tolerance to Single Event Effects, which have been confirmed by simulation results. An array of RH-CAM cells can be employed in readout electronics in extreme applications such as ATLAS experiment in LHC, for real-time pattern recognition tasks. It has the advantages of being programmable during the operation by changing the stored data which will be used for the comparison.

References

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