Design of the ATLAS phase-II hardware-based tracking processor

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Abstract

The expected factor four increase in peak luminosity of the high-luminosity LHC (HL-LHC) compared to the current LHC system will force the ATLAS experiment to increase early stage trigger selection power. The agreed strategy is to implement precise hardware track reconstruction, through which sharper trigger turn-on curves can be achieved for primary single-lepton selections, while contributing to b-tagging and tau-tagging techniques as well as pileup mitigation for hadronic signatures, such as multijet and missing transverse momentum.

This work discusses the requirements, architecture and projected performance of the system in terms of tracking capability, and trigger selection, based on detailed simulations.

Keywords: ATLAS, Trigger selection, FPGA, Associative memory, Track reconstruction
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1. Introduction

The expected increase in peak luminosity to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ of the HL-LHC will force the ATLAS experiment [1] to increase early stage trigger selection power. The strategy for the ATLAS phase-II trigger and data acquisition system upgrade is to implement precise hardware-based track reconstruction. The hardware-based tracking for the trigger (HTT) system uses a combination of associative memory (AM) ASICs for pattern recognition and FPGAs for track reconstruction and fitting. It provides the upgraded software-based trigger system, the event filter (EF), with access to tracking information.

2. Hardware-based Track Reconstruction

Particle hits in the pixel and strip detector from the ATLAS inner tracker (ITk) (Fig. 1a) are sent by the EF to the HTT where two stages of processing are implemented.

2.1. First Processing Stage

In the first processing stage, the particle hits from eight ITk layers are clustered in FPGAs into consecutive ITk strip or pixel channels (Fig. 1b). The cluster information is sent into the AMs where it is compared to a large bank of pre-computed patterns derived from simulation. The track candidates corresponding to a positive match are in this way identified (Fig. 1c). The quality of the track candidates is computed as a χ^2 in FPGAs, using the corresponding full-resolution hits coordinates. After a χ^2 cut, five track parameters (d_0, z_0, ϕ_0, q/p, $cot(\theta_0)$, or equivalent) are calculated (Fig. 1d). This concludes the first stage of processing.

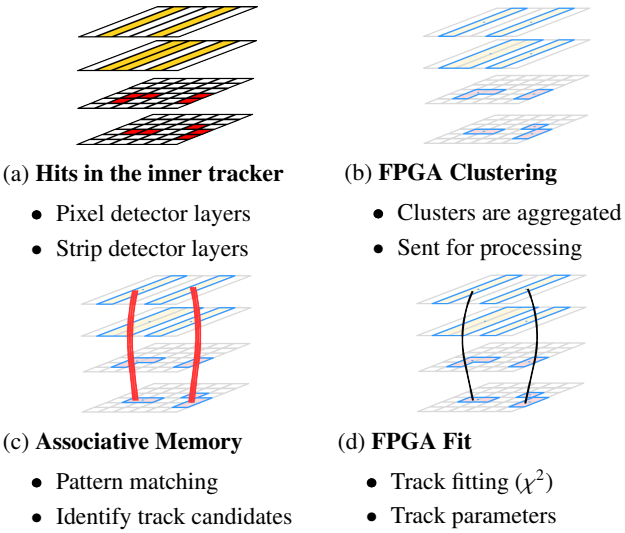

Figure 1: Track reconstruction scheme. Starting from (a) particle hits in the pixel and strip layers of the ATLAS ITk, (b) the hits are then clustered and aggregated in FPGAs. This information is passed to AM ASICs for pattern matching, which identifies possible track candidates. Finally (d) The track parameters are computed in FPGAs together with a χ^2 as quality indicator.

2.2. Second Processing Stage

The second processing stage refines the first-stage fitting by taking into account hits from every ITk layer. It is optional

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and it starts right after the first stage. It extrapolates each first-stage track to the other ITk layers and it associates any matching hit. The tracks are then fitted again in order to achieve better parameter resolution.

3. The HTT System

The HTT system is organised as independent logical tracking units called HTT units (Fig. 2). Each unit comprises two types of trigger processing boards: the associative memory tracking processor (AMTP), corresponding to the first processing stage, and the second-stage tracking processor (SSTP), corresponding to the second processing stage.

Each HTT unit has 6-to-1 AMTP and SSTP boards respectively. The AMTP board holds two pattern recognition mezzanine (PRM) cards, which carry out the first processing stage, while the SSTP holds two track fitting mezzanine (TFM) cards, which carry out the second processing stage.

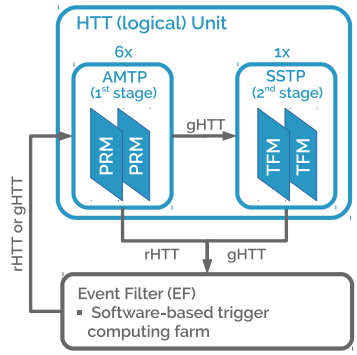

Figure 2: Schematic view of the HTT Unit. The AMTP processes ITk data and produces first-stage tracks, which is sent back to the EF in case of rHTT request or to the SSTP in case of gHTT request for further processing. The SSTP uses the AMTP output to process additional ITk data and returns second-stage tracks to the EF.

3.1. Regional and Global Tracking

Depending on the trigger signature two types of track reconstruction requests can be sent from the EF to the HTT system: regional (rHTT) or global (gHTT), corresponding to the first stage only or to the first plus second stage of processing.

The rHTT searches for all tracks with $p_T > 2$ GeV in limited $\eta \times \phi$ regions of interest defined by the previous level of trigger decision, and it operates at the rate of 1 MHz. It uses only eight ITk detector layers and it processes on average 10% of all ITk detector data in these events. The gHTT searches for all tracks with $p_T > 1$ GeV at a rate of 100 kHz. Both rHTT and gHTT cover the full ITk acceptance ($|\eta| < 4$).

4. Tracking Capability

Each pattern stored in the AM ASICs corresponds to a sequence of eight clusters. The choice of layers and the mixture of strip and pixel layers depends on the track pseudorapidity (Fig. 3) and affects the number of patterns to be stored in the AM, the number of false matches produced and the resolution of the tracks.

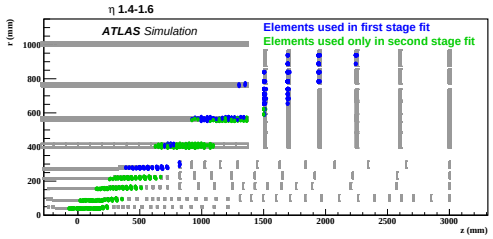

Figure 3: Inner Tracker Layers used for 1st and 2nd stage track fitting corresponding to the 1.4-1.6 η-region. In blue, the eight layers hits used in the first-stage. In green, the additional layers used in the second-stage [2]

4.1. Regional Tracking Performance

The regional tracking performance is calculated assuming a $\eta \times \phi$ region of 0.2×0.2 for primary leptons, while for small-R (large-R) jets 0.8×0.8 (2.0×2.0) regions would be used instead.

The rejection as a function of efficiency when requiring a track with a minimum p_T for the electron is shown in Figure 4. The rejection is approximately a factor 5 (3) for 95-97% (96-99%) signal efficiency and a trigger threshold of 18 GeV (10 GeV).

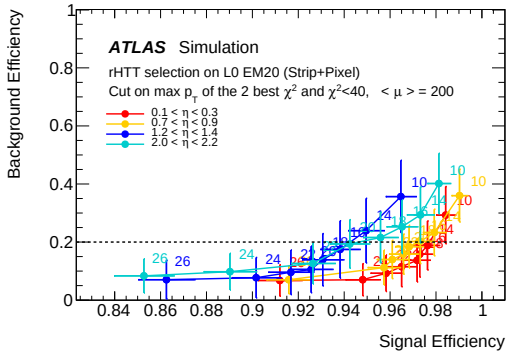

Figure 4: Regional tracking (rHTT) background rejection as a function of the signal efficiency for electrons. The EF track p_T trigger threshold is indicated next to the lines [2]

References

[1] ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST 3 (2008) S08003. doi:10.1088/1748-0221/3/08/S08003.

[2] ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System, Tech. Rep. CERN-LHCC-2017-020. ATLAS-TDR-029, CERN, Geneva (Sep 2017).