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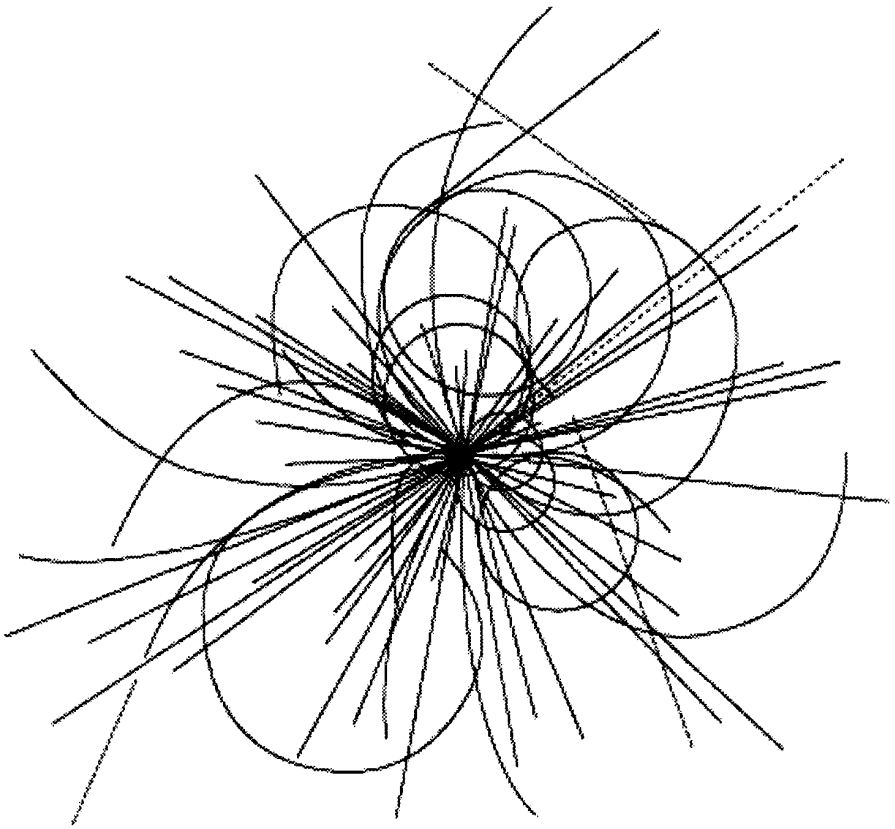

Superconducting Super Collider Laboratory

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A Bipolar Integrator for Secondary Emission Profile Monitors at the SSCL

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A Bipolar Integrator for Secondary Emission Profile Monitors at the SSCL

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Abstract

Many invasive techniques for monitoring beam profile and intensity require secondary emission signals in order to make the measurement. Signal acquisition and processing can take many forms. This paper describes a bipolar integration technique which uses the Burr-Brown ACF2101 Dual Switched Integrator chip and applications for accelerator beam instrumentation.

1.0 INTRODUCTION

Invasive accelerator instrumentation devices based on the principle of secondary emission can accommodate a variety of readout electronics. The decision on what type of electronics to use depends on what information is needed from the measurement. If temporal waveform information is required then a simple current to voltage converter (I-V) can be used as the first stage of the acquisition system. This method preserves time information and allows for waveform digitization of the signal. Once the waveform has been recorded off-line data analysis can be used. However, this method can be costly when multiple channels are required and high data transmission rates are a concern. When the instrument is used in a noisy environment, the signal-to-noise can be a problem. For most of these problems, integration is the reasonable solution if temporal information can be sacrificed for improved signal-to-noise. The Burr-Brown ACF2101 dual switched integrator provides a good solution for signal integration of waveforms where accuracy and dynamic range are of importance. A circuit which is configured to handle bipolar signals can be easily designed around the Burr-Brown chip. The technique describe in this paper uses multiple channels of bipolar integrators multiplexed into a single 12-bit Analog to Digital Converter (ADC). The integrator circuit consists of two channels of the ACF2101, a bias current source and an instrumentation amplifier. See Figure 3 for a more detailed circuit description.

2.0 UNIPOLAR CIRCUIT

The Burr-Brown ACF2101 dual switched integrator is a two channel integrating chip designed to measure current for precision applications. Each channel has an internal integrating capacitor, reset, hold and multiplexing switch circuitry.[1] By having all components on a single chip the need to match discrete components has been eliminated. The chip internal layout has been designed so many different configurations can be realized. The internal integrating capacitor can be bypassed when the need arises or an external capacitor can be placed in parallel with the internal capacitor. Also, if multiplexing is not needed the switch circuitry can be bypassed. Figure 1 shows one channel of the chip.

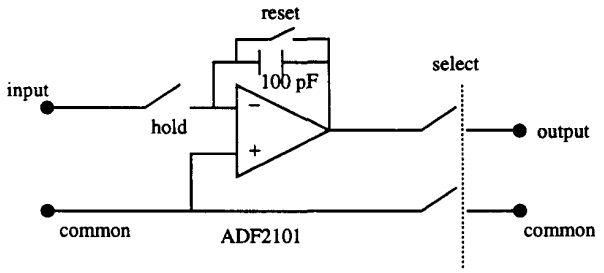

Figure 1. One Channel of the Burr-Brown ACF2102 Showing the Internal Capacitor and Switching Circuit.

In normal operation the integration process is begun by closing the HOLD switch and opening the RESET switch. Charge accumulates on the integrating capacitor until the HOLD switch is open. It is important to account for the relatively high ON resistance of the hold switch for those applications where the current source is less than perfect. The circuit timing diagram for the standard integration mode is shown in Figure 2. The switches work with TTL active LOW logic, therefore a LOW is required to close the switch.

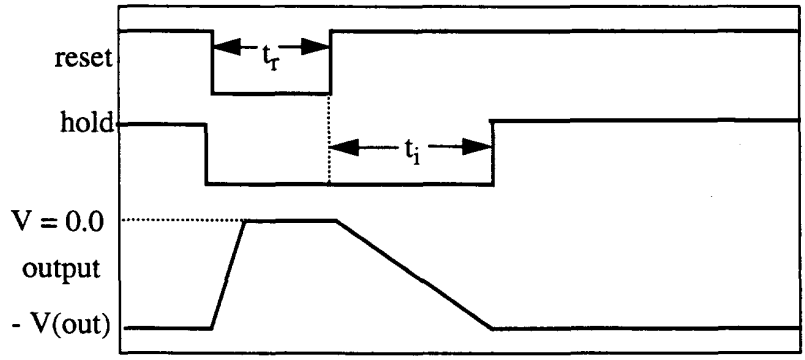

Figure 2. Time Diagram for the ACF2101.

The output voltage of the circuit is given by the transfer function:

$$V(t)_{(out)} = \frac{-1}{C_{(int)}} \int i(t)\, dt. \qquad (1)$$

Where:

$V(t)_{(out)}$ = Output voltage (V) as a function of time.

$C_{(int)}$ = integration capacitor (Farads).

i = is the instantaneous input current (Amperes).

t = is the integration time (seconds).

Table 1 lists some typical integration parameters with the corresponding output voltage for constant input current.

Table 1. Typical Beam Parameters and Output Voltages.

I (μA)	Δt (μs)	$C_{(int)}$ (pF)	$V_{(out)}$ (V)
1	10	100	–0.1
10	10	100	– 1.0
100	10	100	–10.0

3.0 BIPOLAR CONFIGURATION

For bipolar configuration both channels must be used for one output to the ADC. The single channel bipolar configuration of the ACF2101 is shown in Figure 3.

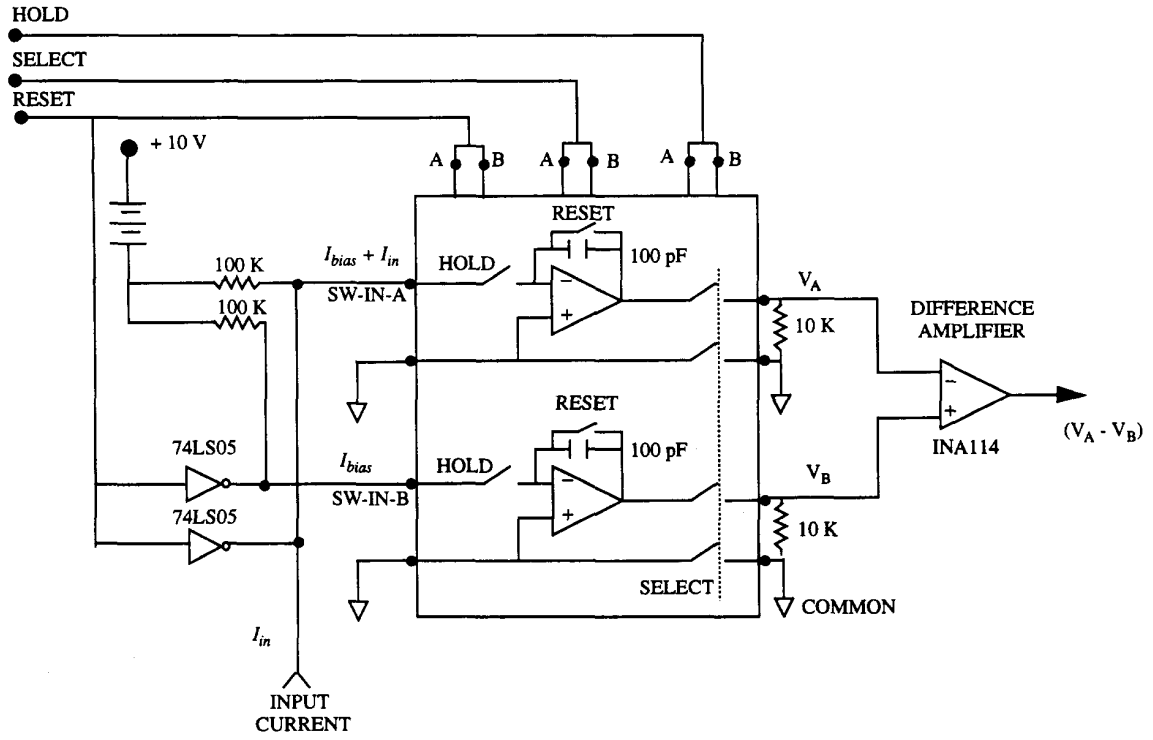

Figure 3. The Bipolar Configuration of the Burr-Brown Integrator ACF2101.

In the configuration shown in Figure 3 the internal capacitor is used. The signal input (I_{in}) is connected to SW-IN-A along with an offset bias current (I_{bias}). The offset bias current is also connected to SW-IN-B. This method generates equal bias currents on both inputs for any given integration time. Therefore the bias current is independent of integration time yielding a larger dynamic range for a given application. The input signal from the detector is then summed with the offset bias current on channel A. When the difference of channels (V_A–V_B) are taken at the output, the remaining voltage is the result of the signal input current only. Equations (2)-(7) below illustrate the current paths for each input.

$$I(A) = I_{(in)} + I_{(bias)}, \tag{2}$$

and

$$I(B) = I_{(bias)}, \tag{3}$$

where:

$I_{(in)}$ is the input current from the source.

$I_{(bias)}$ is the bias current for each channel.

$I(A)$ is the total current at the input to channel A.

$I(B)$ is the total current at the input to channel B.

The voltage produced at the output of each channel for a given integration time is given by:

$$V(A) = (\frac{-1}{C}) I(A) \times \Delta t \quad , \tag{4}$$

and

$$V(B) = (\frac{-1}{C}) I(B) \times \Delta t \ . \tag{5}$$

The difference is then:

$$V(A) - V(B) = \frac{-1}{C} (I(A) - I(B)) \times \Delta t \ . \tag{6}$$

By replacing the values for I(A) and I(B) from Eqs. (2) and (3) the output voltage is then:

$$\Delta V(out) = \frac{-1}{C} (I(in)) \times \Delta t \quad . \tag{7}$$

To prevent charge transfer when the HOLD switch is closed, an open collector (74LS05) operating in the saturated mode is connected to the input and is gated ON when integration is completed. This prevents voltage breakdown across the HOLD switch by maintaining a voltage on the order of 200 mV at the input node.

The following example will help explain the difference between the unipolar and bipolar full scale outputs of the circuit. A circuit configured in a unipolar mode to produce a maximum output voltage of –10.0 V across a 100 pF capacitor requires an input current of 100 µA during an integration time of 10 µs. The bipolar mode is configured for an offset voltage of –5.0 V on each channel do to a bias current of 50 µA. This limits the full scale signal current to ± 50 µA. +50 µA on the input will produce a difference output of –5.0 V and a –50 µA input will produce a +5.0 V difference output. Table 2 lists some typical voltage output values based on the bipolar configuration and using the 100 pF internal capacitor of the chip.

Table 2. Output Parameters for the Bipolar Integrator.

$I_{(input)}$ (μA)	Bias Current (μA)	Integration Time (μs)	Output A (V)	Output B (V)	Difference Output (V) (A - B)
0.0	50.0	10	-5.0	-5.0	0.0
+10.0	50.0	10	-6.0	-5.0	-1.0
+20.0	50.0	10	-7.0	-5.0	-2.0
+50.0	50.0	10	-10.0	-5.0	-5.0
-10.0	50.0	10	-4.0	-5.0	1.0
-20.0	50.0	10	-3.0	-5.0	2.0
-50.0	50.0	10	0.0	-5.0	5.0

3.0 EXPERIMENTAL RESULTS

Frequency response for the ideal integrating function is given by $1/s\tau$ where $\tau = RC$ and $s = j\omega$. R is the resistance of the HOLD switch (1.5 kΩ) in the closed position and C is the capacitance used for integration. Finite open-loop gain and bandwidth limitations permit a real device to only approximate this ideal frequency response.[2,3] Figure 4 shows the ideal and measured frequency response of an integrator. The real integrator deviates from the ideal case at a frequency of approximately 100 kHz.

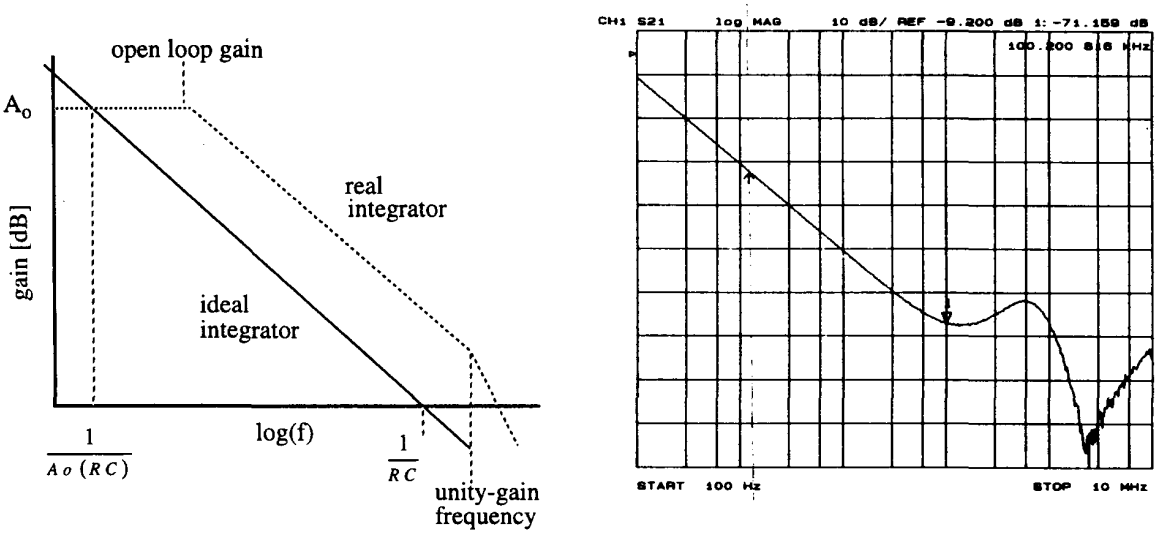

Figure 4. Integrator Frequency Response. The plot on the left is the theoretical response for an integrator. The plot on the right is the measured frequency response of an integrator in the bipolar configuration.

The pole at 100 kHz becomes significant when the circuit is used to measure a waveform in time. Input signals which contain frequencies above 100 kHz will be filtered out and the integral slope will not be a true representation of the input waveform. The final result will be correct but sufficient time must be allowed for the output to stabilize. In the application presented here only the final value is of interest.

3.1 Linearity

A measure of the integrator's ability to give a linear voltage response over a large range of input charges is called the linearity. By plotting the output voltage as a function of the input charge, a determination of the integrator's linearity can be made. For an ideal integrator the output voltage should be directly proportional to the input for all charges as shown in Eq. (8):

$$V = \frac{Q}{C} \,. \tag{8}$$

In Figure 5 a plot of the calculated and measured voltage output for a given charge input of the Burr-Brown ACF2101 is shown. The input charge was determined by producing a known current at the input and integrating for a fixed amount of time.

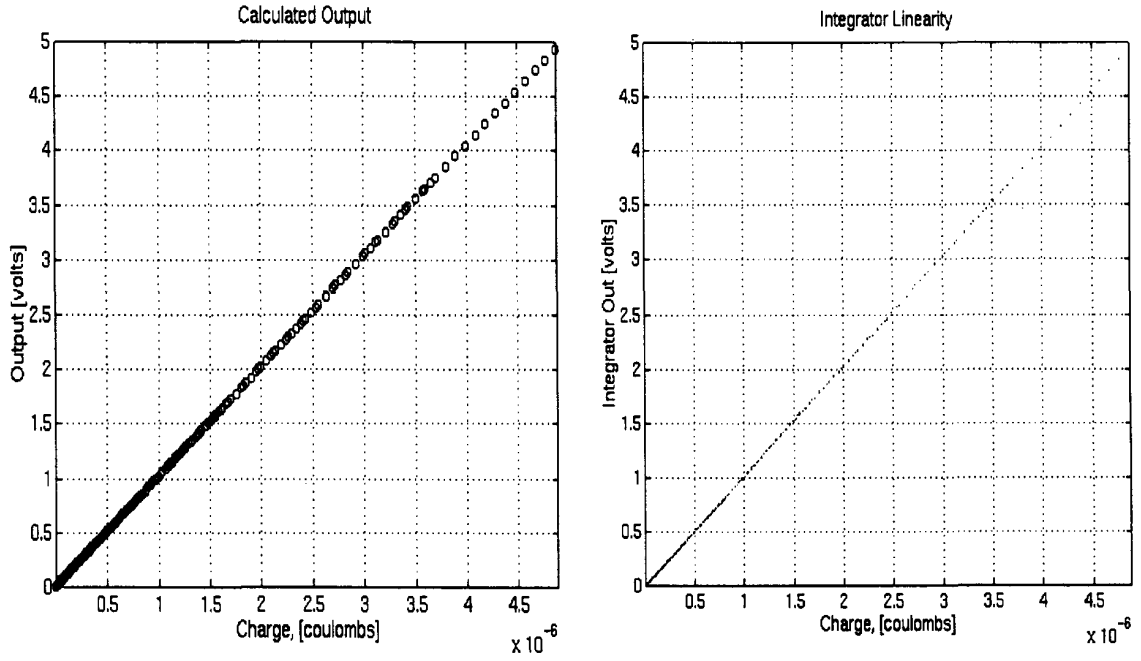

Figure 5. Linearity Plots for the Burr-Brown Integrator ACF2101. The plot on the left shows the calculated values and the plot on the right shows the measured values.

Once the calculated and measured values have been determined an error plot of the difference and percent difference between the calculated and a line fitted to the measured values can be made. The difference values yield the performance of the system under test. Figure 6 shows the difference and percent difference of the ACF2101.

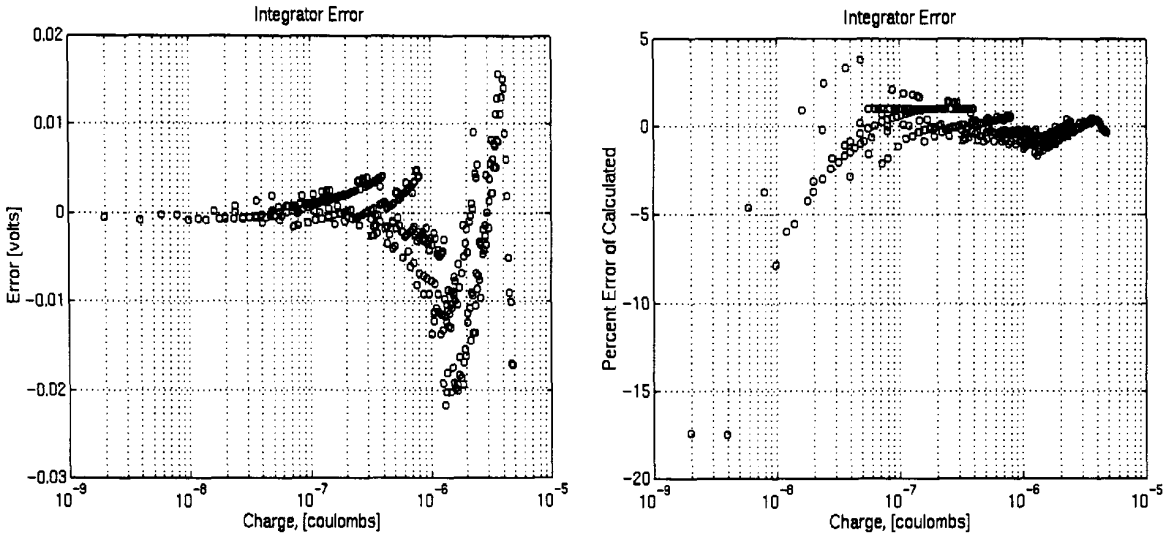

Figure 6. Difference and Percent Difference Errors for the Burr-Brown ACF2101 Integrator Circuit. The plot on the left is the difference between the calculated and measured values. The plot on the right is the percent difference between the calculated and measured values. From the error plot it can be seen that the maximum voltage error is less than 22 mV or 0.2% of full scale. If a 12- bit ADC were to be used for data acquisition this would be less than 1 LSB.

3.2 Output Results

Figure 7 is a plot of the ACF2101 integrator output of each channel before the signal enters the difference circuit using an integrating capacitor of 100 pF. The top trace is the RESET line which shorts the integrating capacitor when active LOW. The second trace is the HOLD switch and is closed when active LOW. The bottom two traces are the outputs from each channel when a fixed current of 68 μA was applied to each channel for 10.2 μs.

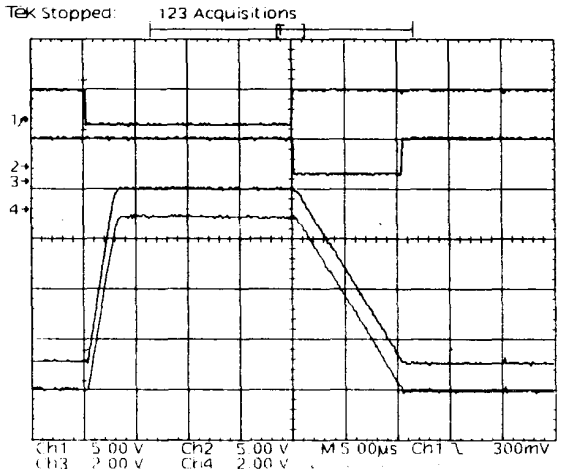

Figure 7. Typical Output from the ACF2101 Chip.

Figure 8 is a plot of the output from the difference circuit when ± 25 μA has been applied to the input with an integration time of 100 μs and an integrating capacitor of 1000 pF. The top trace is the integration time. The middle two traces are the outputs of the integrator before entering the difference circuit. The bottom trace is the output from the difference circuit.

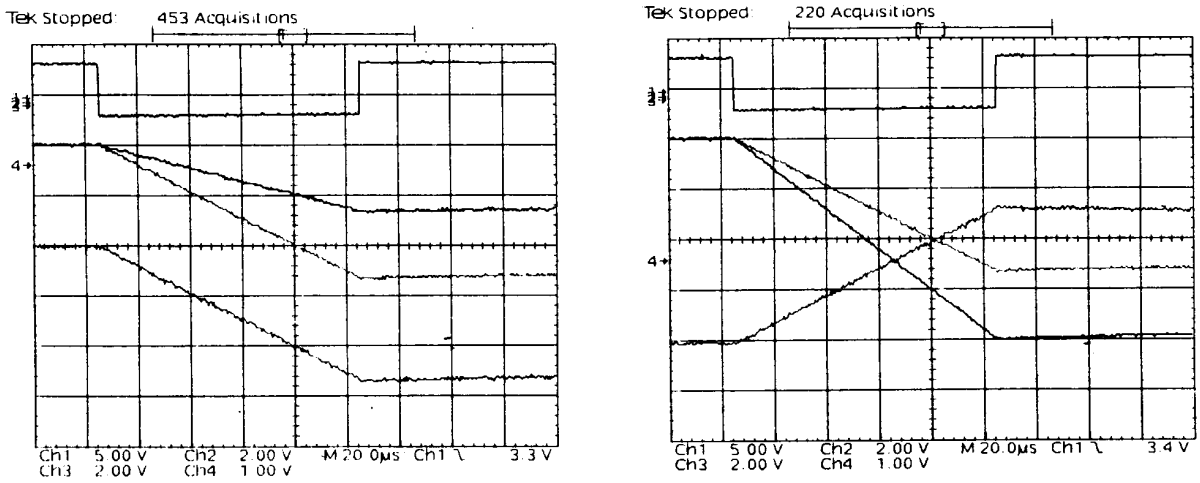

Figure 8 Output Plot when ± 25 μA Has Been Applied to the Input with an Integration Time of 100 μs. The plot on the left has an input current of -25 μA and the plot on the right has an input of ± 25 μA.

4.0 BIPOLAR MULTIPLEXING

Multiplexing of the ACF2101 is straightforward because of the integral design of the multiplexing circuitry on the chip. With a proper layout design, 200 ns switching times can be achieved. A typical multiplexing circuit for the bipolar configuration is shown in Figure 9.

The maximum number of multiplexed channels is determined by the board size, surrounding circuitry and multiplexing requirements to name a few. The least expensive approach is to have multiple channels and one ADC. Typical conversion times for a 12 bit ADC with a full scale of 5 volts output are less than 10 μs. For a measurement that requires a full scale accuracy of 1% or 50 mV, the number of channels for each ADC is determined by the multiplexing switch time and the ADC conversion time. The ADC conversion time also includes the settling time of a sample and hold if required.

The sum of the switch times (t_s) and ADC conversion time (t_c) must be less than or equal to the droop time (t_d) of 12.5s @ 40°C for 1% accuracy of 5 volt full scale ($T_s + T_c <= t_d$). Where T_s and T_c are the total number of switching cycle times and the number of conversion times respectively.

The droop rate is dependent on the temperature and the integrating capacitor that is chosen. The droop rate can be calculated by:

$$Droop = \frac{100fA}{C_{(int)}} , \tag{9}$$

where $C_{(int)}$ is the integrating capacitor of the system. The droop rate doubles for every 10°C rise in temperature. For an internal capacitor of 100 pF @ 40° C this corresponds to four times 1nV/µs or 4nV/µs.

See Figure 10 for droop timing information.

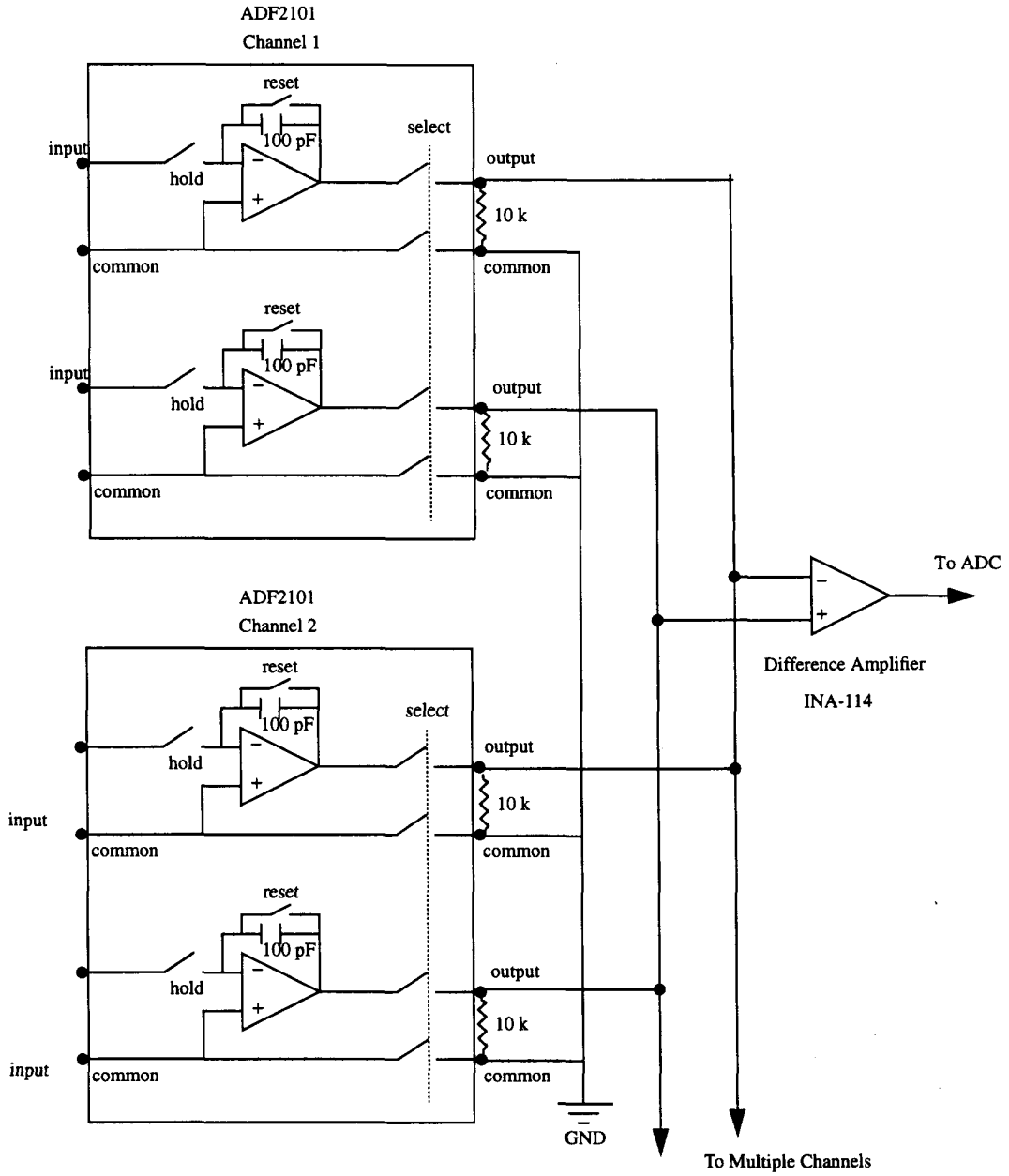

Figure 9. Bipolar Circuit Configuration for Multiplexing of the ACF2101 Chip.

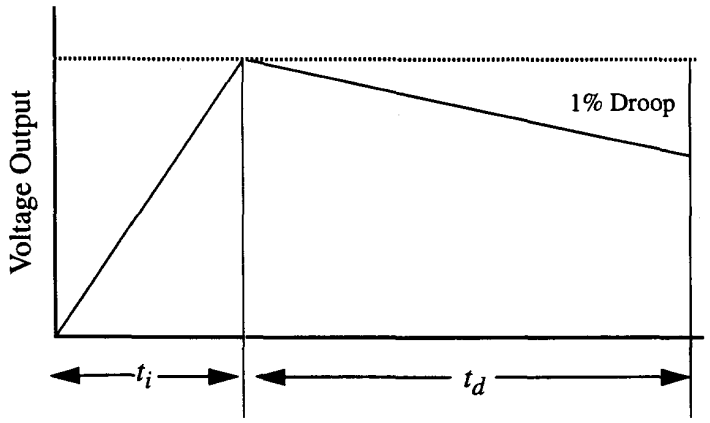

Figure 10. Droop Rate Timing Diagram.

The total switching time can be determined by viewing the switching logic for multiple channels as shown in Figure 11.

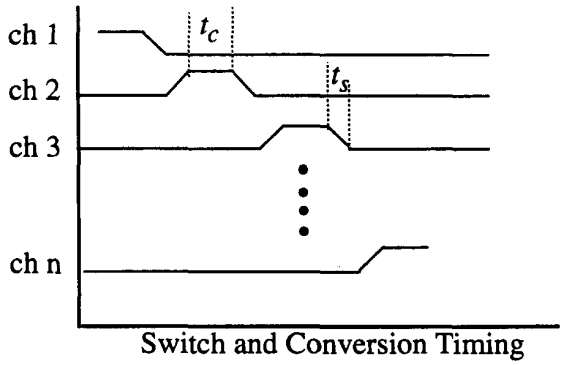

Figure 11. Timing Diagram Showing the Switch and Conversion Cycles for Each Channel.

If there are "N_{ch}" channels then the total conversion time would be:

$$T_c = (N_{ch} - 1) \times t_c \ . \tag{10}$$

The total switching time would be:

$$T_s = 2(N_{ch}) \times t_s \ . \tag{11}$$

For an eight-channel system the total time would be less than 100 μs. Figure 12 shows a typical multiplexed output for the ACF2101 on a prototype board. The top trace is the waveform before the signal is multiplexed. The middle and bottom trace are two channels from a multiple channel system. The multiplexing switch time is on the order of 400 ns. This time could be decreased when proper attention has been considered during the layout

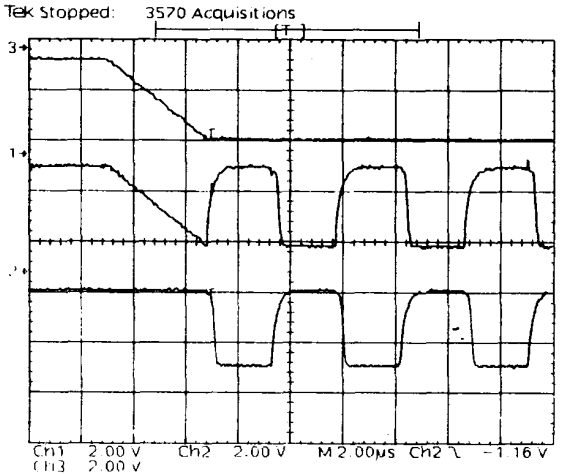

Figure 12. Multiplexed Output of the ACF2101 Burr-Brown Integrator Chip.

5.0 APPLICATIONS

This bipolar integration technique is used at the present time on all data acquisition systems for the intercepting monitors and beam current monitors in the SSC LINAC.[4,5] The main application and design effort shall be for multiwire profile monitors which will be located in the test beam line, transfer lines and beam bumps. In applications that require preamplification for signal transmission through long cables lengths, a (V-I) converter will be part of the circuit design located before the integrator. Figure 13 shows a typical test pulse and integrated pulse from a current monitor in the LINAC. The waveform is 35 μs long and both were signals were digitized at 200 ns per point.

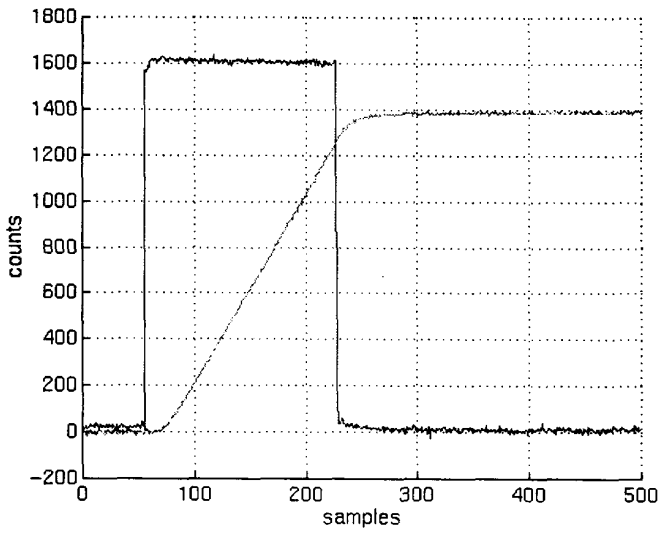

Figure 13. Typical Test Pulse and Integrated Pulse From a Current Monitor. The waveform is 35 μs long and both were digitized at 200 ns per point.

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