RGANIZATION FOR NUCLEAR RESEARCH

CERN/ECP 92–6
11 August 1992

DESIGN AND PERFORMANCE OF THE OMEGA-ION HYBRID SILICON PIXEL DETECTOR

CERN Detector R&D Collaboration RD-19, presented by Michael Campbell

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ABSTRACT

Specific features of the Omega-Ion pixel detector are the adjustable delay with external trigger capability and the detector leakage current compensation. A row of pixels can be used for testing the electrical performance of the amplifier and comparator circuits. Detailed results of these electrical tests are presented. The readout chip has been bump-bonded to a silicon detector with 75 μm × 500 μm elements. Three complete hybrid detectors have been tested with ionizing particles from heavy ion interactions in the Omega spectrometer. The event information for several million triggers is analyzed for various conditions of strobing, delay and threshold setting.

Presented at the 6th European Symposium on Semiconductor Detectors
24–26 February 1992, Milano, Italy

(Proceedings to be published by Nucl. Instr. and Methods)

Mac/Word/8023F/MC/sj

1. INTRODUCTION

A hybrid silicon pixel detector has been tested in the Omega-Ion experiment WA94 at CERN. This device combines a two-dimensionally segmented silicon detector of 1006 sensor elements in 16 columns and 64 rows with a geometrically identical matrix of readout electronic circuits with active, fast pulse processing electronics in each cell.

Pixel detectors present obvious advantages in particle physics applications, particularly in high multiplicity and high rate environments like heavy ion experiments and hadron colliders. After a number of preliminary studies [1, 2 and 3], we published in November 1991 the first results obtained in an experiment with this 1006 element hybrid pixel detector [4]. Besides our own effort, other groups have been studying pixel detectors for similar applications. In particular, should be mentioned the group at the Rutherford Appleton Laboratory which pioneered CCD-type pixel detectors [5] and a separate effort aiming at direct readout pixel detector structures [6]. At Stanford a monolithic detector has been manufactured and the first results are reported in these proceedings [7]. An SSC collaboration has worked with Hughes Aircraft on a hybrid device [8]. In the Max Planck Institut in Munich pixel detectors with integrated amplification and charge storage are being developed [9]. At IMEC in Leuven various types of pixel detector have been developed by Vanstraelen and Dierickx [10, 11].

In this paper we study much more closely the performance of the hybrid pixel detector described in ref. [4]. In sects 2 and 3 we present a detailed functional description of the readout chain for an individual pixel element and the general architecture of the readout chip. This chip was tested electrically and the results obtained are discussed in sect. 4. A small telescope was constructed using three planes of pixel detectors and this was placed in the heavy ion experiment WA94 in the Omega spectrometer at CERN. The particle beam results described in sect. 5 illustrate the usefulness of these pixel detectors as well as highlighting some problems. Finally, we draw some conclusions and discuss further work.

2. PIXEL ELECTRONICS

Each sensor element of the pixel detector is coupled to a complete electronics readout chain which is contained within a silicon area equal to the area of the sensor element, $75 \times 500\ \mu m^2$. A block diagram of this readout chain is shown in fig. 1. It contains a fast, charge-sensitive preamplifier (CSA), a comparator, a delay and a memory element. A signal from a sensor element is amplified by the CSA, discriminated by the comparator, delayed and gated into memory by the strobe, provided the strobe signal coincides with the delayed comparator signal.

Figure 2 shows the CSA with feedback which incorporates leakage current compensation. Transistors M1 and M3 form a folded cascode pair which provides the transconductance g_m required to transfer the input signal charge to the 7 fF feedback capacitor C_{fb}. The decay time constant of the CSA is around 1 μs. Transistors M2 and M4 control the bias currents of the folded cascode. M6 and M7 are two diodes connected in series which fix the DC operating point of the preamplifier. M9 is a diode which clips the output of the preamplifier for large input signals avoiding any saturation phenomenon which could block the circuit over a long period of time. The detector leakage current is compensated by using M5 to subtract a DC current equal to the leakage current detected on a dummy pixel.

Figure 3 is the schematic of the latched comparator. Transistors M10 and M11 form a differential stage which is AC coupled by the capacitor C_c. This differentiates the output of the preamplifier such that the resulting current in the pair has a peaking time of around 50 ns. The cross-coupled pair M16 and M17 behaves as a bistable feedback element which switches state when the differential current output of M10, M11 exceeds the bias current of M18 which is fixed by I_{dis2}. Thus, I_{dis2} can be used to adjust the threshold of the comparator. The regenerative circuit which is made by transistors M21 to M27 senses the switching of the comparator and latches the comparator output.

The latched output of the comparator is connected to the delay element which, as shown in fig. 4, is a series of three inverters whose switching speed is controlled by currents I_{dn} and I_{dp}. The I_{dn} (and subsequently I_{dp}) can be adjusted externally enabling the delay to be varied. The final inverter is not controlled in switching speed and it is used to clean up the edges of the output signal. The output from the delay resets the comparator via an OR gate. The delay thus defines the pulse width of the signal from the comparator.

Figure 5 shows the architecture of the coincidence logic and memory element. The multiplexor, MuxA, is used to ensure that the trailing edge coming from the delay inverters after twice the delay sets the D flip-flop if it coincides with the strobe. If a falling edge is present then a one is clocked into the D flip-flop element. When the strobe is low, MuxB connects all of the D flip-flops in one column of pixels together forming a vertical shift register which can be clocked using the *clkout* signal through MuxA. A drawback of this architecture is that the *clkout* must undergo a low to high transition during the strobe high phase to avoid false hits.

3. CHIP ARCHITECTURE

Figure 6 shows the architecture of the readout chip. After a strobe has been applied, each pixel which has been hit has a one in its D flip-flop. When read out the pixel readout cells form 16 parallel 64-bit long shift registers which are clocked out using a train of 64

pulses applied to the *clkout* terminal. Each column on the readout chip has 65 elements in total. The top row of pixels is not connected to the detector, but is coupled capacitively to an electrical input enabling the electrical performance of the chip to be evaluated independent of the detector bonding. This test input can be used for a functionality test prior to scribing and mounting of the chips and also during the detector operation for testing if there are no particles. An extra row of pixels at the bottom (not shown in fig. 6) serves as a row of dummy cells for detector leakage current detection and for the generation of bias currents for the column. The leakage current detected in the bottom cell of one column is mirrored to and subtracted from the input of each of the cells in that column.

A picture is taken (fig. 7) with a scanning electron microscope (SEM) of a small part of the readout chip. One recognizes the cells having each a solder bump ready for the input connection to the silicon detector chip.

4. ELECTRICAL MEASUREMENTS

As described above, all pixels in the top row are connected capacitively to an input bonding pad. The approximate value of the capacitor (calculated from the manufacturer's parameters and the drawn size) is around 30 fF. Note that in ref. [4] this capacitance was estimated at the lower value of 20 fF. The higher, but more precise estimation has forced us to scale up our original estimates of noise and threshold variation. The noise after rescaling is ~ 90 e^- r.m.s. Unambiguous determination of the noise figure needs absolute measurements in terms of the electron charge. Such measurements are currently performed using photon-emitting radioactive sources.

Figure 8 shows the thresholds of one row of 16 pixels at two different values of threshold current, I_{dis1}. The pixel-to-pixel variation is around 750 e^- r.m.s. and appears to be of a random nature suggesting that it is due to the poor reproduction of bias currents from one pixel to the next due to geometrical uncertainties in processing. This variation is calculated to be equivalent to 15 mV r.m.s. at the input to the discriminator. As the maximum size of the current mirror transistors is limited by the size of one pixel, we do not expect to be able to improve significantly this random variation in future versions. One possible remedy would be to increase the gain of the preamplifier in order to reduce the size of the r.m.s. variations relative to a given input signal. However, it would be difficult to reduce the size of the 7 fF feedback capacitor any further.

Measurements of the slew of the discriminator were made on a separate chip with pixels which had only the preamplifier and discriminator and no delay or coincidence logic. This slewing measured from 2x threshold to 10x threshold is < 15 ns and is constant for all cells.

A study was made of the strobe timing and variations as this ultimately limits the efficiency of the pixel detector device in a fixed-target application. A first observation proved that the minimum width of the strobe was around 150 ns. This was larger than expected, but it can be explained by the slewing of the strobe signal across the chip due to the large capacitances of the strobe lines. Figure 9 shows the delay between the arrival of the input test signal and the output of the delay element resulting from an input signal of 50 000 e^- for two values of delay control current, I_{dn}. There appear to be two effects superimposed in this case. Firstly, there is a random effect which presumably comes from the geometrical matching problems which we encountered with the threshold non-uniformity. Secondly, there is a left-right effect in the strobe timing. A detailed examination of the chip layout reveals that the power supplies were under-dimensioned leading to a drop in voltage across the chip from left to right. As the external delay control current is applied in parallel to one diode connected transistor per column, each of these diodes generated a slightly different I_{dn} and I_{dp} for each column. This led to the left-right variation in the delay timing.

The maximum readout frequency was measured to be 5 MHz. This was lower than simulations suggested, but it may be explained by the slewing of the *clkout* signal due to the large capacitance of the lines.

5. BEAM TEST RESULTS

Three pixel detectors were placed in the Omega heavy Ion experiment WA94 at CERN as discussed in ref. [4]. Each time a strobe was received from the experiment, an image was taken on all three planes and these planes were read out. Off-line analysis has been performed for various runs under different operating conditions. We report here only some results pertaining to the electrical operation of the readout chips.

Figure 10 shows a typical high-multiplicity event. It indicates very clearly the advantage of a true two-dimensional detector over a crossed strip approach.

A first set of runs was made under nominal bias conditions. The results of such a run are shown in fig. 11. Here each pixel is represented as a box whose length is proportional to the accumulated number of hits in the pixel. As the areas of the boxes are proportional to the square of the accumulated number of hits, the differences are exaggerated by these plots. There are several points of interest. Firstly, all pixels in all planes detected particles (no blank spaces) and there was only one noisy pixel (plane 3, column 8, line 0) which has been removed from the plot. Secondly, on all three planes there seem to be more pixels hit in the top left corner of the device and less at the opposite corner. The beam was at the top left corner of the chip and this means that the distribution of the hits could be due simply to the beam drop-off. We note here that in planes 1 and 2

the left-hand column seems to receive fewer hits than the rest. Also in plane 3 this effect is seen over the first 4 columns. This is explained later.

The next set of data taken was to look at the effect of varying the threshold of the discriminators to see if there was some change in the behaviour. The bias current I_{dis2} was varied only on the plane 2 leaving planes 1 and 3 under nominal bias conditions. Figure 12 shows that the pixel behaviour changes only slightly over a wide range of threshold currents. This result is not surprising when one realizes that the discriminator threshold is around 6000 e^- under nominal biasing conditions and the charge deposited by a typical crossing particle is 25 000 e^-.

A further set of data was taken to consider the effect of varying the delay by controlling the bias current I_{dn}. This test was also performed only on plane 2. Remembering the results of the electrical tests one would expect a left-right effect across the chip. In the experiment the strobe delay corresponded to the first level trigger and was around 400 ns. The strobe width was fixed at around 400 ns. Figure 13(a–b) indicates very clearly the effect of varying the current I_{dn}. It can be seen that there exists an optimum value of I_{dn} which allows all of the pixels of one chip to be sensitive. It is interesting to see that the result of I_{dn} = 2.48 V is almost identical to plane 1 in fig. 11 and the result of I_{dn} = 2.6 V is also very similar to plane 3 in fig. 11. This indicates that the values of I_{dn} were not optimized for planes 1 and 3 at the nominal biasing conditions. However, it must be said that this observation is one which only became obvious after off-line analysis.

6. CONCLUSIONS

In a complicated device like this first operational hybrid detector with active signal processing it is essential to provide means for electrical testing. The electrical test results have been correlated with the results from the particle testing in the experiment. Even though the detector worked satisfactorily, a few problems were revealed in this way. In particular, power supply and bias distribution must be implemented carefully. Equally, the ultimate timing accuracy of the circuit is determined by careful line driver design.

This evaluation enables the design of an improved version in the near future. However, the beam test results indicate that even this present version is a very useful detector for the high multiplicity environment. A larger array, still using this first chip, is now under construction in order to study the practical aspects of assembly, yield and reliability.

Acknowledgements

It is a pleasure to acknowledge the effective work of our industrial partners. The encouragement by the project referee P. Sharp is much appreciated. The initial stage of the development of this silicon pixel detector has been a part of the CERN-LAA detector R&D project which is gratefully acknowledged.

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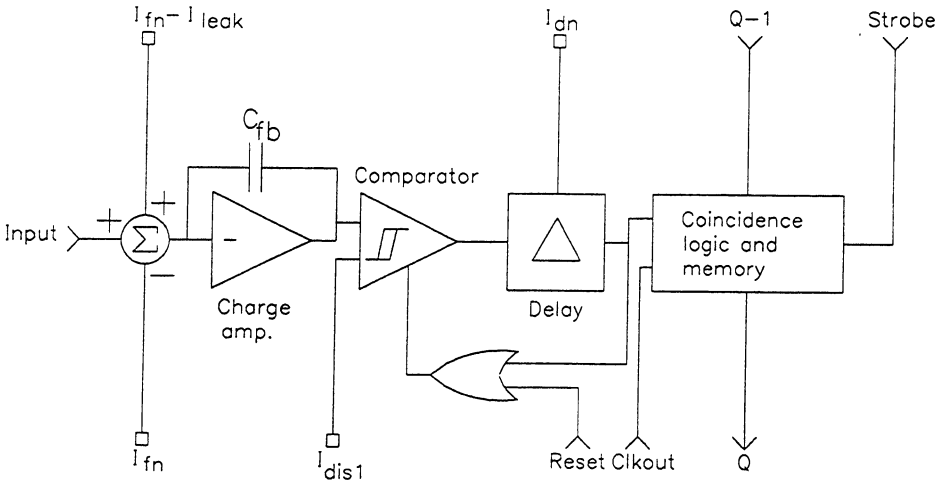

Fig. 1 Block diagram of the pixel readout circuit D Omega-Ion.

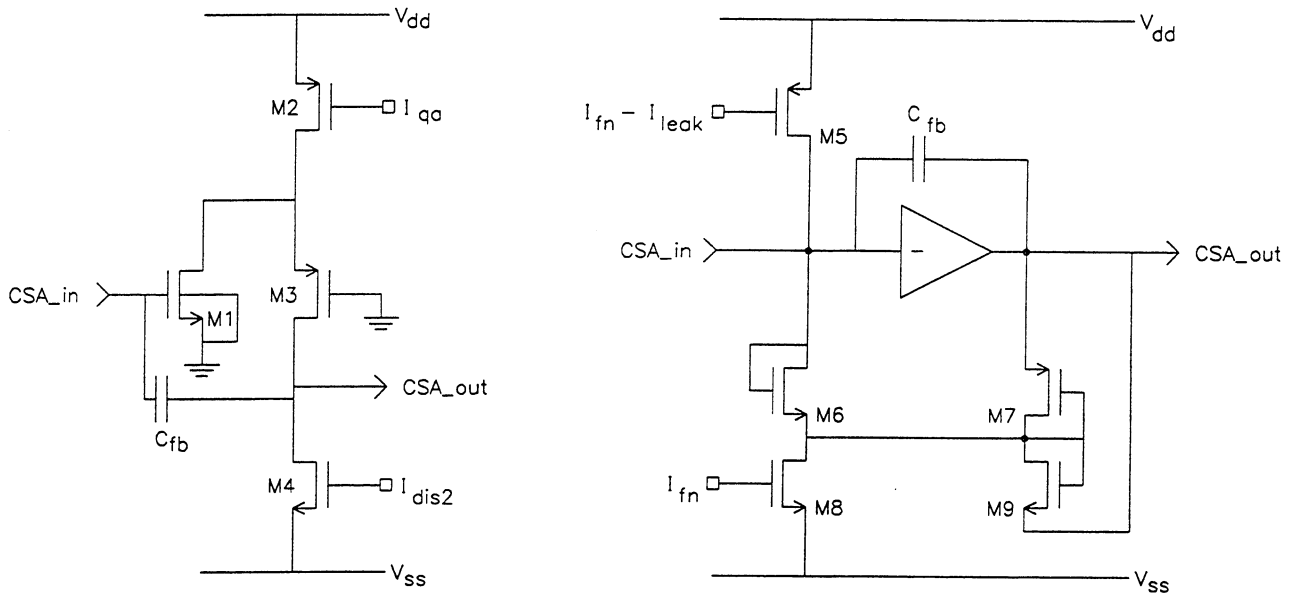

Fig. 2 (a) Partial schematic of the charge sensitive amplifier (CSA).
(b) Overall schematic of the CSA including biasing and leakage current compensation circuits.

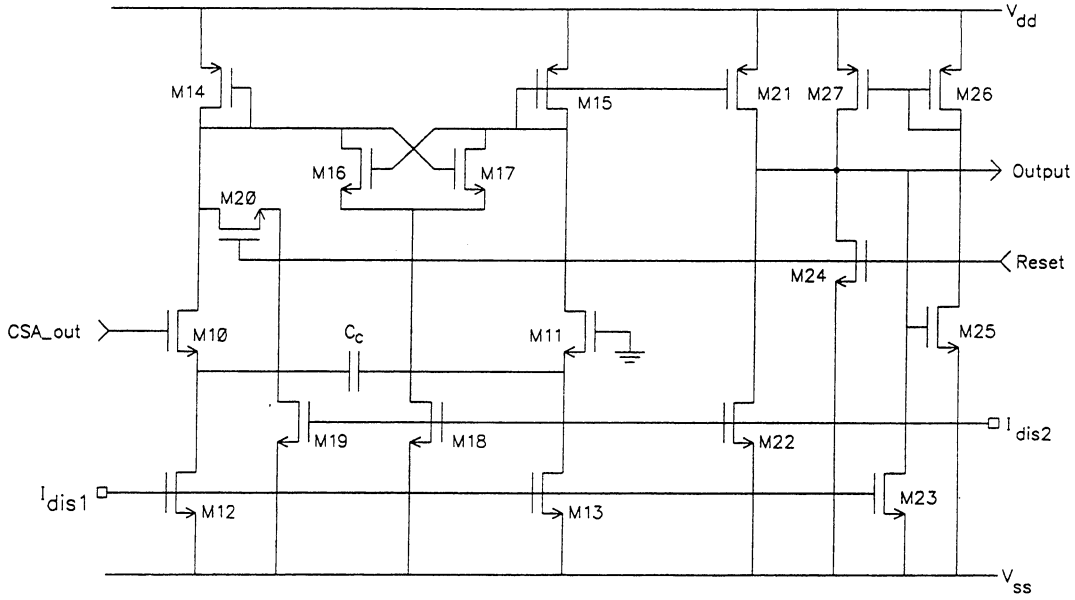

Fig. 3 Schematic diagram of the comparator in the pixel cell. I_{dis1} and I_{dis2} are externally adjustable current sources which control the threshold.

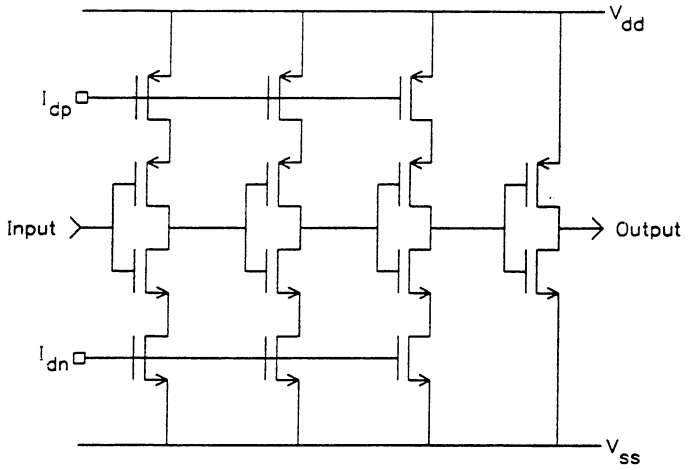

Fig. 4 Schematic of the inverter delay line which is adjustable via the currents I_{dn}, I_{dp}.

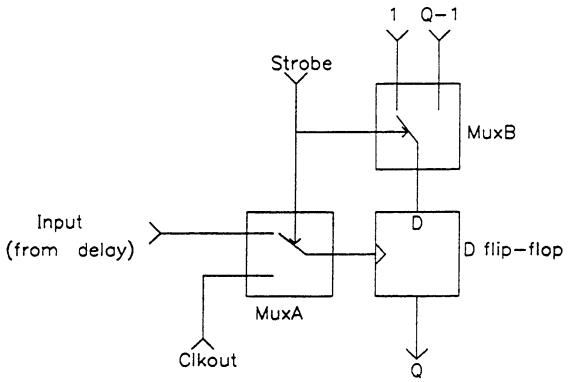

Fig. 5 The coincidence logic and the memory, which becomes part of the output shift register upon readout.

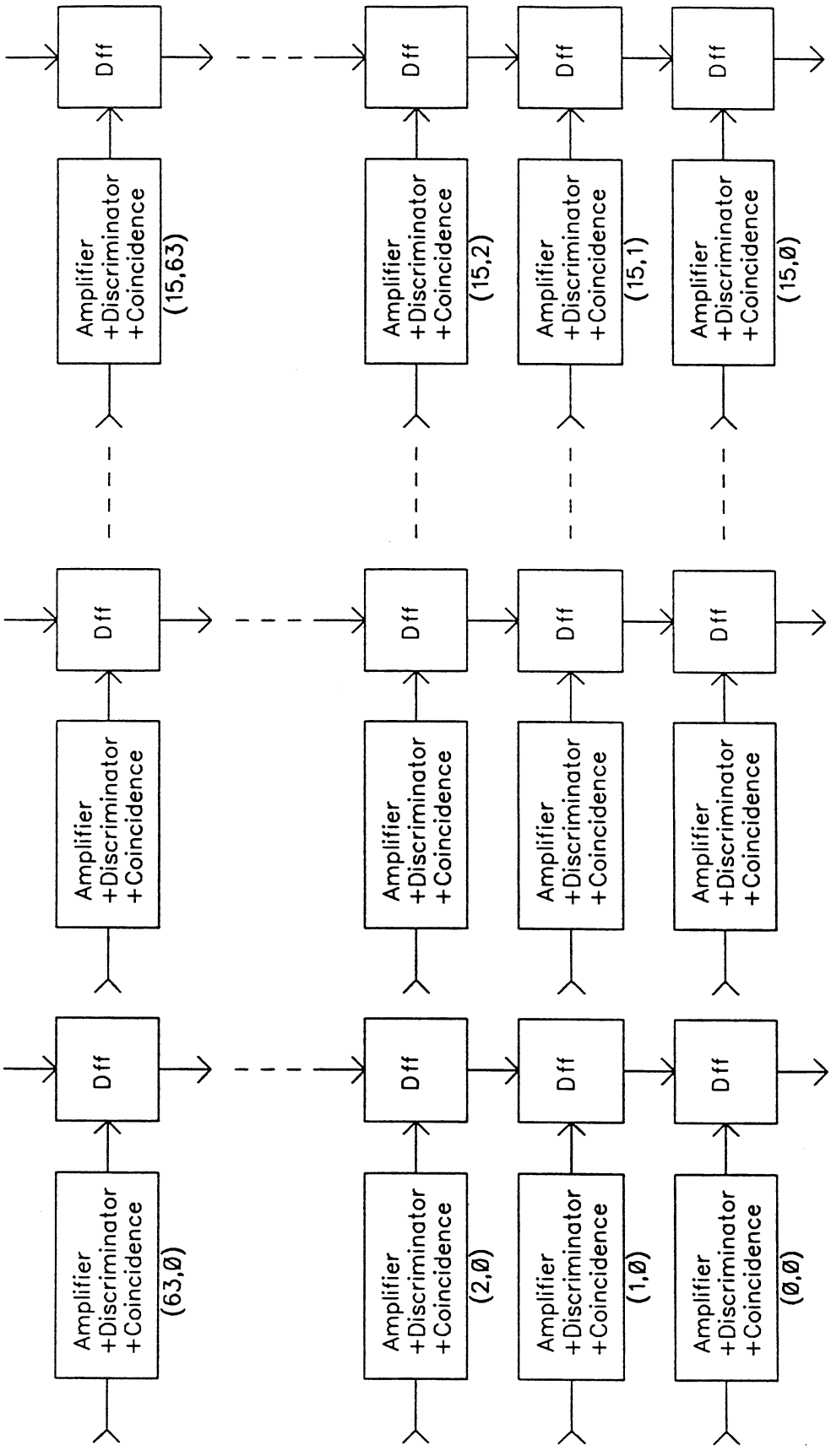

Fig. 6 Block diagram of the readout chip architecture.

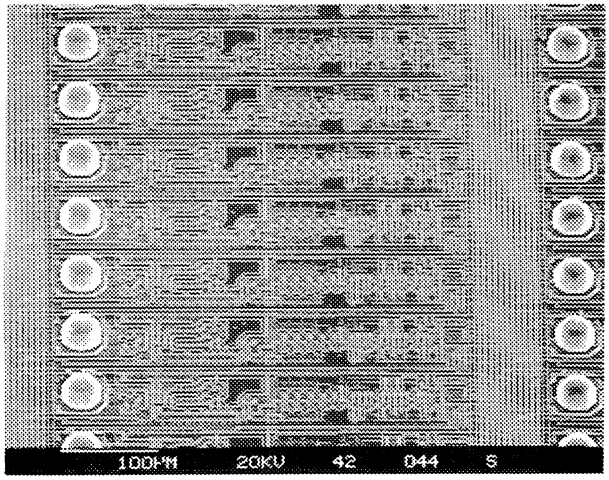

Fig. 7 Scanning electronic microscope (SEM) photograph of a few cells of the readout chip with solder bumps already prepared.

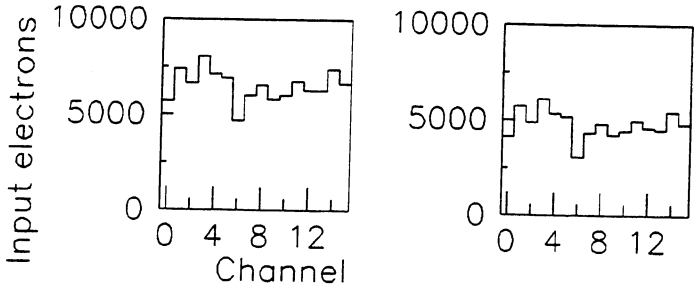

Fig. 8 The distribution of thresholds of the 16 pixels in the electrical test row at two values of the current I_{dis1}, 44 µA (left) and 30 µA (right). The current I_{dis2} was kept constant at 30 µA.

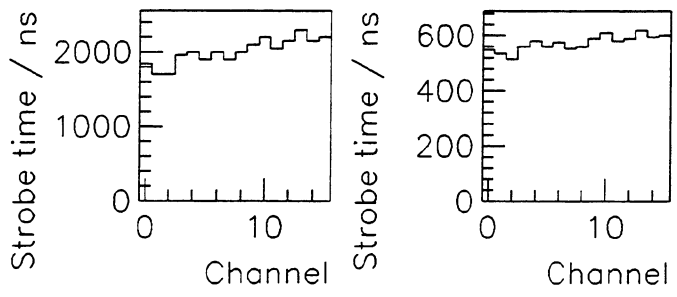

Fig. 9 The distribution of the binary signal delay for the row of test pixels at two settings of the adjustable current I_{dn}.

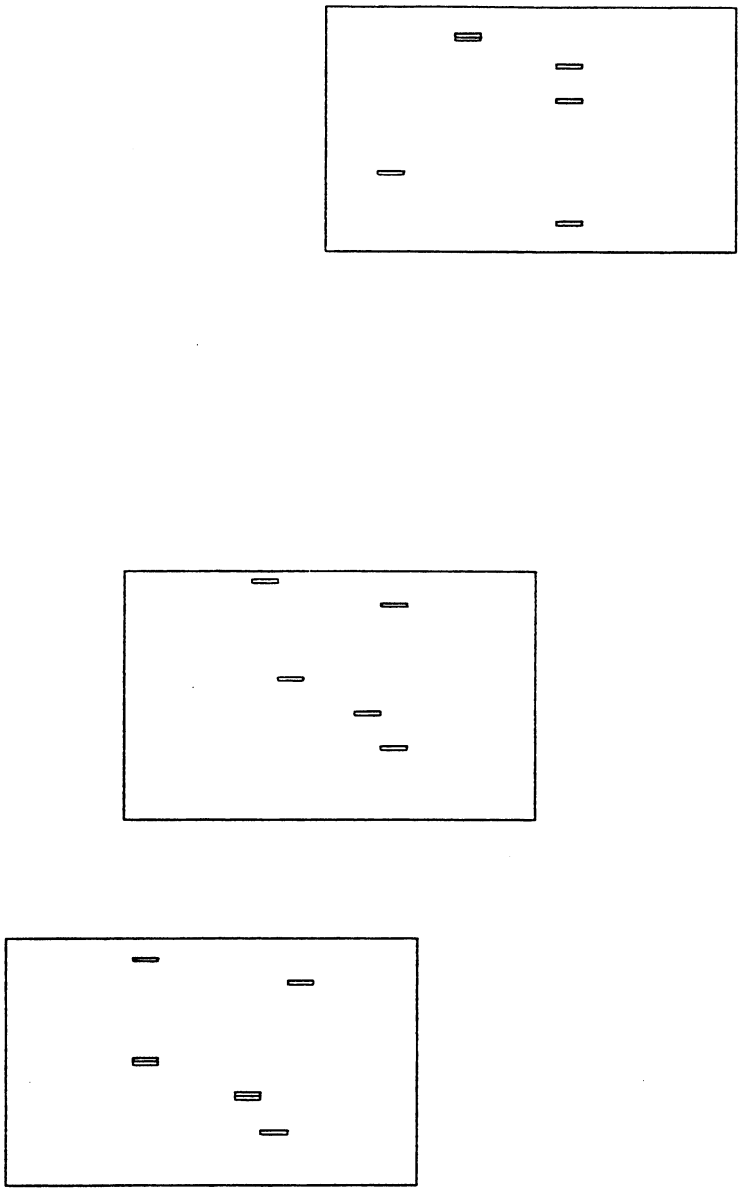

Fig. 10 Reconstruction of a "good" high-multiplicity hit on three pixel planes in the Omega spectrometer.

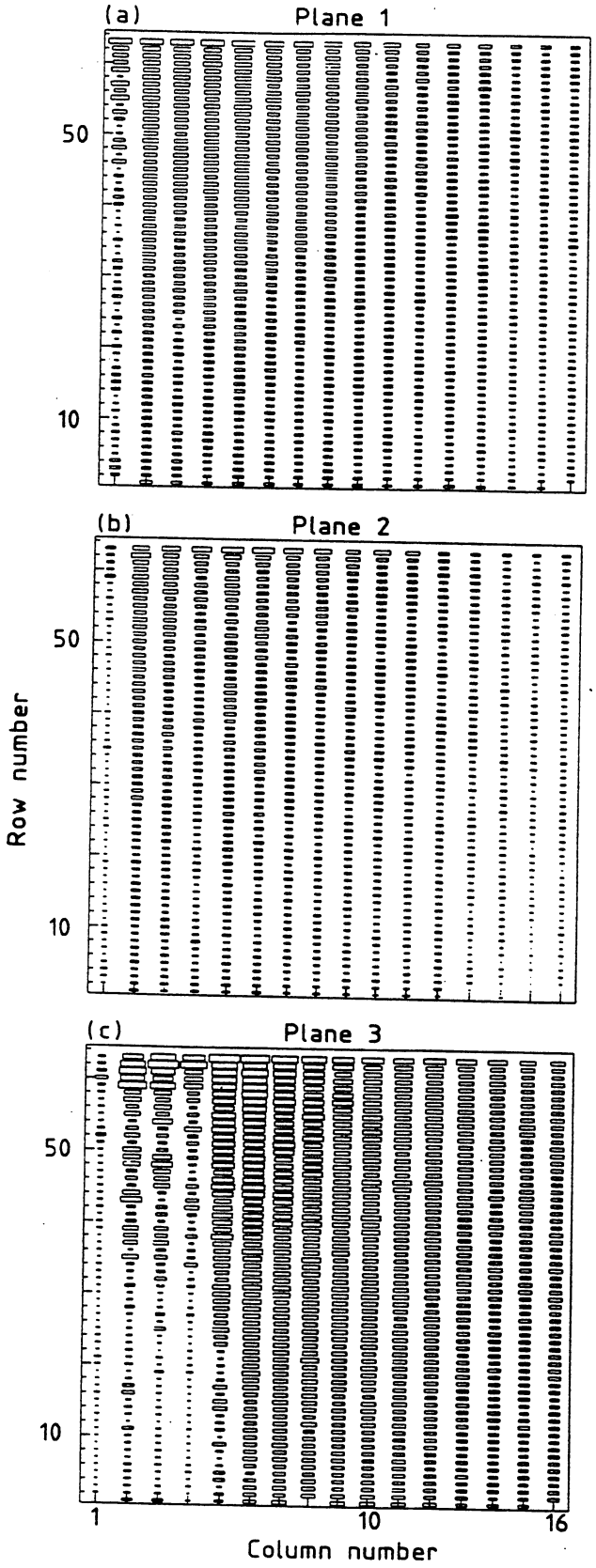

Fig. 11 Diagrams representing the number of hits detected during a run in the Omega experiment for each pixel cell in three successive 63 × 16 cell detectors, planes 1, 2 and 3. The beam passed perpendicular to the detectors, ~ 10 mm above the top left corner.

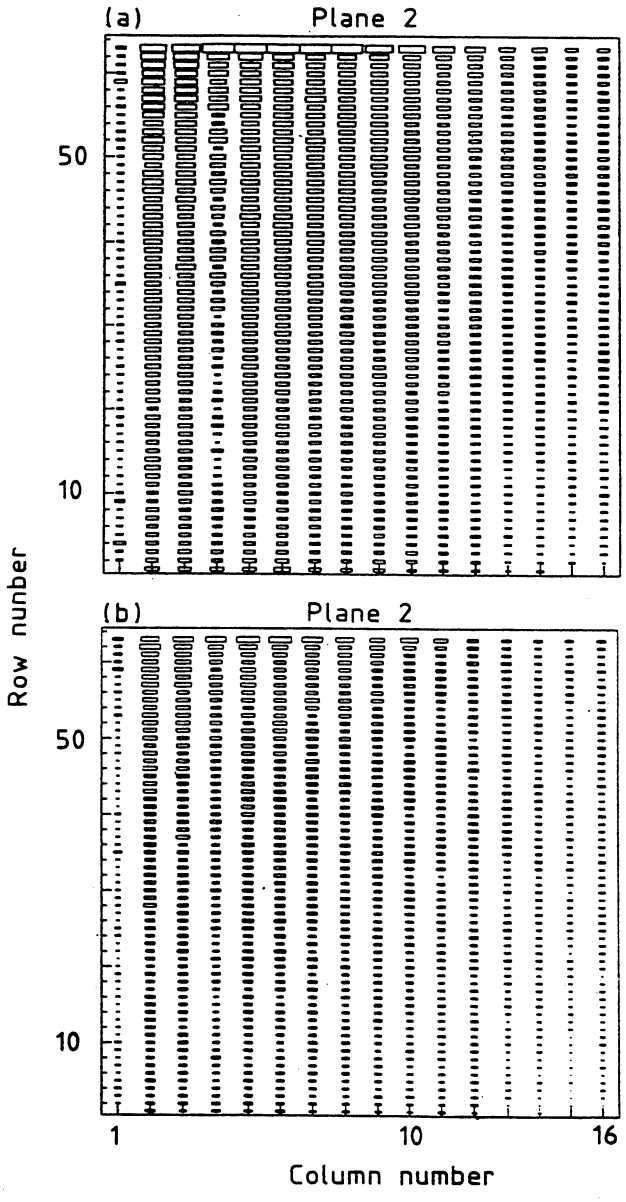

Fig. 12 Same as fig. 11, but only the middle plane 2 is shown for two different settings of the threshold.

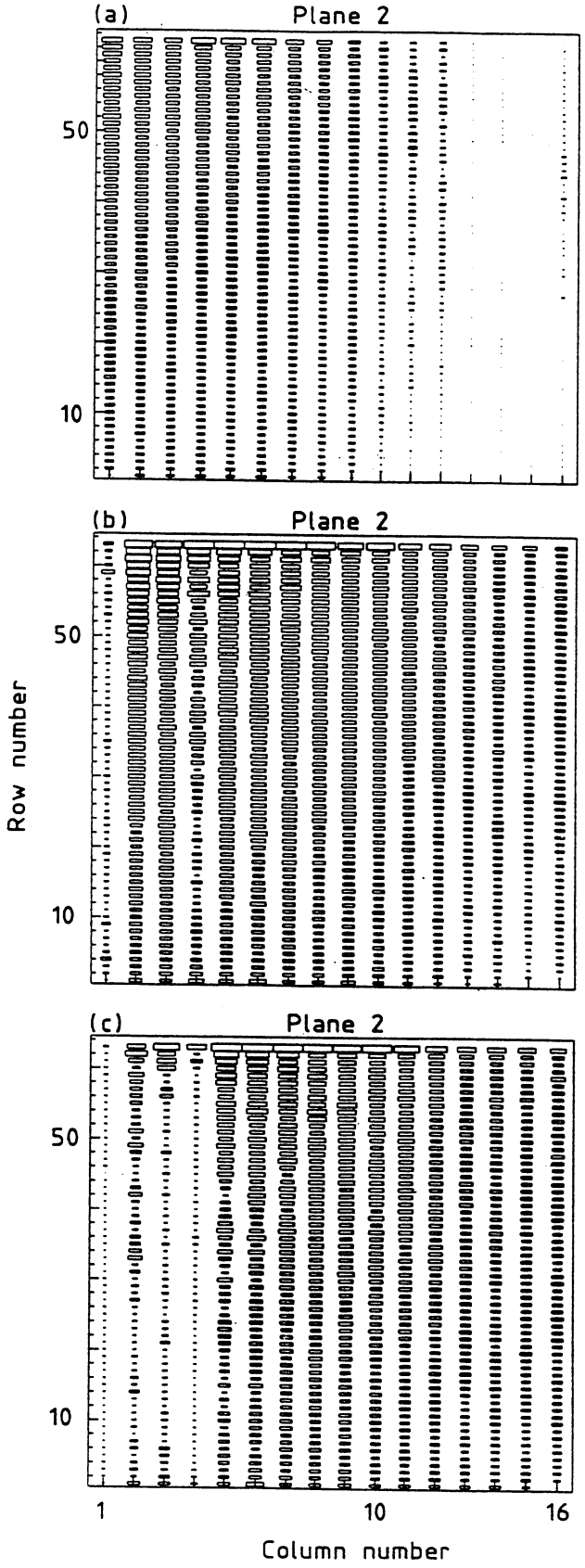

Fig. 13 Same as fig. 11, but only the middle plane 2 is shown for three different settings of the binary delay. The left-right asymmetry is becoming apparent.