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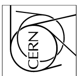

Development of Integreted Electronics for Monolithic pixel detectors for the ALICE-ITS upgrade

Alessandra Lattuca

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Scuola di Dottorato in Scienza ed Alta Tecnologia

Indirizzo di Fisica ed Astrofisica

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Candidate: Alessandra Lattuca

Tutor: Professor Beolè Stefania
Co-Tutor: Dr. Giovanni Mazza

Abstract

This thesis is part of the ongoing studies for the upgrade of the Inner Tracking System (ITS) which is the innermost detector of ALICE (A Large Ion Collider Experiment) at CERN LHC. ALICE is a dedicated heavy-ion detector aiming to study and the characterize the Quark-Gluon Plasma (QGP). It will be undergone to an upgrade program to enable it to reach its physics objectives concerning the dynamics of the QGP after the Long Shutdown 2, foreseen 2018-2019. Indeed, an increase of the LHC instantaneous luminosity up to $\mathcal{L} = 6\times10^{27}\text{cm}^{-2}\text{s}^{-1}$ for the Pb-Pb collisions will bring ALICE to accumulate 10 nb^{-1} for Pb-Pb collisions and to deal with an interaction rate of 50 kHz. In this way, a gain of 100 in statics will be possible in order to have access to rare probes at low and intermediate range of p_T.

The crucial limitations of current ALICE detector concern the overall material budget and a limited read-out rate capability. In particular, to overcome those limitations the ITS will be replaced with a new one with an higer spatial resolution together with an enhanced read-out rate capability. Actually, the ITS is the nearest detector to the interaction points and it deals with a large track densities, thus is essential to have a good impact parameter resolution.

The new ITS will be made up of seven layers of Monolithic Active Pixel Sensors (MAPS). Indeed, the monolithic technology allows to reduce the overall material budget since one of the key feature of MAPS is the integratation in the same silicon die of the sensor and the read-out electronics. The baseline for the pixel chip devolped for upgraded ITS is the ALPIDE pixel chip. It is implemented with the TowerJazz 0.18 um CMOS Imaging Sensor process since it offers a non standard MAPS with the quadruple well option which is essential to implement a full CMOS in-pixel circuitry an have a good resistance at the radiation damages of the ALICE environment. The sensor chip will measure 3 cm by 1.5 cm and contain about 500 000 pixels of about 28 by 28 microns. It consists of a pixel matrix and a chip periphery.

The development of some key circuits located in the chip periphery will be treated in detail in this thesis.

The chip periphery hosts those circuits which are necessary to link the ITS with an external Read-out Unit (RU) placed on a patch panel. These circuits are a Multipoint Low Voltage Differential Signaling (M-LVDS) transceiver and a pseudo-LVDS driver with pre-emphasis. They are respectively a slow speed and a high speed transmission circuit based on the LVDS standard transmission protocol. This standard allows for multipoint or point-to-point communications by ensuring a reduced power consumption and a good signal quality even at high data rate.

The M-LVDS transceiver allows a bidirectional communication between the chips and/or the patch panel. It consists of a pseudo-LVDS driver and a LVDS receiver and it is in charge to broadcast the slow signals as the LHC 40 MHz clock, triggers and configuration settings. Thes driver is a three state buffer which allows a half-duplex bus topology in which only one driver at a time can transmit while every receiver in the line is receiving. Even if the driver works at 40 MHz (80 Mb/s), it has to drive a 6.5 m differential line at which multiple transceivers are connected. For this reason the driver strength of the MLVDS driver has to be high enough to overcome the bandwidth limitations due to the presence of the transmission line and the loads.

The pseudo-LVDS driver is the high speed output circuit which sends out data from the chip periphery. The target speeds which will not limit the read-out of the full pixel chip are 1.2 Gb/s for the IB and 400 Mb/s for the OB. Therefore, these are the speed rates at which the driver has to transmit. Furthermore, it has to drive a full 5m/6.5m transmission line linking the detector with the patch panel. For this reason this high speed output is made up of a main driver and an ancillary pre-emphasis driver. Indeed, in the case in which data have to be broadcast at high speed and for long distances the pre-emphasis technique becomes essential to have a good transmission quality at the end of the lines.

The last circuit that will be analized is a monitoring Analog to Digital Converter (ADC). This device controls some voltage levels inside the chip itself to guarantee the correct chip operation. The resolution foreseen for this device is 11-bit and the architecture takes advantage of the 2 conversion steps principle.

All the circuits listed before are designed in the same 0.18 μm CMOS technology and operate from the same 1.8 V supply. All of them, with the exception of the ADC, will be integrated on the pixel chip prototypes.

This thesis illustrates the design of the data transmission circuits and the development and characterization from simmulations and test results. Furthermore, the prelimary studies on this novel architecture are shown to demonstrate that the operating principle works.

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Introduction

ALICE (A Large Ion Collider Experiment) at the Large Hadron Collider (CERN) is addressing the study and the characterization of the Quark Gluon Plasma (QGP). This is the state of the matter in the early moment of the Universe and in ALICE it is investigated by means of the collisions between ultra-relativistic heavy ions particles. Indeed, the extreme conditions of temperatures with the Pb-Pb collisions allow to study the QGP signatures revealing the QGP formation. A direct observation of the phenomenon is impossible since the QGP lifetime is about 10^{-23} s and it does not exist any trigger able to reveal it. The ALICE expectations in the first run were to observe a QGP at extreme condistions of temperature (T$>$ 170 MeV) as a weak-interacting gas of quarks and gluons. In contrast, ALICE recognized that the QGP is a strong coupled plasma similar to an inviscid liquid, confirming the results provided by CERN SPS and BNL RICH. After the Long Shutdown 2, foreseen in 2018-2019, the experiment has the aim to characterize the dynamic of the condensed phase of the QCD for which high precision measurements and high statistics are nedeed. For this reason the detector will be undergone to an upgrade program which will allow it to deal with the increase of the LHC instantaneous luminosity up to $\mathcal{L} = 6{\times}10^{27}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for the Pb-Pb collisions, thus having access to rare probe for a wide range of transverse momenta.

Until now, the ALICE apparatus has two crucial limitations concerning the overall material budget and the read-out rate capabilities. Actually, the first degrades the impact parameter resolution whilst the latter restricts the detector to use only a small fraction of the Pb-Pb collisions. For this reason, an upgrade of the innermost detector, e.g. the Inner Tracking System (ITS), will fully enhance the features of current system (see Chapter 1) even if it will miss the particle identification functionality.

The new ITS is designed to have a low material budget and high spatial resolution, thus ensuring to efficiently reconstruct the particles tracks together with a faster event read-out. With this purposes, the upgraded system will be equipped with 7 layers of pixel chips developed by using the

Monolithic Active Pixel Sensors (MAPS). It has to be pointed out that, until now, the ALICE experiment is the first one at CERN using this monolithic approach against the hybrid one to solve the two major issues in the accomplishment of its physics goals.

The main chatracteristics of MAPS technology is the integration of the sensor and the read-out electronics on the same silicon wafer. Then, the monolithic approach permits to reduce the overall detector material budget. Furthermore, an enhancement of the impact parameter resolution is obtained thanks to a reduced pixel size since it brings an increase of the detector granularity.

Despite of the great advantages in the use of MAPS technology, the standard MAPS limit the complexity of the in-pixel circuitry and sometimes the sensor collection efficiency is degraded because of the collection mechanism by diffusion (see Section 2.2). For this reason the 0.18 μm CMOS Image Sensor technonology by TowerJazz has been selected as the best solution for the ITS upgrade.

One of the most important features of this technology is the deep p-well option allowing the implementation of a complete CMOS in-pixel circuitry. Furthermore, the MAPS by TowerJazz can be reverse biased and the sensitive volume can be partially depleted. Then, the charge collection will be made by drift, thus reducing the trapping and recombination probability. The feature size of the technology node, the doping level characterics and the reverse bias that can be applied are beneficial in terms of radiation hardness of the devices. Furthermore, the measurements executed on some test structures and presented in [1] shown that the TowerJazz technology is suitable in terms of radiation hardeness at the ALICE radiation environment.

Many different design approach have been developed for the ITS pixel chip besed on MAPS. However, the baseline solution is the ALPIDE pixel chip which has a novel front-end performing the in pixel-discrimination together with a data driven read-out and zero-suppression in the matrix. The final chip will measure 3 by 1.5 cm and contains about 500 000 pixels of about 28 by 28 microns. Then, the upgraded ITS will result in a 12.5 Gpixel camera covering 10 m^2.

The seven ITS layers are divided in two groups. The Inner Barrel (IB), grouping the innermost three layers, and the Outer Barrel (OB), consisting of the outermost four layers. The main difference between them concerns the track density and then the physical disposition of the pixel chips in each layer. The guidelines for the arrangement of the layers in the upgraded ITS has been based on the physics simulations showing that it is necessary to send data out of the chip at the target speed of 1.2 Gb/s (IB) and 400 Mb/s (OB) to efficiently read the pixel matrix (see Section 3.1). Furthermore, a slow

speed communication at the rate of 40 MHz or 80 Mb/s between the patch panel and the ITS is necessary to broadcast the pixel chips configuration settings, the trigger and to distribute the clock to the entire system.

To respond to transmission speed requirements, the APLIDE chip periphery has been equipped with two custom differential interfaces besed on the Low Voltage Differential Signaling (LVDS) transmission protocol (see Section 3.3). Actually, a Multipoint LVDS (M-LVDS) transceiver is in charge to distribute the clock or to receive data at slow speed whilst a pseudo-LVDS driver is the high speed output sending out the data at 1.2/0.4 Gb/s.

The M-LVDS transceiver consists of a custom differential driver and a custom receiver 3.4. It is implemented in ALPIDE for chip-to-chip and Module-to-Module communications. The pixel chip periphery hosts three of those slow speed systems which are in charge for the distribution of the 40 MHz clock, and the broadcasting of the trigger and configuration settings.

A M-LVDS system is made up of multiple transceivers connected on the same line to achieve a bidirectional half-duplex connection topology. This simply means that a M-LVDS transceiver is able to send and receive the data transmitted on the shared bus. Furthermore, this multipoint system works similarly to a "walki-talki" radio. Indeed, only one driver at a time is allowed to broadcast signals along the transmission lines whilst every receiver on the same channel is able to acquire the informations. Only when those driver stops to talk, another enabled driver can start to transmit.

To develop this kind of system, a custom M-LVDS driver has been designed as a three state buffer which will be enabled or disabled to avoid communication contention on the bus. In the same way, even the receiver can be disabled since it is designed with an AND logic that allow to fix the receiver output at a defined logical value. A detailed explantion on the implementation of the M-LVDS system and the related issue is reported in Section 3.4.

To enable the ALPIDE pixel chip to send data up to 1.2 Gb/s, the periphery is equipped with a high speed serial link, named Data Transmission Unit (DTU). This interface is made up of a 600 MHz clock multiplier PLL, a serializer working in Double Data Rate mode and a pseudo-LVDS driver. This link works with a power supply of 1.8 V and it is entirely designed in the TowerJazz 0.18 μm CMOS Image Sensor technology.

The design phases for the implementation and optimization of the high speed driver are presented in Section 3.5. The pseudo-LVDS driver is the unique active device which links the output of the pixel chip with an external FPGA in the patch panel. This high speed output has to send data at 1.2 Gb/s at the distance of 5.3 m and then it turned out to be essential to equip the main driver with an ancillary one for the pre-emphasis technique use.

The design phases were a long way to find a comprimes between the power consumption of those devices and to have a good signal quality at the ends of the long transmission lines.

The slow speed and high speed data transmission systems were fully simulated to verify that they respond to the ITS upgrade requirements. Furthermore, the test measurements on the pseudo-LVDS driver prototypes shown that the pre-emphasis technique helps to enhance the signal quality at the end of the lines and that the entire DTU chain works well in data sending (see Section 4.6.2, 4.6.3).

To complete the features of the ALPIDE pixel chip, a monitoring Analog to Digital Converter (ADC) has to be implemented to check some voltage values which guarantee that the chip is working properly. A preliminary study on a novel ADC architecture is presented in Chapter 5. It will be used to control voltage values not variable with time, therefore the conversion speed will not be an issue as well as the power consumption.

This architecture takes the advantages of two principle, the 2-steps conversion and the successive approximation.
This ADC is implemented using a coarse and a fine Digital to Anlog Converters (DAC) performing a kind of zooming. Actually, the coarse converter define the range in which the monitored voltage lays whilst the fine converter track-down the nearest voltage value that has to be converted.

The principle of operation is based on a double conversion from a voltage value to a current value and, again, this current gives a voltage drop across a resistor(see Section 5.1.1). The first preliminary studies on this ADC show that the principle of operation is working and then the architecture could be optimized in terms of area and power consumption in another design stage to meet the ALPIDE requirements.

Chapter 1

The Upgrade of the ALICE Inner Tracking System

1.1 The ALICE Experiment

ALICE (A Large Ion Collider Experiment) is a dedicated heavy-ion detector at CERN-LHC which has the aim to study the physics of the strongly interacting matter. In particular, this experiment exploits the extreme temperature and energy densities which are created from the Pb-Pb collisions in order to investigate the formation and the characteristics of a new state of matter which is called the Quark-Gluon Plasma (QGP). The ordinary matter is made by quarks and gluons which are confined inside the hadrons by exchanging the colour charge thanks to the strong interaction. However, the QCD theory foresees a phase transition for the hadronic matter if it is undergo to particular energy density and temperature conditions. Generally speaking, the two most important physical quantity which play a role in the QGP formation are the temperaturature T and the baryonic density ρ of a set of hadrons. As shown in the phase transition diagram in Figure1.1, there are two ways to allow a phase transition from the ordinary matter to QGP:

- **Increase the baryonic density in a small volume.** Consider that the baryonic density of the ordinary matter is $\rho_N = 10^{14} g \cdot cm^3$. If $\rho > 5\rho_N$ and $T = 0$, then quarks and gluons are not anymore related to a single nucleon but they are shared between nucleons and free to move in the high density region.

- **Increase the hadrons temperature.** When a set of hadrons has a temperature T well above of a critical value $T_c = 170 MeV$, the quarks kinetic energy is so high to overcome the strong force which confines

them inside a nulceon. In this way, quarks and gluons are free to move in the high temperature volume so allowing the QGP formation.

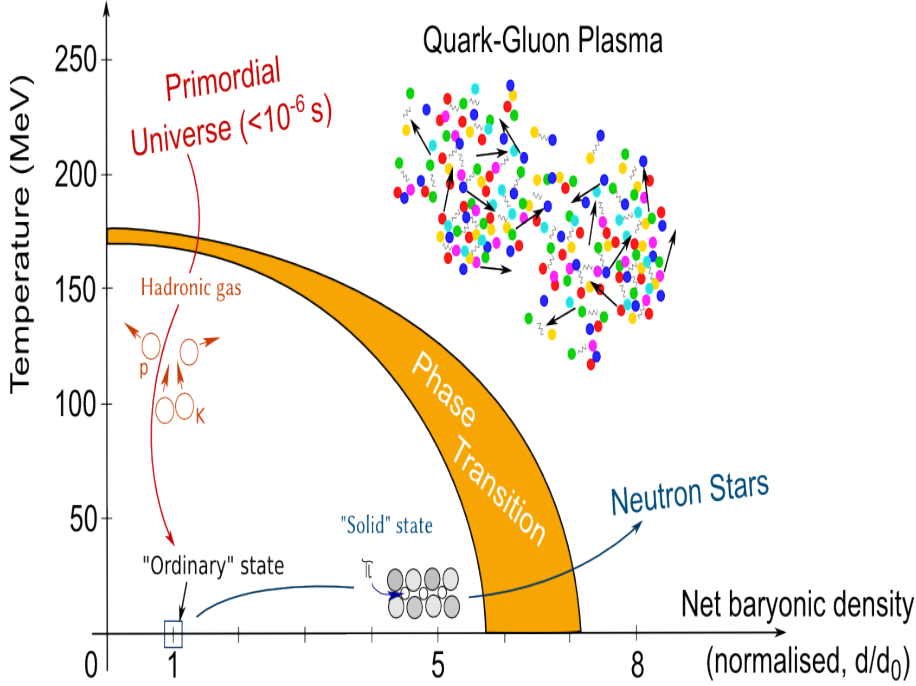


Figure 1.1: Phase Transistion Diagram of the hadronic matter. [3]

The second option is explored in the laboratory [4].
To understand the physics and the characteristic of the QGP helps in the comprehension of two main aspect of the QCD: the origin of the deconfinement and the mass generation mechanism. For this reason, in the general purpose detector ALICE, the Pb-Pb collisions at center-of-mass energy ~ 5.5 TeV per nucleon will allow an inclusive study of hadrons, electrons, muons and photons which are produced during the interactions. For the ALICE goals, collisions for lower mass ions and proton-nucleon interactions are also foreseen, since they allow to expand the energy density and the interactions volume ranges.
Moreover, data taking during proton-proton runs will provide reference data for the heavy-ion program and measurements on specific strong-interactions topics which complete the Standard Model theory [5].

Since the QGP lifetime is about $10^{-23}s$, free quarks and gluons are never detected. For this reason the ALICE experiment is focused on the study of some observables which reveal the QGP signatures, i.e. specific signals of the QGP formation [2].

Actually, the measure of the multiplicity and the transverse energy flow are related to the global event features and primarly reveal the geometry of the interactions. Prompt photons, high p_T hadrons and the J/Ψ suppression indicate whether there was a plasma formation. Strangeness production, multiplicity fluctuations and particle interferometry, particle ratios, transverse momentum distribution define the characteristics of the system in proximity of the phase transition [2].

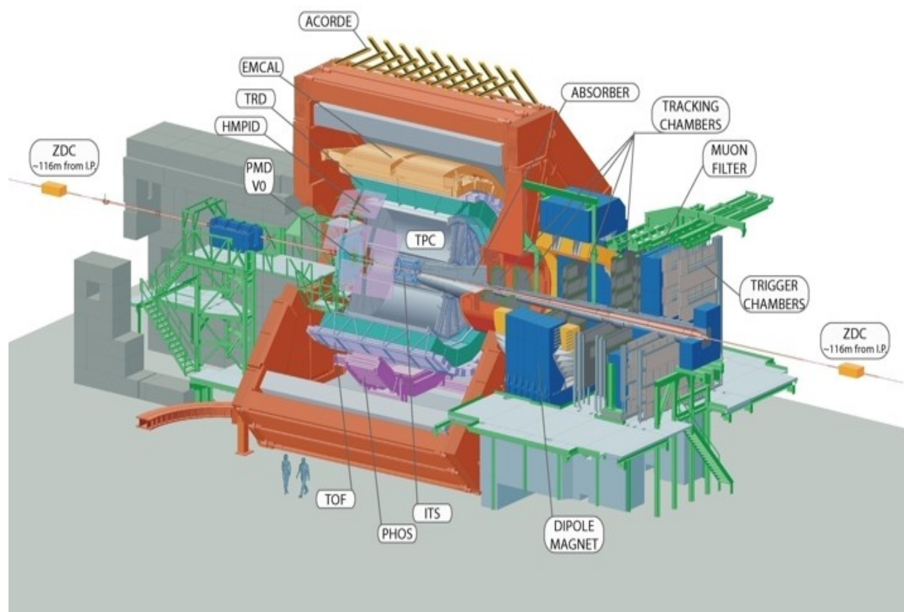


Figure 1.2: The ALICE general purpose detector [7].

The main part of the ALICE detector consist of a central barrel and a forward muon spectrometer, as shown in Figure1.2. The central barrel covers polar angle from 45° to 135°, i.e. $|\eta| \leq 0.9$, and it is made by detectors which perform particle tracking and particle identification.
Starting from the innermost part, there is a six-layer silicon vertex detector Inner Tracking System (ITS), a cylindrical Time Projection Chamber (TPC) which acts as the main tracking detector, a Transition Radiation Detector (TRD) which is used to identify electrons with momentum <1 GeV/c and a three particle identification arrays of Time-of-Flight (TOF). A High-Momentum Particle Identification Detector (HMPID) is adopetd for the recognition of hadrons with high momentum by covering an acceptance range from 1.2° to 58.8° ($|\eta| \leq 0.6$). Finally, two calorimeters, PHOS and

EMCAL($|\eta| \leq 0.12$ and $|\eta| \leq 0.7$, respectively) give more insight on some hard QCD processes, jets productions and fragmentation function [5]. The central part is sourrounded by a solenoidal magnet which was designed for the experiment L3 at LEP and which generates a magnetic field of ∼0.5T.
Moving toward large rapidity range, there is the forward muon spectrometer which detects the muons generated by the fragmentations of the particles produced in the collision. The muon detector consists of several absorbers, a large dipole magnet and fourteen planes of tracking and triggering chambers. It is located outside of the L3 magnet and it covers the acceptance range $-4 \leq \eta \leq -2.5$.
The main ALICE apparatus is equipped with several small detectors (ZDC, PMD, FMD, T0, V0, ACORDE) which enlarge the rapidity range to high value and which provide both, the characterization of global event and triggers [5].

The detectors types and the layout described above are set for the ALICE experiment to meet the physics requirements and the experimental conditions foreseen for the collisions. In particular, of primary importance is the very high multiplicity expected after a nucleus-nucleus collision. For this reason the system is optimized and tested to deal with values of about 8000 charged particles per unit of rapidity, at mid-rapidity [6] and tracking is perfomed by using a three-dimensional hit information with 150 point in the L3 magnet. A very low material thickness and a large tracking lever arm of up to 3.5 m are essential to guarantee measurents of a wide momentum range, from values <100 MeV/c up to 100 GeV/c. Finally, since ALICE will concentrate in mid-rapidity region, the central barrel detectors cover two units in rapidity around mid-rapidity whereas the muon measurements covers 1.5 units in rapidity at small angles. In this way it is possible to study some variables event-by-event and to have a good reconstruction even for particles with very low p_T.

1.2 The ALICE Upgrade

Despite of the theoretical expectations which described the QGP at high temperature like a weak-interacting gas of quarks and gluons with a realatively long mean free path, heavy-ion experiments shown that the state of the matter generated from the collisions is a strongly-coupled plasma with a very short mean free path more similar to a perfect liquid than a gas. Until now, the ALICE detector has shown that the Quark Gluon Plasma is an almost inviscid liquid by means of the measurents on the radial and elliptic flow

for identified hadrons at values of the transverse momentum $p_T \leq 3\text{GeV}/c$, confirming the results provided by CERN SPS and BNL RICH [8]. Although these results are very important for the characterization of the QGP, high statistics and high precision measurements are needed to understand the dynamics of the condensed phase of the QCD. In view of this aim, having access to rare probe at low and intermediate p_T will be essential. For this reason the ALICE detector has to be upgraded in order to deal with an increase of the LHC instantaneous luminosity of the Pb-Pb collisions at the value of $L = 6 \times 10^{27} cm^{-2} s^{-1}$. In this way, the general purpose detector will be enabled to accomulate 10 nb^{-1} of Pb-Pb collisions after the Long Shutdown 2 (LS2) in the years 2018-2019, dealing with an interaction rate of 100 kHz. After this upgrade a gain factor of 100 in statistics for minum bias trigger over the current program will be reached. Furthermore, an improvement of the vertexing and tracking capabilities is needed. Therefore, the ALICE upgrade consists in([8], [10]):

- A new beam pipe with smaller diameter;
- A new, high resolution, low material budget ITS. The new ITS will produce an enhancement of a factor 3 in the resolution of the distance of closest approach (dca) together with an improvement on the standalone tracking capabilties;
- The TPC upgrade with the replacement of the read-out multi-wire chamber with the Gas Electron Multiplier detectors and a new pipelined read-out electronics, thus allowing a continuous read-out of the system;
- The upgrade of the read-out electronics of TRD, TOF, PHOS, and Muon Spectrometer;
- The upgrade of the forward detector and the trigger system for an high rate operation;
- An online data reduction.

1.3 Physics Motivations for the ITS Upgrade

The increase of the LHC luminosity allows high statistics measurements that will give acces to rare probes channels necessary to better characterize the QGP dynamics. Indeed, the integrated luminosity of 10 nb^{-1} represents an increase of a factor 10 in statistics for the data sample collected with the rare physics channels and 100 for the minimum-bias data. This last aspect will

be important mainly for low p_T heavy-flavour and charmonium production and for low-mass dilepton production. After the LS2 the physics program of the ITS will be focused on the heavy-flavour measurements and for this reason it is necessary to enhance the tracking performance and the read-out rate capabilities of the innermost detector. Furthermore, a reduction of the material thickness will contribute on a detailed measurment of low mass dielectrons [10]. There is a special interest in heavy quarks since they are a mark for their interaction with the QGP. Indeed, heavy quarks preserve their mass, flavour and colour charge during the interaction with the medium so giving some insights in the hydrodynamics of the medium itself. Since they can be thought as Brownian particles, from the study of the kinematical distributions it is possible to reconstruct the interaction history [10].
Actually, some aspects about the intraction between heavy-flavour and QGP medium have to be studied([9, 10]):

- *Thermalization and hadronisation of heavy quarks in the medium.*
  This topic will be investigated by means of specific studies on heavy flavour charmed and beauty baryons which includes the azimuthal anisotropy coefficient v_2 for mesons and baryons, the barion/meson ratios Λ_c/D and Λ_b/B and the the strange/non-strange ratio for charm (D_s/D), nevertheless the possibility to create charm quarks in-medium via thermal production. The measurements that will benefit of the ITS upgrade are:
  - the Elliptic flow of charmed and beauty mesons and baryons down to transverse momenta less than 1 Gev/c;
  - D mesons, including D_s down to zero p_T;
  - Charmed baryon Λ_c via the decay channel $\Lambda^+{}_c \rightarrow pK^-\pi^+$ and, for the first time, beauty baryon Λ_b via the decay channel $\Lambda_b \rightarrow \Lambda_c + X$;
  - Baryon/meson ratio Λ_c/D down to 2 Gev/c
- *Energy loss in-medium of the heavy quark and its mass dependence.*
  This study will be addressed via the nuclear modification factor R_{AA} for a wide range of transverse momentum for D and B mesons. In this case the ITS upgrade will have a very important impact in the Pb-Pb run for the measurements of:
  - Charm for a very wide range of p_T down to zero;
  - Beauty via displaced $J/\psi \rightarrow ee$ and $D^0 \rightarrow K\pi$;
  - Displaced electrons;

– Beauty decay vertex reconstruction using the decay channels plus an additional track.

- *Thermal radiation from the QGP.*
- *In-medium modifications of hadronic spectral functions related to chiral symmetry restoration, in particular for the ρ meson in its e^+e^- decay mode.*

Finally, the improved ITS tracking resolution will have a beneficial effect also in the hypernuclear states measurements like ${}_{\Lambda}{}^{3}\mathrm{H} \rightarrow {}^{3}\mathrm{He} + \pi^-$.

1.4 The Current Inner Tracking System

The commitment of the ITS is to deal with a large track densities in proximity of the interaction points. Actually, the ITS surrounds the $800\mu m$ thick berillium beam pipe and it is the innermost ALICE detector encountered by the produced particle. The basic function of the ITS are [5]:

- localize the primary vertex of interaction with a resolution better than $100\mu m$;
- reconstruct the secondary vertices from the the decays of hyperons and D and B mesons;
- track and identify particles with momentum below 200 MeV/c;
- improve the momentum and angle resolution for particles reconstructed by the TPC;
- reconstruct particles traversing dead regions of the TPC.

As shown in 1.3, the inner tracker consist of six cindrical coaxial layers equipped with three different kinds of silicon detectors. The position of the layers and the pseudorapidity-range coverage ($|\eta| \leq 1.98$ for the first layer and $|\eta| \leq 0.9$ for the five remaning) were determined so that the ITS can produce informations which are complementary to those about the tracks and the charged particle multiplicity produced by the TPC and the Forward Muon Detector respectively [5].
The overall detector design was made to guarantee an efficient track finding and a high impact parameter resolution. In particular, silicon detector technologies were chosen since they show an exceptional spatial resolution together with a high granularity. The particle densities expected from the

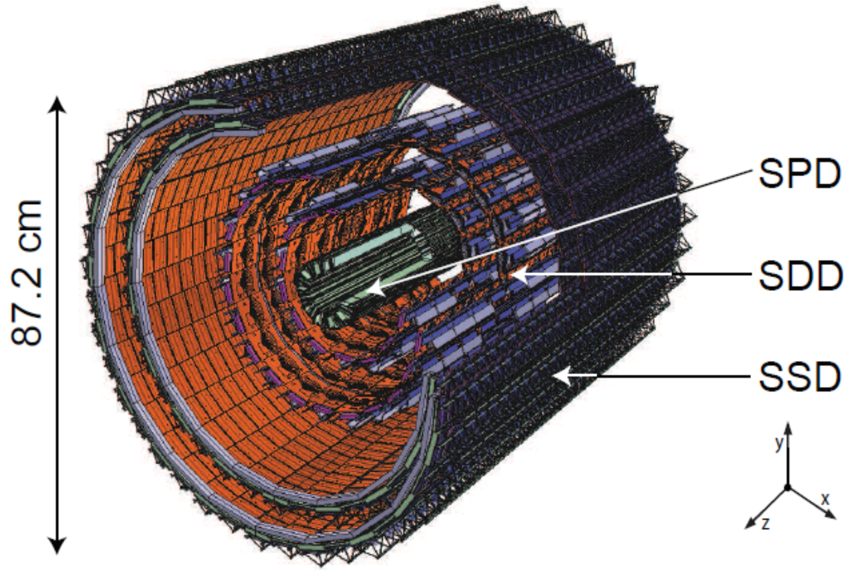


Figure 1.3: Layout and reference system of the current ITS.[11].

Pb-Pb collisions have been determined the sensor technologies with which the detector is assembled. In order to guarantee a suitable accuracy in the localization of interactions vertex, the two innermost layers of the ITS are equipped with Silicon Pixel Detectors (SPD), the two intermediate layers with Silicon Drift Detectors (SDD) and the two outermost layers with Silicon Strip Detectors (SSD). Since, the four innermost layers have to deal with a very high number of tracks, non-projective truly two-dimensional devices are fundamental in order to minimize the number of cells that has to be read-out for the track reconstruction with a good two tracks resolution. Conversely, the double sided micro-strip detector are a suitable option for the two ITS outermost layers where the track density is as low as 1 cm^{-2}. Furthermore, the two layers of SDD and the two with the SSD have a charge measurement read-out in order to perform the particle identification via *the linear stopping power* dE/dx in the non-relativistc region. In this way the ITS has a stand-alone capability as a low p_T particle spectrometer. The table 1.1 summarize the main parameters of the current ITS.

In the following the design considerations for the ITS silicon detectors are presented.

Table 1.1: Layout of thecurrent ITS [5]

Parameter	SPD		SDD		SSD	
Layer	1	2	3	4	5	6
Radius (mm)	39	76	140	240	400	450
Length (mm)	282		444	594	862	978
Cell Size (μm^2)	50×425		202×294		95×40000	
Active area (mm^2)	12.8×69.6		72.5×75.3		73×40	

1.4.1 Silicon Pixel Detectors

The firts two layers of the ITS are foundamental for the determination of the position of the primary vertex and for the measurement of the impact parameter of secondary tracks from the weak decays of strange, charm and beauty particles. Since the environment of the SPD sees a track densisty as high as 50 tracks/cm^2 as well as a radiation level of 200 krad in 10 years of operation, the SPDs were chosen since they are very precise in the tracks reconstruction and they allow a high granularity pixel detector with a high radiation tolerance. A high detector segmentation involves a high signal-to-noise ratio at high speed thanks to a low diode capacitance.
These two SPD layers play a key role for the ALICE trigger levels, L2 and final respectively. L2 is based on the event centrality and it triggers the ALICE read-out at 40 Hz. In this case, the signals of the SPD are combined with the ones generated by the SDD and SSD as well as the ones coming from the TPC for the global tracking. The second level trigger final works at 1 kHz and it triggers the read-out of the SPD and on the muon arm to obtain information about the primary vertex of interaction.

The current ITS is equipped with the silicon hybrid pixel detector for which the sensor and the related front-end electronics are segmented on two different silicon wafers. These two wafers are then aligned and bump bonded via solder balls.
The technology node used for the design of the pixel read-out chip is the IBM 0.25 μm CMOS process for which the enclosed layout technique was adopted in order to enhance the radiation tolerance of the ASIC. The front-end chip contains both analog and digital electronics for the read-out of the 8192 detector cells. Each read-out circuit consists of a pre-amplifier, with leackage current compensation, followed by a discriminator with an individual threshold fine tuning. The read-out of the cell is binary where each cell sends a logic 1 or a logic 0 if the stored signal exceeds or not a given threshold. A logic 1 is propagated through a delay line for 6 μs before the arrival of a trigger signal. A 4-hit deep front-end buffer on each cell performs

the derandomization of the arrival time [5].
The basic building block of the two layers of SPD is a ladder which consist of a 256×256 cells detector matrix flip-chip bonded with 8 front-end chips. As reported in the Table1.1, the cell size is 50×425 μm^2 for a overall thickness of 250 μm. Four ladders in a line form a 33 cm long stave and they are glued and wire bonded to a bus which contains the signals and power lines. For each stave there are two pilot chips located at the two ends of the stave bus in order to perform the read-out, the control functions and transmit the binary data from the pixel cells to a remote router via a serial copper link [6].

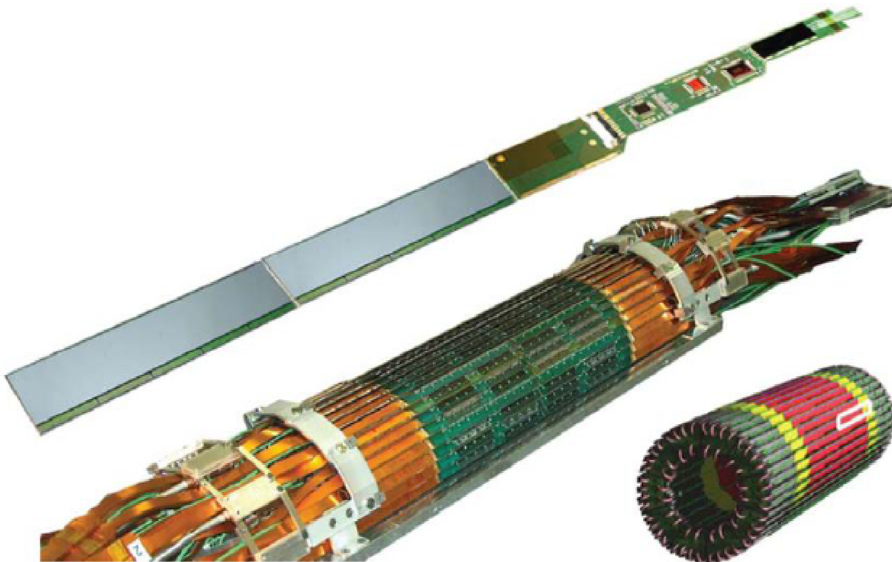


Figure 1.4: Stave assembly of the SPD layers.

1.4.2 Silicon Drift Detectors

The charged particle density for the two ITS intermediate layers is as high as 7 cm^{-2} and for this reason they are equipped with Silicon Drift Detectors (SDD) which have a good multi-track resolution. Actually, they are truly two dimensional devices like the SPD. Nevertheless, those two layers have a charge measurement read-out since they are used for particle identification via dE/dx together with the two Silicon Strip Detectors in the two ITS outermost layers. Despite of the limited speed, those technology is suitable for the layer 3 and 4 of the ITS since they see an high particle multiplicity with a low event rate. Layer 3 is covered by 14 structures called ladders

which contains 6 detectors whilst layer 4 is equipped with 22 ladders, each provided with 8 detectors.

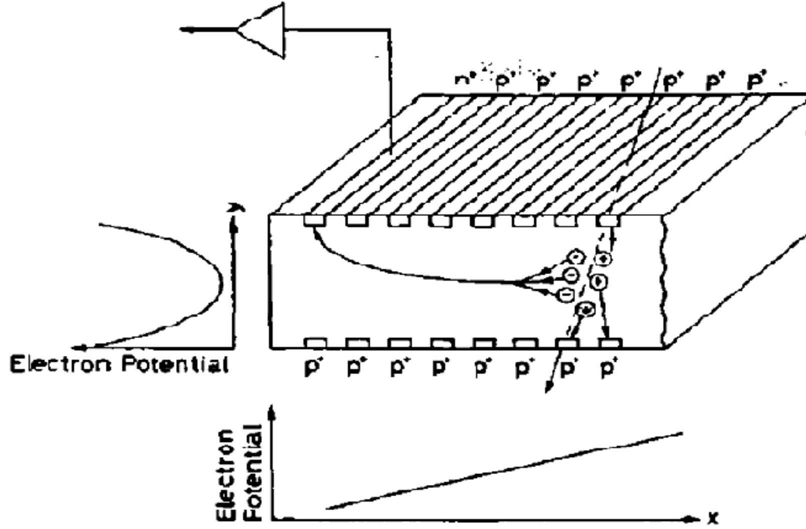


Figure 1.5: Cross section of a typical silicon drift detectors with the elctical field and potential generated [6].

The SDDs were produced by using a high resistivity 300 μm thick Neutron Trasmutation Doped (NTD) n-type silicon wafer. As shown schematically in Figure1.5, the wafer is segmented on both surfaces with 291 parallel p^+ cathode strips which fully deplete the detector volume and generate a drift field parallel to the wafer surface. The distance between two strips is 120 μm and, in total, the SDDs cover a sensitive area of 7.25×7.53 cm^2. A central cathode strip is held in the range (-1.65 ÷ -2.4) kV high voltage bias and dividse the drift region in two parts. To date, the operating voltage is - 1.8 kV. A traversing charged particle produces in the sensor electron-hole pairs which will be separated from the sensor electrical field. In particular, holes will be collected by the p^+ implants whereas the electrons will be canalised in the middle plane of the detector and pushed towards one of the edges of the detector in order to be collected by 512 collection n^+ anodes, 256 for each drift region, which are separated by a -2.4 kV bias voltage. The size of the sensitive element of 294 × 202 μm^2 is set by the drift velocity and the sampling frequency of the front-end electronics. Actually, at a -2.4 kV bias voltage corresponds a drift velocity of 8.1 $\mu m/ns$ whereas the front-end samples the signal at 40.08 MHz. Since the drift velocity v_{drift} depends on the temperature like $v_{drift} \propto T^{-2.4}$, 33 MOS charge injectors are used to

monitor it. A small 50 fF capacitance of each anode allows for a low noise and a good energy resolution [6]. The obtained spatial resolution is 35 μm along the rϕ direction for the whole detector and 25 μm in the z (along the anode) direction. Furthermore, the detection efficiency is abut 99.5% for signals which are at least 10 times the electronic noise [5].

The three ASICs PASCAL, AMBRA and CARLOS are devoted to readout the SDDs. In particular, PASCAL carries the signals preamplification, the analog storage with a 40 MHz sampling frequency during the carriers drift and the analog-to-digital conversion. AMBRA, a digital 4 event buffer, receives data from PASCAL and performs data derandomization, baseline equalization on an anode-by-anode basis and data compression. AMBRA sends data to CARLOS which implements a zero suppression logic and data compression. The three ASICs are developed by using a 0.25 μm CMOS process and a radiation tolerant technique was used for the layout [6].

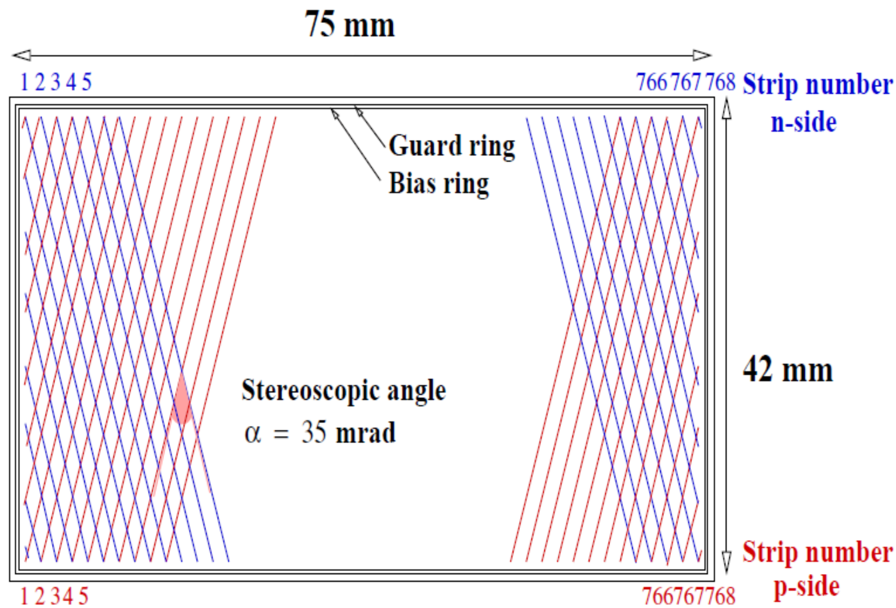


Figure 1.6: View of the SSD detector in which the stereo angle of 35 mrad is show [6].

1.4.3 Silicon Strip Detectors

In the two outermost layers, where the particle density is so low as 1 cm^{-2}, the Silicon Strip Detector (SSD) technology was chosen. Together with the two ITS intermediate layers, these two layers carry the particle identification for low-momentum particle and they are crucial for the tracks reconstruction

of the ITS and TPC.
For the ALICE purpose, the double sided SSD were preferred with a stereo angle of 35 mrad in order to minimize the "ghost hits effect" without loose in the stereo view (see Figure1.6).

One SSD and its associated front-end electronics equips a detector module by covering a sensitive area of 75×22 mm^2. Actually, 768 strips with a pitch of 95 μm cover each side of a 300 μm thick silicon sensor.
The read-out electronics for the strips consists of the front-end chip, the end-cap electronics and the front-end read-out modules. A front-end chip with 128 preamplifier-shaper circuits followed by a sample and hold circuit was designed for each detector. This chip was optimized to reduce power consumption and it allows a sequential read-out of the analog signals which are controlled by an external trigger [5].

1.5 Limitations of the current ITS

As shown before, the aim of the ALICE experiment is the characterization of the QGP by making precision measurements of rare probes over a large transverse momentum range. The way to do this is ideally a Rutherford scattering experiments where the probes, i.e. quarks, have the same dimensions of the plasma constituents and one can study the properties of the medium by studing the properties of the emerging particles. Unfortunately, the QGP exists only for 10^{-23}s, so it is really impossible to synchronize an external probe for this brief period of time and no free colour charges exist to be used as probes. What can be done is to use probes which are directly produced during heavy-ion collision events, in an initial purpose scattering, before the plasma formation, the production rate of which is well known. At this point the goal is to analyze the probe interactions with the QGP. The probes which respond to these requirements are heavy flavour hadrons which contain charm and beauty quarks, as said before, but it is really difficult to deal with them because it is not possible to trigger the events and the reconstruction efficiency is low. In these respects the current ITS is not adequate to carry out the physics programs of ALICE because of the major limitations which concern the limited read-out rate capabilities and the inability to measure charm baryons [8].

The ITS, as it is now, has a flaw in the read-out rate capabilities for which it uses only a small fraction of the full 8 kHz Pb-Pb collision rate. Actually, it runs at a maximum rate of 1 kHz irrespective of detector occupancy. For this reason the ITS is more lacking in view of the LHC upgrade, after which the interaction rate of the Pb-Pb ions will be pushed up to 50 kHz, since the

current apparatus will be insufficient to cope with all interactions.
Concerning the charm baryons produced in the central Pb-Pb collisions, at the moment ALICE is not able to mesure them because of the poor impact parameter resolution. Figure 1.7 shows the resolution obtained experimentally with the current detector as a function of the transverse momentum. A resolution better than 65 μm is obtained only for p_T greater than 1 Gev/c, so it will be impossible to detect the most abundantly produced charm baryon Λ_c which has a decay length of 60 μm [12].

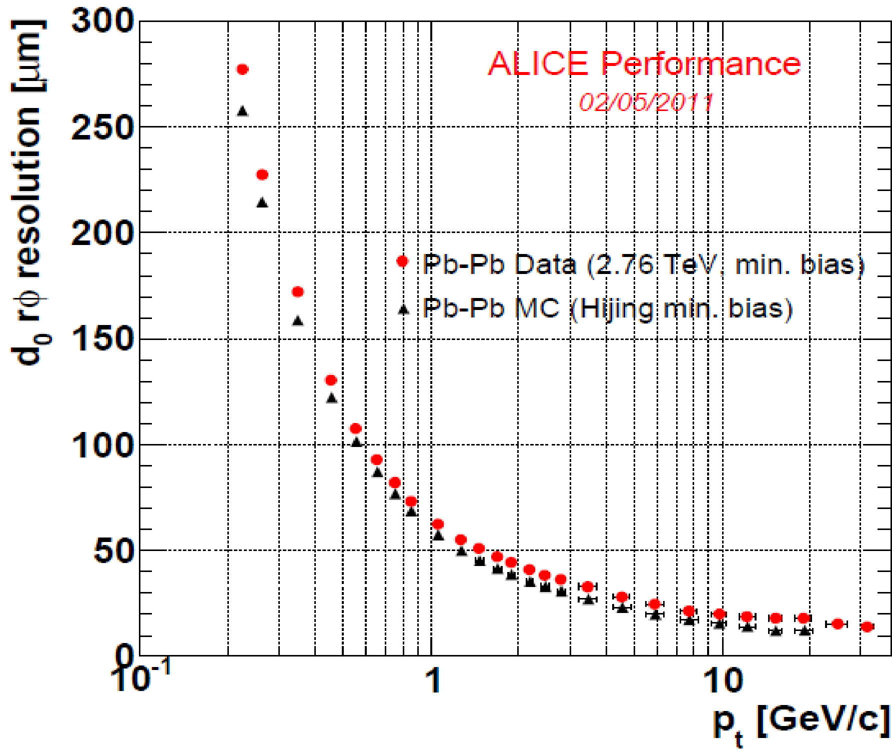


Figure 1.7: Impact parameter resolution in the transverse plane vs p_T. The panel shows that there is an agreement within 10% between the red curve and the black one, obtained experimentally and from the Monte Carlo simulations respectively [12].

Moreover, the good quality of data is limited by the detector inaccessibility for maintenance and repair interventions.

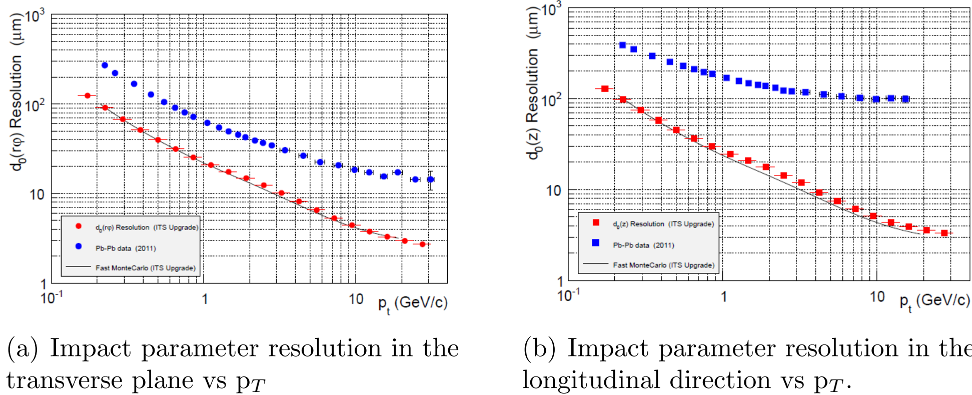
1.6 The ITS Upgrade Strategy

Despite of the success of the current ITS in the first characterization of the QGP, an upgrade strategy have been studied for this system in order to enable

it to carry out the physics program of ALICE. The two starting points that justify such an upgrade are the increase in the integrated luminosity up to 10 nb^{-1}, which calls for high statistics, and the precision measurements. So the new ITS has to be able to read-out and record all the Pb-Pb interactions at 50 kHz and to have an enhanced vertexing and tracking capabilities at low p_T.
The design objectives of the ITS upgrade are grouped below:

- **Improve impact parameter resolution by a factor 3 respect the current value.** This goal will be achieved by going closer to the interaction point, by reducing the entire material budget of the apparatus and increasing the detector position resolution.
  Thanks to the reduction of the beam pipe diameter at a value of 19 mm, even the first ITS layer radius will be reduced from 39 mm to 23 mm. Reducing the material budget of the first detection layer is important in order to diminish the effect of the multiple scattering which modifies the particles trajectories so deteriorating the detector tracking efficiency. For this reason the new ITS will be equipped with Monolithic Active Pixel Sensors (MAPSs) which can be thinned down to 50 μm. This thickness represents a gain factor of seven respect to the 350 μm of the present detector. With the MAPS technology the pixel chip can be optimized in order to minimize the power consuption so lighting the machanical, cooling and the other ancillary detector structures. In this way the ratio x/X_0 will be lower than 0.3% for the inner layers and 0.8-1% for the outer layers.
  The overall detector technology is based on the pixel sensors which allow for a precise position resolution thanks to the reduction of the pixel size down to $\sim 28\times28$ μm^2.
  Figure 1.8 reports a comparison between the resolution of the current ITS as obtained experimentally and the resolution expected in an upgraded scenario for primary charged pions. As shown in these panels, the impact paremeter resolution in the transverse plane and in the longitudinal direction is expected to have an improvement of a factor ~ 3 for a transverse momentum less than 1 Gev/c. This gain in resolution will be even higher for $p_T > 10$ GeV/c. Note that the red points are obtained by using a Fast Monte Carlo Simulation Tools for which the same values of the material budget cited above for the inner layers and the outer layers are set together with a pixel dimension of 20×20 μm^2 [10].

- **Enhance tracking efficiency and p_T resolution at low p_T.** In order to increase the detector granularity, the upgraded ITS will have



(a) Impact parameter resolution in the transverse plane vs p_T

(b) Impact parameter resolution in the longitudinal direction vs p_T.

Figure 1.8: Impact parameter resolution measured experimentally at $\sqrt{s_{NN}}$= 2.76 TeV (blue points) and expected in the after the upgrade (red points). The two set of points are referred to the resolution for primary charged pions as a function of p_T [10].

seven layers instead of six. But the major improvements is the granularity of the outermost layers with the replacement of the SDDs and the SSDs with pixel detectors.

- **Fast read-out.** The new detector will miss the particle identification feature. Actually, it was demostrated that the benefits which come from the measure of the ionisation in the silicon layers, mainly in the low momentum region, will be marginal. For this reason a binary read-out was chosen as the most suitable for the upgrade. Furthermore, the new detector will guarantee an improvement factor of 100 for the read-out rate capabilities since it has to be able to read event by event the Pb-Pb interactions at a rate greater than 100 kHz.

  The results of the design objectives above illustrated is shown in Figure 1.9 and 1.10. The new ITS will be a 12.5 G-pixel camera whitch covers an area of 10 m^2. The requirements for the Pixel Chips are shown in Table 1.2. The design streams for the R&D of the ITS will be discussed later in this thesis.

- **Fast insertion/removal for yearly maintenance.** A careful design of the entire apparatus has been planned in order to have a layout which allow the fast substitution of the damaged detector modules during the yearly shutdown.

Table 1.2: Pixel Chips requirements [10]

Parameter	Inner Barrel	Outer Barrel
Max. Silicon Thickness	50μm	50 - 100 μm
Intrinsic Spatial Resolution	5 μm	10 μm
Chip Size	15 mm $\times$ 30 mm ($r\phi \times z$)	
Max. Dead Area o Chip	2 mm ($r\phi$), 25 μm (z)	
Maximum Power Density	300 mW/cm^2	100 mW/cm^2
Max. Integration Time	30μs	
Maximum Dead time	10% at 50 kHz	
Min. Detection Efficiency	99%	
Max. Fake Hit Rate	10^{-5}	
TID Radiation Hardness	700 krad	10 krad
NIEL Radiation Hardness	10^{13} 1 Mev n$_{eq}$/cm^2	3 $\times 10^{10}$ 1 Mev n$_{eq}$/cm^2

1.6.1 The upgrade ITS layout

The detector will consist of seven concentric layers which have a radial coverage from 23 mm to 400 mm and a presudorapidity coverage of $|\eta|<1.22$. The seven layers will be equipped with MAPSs implemented in the TowerJazz 0.18 μm CMOS sensor technology.
For the mechanical point of view the new ITS consists of two indipendent barrels. The Inner Barrels is made up of the three innermost layers, whilst the Outer Barrel counts the two middle layers and the two outermost ones. Table 1.3 resumes the geometrical parameters of the upgraded ITS layout. Each layer is segmented in the azimuthally direction in units called Staves which are mechanically indipendent. A Stave covers the layers for the total length and it is the smallest operable part of the detector since contains all structural and functional blocks listed below, in addition to the Pixel Chips:

- Space Frame: A carbon fiber support which has a suitable stiffness to mechanically support each Stave;

- Cold Plate: A high-thermal conductivity carbon fiber which is used to cool down the Pixel Chips or Module Carbon Plate. The Cold Plate is integrated in the Space Frame for the Inner Banner Staves whilst it is attached to the Space Frame in the Outer Barrel

- Hybrid Integrated Circuit (HIC): A polymide Flex Printed Circuit (FPC) which integrates the Pixel Chips and some passive components.

Table 1.3: Layout of the upgraded detector [10]

Parameter	Inner Barrel			Outer Barrel			
Layer	0	1	2	3	4	5	6
Min. Radius (mm)	22.4	30.1	37.8	194.4	243.9	342.3	391.8
Max. Radius (mm)	26.7	34.6	42.1	197.7	247.0	345.4	394.9
Length (mm)	271			843		1475	
Pseudo-rapidity coverage	±2.5	±2.3	±2.0	±1.5	±1.4		±1.3
Active area (cm^2)	421	562	702	10483	13104	32105	36691
#Pixel Chip	108	144	180	2688	3360	8232	9408
#Staves	12	16	20	24	30	42	48
Staves overlap in $r\phi$ (mm)	2.23	2.22	2.30	4.3			
Chip Spacing	150 μm						

- Half-Stave: A segmentation in the azimuth direction of the Outer Barrel Stave which covers the total lenght of a Stave. Each Half Stave consist of 7 HICs glued together on a common cooling unit.

An aspect that has to be mentioned is that the radiation load at which the ITS is exposed is relatively light if compared with the others LHC experiments. Actually, the Total Ionizing Dose (TID) is $\sim$ 2.7 Mrad where the NIEL is 1.7×10^{13} 1 MeV n_{eq}/cm^2. Even if MAPSs are more sensitive to radiation damages, the chosen technology is able to sustain a TID even higher than the value mentioned above.

1.6.2 Layout of the Inner Barrel Stave

The three innermost ITS layers have a Stave layout as shown in Figure 1.9. It consist of nine Pixel Chips in a row which are laser soldered to the FPC. Since each Pixel Chip has a size of 30 mm×15 mm and there is a chip pitch of 150μm, a Inner Barrel Stave covers a total area of 15 mm×270.8 mm. The HIC is glued to the cooling system with the Pixel Chips facing it in order to maximize the cooling efficiency. Both ends of a Stave have a mechanical connector to fix and align it to the end wheels. In order to guarantee the detector hermeticity the Staves are partially superimposed. The Stave material budget is 0.3% X_0 and it takes into account the contribution of the HIC, the cooling system and the space frame.

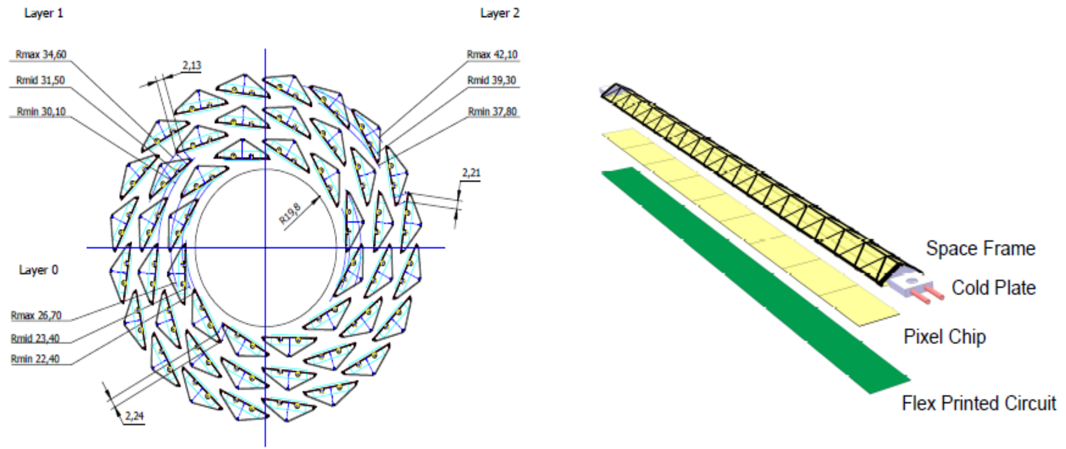


Figure 1.9: Cross section and Stave layout for the Inner Barrel Modules.

1.6.3 Layout of the Outer Barrel Stave

The Middle Layers and the Outer Layers have the same layout even if the two outermost layers are twice longer. In the azimuthal direction they are divided in two Half-Stave whilst over the full length they are subdived in four or seven Modules for the Middle and the Outer Layers respectively. The Space Frame supports two Cold Plates which holds up four or seven Modules. They are superimposed in the transverse plane in order to ensure the full detector coverage. In case of the Outer Barrel Stave, the HIC supports two rows of seven Pixel Chips each for a total area of 30 mm×210 mm. The FPC distributes the clock, the configuration signals and it is used also for the data read-out and power distribution to the Pixel Chips and to the HICs. An additional power bus which covers the FPC of the Half-Stave is used to distribute the power with a proper voltage drop which is compliant with the power density constraints. Finally, the extimated material budget for the Outer Barrel Stave is 1% X_0.

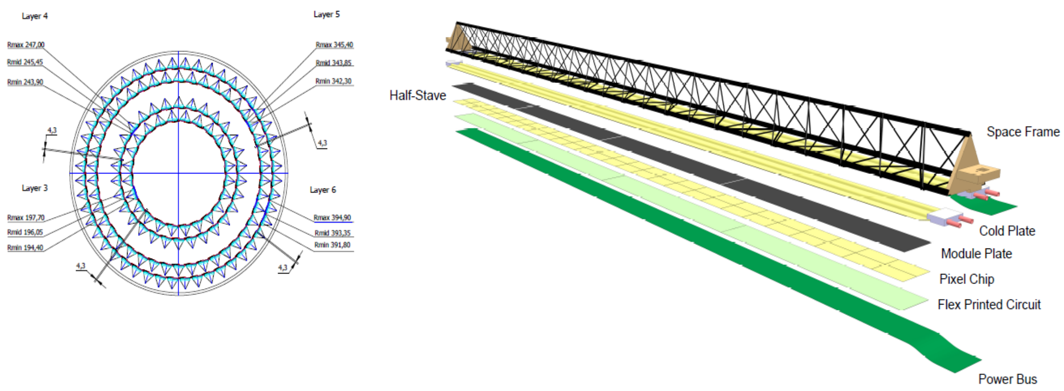


Figure 1.10: Cross section and Half-Stave layout for the Onner Barrel Modules.

Chapter 2

Monolithic Active Pixel Sensor for the ITS upgrade: the ALPIDE Pixel Chip

Within the R&D of the ITS upgrade variuos option have been explored to design a pixel chip fitting the requirements of the ALICE experiment. As explained in the previous chapter, the ITS upgrade aims to enhance the performance of tracking detector in terms of resolution on the distance of closest approach, read-out rate capability, power consumption and radiation hardness. For this reason semicondutor detectors have been selected to equip the entire upgraded ITS, like in the current version. However, the new tracker will be covered with a new technology of pixel sensors, i.e. Monolithic Active Pixel Sensor (MAPS). Actually, MAPS is a well know technology optimized for commercial use, like in the pixel camera, and it is thought to be a suitable option for the upgrade of the LHC tracking detectors. In particular, this option has been widley explored for the ITS upgrade which comes out with two main design streams based on MAPS: the ALPIDE and MISTRAL-O pixel chips. The former has an innovative read-out architecture, based on data compression made by an in matrix data driven read-out whilst the latter uses a classical rolling shutter architecture to read the entire matrix. Despite the fact that both developments meet the ITS requirements on the pixel sensor, the most promising one is the ALPIDE chip and for this reason it has been taken as a baseline for the development of the new tracker.

After a general overview on the principle of operation of a semiconductor detector and its operation in a high radiation enviroment, this Chapter will describes the MAPS technology and its application in case of the ALPIDE chip development.

2.1 Introduction - Semiconductors Detectors

The principle of operation of a detector is the conversion of the energy deposited by a particle in the detector sensitive volume in a signal which can be processed by an electronics circuit. A simple example is shown in Figure 2.1.

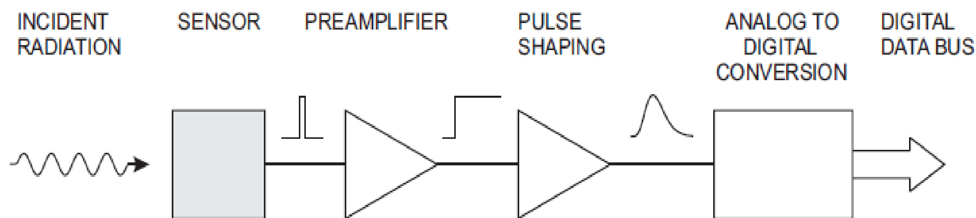


Figure 2.1: Operating Principle of a detector: the radiation which passes in the sensor release energy which will be converted in an electronic signal. This signal so obtained will be processed to extract informations about the radiation itself. [17]

This section gives a review on the working principle semiconductors detectors, especially silicon devices, which are widely used in High Energy Physics (HEP).
Actually, solide-state detectors combine high resolution measurements for the energy released from a passing charged particle together with a high spatial resolution on a track reconstruction. Another key characteristic is also the radiation hardeness of the material which allows for a good data quality even in high radiation environments. For these reasons semiconductor detectors equip the trackers of HEP experiments where particle identification as well as particle tracking and vertexing reconstruction are performed.

A semiconductor detector works as an ionization chamber for which a gas is replaced by a semiconductor crystal. The high energy resolution is obtained thanks to the low ionization energy and the high density of a semiconductor. Indeed, a particle which traverses a semiconductor material generates electron-hole pairs which will be collected by the electrodes. The number of charges so generated is higher than the one generated in the ionization chamber since the energy required for a pair creation in a semiconductor is much lower then a gas. As an example, the silicon ionization energy is E_i=3.6 eV whilst the mean energy required for He gas to create an ion-electron pair is 41 eV. Furthermore, the energy released for a unit path length by a charged particle is greater than a gas [14].

2.1.1 Principle of operation of silicon Sensors

Because of their physical features, semiconductors are a suitable option for particle detection. Among Ge, Si and GaAs, silicon sensors are the mainstream typology used for tracking detectors. Indeed, silicon devices have lower leakage current than Germanium and the silicon Oxyde (SiO_2) is not soluble in water, unlike Germanium Oxyde, so that silicon is more suitable to build transistors. Furthermore, high quality SiO_2 can be grown thermally. Moreover, silicon is less expensive than the other semiconductors since it is one of the most abundant element Earth's crust.

A silicon detector is based on the creation of a *p-n junction*, as the one shown in Figure 2.2, which works as a collection diode for the charge generated by a traversing particle. With this aim, the silicon resistivity is modified by adding doping atoms to the crystal which alter the number and the type of majority carriers[1]. Doping atoms like Arsenicum (As) are said *donors* because they replace a Si atom in the crystal by giving an excess electron to the valence silicon band, so generating a n-type silicon (here the majority carriers are electrons). Conversely, atoms like Boron (B) are called *acceptors* since in the silicon replacement they leave a hole, i.e. a unpaired valence electron, so producing a p-type silicon (here the majority carriers are holes). The resistivity ρ at the microscopic scale is defined as

$$\rho = \frac{1}{q(\mu_n n_n + \mu_p n_p)} \tag{2.1}$$

where $\mu_{n,p}$ is the carriers mobility[2] and $n_{n,p}$ is the doping density. By varying the ratio betwen n_n and n_p it is possibile to set the majority carriers in the material. Generally speaking, typical doping densities are $10^{14} - 10^{19}$ atoms/cm^3, depending on the application.

The most important thing in the doping of a semiconductor is that the donors or acceptors impurities create energy levels which are very close to the conduction band (n-type) or to the valence band (p-type). These energetic steps allow for an easier promotion of an electron in the conduction band and a hole in the valence band.

A sensitive diode is assembled by putting together a n-type and a p-type silicon pieces. Since a gradient of concentrations of holes as well as electrons exists between the two regions, the majority charge carriers start to move across the junction because of the thermal diffusion. In this way,

[1]Majority carriers in semiconductors are the particles which dominate the current flow

[2]The mobilty values for electrons and holes in the silicon are respectively $\mu_n = 1345$ $cm^2/(V \cdot s)$ and $\mu_p = 450$ $cm^2/(V \cdot s)$. Note that these value can vary depending on the temperature and the doping levels.

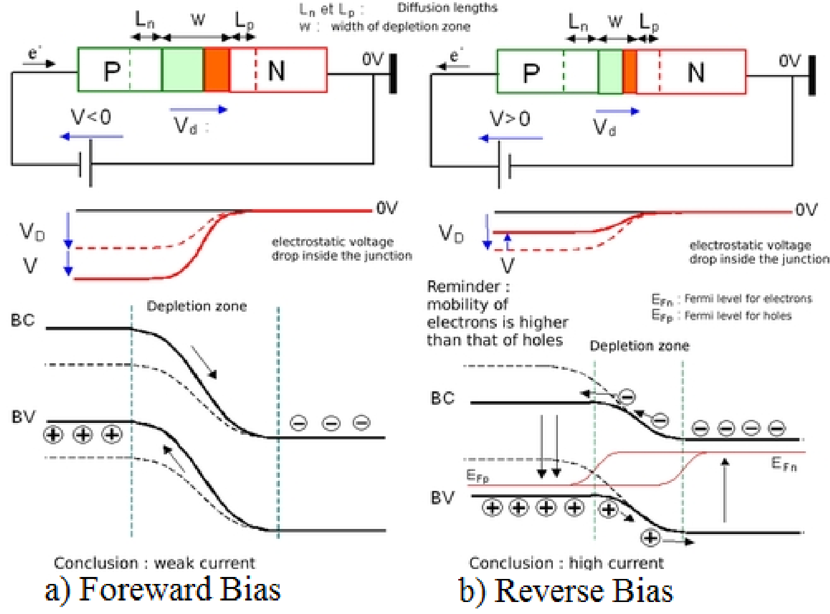


Figure 2.2: Detector principle of operation [18].

a region of non-mobile space charge is formed around the junction, since the majority carriers flow leaves in the p-type region an excess of negative ions and in the n-type an excess of positive ions. The carriers diffusion will be blocked at the equilibrium thanks to the potential barrier V_{bi} (built-in voltage) that is generated between the two space charge densities. This means that an electrical field $\vec{\mathcal{E}}$ exists between the space charge densities which pushes particles of opposite charges in opposite direction.
The central zone W of the junction is named depletion zone since there are no mobile charge carriers except those thermally generated and that are pushed away by $\vec{\mathcal{E}}$.

The spatial extent of W depends on the donors doping density N_D for the n region and the acceptors doping density N_A for the p region:

$$W = \sqrt{\frac{2\epsilon_s V_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{2.2}$$

Here ϵ_s[3] is the silicon dielectric constant and q is the electron charge.
Since the density of the dopants can be not symmetrical, W is wider in the side in which the doping level is lower. For example, if we consider $N_D >> N_A$ the junction is asymmetrical with a very strong doping level of

[3] $\epsilon_s = 11.7$

the n region ($p-n^+$), so the depletion zone is more extended in the p region than in the n region.

The main feature of a diode is that the electrical current flows in one direction only. When the diode is forward biased the magnitude of the potential barrier between the junction is lowered, in favor of the majority carriers current. The ideal I-V characteristics of the diode is then:

$$I = I_s(e^{\frac{qV}{k_B T}} - 1) \tag{2.3}$$

A diode shows the best performance as a detector when a reverse bias voltage V_{rb} is applied between its terminals since a larger depletion zone is necessary in order to stop high energeretic particles and to have a small diode capacitance for a good signal-to-noise ratio. Actually, V_{rb} contributes to further stop the diffusion of the majority carriers by rising the height of the potential barriers of the junction. It widens the junction as:

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} + V_{rb})}{q}\Big(\frac{1}{N_A} + \frac{1}{N_D}\Big)} \tag{2.4}$$

This fact has an impact on the capacitance C associated to the junction and which depends on the depth of the depletion zone and then on the bias voltage as:

$$C = \epsilon_s \frac{A}{W} = A\sqrt{\frac{\epsilon_s e N_{D,A}}{2(V_{rb} + V_{bi})}} \tag{2.5}$$

From this formula it can be argued that C decrases at higher reverse bias voltage and the results are shown in Figure2.3. However, the reverse bias that can be applied to the junction is limited by the junction breakdown [14].

2.1.2 Particle Energy Loss

When a ionizing particle hits the sensor and traverses the sensitive volume of the collection diode, it loses energy according to the **Bethe-Bloch** formula (Figure 2.4):

$$-\langle\frac{dE}{dx}\rangle = Kz^2\frac{Z}{A\beta^2}\Big[\frac{1}{2}ln\Big(\frac{2m_e c^2\beta^2\gamma^2 T_{max}}{I^2}\Big) - \beta^2\Big] \tag{2.6}$$

This formula describes the average energy loss of a particle per unit path

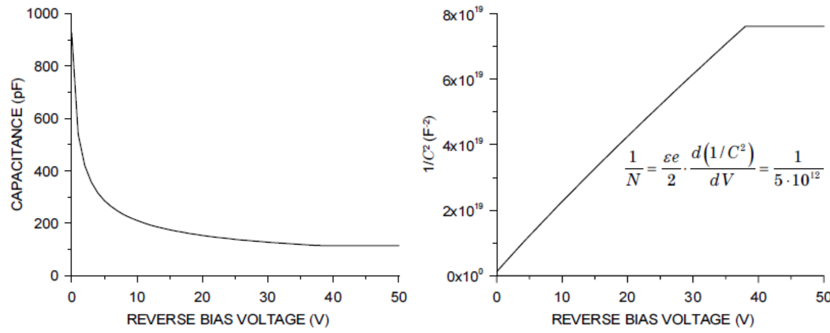


Figure 2.3: Diode capacitance vs reverse bias. With a suitable choice of the reverse bias is possible to minimize the sensor capacitance [17].

lenght, i.e. the *linear stopping power S*, by taking into account the quantum-mechanicanical nature of the scattering between the traversing particle and the atomic electrons of the sensitive volume ([14], [19]). It depends on the particle energy and the material characteristics, as shown by the parameters below:

$S = \langle \frac{dE}{dx} \rangle$	energy loss expressed in $\frac{eV}{g/cm^2}$;
K	$4\pi N_{av} r_e^2 m_e c^2 = 0.307075 MeV cm^2$ e r_e classical electron radius;
z	charge of incident particle in units of the electron charge;
Z	atomic number of absorption medium (14 for silicon);
A	atomic mass of absorption medium (28 for silicon);
$m_e c^2$	$0.511 MeV$ rest energy of the electron;
β	velocity of the particle in units of the speed of light;
γ	Lorentz factor defined as $(1-\beta^2)^{-\frac{1}{2}}$;
T_{max}	maximum kinetic energy transferred to the particle;
I	mean excitation energy (137 eV for silicon).

The energy loss causes the generation of the free charge carriers that are efficiently separated by the electrical field of the junction. The application of a reverse bias voltage speeds up the particle by enhancing the collection efficiency.

Although the reverse bias at the junction limits the thermal diffusion of

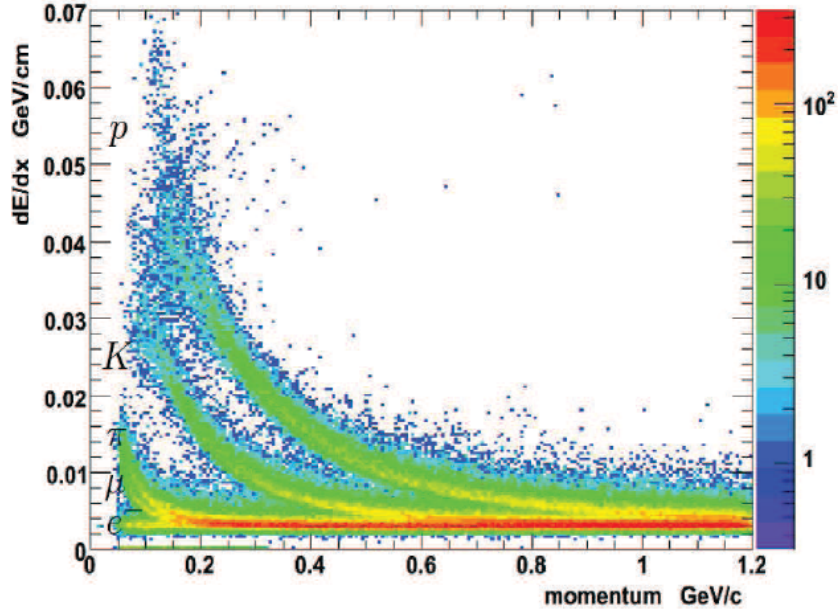


Figure 2.4: Energy loss of charged particle in silicon sensors [15].

the majority carriers, this is not true for the minority charge carriers[4] which can derive across the junction. This flow results in a leakage current across the junction of some nA/cm^2. Actually, the leakage current depends on the intrinsic carrier concentration n_i of the silicon ($n_i = 1.45 \cdot 10^{10} cm^{-3}$), the diffusion constant $D_{p,n}$ of both holes and electrons, the diffusion length $L_{p,n}$ of the charge carriers [5] and on the diode section A:

$$I_s = -q\Big[\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\Big] n_i^2 A \tag{2.7}$$

Another contribution of some μA/cm^2 to this parasitic current that cannot be forgotten is due to the carriers which are thermally generated in the depletion region because of the trap densities and that are separated quickly by the electric field. However this contribution can be reduced by using a high purity silicon wafer [16].

[4]Minority carriers are electrons in a p-region or holes in n-region

[5]The diffusion length is the mean specific distance that a free charge covers in the material because of the thermal diffusion, before recombining it with a carriers of opposite charge. $L_{p,n}$ is given by: $L_{p,n} = \sqrt{D_{p,n}\tau_{p,n}}$, where $\tau \approx \mu s$ is the time needed for a decrease of 1/e of the minority carriers.

2.1.3 Radiation Damage in silicon Sensors

High Energy Physics demands for radiation tolerance of sensor and electronics to guarantee high data quality even in a high radiation environment. Actually, a single particle which traverses a detector can wreak mulfunctions in the electronics devices (Single Event Effects) whilst a high radiation dose can alter the structure (displacement damage) or the charge density (ionization damage) in the silicon bulk cristal or in the silicon oxide.

1. **Single Event Effects**

   Single Event Effects (SEE) have an influence on the detectors electronics. They are not cumulative effects since they can be produced by a single taversing particle. For this reason SEE have a stochastic nature since they can happen at any instant during the circuits operation. In general one can distinguish between:

   - Single Event Upset (SEU) which is a non desctructive and not permanent event. It manifests itself as a bit flip in the digital IC, mainly in the registers, in memory cells and in the storage nodes in general [19].
   - Single Event Latchup (SEL) which is destructive and it can occurs when a parasitic PNPN structure is present. Actually, when a SEL takes place the current which flows in the device can reach forbidden destructive values. This effect influence mainly power MOSFET, BJT and diodes.

   The probability to have a SEE dipends on circuit complexity, on the deposited charge and on the volume in which the charge has been deposited. For this reason SEU and SEL are described in terms of probability by means of a cross section. Given by the stochastic nature of the event, to foreseen a SEE it impossible. However, it is possible to equip the circuit with some ancillary blocks which correct or reconfigure it when a SEU is present (triplication, redundancy, etc..).

2. **Cumulative effects**

   Cumulative effects depends mainly on the flux and on type of the radiation which invests the sensor and the electronics. Their influence is on the silicon bulk of a diode and on the SiO_2 gate surface of a transistor, as reported below.

- **Displacement Damage**. This is a non-ionizing damage which take place in silicon bulk. Actually, it corresponds to a modification of the silicon crystal due to an incident radiation which kicks out a silicon atom from its natural position. As can be argued, a displacement damage is due to the stransfer momentum between an incident particle and the crystal atoms. For this reason, the effect is specific for each hitting particle since it depends on the mass and on the energy of the particle itself. A displacement damage generates clusters of defects and then the electrical charatcteristics of the Si crystal are modified as well as its bands structure. This kind of damage manifests in the presence of mid-gap states, of defect levels close to bands edges and in the inversion type mechanism.
  Mid-gap states between the valence and the conduction band of the semiconductor are intermediate energy steps which ease the promotion of electrons in the conduction band and holes in the valence band, hence contributing to a modification of the current in a p-n junction. Mid-gap states in the depletion region can increase the leakage current due to the generation mechanism whilst the direct current can be reduced because of the recombination mechanism. The reverse bias current in a diode after the irradiation is a sum of the leackage current I_0 before the irradiation and a term which takes into account the particle and fluence (Φ) which impact on the diode and the device volume ($A \cdot d$), as follows:

$$I_d = I_0 + \alpha \cdot \Phi \cdot A \cdot d \tag{2.8}$$

  The traps levels near to the bands edges contribut to modifie the current of the junction since they capture a free charge carrier and release it with some time. In contrast, displacement damages ususally generate acceptor-like states in n-type silicon which can be populated by the thermally excited electrons. In this way a negative space charge will form in the depletion region. Even if the acceptor states can compensate the original donor states, at some fluences extent they are so high that the inversion type takes place. This means that the material appears like a p-type but none mobile holes are generated in the device. This effect depends on multiple process and it can varies with the temperature. It has been demostrated that to limit the change in doping characteristics can be useful to add Oxygen to the silicon since it prevents the formation of electrical active sites in the sensor bulk

[17].

- **Ionization Damage**

  The SiO_2 and the insulator layers are affected by the ionization damages which allow the formation of free charge carriers that can be trapped during their motion, thus altering the electrical field in proximity of this charge accumulation point. Generally speaking, an ionization damage does not depend on the radiation type but on the energy released from the radiation in the material. The major impact is in the increase of the threshold voltage of MOS transistors since it depends on the traps formed in the oxide and on the mobility of electrons and holes. Actually, the ionization particles generate free electron-hole pairs even in the oxide. Taking the NMOS transistor case, in the oxide free electrons move fast towards the positive electrode whilst the slow holes accumulate in the oxide-silicon interface and create a positive space charge density just above the channel. This means that in order to create a channel in the transistor the voltage gate has to be lowered to allow the transistor to work.

  One has to design upon specifics layout techniques (e.g. enclosed layout) to limit the effects of the ionization damages. However, the shrink of transistors feature size, together with the thinning of the gate oxide, helps to have radiation hard electronics. It can be demonstrated that the holes trapping probability increases roughly linearly with the oxide thickness as well as the number of holes that can be trapped. In this way, by using thinner oxide, the threshold voltage shift can be reduced [17].

2.2 Monolithic Active Pixel Sensors

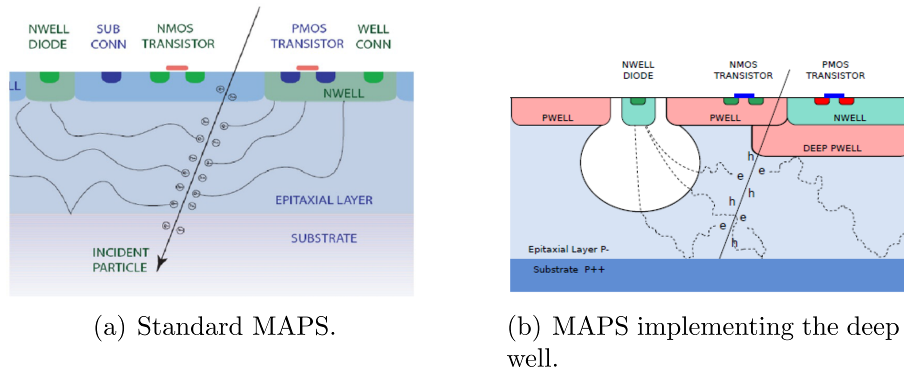
Monolithic Active Pixels Sensor is the technology chosen for the ITS upgrade since it allows to build a Pixel Chip which integrates the sensor matrix and the read-out electronics in one silicon wafer and the hybridization process will not be necessary anymore. This characteristic turns out in benefits in terms of overall detector material budget and production cost reduction. Indeed, MAPS thickness can be thinned down to 50 μm and there is the possibility to achieve very small pixels sizes, up to $2\times$ 2 μm^2. However, a chip size bigger than 10 μm $\times$ 10 μm is already suitable for the high energy physics purpose. Furthermore, MAPSs are produced in standard CMOS technology since they are widely used in commercial image sensors like the full frame digital cameras and then they are available for a very reduced cost [20].

These are two keys characteristics to build a particle detector at a restrained cost but with improved vertexing and tracking capabilities obtained thanks to the reduced material budget and the improved pixel granularity.

Since pixel hybridization process is not necessary for MAPS, one has to find the material which better suites the requirements both for the in-pixel electronics and for the sensor.

Electronic grade silicon wafers with low resistivity and grown with the Czochralski (CZ) method are used to develop transistors in a standard CMOS technology. The CZ technique leaves defects and atoms of impurities in the bulk silicon crystal and a further formation of structural defects may occur. Because of that, this kind of silicon wafer is not suitable to develop a sensor for which a high resistivity together with a special pureness degree are essential to have a very high collection efficiency. Indeed, for the *detector grade* silicon a high resistivity allows to deplete easily the sensitive volume whilst a low defects density is necessary to reduce the generation-recombination of the carriers by the mechanism of trapping which influences the leakage current flowing in the device.

A standard MAPS is shown in Figure 2.5(a). It is assembled by growing a silicon p^- epitaxial layer on the p^{++} CZ substrate. The epitaxial growth allows for an ordered atomic layers with a scarce probability of structural defects formation. Finally, a n-well on the p epitaxial layer collects the charges generated in the sensor. The overall thickness occupied by sensor and electronics can be reduced to less than 50 μm in which up to 20 μm can be occupied by the epitaxial layer.



(a) Standard MAPS.

(b) MAPS implementing the deep p-well.

Figure 2.5: Cross section of Monolithic Active Pixel Sensor (MAPS) i the standard configuration and with the deep p-well option.

The operating principle of a MAPS is based on the creation of a p-n junction that works for the collection of the charge produced by a ionizing particle traversing a detector. It has to be noted that the number of charges

created in this thin sensor is moderate. Actually, a Minimum Ionizing Particle (MIP) which crosses a silicon sensor generates ≈ 80 electron-hole pairs per μm, i.e. less than 2000 charged particles in 20 μm in the case of MAPS. The carriers so generated into the device move because of thermal diffusion. Unfortunately, this fact has two drawbacks which influence the standard MAPS charge collection performance, namely the spread of the collected charge among a small number of pixels (clustering) and the comparatively long collection time of ≈ 100 ns.

Large cluster sizes have an influence on the pixel performance since they affects the signal-to-noise (S/N) ratio of each pixel and all the parameters which depend on this ratio. Furthermore, special circuit architectures have to be provided for the information handling, since even a single hit event can involve a big mole of informations that have to be retained or not.

Due to the long collection time, the probability of charge recombination and charge trapping is increased. This may become a problem when the devices are exposed to non-ionizing radiation that damages the silicon bulk by affecting the collection efficiency. Actually, the use of MAPS in high energy physics (HEP) experiments requires radiation tolerant devices up to $10^{16}\mathrm{n}_{eq}/\mathrm{cm}^2$.

A solution which is beneficial for the two cons of collecting charge by diffusion is the application of a reverse bias to the MAPS collection diode. In this manner the sensible volume can be depleted and the collection mechanism is mainly due to the carriers drift, so that the charge collection time can be reduced to few ns. Moreover, as shown in Section 2.1.3, the shrinked CMOS technolgies can be useful to enhance the radiation tolerance of MAPS thanks to the reduced gate oxide thickness [21].

In addition to the collection by drift to enhance the radiation hardness, a high S/N to minimize power consumption can be obtained using MAPS. It has to be outlined that having a limited power consumption helps to diminish the tracker material budget thus entailing for a lightening of the electrical power and signal cables as well as of the mechanics and cooling systems.
The power nedeed to analog and digital circuits inside the chip and the power used to link the detector to the patch panel are some of the contributions that have to be take into account to define the overall pixel chip power consumption, which is about hundreds of $\mathrm{mW/cm}^2$ at LHC trackers.

It can be show that the ratio between the collected charge Q and the capacitance of the input electrode C is the key parameter to lower the analog power consumption. In particular, the Q/C ratio can be maximized by reducing the input capacitance C at values of few fF. The S/N ratio at a given bandwidth is proportional to Q/C, the proportionality factor being the transconductance of the front-end input transistor.

Providing that the signal that has to be handle is a voltage (Q/C), even the noise of input transistor has to be a voltage. The power spectral density of this noise depends on the transistor size and bias conditions and it can be expressed as ([21], [22]):

$$\frac{dv_{eq}^2}{df} = (\frac{K_F}{WLC_{ox}^2 f^\alpha} + \frac{2k_B T n}{g_m}) \quad \text{transistor in weak inversion}$$
$$\frac{dv_{eq}^2}{df} = (\frac{K_F}{WLC_{ox}^2 f^\alpha} + \frac{4k_B T \gamma}{g_m}) \quad \text{transistor in strong inversion}$$

In the previous equations the first term shows the contribution of the 1/f noise whilst the second one represents the thermal noise which directly influences the power consumption. By doing the convolution of one of those equations with the front-end transfer function and taking the integral in the frequency domain only for the thermal component, the S/N ratio will be

$$\frac{S}{N} \sim \frac{Q}{N}\sqrt{g_m} \tag{2.9}$$

Since g_m is directly proportional to the transistor bias current and then to the power, the equation 2.9 is rewritten as:

$$\frac{S}{N} \sim \frac{Q}{N} \sqrt[m]{I} \sim \sqrt[m]{P} \tag{2.10}$$

where $2 \leq m \leq 4$ is a factor which depends on the transistor bias condition. From here it can be argued that operating the input transistor in weak inversion weakly improves the S/N ratio. However, by handling equation 2.11 the power dissipated by the circuit is:

$$P \sim \left(\frac{S}{N}/\frac{Q}{C}\right)^m \longrightarrow P \sim \left(\frac{Q}{C}\right)^{-m}. \tag{2.11}$$

As said before, by minimizing the input capacitance the pixel power consumption can be reduced.

2.3 MAPS application for the ITS Upgrade

Despite of the fact that standard MAPS allow to diminish the material budget inside the overall detector and to lower the power consumption, they cannot satisfy the specifications for the ITS upgrade reported in Section 1.6. The major limitation of stardard MAPS is that it does not allow to have complex in-pixel circuitry since the use of PMOS transistors can be deleterious for the charge collection since a competition could be with the collencting n-well diode. Actually, as it is possible to see in Figure 2.5(a), PMOS transistors demand for a deposition of a second n-well in the epitaxial layer. In this

Table 2.1: ALPIDE and MISTRAL-O design specifications, [13]

Pixel Pitch (μm)	28×28	36×64
Event Time Resolution (μs)	<2	∼ 20
Power Consumption (mW)/cm^2	∼ 35	97
Dead Area (mm^2)	1.1×30	1.7×30

way the electrode and the extra n-well will compete for the charge collection hence degrading the collection efficiency of the sensor. In this sense, the 0.18 μm CMOS technology by TowerJazz is the solution selected to design the Pixel Chip for the ITS upgrade since it has some specific features.

The key aspect is the deep p-well option which gives the opportunity to implement PMOS transistors. As shown in Figure 2.5(a), a deep p-well is deposited in the epitaxial layer, just above the n-well which hosts the PMOS transistors. This deep p-well shields the n-well to collect the particles generated inside the sensitive volume, thus preserving the charge collection efficiency of the collection diode. Furthermore, it generates a electrical potential which drives the charged particle towards the collection diode. As a result, the deep p-well option is fundamental for the implementation of most complex in-pixel circuits allowing a pixel chip with a different kinds of features, like the in-pixel hit discrimination [10].

Another important aspect is that the TowerJazz technology is expected to be more robust to the radiation damages because of the feature size and the doping characateristics. The 0.18 μm technology node is beneficial for the tolerance to the total ionizing dose (TID) since it foreseen a gate oxide thickness below of 4 nm. Furthermore, to ensure the resistivity to non-ionizing radiations together with an improved S/N ratio this technology offers the possibility to slim down the thickness of the epitaxial layer up to 40 μm and to select its resistivity in a range (1÷6) k$\Omega \cdot cm$. Indeed, this resistivity values allow the application of a moderate reverse bias ranging between (1÷6) V. In this way the sensor volume can be depleted and the charge collection will be done mainly by drift, thus reducing even the collection time. Moreover, this MAPS technlogy gives also the opportunity to use six levels of metallization that guarantees a high density and low power digital circuits together with the feature transistor size.

2.3.1 Pixel Chip options: ALPIDE &MISTRAL-O

Different options for the pixel chip of the ITS upgrade have been developed in parallel during the R&D phase. In particular ALPIDE and MISTRAL-O

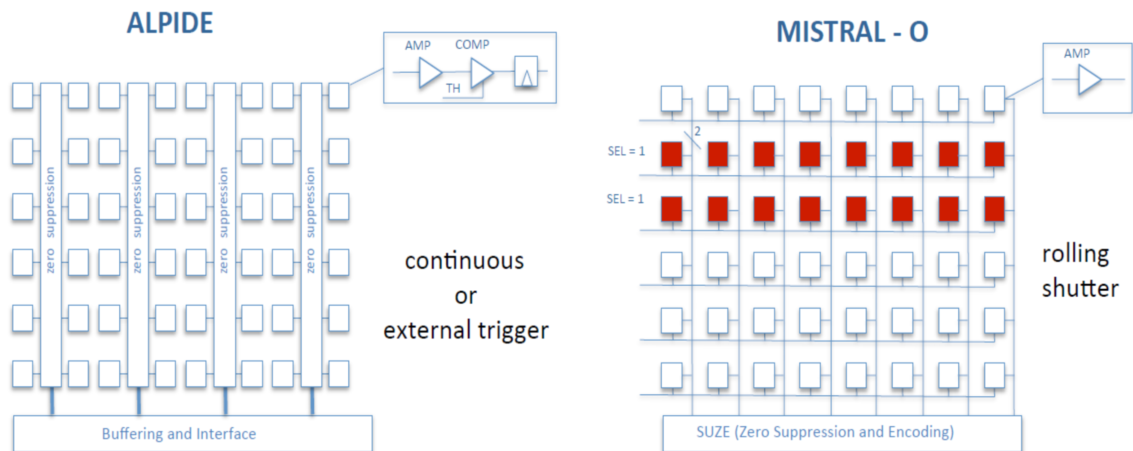
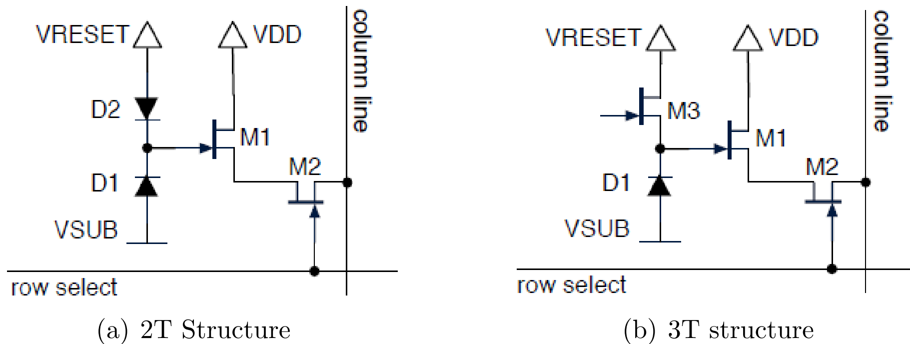


Figure 2.6: ALPIDE and MISTRAL-O read-out schemes, [13]

were the two possible design alternatives to equip the new silicon tracker. Those chips have the same dimensions of 3×1.5 cm^2 and they are fully compatible in terms of pads positions and data transmission protocol. Actually, each of them consists of a pixel matrix which stands above the chip periphery where the slow control and clock distribution circuits as well as the high speed output are hosted. However, ALPIDE and MISTRAL-O differ in terms of the pixel sizes which cover the matrix, the number of rows and colums in the matrices and the read-out architecture, as summarized in Table 2.1 and shown in figure 2.6. Since for the ITS upgrade purposes the essential information is about the particle hit, a binary read-out is needed which reports whether a pixel was fired or not. For this reason the read-out architecture has to have a comparator feeded by a threshold and the analog signal from the collection node. Then, the key difference from ALPIDE and MISTRAL-O is where and how this binary information is obtained.

MISTRAL-O is based on the experience of MIMOSA chips, developed for the STAR PXL detector [23]. In this case the pixel has only the amplification stage and the analog signal is shifted to the periphery where the comparator needed for the binary information is located. Indeed, the read-out architecture is the traditional rolling-shutter scheme which is based on the 2T and 3T pixel structures shown in Figure 2.7. Those two schemes differ for the pixel reset mechanism. In the 2T architecture the reset is made by a diode (D2) whilst for the 3T scheme the pixel is actively reset by the transistor M3. Except for this aspect, the working principle is the same: the collection electrode (D1) is connected to the gate of transistor M1 which buffers the input signal to the output. Transistors M2 works like a switch by selecting the output signal that has to be buffered and sent to the column line. Here,



(a) 2T Structure (b) 3T structure

Figure 2.7: Basic structures for the rolling-shutter architectures.

the row select signal drives the switch and works like a shutter since the signal will be integrated between two consecutives row select signals [10]. The rows in the pixel matrix are paired and each pair is read one after the other, always being sensible. This is done at the cost of a more important power consumption and a longer time to read the entire matrix than ALPIDE, as shown in Table 2.1. In order to fit these two last parameters with the ITS requirements, MISTRAL-O has a less dense pixel matrix, 208 row×832 colums with a pixel pitch of 36 $\mu m \times 64 \mu m$, which does not allow to have a spatial resolution better than 10 μm.

ALPIDE has a more advanced read-out architecture which takes advantages of the TowerJazz features by integrating the full signal processing in the pixel matrix. This means that each pixel contains an amplifier, a comparator and a multi-hit buffer. Furthermore, the zero suppression read-out is even integrated in the matrix. Even if ALPIDE as well as MISTRAL-O meet the ITS requirements and a full-scale prototype is ready, the former has been chosen as the baseline for the chip that was decided to adopt for the ALICE ITS upgrade given its superior design specifications (Table 2.1). For this reason the following sections will give a detailed description of the ALPIDE implementation.

2.4 ALPIDE

The R&D of the ALPIDE (ALice PIxel DEtector) pixel chip started in 2012 with the development of the prototypes of the Explorer family to asses the radiation tolerance of the MAPS technology chosen, to study the possibility to back-bias the sensor and to optimize its shape in terms of charge collection [24]. After that, the small scale and full scale prototypes of the ALPIDE chip

(pALPIDEfs, pALPIDE-1-2-3) have been developed with the aim to study the novel front-end with the in-pixel discrimination together with a data driven read-out architecture and a zero-suppression in the matrix. Actually, this novel front-end turns out in design objectives a bit more aggressive than the ITS requirements since it has a power density less than 30 mW/cm^2 and an integration time around 2 μs.

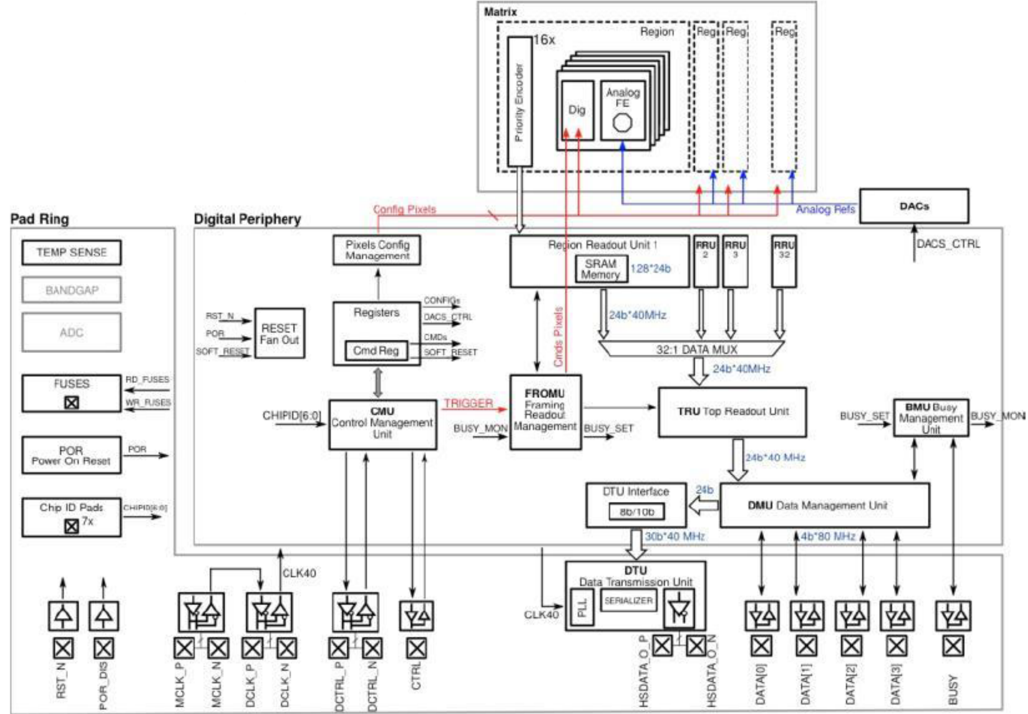


Figure 2.8: Block Diagram of the ALPIDE full scale chip [25]

The block diagram of the last full scale ALPIDE chip which integrates all chip features and which is the closer to the final version is shown in Figure 2.8. As explained before, the pixel matrix stands above the chip analog periphery, which hosts the data read-out circuits, and it is surrounded by the digital periphery with the control interfaces which are needed to identify the chip and its position in the matrix, to write and read access to internal registers and memories, to distribute trigger commands, configuration settings and broadcast synchronous signals. The overall chip is powered by separated analog and digital 1.8 V power supplies. The two power domains are separated to reduce the coupling between the analog and the digital part of the chip.

A p$^+$ seal ring is around the entire pixel chip to avoide leackage and breakdown effects at the boundary whilst a n$^+$ ring shields the sensitive

area of the matrix from the rest of the circuitry. This well collects the charges running away from the sensor or those which are produced outside the sensitive are and diffuse to it. The thikness is 50-100 μm where 18 μm are occupied by the epitaxial layer. As foreseen by the MAPS technology, the deep p-well shields all the chip circuitry allowing to maximize the charge collection efficiency of the sensor.

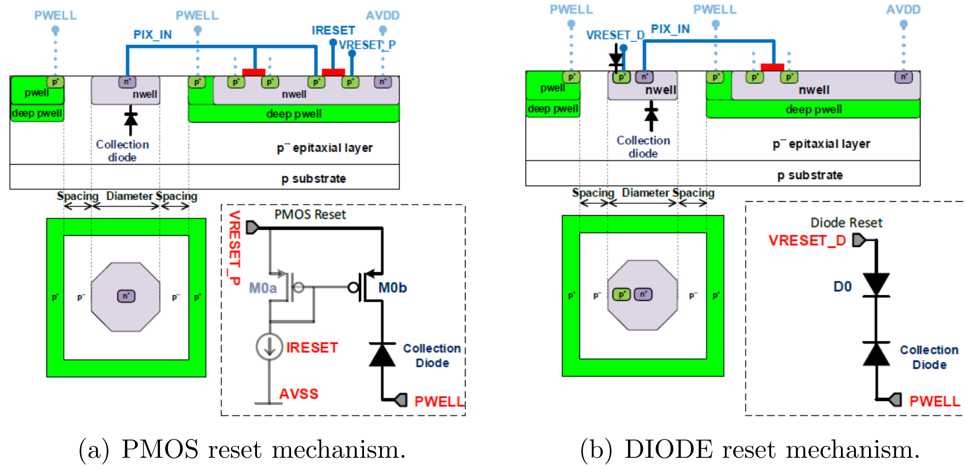
The hit/no hit binary information is obtained in the pixel by using a non linear current comparator. Only when the pixel is hit this digital signal is processed by the in-matrix Address-Encoder-Reset-Decoder (AERD) circuit (data driven read-out). The AERD tracks down the address of the hit pixel with the highest priority and propagates back a signal to reset it. Because of layout and power constraints a priority encoder is shared between each double column.The signals from the encoder are sent to the end-of column circuit where the data compression is done [26].

There are to ways to connect ALPIDE to the external patch panel. Actually, this pixel chip is compatible to be wire bondend and laser soldered to the Flex Printed Circuit for the power distribution and data transmission. For this reason the south edge of the chip hosts the standard type pads which are 92×92 μm^2 squares, in charge for the wire bonding, whilst the so called *pads over logic* are 300×300 μm squares. They are placed over the matrix and the chip periphery and are used for laser soldering [25].

2.4.1 Pixel Matrix - The sensor and the in-pixel discrimination circuit

The pixel matrix is formed by 512 row and 1024 columns which are covered by circa 500k 28×28 μm^2 pixels for a total of 14.3×28.7 mm^2 active area. The electrode is an octagonal shaped n-well which has a diameter of 2 μm. It is sourrounded by a squared deep p-well, as it is shown in Figure 2.9. The distance between the n-well and the p-well is around 3 μm. This geometry has been chosen to maximize the Q/C ratio and to minimize the coupling between the two wells. The sensor can be back-biased since the potential of the substrate can be below zero. By default the p-well potential is at ground but, by adjusting this voltage together with the substrate voltage, the depletion volume can be varied. Unfortunaly, the full depletion of the sensor is not possible without worsening the Q/C signal.

Figures 2.9(a) and 2.9(b) show the PMOS and diode reset mechanism that have been explored for the ALPIDE sensing diode. In case of reset via PMOS, the voltage of the n-well is pushed to reset voltage by using VRESET_P whilst the IRESET defines the maximum reset current. This



(a) PMOS reset mechanism.

(b) DIODE reset mechanism.

Figure 2.9: Sensor cross section and the two possible implementation of the reset mechanism.

scheme allows to adjust the reset time simply changing the IRESET current but the layout is not compact. Viceversa, the diode reset mechanism is made by placing a reset diode in a p^+ implant in the n-well collection diode. In this way it is possible to push the sensing diode at the correct reset value by forward biasing the reset diode through VRESET_D. Despite of the very compact layout, this kind of reset has a fixed time constant of about 10^{-3}s [27].

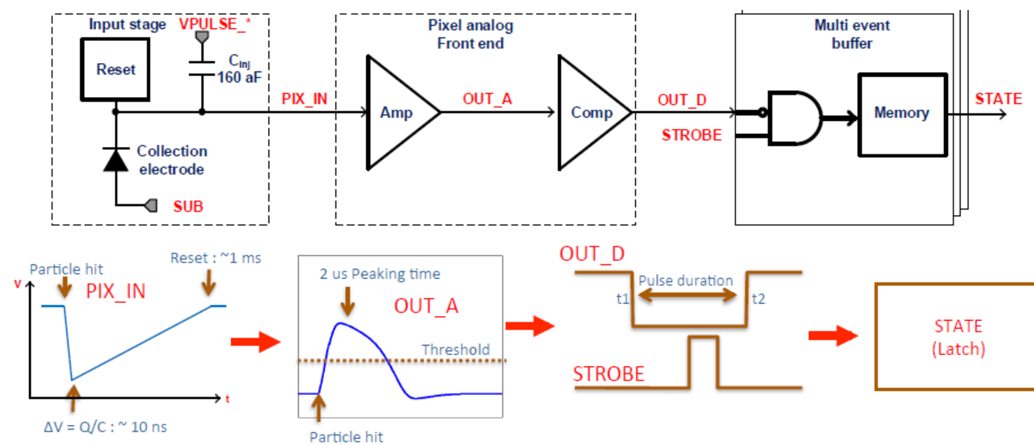


Figure 2.10: Principle of operation of the ALPIDE front-end with a schematic view of the signal processing [13].

The time evolution of the signal processing is resumed in Figure 2.10.

Whatever will be the reset mechanism, the collection diode is continuosly reset with a time constant of $\sim$ 1 ms for the baseline voltage restoration. The signal charge Q_{IN}, due to a traversing particle, is converted in a voltage signal by means of the input capacitance C_{IN}. This voltage value is integrated by the shaping amplifier with a $2\mu s$ of peaking time and the output OUT_A feeds the comparator input to generate the binary information after the comparison with a threshold voltage value. The active low output OUT_D of the comparator is put in coincidence with an external STROBE signal to a multi-event buffer, i.e. to the digital part of the front-end, where the hit information is stored until to be red-out. The STROBE signal is related to an external trigger but the circuit can be operated also in continuous mode by asserting the STROBE continuously. Finally, the multi-event buffer sends the pixel state register (STATE signal) to the priority encoder. The discrimination circuit is based on a non linear current comparator which works with 20 nA of current. The transistors in the analog part of the front-end work in weak inversion thus reducing the power consumption. This scheme correspond to a ultra low power circuit since it consumes only 40 nW/pixel with a 1.8 V power supply.

2.4.2 In Matrix data compression: the Address-Encoder and Reset-Decoder

Once the signal is stored in the multi-event buffer it will wait to be read-out from the Address-Encoder-Reset-Decoder (AERD). Since the requirements of the ITS upgrade about a low material budget, a reduction of the integration time and a improved detector read-out rate capability, call for a low power and a fast read-out technique, the asynchronous AERD has been designed to perform a data compression in the matrix. In fact, this method represents a way to overcome the limitation of the typical rolling-shutter architecture for which the intregration time depends on the number of rows that has to be read at each clock ferquency [28]. In case of the ALPIDE chip, data compression is made by a data driven read-out architecture with a zero suppression logic. This circuit is based on an arbitration tree which reads only the hit pixels, forwards down to the chip periphery the address of those pixels and propagates back a signal to reset them. The entire matrix is arranged in 512 double-columns, each sharing an AERD, and the pixel are indexed like shown in Figure 2.11. The front-end architecture (2.4.1) together with the AERD implement a read-out scheme which disentangles the signal integration time from the matrix read-out time [29]. The AERD arbitration tree structure is organized in hierchical levels made of the same basic blocks shown in Figure

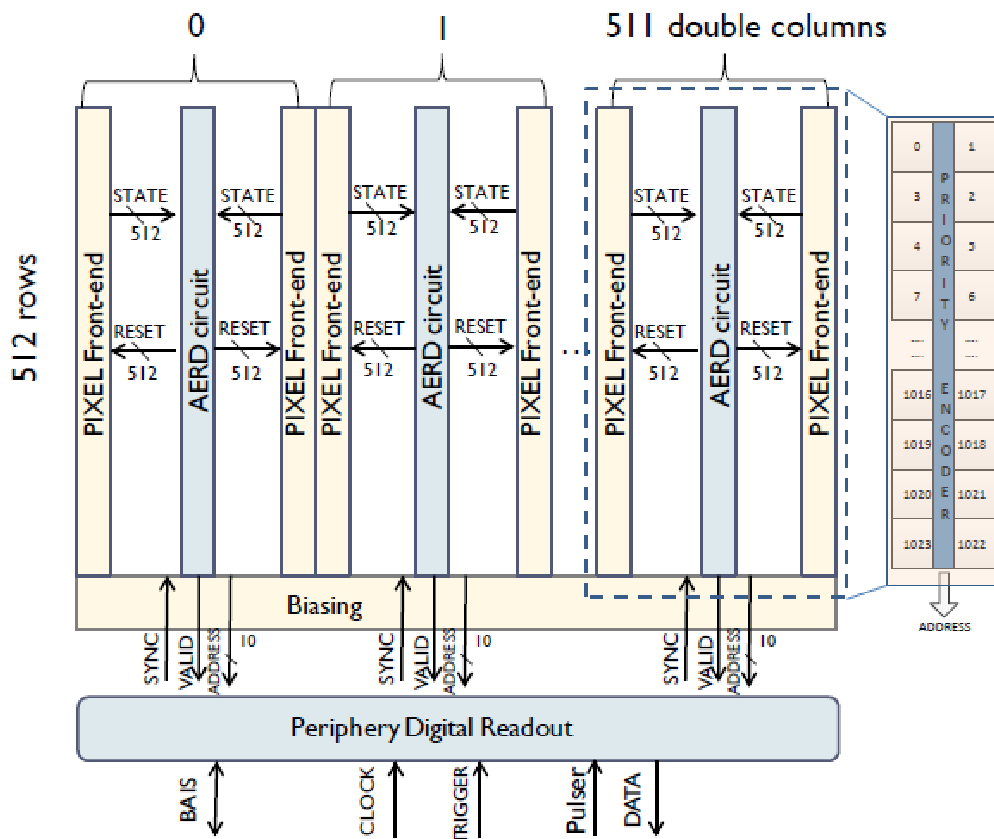


Figure 2.11: ALPIDE chip structure. The 512 double column share a priority encoder being indexed in a twisty way. Upon the address of the hit pixels is read-out, the information is sent to the pixel chip periphery to be handled.

2.12. The fundamental components of the AERD basic block are:

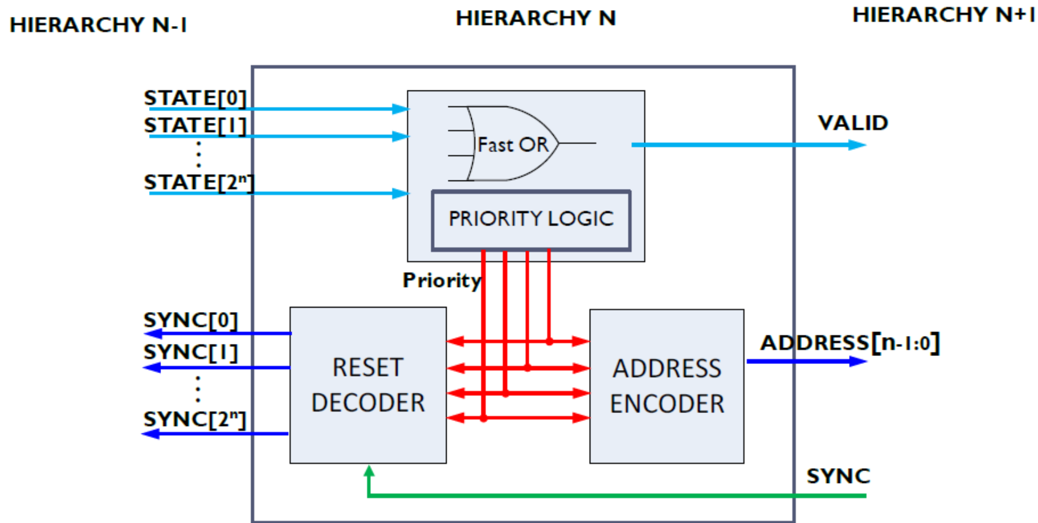


Figure 2.12: Basic block of a AERD hirarchical level.

- **Fast OR and Priority logic**. This block inputs the STATE signals from the pixel front-end. When at least one pixel is fired, the Fast OR gate circuit generates the VALID signal and propagates it from the lowest to the highest level in the hierarchy up to the chip periphery whilst the priority logic outputs feed the Address-Encoder and the Reset-Decoder circuits. The VALID signal is always active during the read-out phase.

- **Address Encoder**. This circuit is implemented using a three-state logical circuit which encodes the hit pixels and sends the address to the chip periphery. Here the address bus is controlled by the SYNC signal which is synchronous with the clock and enable or disable the output states of each block.

- **Reset Decoder**. Once the fired pixel are localized, they have to be reset. For this reason the SYNC signal propagates back from the chip periphery to the highest level during the read-out phase. This block generates also a SYNC signal which is propagated to the lowest levels of the hierarchy where it is combined with the priority logic outputs to reset only the pixel with the highest priority along the same clock cycle.

At the bottom of the pixel matrix, the End-of Column (EoC) circuit receives the ADDRESS and VALID signals. The ADDRESS is there propagated during half a SYNC cycle, when this signal is high, and the circuit provides to compresses and de-randomizes data. The addresses compression is based on the fact that the pixels which are fired by a traversing particle form a cluster, then the addresses of the pixels are almost consecutive [10]. Once the indexing of the hit pixel is trasmitted to the EoC, those pixel will be reset during the falling edge of the SYNC. In the remaining of the SYNC cycle, when the signal is low, the VALID signal and the internal signals are set to prepare the next hit pixel to be read.

DACs for the voltage and current references of the pixel and for the threshold of the front-end are also host in the EoC above the circuits for compressing and derandomizing data.

With the aim to reduce the power consumption and area occupied by the AERD logic, the address of the hit pixel is indexed at each level [29]. The number of levels in the hierarchy, the number of blocks in each level as well as the number of routing channels for the hierarchical signals (VALID, SYNC) depends on the number of pixel N_{pix} that have to be encoded as follows:

$$N_{Layer} = log_b(N_{pix}) \tag{2.12}$$

$$N_{block} = \sum_{i=1}^{log_b N_{pix}} \frac{N_{pix} - 1}{b - 1} \tag{2.13}$$

$$Routing = [log_b(N_{pix}) - 1] \times b \tag{2.14}$$

$$\tag{2.15}$$

In those formula the parameter b represents the number of inputs of the basic block. It has been demonstrated that b = 4 is the best value to decode 1024 pixels, i.e. 512 pixels for each column in the double-column arrangement. Actually, b = 4 minimizes the number of routing channels and transistors needed to implement the AERD and which mainly contribute to the area coverage [29].

Looking at the power consumption to read the entire matrix, it stops to 24 mW when the hit density is only the 0.1% at high read-out speed of 40 MHz. The EoC DACs consume about 720 μW whilst a power consumption of 211 mW is attributed to the memories in the digital periphery when a continuous clock is applied. However, by using a clock gating, the memories contribution to the power consumption can be reduced down to 700 μW.

2.4.3 Chip Periphery: Data Transmission blocks

Figure 2.8 shows that the ALPIDE chip periphery is located to the edges of the chip.

The digital part of this periphery contains memories and configuration/ status registers which are Hamming protected against the SEU effect. The **CHIPID[6:0]** port allows to select the operating condition of the chip. Actually, the same ALPIDE chip will equip all the 7 ITS layers and it will be operated as a Inner Barrel Module chip, a Outer Barrel Module Master chip or Outer Barrel Module Slave chip. Furthermore, this port provides an address to the chip for the slow control transactions [25].

The control interface is a Multipoint-Low Voltage Differential Signaling (M-LVDS) transceiver which is used to distribute the configuration settings, the trigger, the clock and the synchronous signals. It also provides access to the internal chip memories and registers. This interface works at 40 MHz and/or 80 Mb/s.

To send data out of the chip at the terget speeds of 1.2 Gb/s for the Inner Barrel Module and 400 Mb/s for the Outer Barrel Module the chip periphery is equipped with a high speed serial link which is made by a 600 MHz clock multiplier Phase Locked Loop, a Double Data Rate serializer and a pseudo-LVDS driver. This link is called Data Transmission Unit (DTU) and drives the data from the sensor periphery to a external patch panel.
A detailed description of the read-out circuits as the M-LVDS and the DTU will be presented in the next chapters. Indeed, those custom circuits are the responsible of the ALPIDE slow and high speed data transmission. Then, the characteristics of the blocks together with the simulation and test results to verify that they are a suitable option for the ITS upgrade will be illustrated.

Chapter 3

ALPIDE chip Data Transmission

The ALPIDE chip periphery hosts those circuits which are necessary to link the ITS with an external Read-out Unit (RU) placed on a patch panel. There, the Data Acquisition, Trigger and Detector Control systems, process data coming from the tracker and send the clock, the trigger and the slow control signals to the chip.

After the LS2, the ALPIDE chips will equip each of the 7 ITS layers. Even if those chips are equal from the read-out point of view, the speed at which the Inner Barrel (IB) chips transmit data to the RU and their arrangement along the IB layers are different from the Outer Barrel chips. This is due to the fact that the inner layers deal with a hit density greater than the outer layers. In any case, the data transmission is made by the same units for all the ITS pixel chips. For this purposes, a Data Transmission Unit (DTU) and a Multipoint - Low Voltage Differential Signaling (M-LVDS) transceiver are located in the pixel chips periphery. The high speed and low speed transmissions are made by differential devices since they are less susceptible to the electromagnetic interference (EMI) and ground loop noise.

The DTU is a custom serial link made by a 600 MHz clock multiplier Phase Locked Loop (PLL), a serializer which works in Double Data Rate and a pseudo-LVDS driver with pre-emphasis.
This driver is the unique active component in charge of transmitting data from the tracker to the RU. It has to drive a full 5.3 m - 6.5 m long hybrid transmission line, called e-link, from the IB and OB layers respectively. In addition, data from the inner layers have to be output at 1.2 Gb/s for the IB chips and 400 Mb/s for the OB chips. Those data rates ensure that the chips matrices are fully and efficiently read.

The pseudo-LVDS driver has been equipped with a pre-emphasis driver.

This last driver enhances the main driver strength turning into be essential to ensure a good data transmission quality over the full transmission line at the target data rates.

The clock, the slow control signals and any kind of signals synchronous with the clock are broadcast through the custom M-LVDS transceiver. This is a bidirectional I/O unit consisting of a driver and a receiver thus allowing the chips to send data or to receive them from chip-to-chip and Module-to-Module communications and from the data exchange between the ITS layers and the patch panel. Although the M-LVDS has to drive the same e-links as the pseudo-LVDS driver, the speed at which this transceiver works is limited at 40 MHz or 80 Mb/s. Here the pre-emphasis is not necessary but a good transmission quality has to be guaranteed.

The aspects of major relevance for the data transmission are the signal integrity and power consumption. For this reason, compromises between those two perspectives have been investigated in the design phase of the pseudo-LVDS driver and the M-LVDS transceiver.

The implementation of the data transmission circuits of the ALPIDE pixel chip is the topic of this chapter. In the following, the design of both units will be treated after a general overview of the ITS layers arrangement. It has to be pointed out that those circuits have been fully simulated during the design phases by considering the temperature, process corners and mismatches which can threaten the circiuts operation. The simulations and test measurement results will be addressed in the next Chapter.

3.1 Output Data Rates - Overview

In Chapter 1 has been shown that the current ITS layers have been equipped with different type of silicon detectors technology, according to the hit density of each layer and the their commitements (tracking and/or partcicle identification). Since the new ITS will not have the particle identification feature, only the binary information on the hit/not hit pixel will be provided by each pixel chip. With this aim, the ALPIDE pixel chip will cover the seven layers of the upgraded tracker, despite of the difference in the hit densities. However, compared to the current ITS, this design choice entails a higher granularity for the outer layers of the new ITS.

The layout of the new silicon tracker maintains the angular coverage constant with respect to the interaction point. For this reason, the length of the layers increases with their radii. On the other hand, the physics simulations show that the hit density per layer decreases with the distance of the layer from the interaction point and indicate the data througput for

Table 3.1: Layout of the upgraded ITS and hit densities per layer for Pb-Pb and p-p interactions [30].

		Inner Barrel			Outer Barrel			
	Layer	0	1	2	3	4	5	6
	Radius (mm)	22	31	39	196	245	344	393
	Length (mm)	271			843		1475	
	# Chip	108	144	180	2464	3136	7840	9016
Pb-Pb	Prim.& Sec. particles average (cm^2)	8.77	6.17	4.61	0.34	0.24	0.13	0.11
	Prim.& Sec. particles max (cm^2)	12.45	8.61	6.19	0.45	0.31	0.17	0.13
	QED electrons (cm^2)	6.56	3.39	1.84	0.01	0.00	0.00	0.00
p-p	Prim.& Sec. particles average (cm^2)	0.08	0.05	0.04	0.00	0.00	0.00	0.00
	Prim.& Sec. particles max (cm^2)	0.11	0.07	0.05	0.00	0.00	0.00	0.00

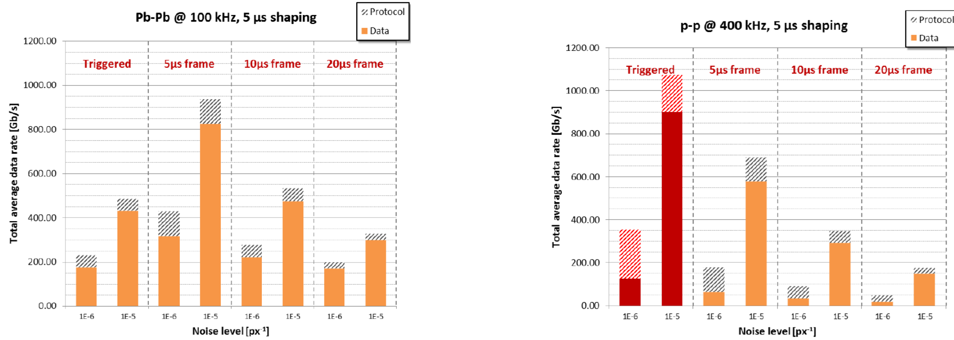
the entire ITS [10].

Table 3.1 shows the hit density for Pb-Pb and p-p interactions for minimum bias events. Those calculations take into account even the secondary particles produced in the interaction with the material and the QED background in case of Pb-Pb collisions. The hit densities for Pb-Pb interactions are calculated considering an integration time of 10 μs, an interaction rate of 50 KHz and a magnetic field of 0.2 T.

To be thorough, the calculation of total data rates expected for each layer has to account for the sensors noise and the data protocol overhead. Actually, a certain number of fake hits will be produced on the pixel matrix depending on noise level and they have to be processed. Furthermore, some extra data not containg useful informations about the physics events are required to monitor the transmission and the protocol adopted for the data exchange. The overhead consists in those additional data and it asks for an additional bandwidth depending on the detector operating condition (particle interacting and noise level) and from the protocol itself.

Simulations for the data rates of Pb-Pb and p-p interactions have been done considering that the sensor can be operated in triggered or continuous mode (2.4.1). For the operation in triggered mode 2, 5 and 10 μs shaping times have been adopted whilst in continuous operation mode the 5, 10 and 20 μs frame widths have been selected. Furthermore, the worse and the best

case of noise level, i.e. 10^{-5} and $10^{-}6$ px^{-1}, have been considered.
Figures 3.1 show the simulations results on the total average bandwidth necessary to fully read-out a pixel matrix for the target interaction rates of 100 kHz for Pb-Pb collisions and 400 kHz for the p-p collisions after the LS2. Here, a shaping time of 5 μs has been adopted, since the difference with respect to the 2 μs shaping time of the ALPIDE chip front-end can be considered negligible. In those graphics each bar represents the bandwidth corresponding to different level of noise and different read-out scheme (triggered/continuous mode) at different frame values. The bandwidth are obtained by adding the contribution from the actual hit addresses (solid) and the one from the protocol overhead (pattern stripes).



(a) Pb-Pb interactions @100 kHz: required bandwith.

(b) p-p interactions @400 kHz: required bandwith.

Figure 3.1: ITS data throughput for Pb-Pb and p-p expected interaction rates. The bars are related to the triggered and continuous operation mode of the sensor. Those results are obtained adding the bandwith needed to tranmsit the hit addresses (solid) and those used for the data protocol overhead (pattern stipes) [30].

The results in Figure 3.1 indicates that to efficiently read the pixel matrices a bandwidth of circa 1.2 Gb/s is necessary for both types of interactions. Those bandwidth value holds at least for the IB layers. Indeed, the physics simulations have been shown that a data rate of 400 Mb/s is appropriate to read the OB pixel chips because of the much lower hit densities.
As a final remark, the red bars in triggered mode for the p-p collision show that the ITS does not support a 5 μs of trigger frequency.

3.2 ITS layers layout

The results presented above have been the guidelines for the design of the detector layers layout and have indicated how to send data from different layers to the patch panel.

The main difference between the IB and OB layers is the chips connection topology. Since the IB chips have to deal with a much higher data rate than the OB chips, an advantageous solution to minimize the number of links, and then the material budget, is to allow that each IB chip drives its own link. On the contrary, the OB chips are connected to parallel bus to send or receive information at 80 Mb/s in a point-to-point connection.

Based on the previous considerations, the IB layers are organized in Staves, each of them containing 9 chips in a row. Insteed, the OB layers are arranged in Half Staves containing a variable number of pixel chips which assemble the HICs. Those topologies indicate the way in which the Flex Printed Circuits (FPC) have to be designed for the chips interconnections. Furthermore, they have an impact on the e-links physical lenght.
As said before, the physical connection between the ITS layers and the patch panel is done by the e-links which are hybrid differential transmission lines consisting of the custom made FPC linked to the Samtec AWG30 Twinax Firefly cables. Once more, the requirements on the material budget minimization inside the detector have stated the material for the FPC production. Indeed, more resistive Aluminium (Al) has been preferred for the IB FPC since its radiation length is lower than the one of Copper (Cu) which, however has been selected for the OB FPC.

Depending on the layer that they are connecting, the lengths of the e-links vary by reaching a maximum of 5.3 m for the IB layers and 6.5 m for the OB layers when the 5 m long Samtec cable is considered (see Table 3.2).

3.2.1 IB layers Staves connection topology

The pixel chips arrangement of the layers from 0 to 2 is represented in Figure3.2. Here the FPC has to host nine chips which are read-out in parallel. and then it has to contain at least eleven differential lines [10]. This number comes from the consideration that to transmit data at the highest data rate of 1.2 Gb/s each chip has to drive its own differential high speed link. However, the slowest signals like the clock (CLK) as well as the configuration settings (CTRL) need another differential pair each. Furthermore, the supply planes have to be added.

The FPC used in the Inner Layers is 15 mm wide and about 300 mm long. The physical length is set by considering that a Inner Layer FPC has

Table 3.2: Transmission Rates and Layout of the ITS Layers. The number of the E-link represents the minimum number of links necessary to transmit data from the entire layer by taking into account the data load of the layer and the data transmission speed.

	Inner Barrel			Outer Barrel			
	Inner Layers			Middle Layers		Outer Layers	
Layer	0	1	2	3	4	5	6
#Modules	–			4		7	
FPC Length (mm)	300			850		1500	
Transmission rate (Gb/s)	1.2			0.4			
# E-link	108	144	180	96	120	168	192

to host nine chips in a row which are separeted one from each other by 150 μm pitch.

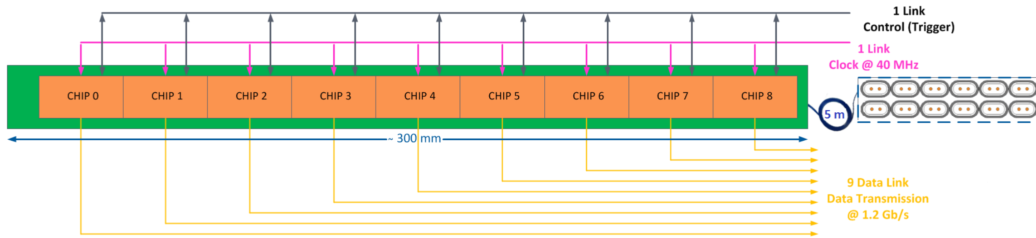


Figure 3.2: Inner Barrel layers arrangement. Each of the nine chips equipping a inner layer Stave has it own high speed differential link (yellow arrows) to the patch panel. Two additional shared differential links are used to distribut the clock (magenta arrow) coming from the RU along the Stave and broadcast the control and trigger signals (grey arrow) between the Stave and the patch panel.

3.2.2 OB Layers Half Staves connection topology

In the last version of the OB Layers, the OB chips are grouped in the Half Stave for which the basic unit is the HIC and the carbon plate will not be used anymore. However, for consistency with the Technical Design Report (TDR) [10] the basic unit will be called Module in the following of this thesis. A Module is made up of 2 rows of seven chips each. From the point of view of the power distribution, each row is considered indipendent and make up a daisy chain. Even if in each row the pixel chips are identical, it is possible to identify between them a Master and six Slaves. In this topology a Slave communicates only with the two nearest chips whilst the Master is

the only chip able to communicate with its Slave, with the other Masters and with the patch panel. It has to be pointed out that by using the slow control signals it is possible to switch the functionality of each chip, allowing a Slave to become Master and viceversa [10]. Actually, the major difference between a Master and a Slave is that the former is enabled to send the high speed data to the patch panel.

With this arrangement, each Module contains two Master chips, one per row, which are used for the Module-to-Module communication, for the high speed data transmission of a Module and for the chip-to-chip communication inside a Module itself. In the last case, the Master chip receives a clock or a slow control signal and provide to distribute it to the Slaves.

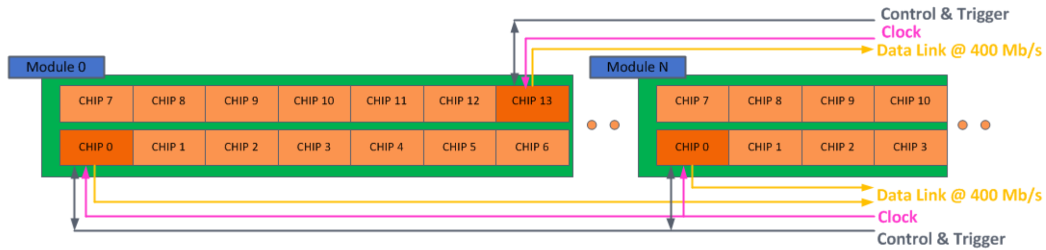


Figure 3.3: Example of Module-to-Module communication. The Masters chip (orange) is the only one in a Module to be physically linked to the patch panel for the high speed data transmission (yellow arrows). In a Half Stave the Modules are connected via seven indipendent links and share the clock (magenta arrow) and slow control (grey arrow) lines.

As summarized in Table 3.2, the Middle Layers count for four Modules whilst the Outer Layers are made up of seven Modules, the difference being due to the Half Stave length.

In the Half Stave there are 7 indipendent links with the RU whilst for each Module there is a bus made up of 4 single ended lines for the point-to-point connections at 80 Mb/s. Therefore, each Master chip of a row Module sends the data out of the Half Stave indipendently.

The OB FPCs are about 210 mm long and 31 mm wide. They are linked by the flex bridge soldering to cover a Half-Stave and for this reason a carefull design of the flex printed circuit was done in order to minimize the number of reflections inside the cable and the transmission quality.

3.3 LVDS and M-LVDS transmission protocol

The Data Transmission Unit (DTU) and the Multi-point Low Voltage Differential Signaling (M-LVDS) transceiver are in charge for the data exchange between the ALPIDE chip periphery and the external patch panel.

The commitment of the DTU is to send data out of the chips at the target speeds of 1.2 Gb/s (IB) or 400 Mb/s (OB). This custom serial link is made up of a 600 MHz clock multiplier Phase Locked Loop (PLL), a fast Double Data Rate (DDR) serializer and a pseudo-LVDS driver. This last circuit is the unique active component which has to drive the long hybrid differential lines doing a point-to-point communication of binary signals for an overall distance of 5.3 m (IB) and 6.5 m (OB). It has to ensure a good transmission quality at the end of the e-links and for this reason it has been equipped with an ancillary pre-emphasis driver to enhance the driver strenght of the high speed output.

The M-LVDS transceiver is involved in different tasks concerning chip-to-chip and Module-to-Module communications taking place at the speeds of 40 MHz or 80 Mb/s. This block consists of a driver and a receiver based on the LVDS protocol. Even for the transmission of those slow signals the differential long e-links are used, having a length of 6.5 m in the worse case. Because of the connection topology, more than one M-LVDS transceiver load up a transmission line and then the M-LVDS driver has more driver strength than the pseudo-LVDS one.

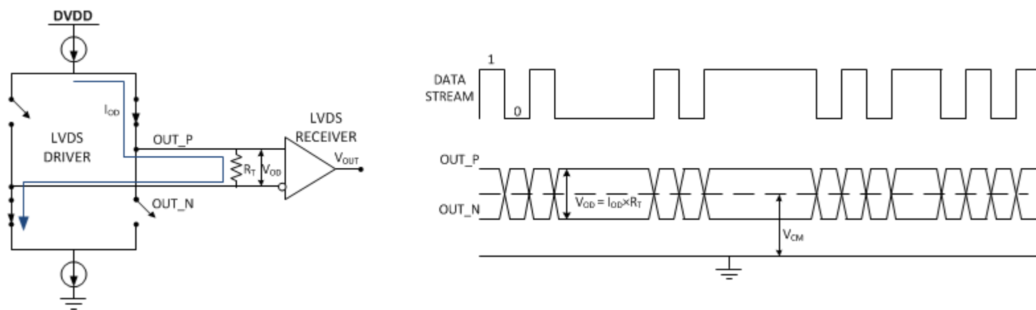


Figure 3.4: LVDS system working principle.

3.3.1 LVDS and M-LVDS protocols

The Low Voltage Differential Signaling (or LVDS) is the most popular standard for differential binary data transmission used to broadcast data, timing

and control signals at high speed rates. Indeed, this protocol allows fast transmissions at low power consumption.

Basically, a LVDS transmission system consists of a driver and a receiver, linked by a pair of balanced wires. The two wires are terminated at the receiver side by a 100 Ω resistor. This resistor counteracts signal reflections at the receiver ends since it has to match the characteristic impedance Z_0 of the transmission lines. Furthermore, the receiver will react only to the voltage drop across this resistive load.
The driver can work in voltage mode or in current steering mode. In both cases the output voltage swing V_{OD} and the common mode value V_{CM} are the key parameter for the receiver [31]. Since for the ALPIDE chip a current steering mode driver has been designed, the following discussion will be centered on those kind of transmitter.

A LVDS driver working in current steering mode is represented in Figure 3.4 with the definition of the output voltage levels. This differential transmitter is made up of a current source on the top, a current sink on the bottom and four switches paired on the two diagonals. These two pairs of switches are opened and closed alternetively to steer the current direction from/to the inverting (OUT_N) and not inverting (OUT_P) transmitter outputs. The current I_{OD} flowing out from the driver goes through a well defined path, thus generating the output voltage levels at the ends of the termination resistor R_T defined as:

$$\begin{cases} V_{OH} = V_{CM} + \frac{1}{2} V_{OD} \\ V_{OL} = V_{CM} - \frac{1}{2} V_{OD} \end{cases} \tag{3.1}$$

A logic 1 is transmitted when OUT_P>OUT_N whilst a logic 0 corresponds to OUT_P<OUT_N.

The electrical characteristics of the LVDS transmission protocol are reported by the standard ANSI/TIA/EIA-644 and listed in Table A.2. This standard indicates the ranges in which the output voltage values, the output common mode and the short circuit currents can vary. There is not an explicit limit on the transmission speed since it is application dependent. A maximum signaling rate is set by the driver transition time characteristics, the transmission lines characteristics, the distance at which data have to be sent and the required signal quality [33]. Conversely, the protocol gives an upper limit of 30% of the Unit Interval (UI) to the driver rise/fall time to guarantee a good transmission quality. Typical current values for the LVDS driver range between 2 and 4 mA, thus producing an output voltage swing in the range 200 and 400 mV. Usually, a LVDS driver is operated at 2.5 V or even higher power supply so that the output common mode is set around

1.2 V.

The LVDS receiver has an input common mode ranging between 0.05 V and 2.35 V, allowing a ±1 V ground shift between the driver and the receiver. A difference of 100 mV at the receiver inputs corresponds to the transmission of a logic 1 whilst a logic 0 is transmitted when the receiver input difference is -100 mV. The standard also requires a 20 μA of input leackage current.

While the LVDS standard is mainly used for point-to-point connection, the M-LVDS standard ANSI/TIA/EIA-899 allows a multi-point connection of a certain number of transceivers on the same bus, as shown in Figure 3.5. The working principle of this kind of system is the same as the LVDS one but here the presence of multiple drivers and receivers makes the difference. First of all, the presence of multiple receivers calls for a double termination of the transmission lines to avoid the propagation of signals reflections. Here two 100 Ω termination resistors are used and then, to obtain the same voltage swing of a LVDS system, the current flowing out from a M-LVDS driver needs to be doubled. Furthermore, this topology allows for a bidirectional

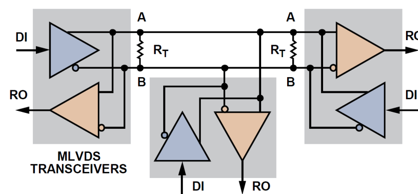


Figure 3.5: Multi-point Low Voltage Differential Signaling (LVDS) topology. Multiple transceivers are connected to the same bus. This topology is adopted for a bidirectional half-duplex connection [34].

half-duplex communication on the lines.

The principle of operation is similar to the "walki-talki" radio. This means that only one driver at a time is allowed to broadcast data along the wires whilst every receiver on the same channel is able to acquire the informations. Only when a driver stops to talk, another enabled driver can start to transmit. To obtain this, a M-LVDS driver designed as a trhee state buffer which will be enabled or disabled to avoid communication contention on the bus. Slew-rate limited drivers are often implemented for the M-LVDS purposes since the multi-point topology is characterized from additional impedance discontinuities due to multiple transceivers and stubs. Actually, the slew rate control enhance the robustness of the signaling limiting the overshoot and undershoot of the signal during a bit transition. Because of the slew rate limitation, M-LVDS transceivers are more suitable for lower data rates than the LVDS.

M-LVDS receivers characteristics account for multiple loads on the transmission lines. Even in this case the standard requires 20 μA at maximum of input leakage current over an input voltage range wider than the LVDS one. However there are 2 categories of M-LVDS receivers, Type-1 and Type-2 receivers. The former is characterized by a ±100 mV of input threshold whilst the second has a narrower threshold of ±50 mV.

For high speed as well as slow speed data signaling, a differential transmission protocol has been chosen for the ALPIDE pixel chip. In Figure 3.6 the location of data transmission circuits is indicated.
Actually, a differential transmission is more robust than the single-ended one in terms of protection against noise and electromagnetic interference (EMI) disturbances.
A trasmitter and a receiver connected by a single wire in a single-ended transmission system need to share a common reference voltage to allow the current to flow in a complet loop and this is a point of weakness of this kind of systems. A common reference voltage generates impedance coupling, simultaneous switching noise and ground shift disturbances which alter the voltage at the incoming receiver wire influencing the transmission itself [17]. Those disturbances are minimized in case of two wires connection, like in the differential transmission, since a reveiver reacts to the difference between its inputs. The current in the two wires has the same magnitude but it flows in opposite directions along the outband and return paths. In this way, the transmission is immune from any kind of noise which shifts the voltages on the two wires in the same direction. Indeed, the noise will be cancelled out in the difference and the same will be true for the magnetic fields generated from the currents between the two transmission lines.

3.4 Slow speed data transmission: M-LVDS transceiver implementation for the ALPIDE pixel chip

As said before, the M-LVDS transceiver is implemented in ALPIDE for chip-to-chip and Module-to-Module communications. The pixel chips have two indipendent M-LVDS devices used for the distribution of the 40 MHz clock, and the broadcasting of the trigger and configuration settings. Each chip acts like a master in the IB Module, thus receiving those signals indipendently from the RU and providing to distribute them at the other circuits in the chip. In a OB Module, the Master chips not only deliver the slow speed data inside the chips but, after a regeration, they circulate every data from the

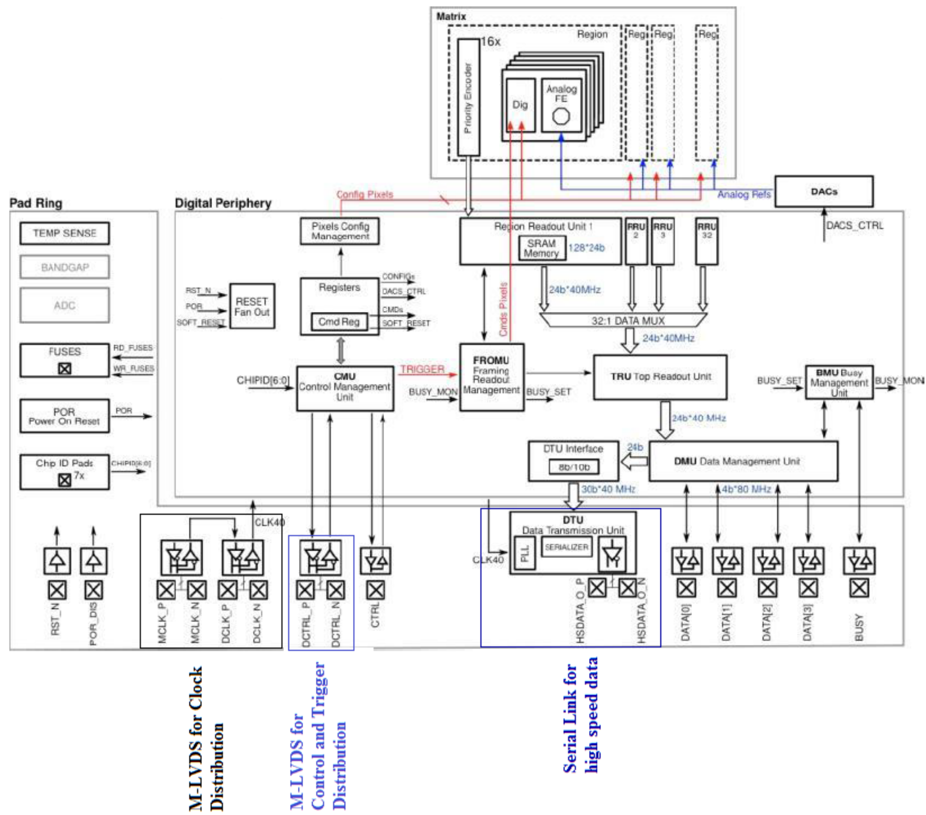


Figure 3.6: ALPIDE 3 pixel chip. In the southern part of the chip periphery the M-LVDS transceivers toghether with the DTU are highlighted.

RU to the Slaves.

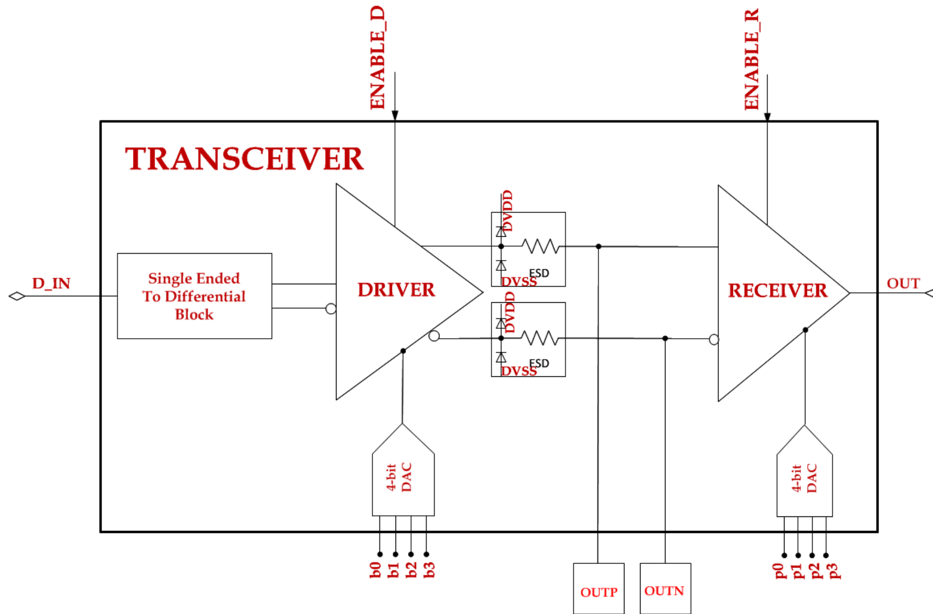


Figure 3.7: Transceiver Block Diagram. The driver and the receiver are internally linked. Bot the driver outputs and the receiver inputs are protected against the electomagnetic discharge (ESD) by using the protection diodes with a resistor. As an example, here only the ESD protection for the drive outputs are shown.

The transceiver block diagram is illustrated in Figure 3.7. It consists mainly of a driver and a receiver which are internally connected. A single ended-to-differential (STD) block provides the driver the differential inputs with the two phases of the same signal, according to the transmission topology. Finally, two 4-bit DACs set the currents respectively for the driver and the receiver. The layout view of the overall system is shown in Figure 3.8 where some components are highlighted. The total area occupied by this transceiver block is 1200×120 μm^2. All blocks are designed using the 0.18 μm CMOS Imaging Sensor technology by TowerJazz with a power supply of 1.8 V. The transmitter and the receiver design is based on the M-LVDS protocol. Actually, those circuits have been implemented to meet the M-LVDS specifications but bearing in mind the ITS chip power consumption requirements and the use of a 1.8 V power supply which is lower than the typical 2.5 V value.

The ITS chips have to be able to transmit and receive slow speed data without causing gridlock to the broadcast. Actually, with the clock exception, the communications between chips, Modules and with the RU are bidirectional. Furthermore, it is possible for a Slave to become Master and vicev-

ersa. Then, to implement a half-duplex topology the ALPIDE chip M-LVDS transceiver is a three state buffer that can be enable, disabled or stay in high impedance mode.
In a chip-to-chip or a Module-to-Module communication each receiver has to be able to receive the broadcast signal and transmit it to the other chips in the system. The designed receiver is sensible to the low differential input voltage and regenerate it with a full CMOS swing output. However, the receiver output can be fixed to a defined voltage value if an idle bus condition occurs. In this way, the receiver output is prevented to make transitions between any voltage level thus limiting undesired power consumption.

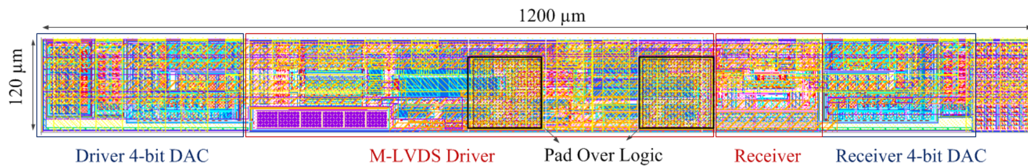


Figure 3.8: M-LVDS transceiver layout. The overall block contains the driver, the receiver, the two 4-bit DACs for the current settings, two Pads Over Logic for the connection with a differencial FPC and some decoupling capacitors (not highlighted).

3.4.1 M-LVDS Driver

The first implementation of the M-LVDS driver integrated on the second ALPIDE prototype is illustrated in Figure 3.9. This is a slew-rate controlled driver circuit based on [35] which has been implemented in a similar way for the LVDS purposes in [36]. In this case the power supply DVDD is fixed to 1.8 V and then the output common mode voltage has been fixed to V_{CM}=1.1 V to allow the transistors to work in their correct point of operation.

The driver output current I_{OUT} ranges between 2 mA and 8 mA thus producing a voltage swing between 100 mV and 400 mV across the $100\Omega||100\Omega$ termination resistor. The tolerance on the resistance value is $\pm10\%$.

A suitable value for the current is set by the 4-bit DAC. This device fixes the gate voltages of tranistors M_{P1} and M_{N1} so that the current of the PMOS is always half of the current of the NMOS. The remaining half of I_{OUT} is released by the common mode feedback circuit (CMFB) through M_{P0}.

The CMFB circuit is a NMOS differential pair loaded by two diode connected transistors. The two inputs are connected to the fixed voltage V_{CMREF} = 1.1 V and to the output common mode voltage V_{CM} respectively. This last node can be different from 1.1 V and then the CMFB circuit

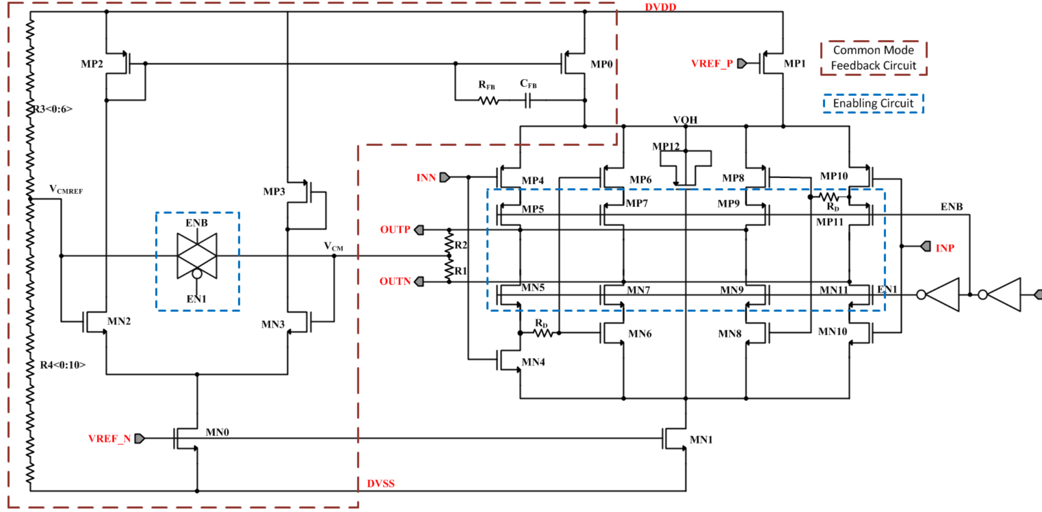


Figure 3.9: M-LVDS driver schematic.

generates a feedback loop adjusting the bias current of M_{P0} to restore the exact common mode value. The $R_{FB} - C_{FB}$ series compensates the CMFB loop frequency response to guarantee the overall system stability.

In the schematic in Figure 3.9, the driver is implemented with two non-linear differential pair MOS current switches, i.e. with two transconductors. The main one is obtained with transistors M_{P4}, M_{N4}, M_{P10} and M_{N10} which are paired along the two diagonals. Their gates are opened and closed alternatively by the full CMOS signals INP and INN and they steer most of the current in the transmission line. Furthemore, they feed the inputs of the second non-linear differential pair formed by the paired transistors M_{P6}, and M_{N8}, M_{P8} and M_{N6}. Those internal switches drive the remaining amount of current with a short delay set by the product between the resistor R_D and the total input capacitance C_D. While the resistor value is fixed, the capacitance depends on the $M_{N7,9}$ and $M_{P7,9}$ transistor sizes. The addition of two inner paired switches is a solution to control spikes as well as ringing which are due to several non-idealities in the circuit. In particular it helps against overshoots or undershoots which can affect the driver output voltages by lowering the output transconductance.

During the transition, before the second transconductor is completely switches, the transfer function of the circuit is:

$$\frac{V_{OUT(s)}}{V_{IN(s)}} = \frac{G_{m1}(1 + R_D C_D s)}{b_0 + b_1 s + b_2 s^2 + b_3 s^4} \tag{3.2}$$

In this formula, G_{m1} is the transconductance value of the main non-linear differential pair of switches, i.e. the one implemented with M_{P4}, M_{N4}, M_{P10}

and M_{N10}. Coefficients b_n, n=0...3, depend on the termination resistor R_T, on the delay $R_D \times C_D$ and on the model used of the transmission line and finally from the transconductance G_{m2} of the second non- linear differential pair of switches, i.e. the one implemented with M_{P6}, M_{N6}, M_{P8} and M_{N8}. It is possible to show that the system is stable if $G_{m2} < \frac{1}{R_T}$.

The total transconductance G_m of the circuit is given by the following expression:

$$G_m(s) = \frac{I_{out}(s)}{V_{in}(s)} = (G_{m1} + G_{m2}) \cdot \frac{1 + sR_DC_D\frac{G_{m1}}{(G_{m1}+G_{m2})}}{1 + sR_DC_D} \tag{3.3}$$

Here, using a pole-zero compensation technique together with a proper ratio between the transconductances it is possible to limit the overshoot on the line.

The pass gate together with transistors $M_{P5,7,9,11}$ and $M_{N5,7,9,11}$ implement the enabling circuit. When the signal ENB is at logic 1, i.e. at 1.8 V, the driver switch from a high output impedance condition to steer the total current I_{OUT}, thus transmitting the input datastream.

The driver outputs are protected against electrostatic discharge (ESD) damages. With this purpose, ESD protections have been implemented by using two counteracting diodes and a 5 ohm resistor.

The M-LVDS driver charateristics are reported in Table A.3 in the Appendix A. To verify that this driver is suitable for the slow speed data transmission of the ALPIDE chip it has been fully simulated by modeling the chip-to-chip and Module-to-Module communications. The test bench as well as the test measurements will be reported in Chapter 4.

3.4.2 M-LVDS Driver issues

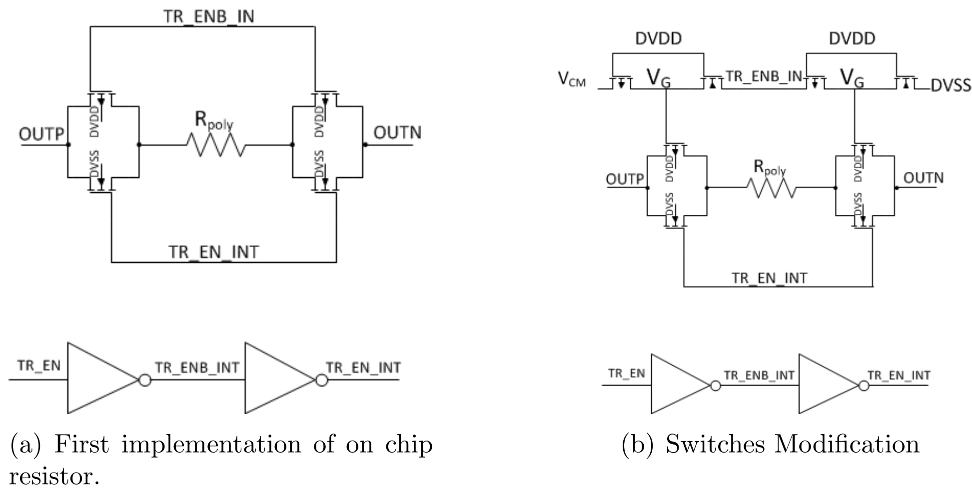
After the firts implementation of the M-LVDS transceiver, a second modified version of the driver has been implemented for the third ALPIDE prototype (pALPIDE 3) to solve the following issue:

1. **Time skew.** The signal skew is the difference in the propagation time between the two signals in a differential transmission line. When the crossing points of the two complementary signals are not symmetric a pulse skew can be originated. Actually, a system needs the same time to switch from a logic 0 to a logic 1 (t_{PLH}) and viceversa (t_{PHL}) in an ideal transmission. When a difference between t_{PLH} and t_{PHL} exists a pulse skew is defined which can entail a signal distortion.

2. **Power down of a Module.** As said in Section 3.2, each Module has its own supply planes whilst shares the differential lines with the

other Modules in a Half Stave. When one of the Module is powered off, it is still connected to the transmission lines through the M-LVDS transceiver. The differential lines are biased at 1.1 V ±0.2 V and this results in a large current in the Module which is powered off.

The digital simulations on the slow speed communications along a full OB Stave have shown that Part-to-Part skew can affect the data transmission. To solve this issue the differential internal connections between the driver outputs and the receiver inputs have been terminated with an on-chip polysilicon resistor, shown in Figure 3.10(a). This resistor can be enable or disabled through the two transmission gates at both resistor ends.
The channel resistance r_{on} of the PMOS and NMOS of the two switches contributes to the overall value of the termination resistance R_T. Since r_{on} is in series with the polysilicon resistance the value of the termination resistance R_T= (105 ±21) Ω is obtained by adding the two contributions. When R_T is active, it will terminate the differential lines closely to the receiver ends, thus minimizing the signal skew propagation.



(a) First implementation of on chip resistor.

(b) Switches Modification

Figure 3.10: On-chip termination resistor (a) is implementented to limit the signal skew. A forward bias current comes from this switch if a Module is power off, then a circuit revisione has been done (b) to limit the indesired effect.

When a Module is off, the indesired current is due to the fact that every diode connected to the differential transmission lines starts to be forward biased. Actually, even if a Module is powered off, the two driver outputs are still connected to the output voltages OUTP end OUTN which assume values in the range 1.1V ±0.2 V because of the voltage swing of another driver in a Half Stave. Then, diodes give a forward bias current.

To solve this issue it has been found a solution for each involved diode to isolate it from the lines.

- **Diodes in the ESD protections.** In Figure 3.7 DVDD is zero as well as DVSS when the Module is off. Then, diodes D1 start to conduce since the voltage difference between its terminal is greater its 0.6 V threshold voltage and a current flows from the driver outputs to DVDD.

  The idea to solve the ESD issue is to lower the voltage difference between the diode terminals under the threshold value, thus blocking the diode conduction. In Figure 3.11 is illustrated the proposed solution. D1 and D2 diodes are replaced respectively by the reverse diode D_{R1} and four forward diodes $D_{F1,2,3,4}$. In this way, the voltage drop across the forward diodes will never reach the 0.6 threshold value and then, no indesired current will flow toward DVDD.

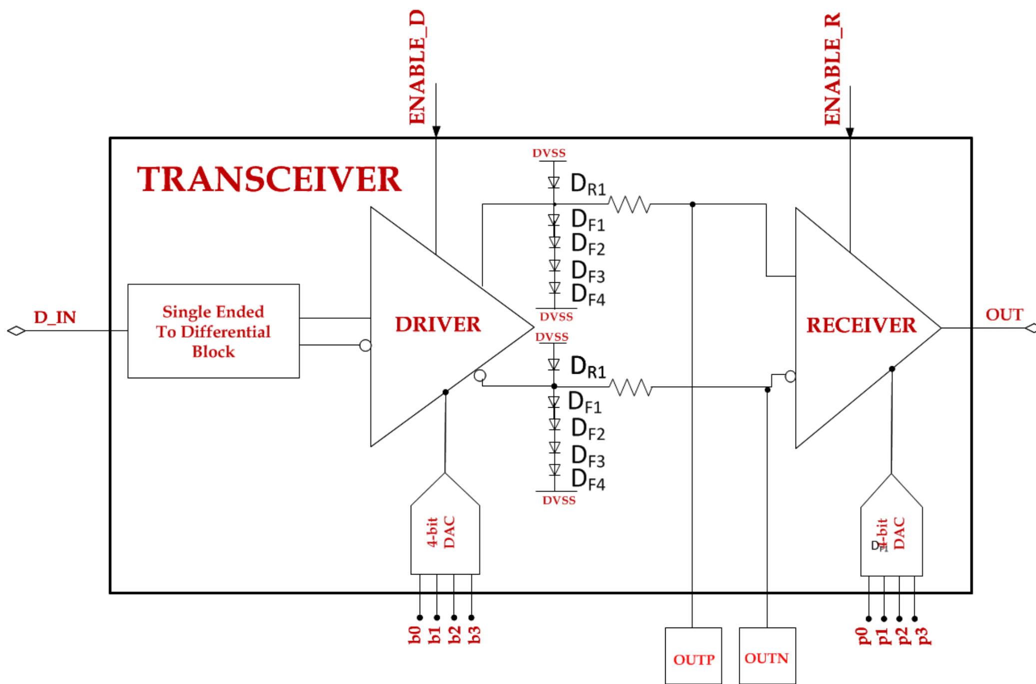
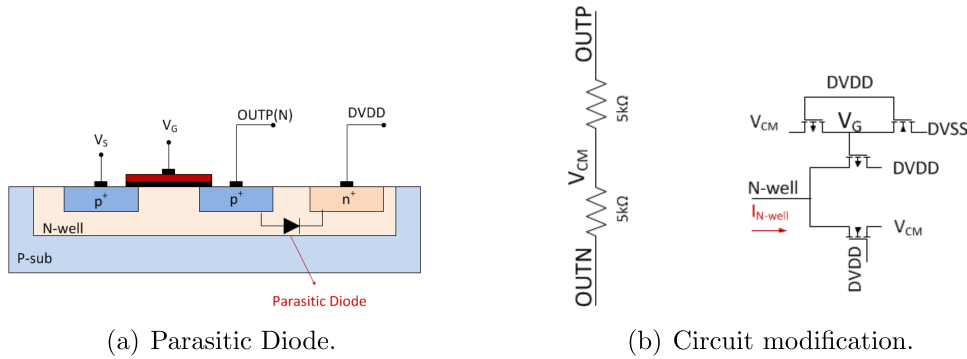


Figure 3.11: Remedy to the protection diode forward biasing.

- **PMOS parasitic diodes at the driver outputs.** Since the Module is off, even the N-well which hosts the PMOS is at 0 V. With reference to Figure 3.12(b), the parasitic diode between the nwell and the PMOS transistor drain is in conduction since it is undergone to the swing of the transmission lines at which the PMOS is connected. However, the

solution is to use a switch to connect the N-well to 1.8 V when the Module is active and to V_{CM} =1.1 V if the Module is powered down, thus avoiding the forward biasing of this parasitic diode.



(a) Parasitic Diode. (b) Circuit modification.

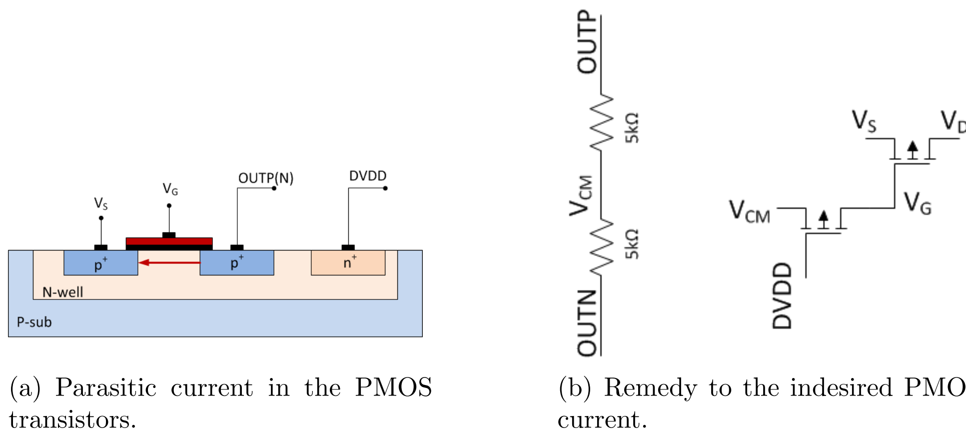
Figure 3.12: To avoid forward bias from parasitics the M-LVDS driver circuit has been with the addition of a CMOS switch to change the N-well potential.

- **PMOS transistors at the driver outputs.** Even in this case there is a current path in the PMOS channel. Indeed, the gate and source potential of this transistor will be at 0 V, whilst the drain voltage is modified by the data stream broadcast from the active Modules. To stop this current flow it is sufficient that the transistor overdrive voltage is less than 0 V, $|V_{GS}|- |V_{TH}| \ll 0$. This is obtained connecting the gate potential to the common mode voltage or to the source with the addition of the enabling circuit shown in Figure 3.13(a).

- **Switches for the termination resistor.** The switches implemented for the termination resistor have been revised to ban the current flow from OUTP to OUTN when a Module is off. Indeed, the PMOS are still in conduction despite of the fact that the NMOS are turned off by the low state of the signal TR_EN. Like in the previuos case, one needs the PMOS transistor of the transmission gate is off. This solution is implemented adding two CMOS switches on the top of the transmission gate. Indeed, when DVDD = 0 no current will flow in the PMOS transmission gate since the gate will be connected to the source, thus making the overdrive voltage less than zero.

3.4.3 M-LVDS Receiver

The M-LVDS receveir has been designed in 0.18 μm CMOS Image Sensor technology by TowerJazz. This architetcure has differential inputs and a



(a) Parasitic current in the PMOS transistors.

(b) Remedy to the indesired PMOS current.

Figure 3.13: To ban the current inside a PMOS transistor connected to the transmission line a switch is added to change the gate potential e forbid the PMOS channel formation.

single ended output. It consists of three different stages pinpointed in Figure 3.14.

The first stage is a CMOS complementary amplifier realized with a NMOS and a PMOS input differential pair connected in parallel. Indeed, this configuration guarantee the most wide common-mode input range, as foreseen from the M-LVDS protocol. The current in the two complementary input stages is set via the dedicated 4-bit DAC for a maximum of 500 μA for both branches.

When the common-mode input signal is high (>1.2 V) only the NMOS input pair is active whilst for a low common mode input signal (<800 mV) only the PMOS input stage is active. For an intermediate value of the input common-mode, the two CMOS differential pair can process the input signal. Each of the two input stages is equipped with a positive decision feedback because it allows both to speed up the switching and introduces hysteresis to avoid oscillations at the output.

The second stage of the M-LVDS receiver is a high gain stage formed by two complementary high gain differential pairs. This stage combines the two signal paths originating from the input stages and converts the output signal to full-swing CMOS.

The receiver output has been equipped with an enable circuit which realizes an AND logic. When ENABLER is at logic 1 the receiver output is allowed to transmit the input data stream. Conversely, ENABLER can be switched to a logic 0 thus fixing the receiver output to DVDD. The possibility to fix the receiver output voltage value is foundamental to avoid a

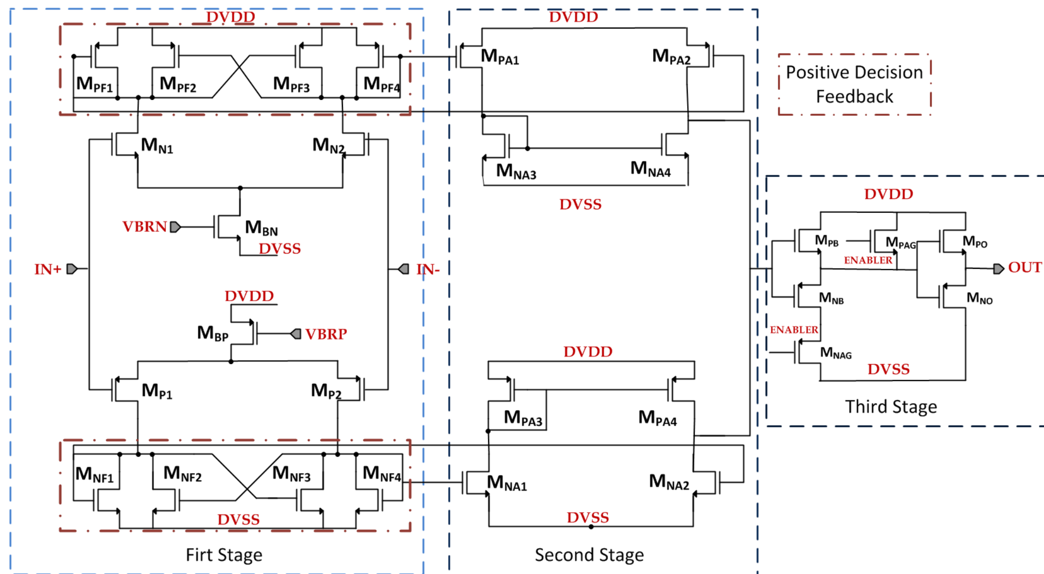


Figure 3.14: Receiver schematic with the highlight on the three stages.

wastefulness of power if the transmission lines are not driven. Indeed, in this idle bus condition the differential voltage drop across the two termination resistors is almost zero. Then, the receiver outputs could assume any voltage value between DVDD and DVSS. Then the ENABLER can be driven to the logic 0 thus preventing the switching activity to cause an indesired power consumption.

3.5 High speed data transmission: pseudo-LVDS Driver implementations for the ALPIDE pixel chip

The LVDS driver is in charge to send out data from the chip periphery at the speed of 1.2 Gb/s and 400 Mb/s from the Inner Barrel and Outer Barrel respectively. This high speed output is part of the Data Transmission Unit (DTU), a fast serial link made up of a 600 MHz clock multiplier PLL, a serilizer working in Double Data Rate mode and a pseudo-LVDS driver.
The DTU works with a power supply of 1.8 V and it is entirely designed in the TowerJazz 0.18 μm CMOS Image Sensor technology. The PLL is used to multiply by 15 the 40 MHz LHC clock to obtain the 200 MHz and 600 MHz clock for the OB and IB chips respectively. The serializer encode a parallel 30 bit stream in four serial outputs to feed the driver inputs. The

pseudo-LVDS driver is the unique active device between the output of the pixel chip and the external FPGA in the patch panel. Since it has to drive the 5.3 m and 6.5 m long hybrid transmission lines, a pre-emphasis driver has been added to enhance the device driving strength.

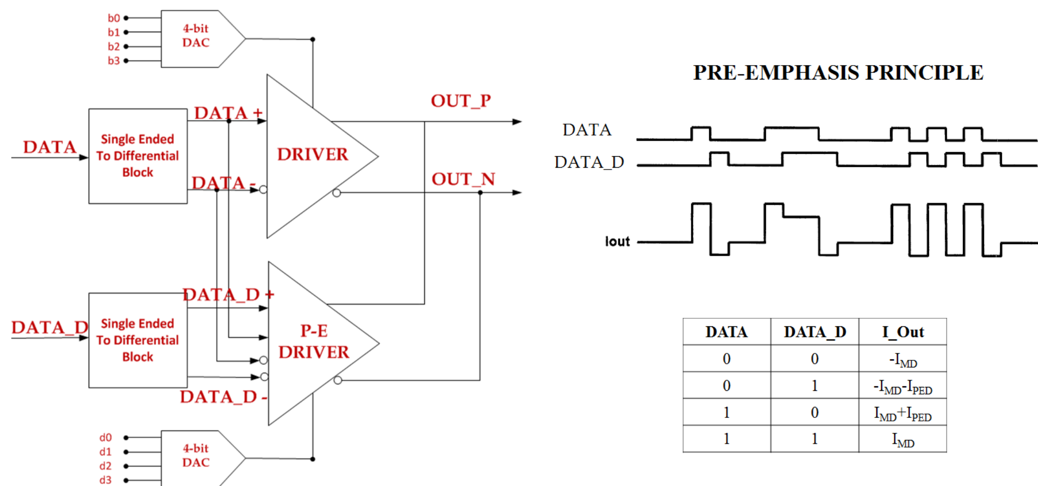
Varius prototypes for the High Speed Output (HSO) driver have been designed for the ALPIDE chip. Actually, it has been a long way to find a compromise solution between the device power consumption and the signal integrity, since the driver has to drive at the speed of 1.2 Gb/s and 400 Mb/s very long e-links.
Each prototype is a pseudo-LVDS driver designed in 0.18 μm CMOS technology with a 1.8 V power supply. It is based on the LVDS transmission protocol TIA/EIA 644 ([37]) that will allow to use very high transmission rate by keeping low the power consumption. The adjective "pseudo" is dictated from the fact that some characteristics of the LVDS protocol have been slightly modified in order to enable the circuit to work with a low power supply . Actually, the power supply of 1.8 V is significantly lower than the 2.5 V or even higher typical value often used for this kind of circuits [38], and then even in this case the output common mode value V_{CM} is lowered from 1.2 V foreseen by the standard protocol to 1.1 V.

The first proposed driver scheme is presented in Section 3.6. A second version of the driver has been used in the full DTU chain illustrated in Figure 3.24 and it has been already integrated in the ALPIDE protptotype. This circuit implementation is introduced in Section 3.7. The circuits simulations together with the test measurements will be the subjects of the next Chapter.

3.5.1 Pre-emphasis technique: principle of operation

To properly reconstruct the signal at the end of the cable, the driver strength has to be high enough so that the energy loss along the lines can be neglected. Sometimes, when very long cables are used for high speed data transmission, the Pre-Emphasis (PE) technique is adopted to overcome the bandwidth limitation coming from this component and which cannot be improved.
Those limitations have a major impact when a fast bit transition between two logic levels is occurring since the output of the driver does not have enough time to settle at the correct voltage value. In this case the PE technique gives an increase of the signal amplitude for a very short time, when the bit transition takes place, in order to speed up the transmission by keeping a high signal integrity [39].

The timing diagram of the PE technique is shown in Figure 3.15.
To drive the PE it is mandatory to have the delayed copy DATA_D of the transmitted data stream DATA so that it is possible to know if two subse-



DATA	DATA_D	I_Out
0	0	$-I_{MD}$
0	1	$-I_{MD}-I_{PED}$
1	0	$I_{MD}+I_{PED}$
1	1	I_{MD}

Figure 3.15: Pre-emphais technique. The data streams DATA and DATA_D are needed to activate the pre-emphasis driver. Depending on the logic values of two consecutive bit, the PED can add current, subtract it or do nothing.

quent bit are different. By looking at the timing diagram, it is possible to see the PE principle. When the data stream maintains the same logical value in two subsequent bit, only the current steered by the main driver (MD) will drive the signal line. Nevertheless, when the data stream switches from 0 to 1 the PE circuit will add the current I_{PED} whilst for the inverse transition from 1 to 0 it will subtract the same amount of current. One possible implementation of a circuit which does this operation will be presented in the following Section [43].

3.6 First implementation of the pseudo-LVDS Driver

The scheme of the first driver implementation is similar to the one designed for the M-LVDS transceiver since at the beginning it was thought for a 640 Mb/s data rate at maximum. Even this high speed driver is based on [35] but, in this case, it has been furnishid of a pre-emphasis driver circuit to guarantee a suitable transmission quality when very long transmission lines has to be driven at high speed rates. Actually, the HSO will have to drive a full 5.3 m or 6.5 m long hybrid differential transmission line, like those shown in Figure 3.17. Here, a pre-emphasis technique is mandatory in order to overcome the bandwidth limitations of the cable.

As shown in the following, the pre-emphasis driver implements a fast

XOR logic in order to add or subtract an amount of current depending on whether there is a bit transition. While the value of the pre-emphasis current is selectable, the pre-emphasis pulse has a fixed duration of circa half clock cycle at 600 MHz whether the transmission speed is 1.2 Gb/s or 400 Mb/s.

The model of the hybrid full transmission line has been simulated in the design phase. It is made of a Al (IB) or Cu (OB) Flex Printed Circuit (FPC) connected with a 5 m long Twinax coaxial cable for different signal. During the simulation phase of the circuits, the physical parameters of the FPC together with the S-parameters of the Twinax have been used.

The Block Diagram of this pseudo- LVDS driver is shown in figure 3.15. It is made up of a main driver (MD), an ancillary pre-emphasis driver (PED) and a 4-bit DAC for each of the two circuits to set a suitable current value for the good signal quality at the end of long transmission lines. The layout view of this block is shown in Figure 3.16.

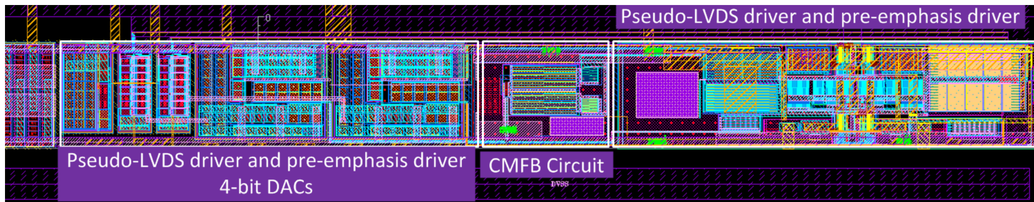


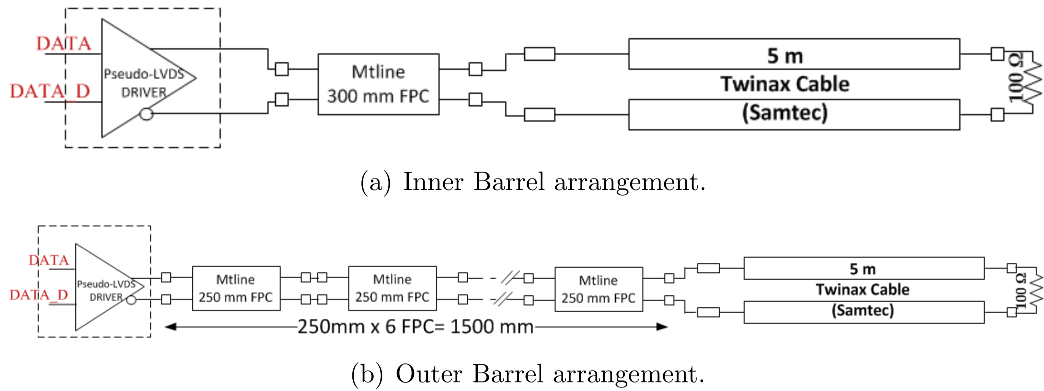
Figure 3.16: Layout of the first implementation of the pseudo-LVDS driver with pre-emphasis. The overall block contains the two 4-bit DACs for the current settings and a custom delay line for the pe-emphasis purposes.

The characteristics of the pseudo-LVDS driver with the pre-empasis are reported in Table 4.6. This first driver implementation had not be integrated in none of the ALPIDE prototypes. However, it was submitted in a separated test chip to verify that the designed pre-emphasis circuit allows for a good signal integrity at the far ends of the transmission lines.

3.6.1 The Main Driver

The Main Driver (MD) circuit is shown in Figure 3.18. It consists of eight transistors which are paired on the two diagonals and a common mode feedback circuit (CMFB). This last circuit fixes the driver output common mode and provides half of the total MD current through the transistor M_{PCFBO} which suitably mirrors the common mode feedback circuit current. The ratio between the current in the CMFB circuit I_{CMFB} and the total driver current I_{MD} is 1:10.

The MD works in current steering mode providing a total current which ranges between 2 mA and 5 mA to a 100 Ω ±10% load resistor placed at the



(a) Inner Barrel arrangement.

(b) Outer Barrel arrangement.

Figure 3.17: Examples of the connection between the chip periphery and the patch panel for the high speed data transmission.

receiver side. This resistance value is set in order to avoid signal reflections due to impedance mismatches between the differential transmission line and the receiver at its ends. The inputs DATA+ and DATA- have a full CMOS swing to open and close alternatively the paired transistors M_{PD1} and M_{ND2}, M_{PD2} and M_{ND1}. In this way those transistors steer most of the current in the transmission line whilst transistors M_{PD3}, and M_{ND4}, M_{PD4} and M_{ND3} drive the remaining amount of current with a short delay to control the overshoot and the undershoot as in the M-LVDS case. With the exception of the circuit enebale, the principle to lower the output transconductance that has been illustrated for the M-LVDS is still valid even in this case. The delay is set by the product between the constant value of the resistor R_D and the total input capacitance C_D which depends on the $M_{ND3,4}$ and $M_{PD3,4}$ widths and lengths. Clearly, for the LVDS purposes, this delay is much shorter than the M-LVDS since the data rate is faster and the transistor capacitance is lower than the previous case. Actually, minimum length transistors have been adopted to not affect the speed of the system. The transistors widths are set to: $W_{PD_{1,2}}$=2.7 $W_{ND_{1,2}}$, $W_{ND_{1,2}}$ ∼1.9$W_{ND_{3,4}}$. This ratio between the inner switches and the outermost resulted as the one which guaranteed a good transmission quality to the far end of the hybryd transmission lines.

By using this 100 Ω resistor, the driver output voltage swing ranges between 200 mV and 500 mV around the 1.1 V V_{OCM} [43].

3.6.2 The Pre-Emphasis Circuit

The PE driver is shown in Figure 3.18 and it is based on [40].
The structure is similar to the MD but it implements a fast XOR logic in

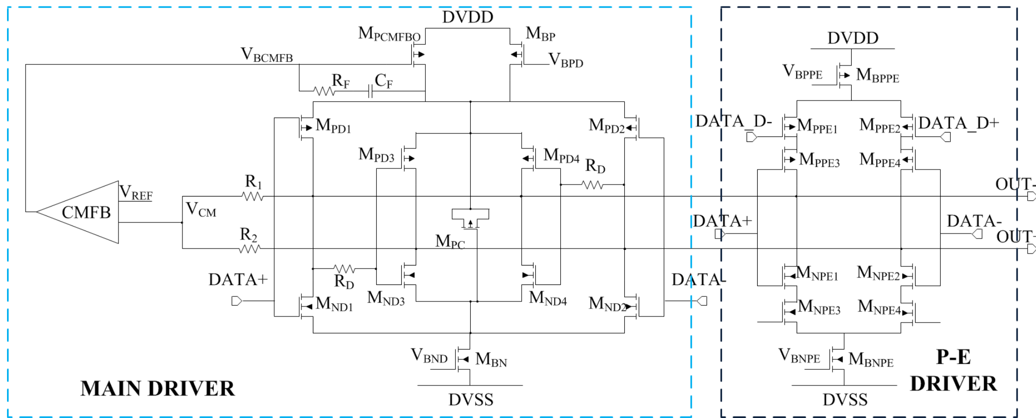


Figure 3.18: The Main Driver and the Pre-emphasis Driver circuits.

order to add or subtract current depending on the data stream. As in the MD, the eight transistors are coupled along the two diagonals. In this case however, transistors M_{PPE3} and M_{NPE4}, M_{PPE4} and M_{NPE3} steer the I_{PED} current in the transmission line whilst M_{PPE1}, M_{NPE2} and M_{PPE2}, M_{NPE1} allow the PE current to be source and sunk in the circuit. As foreseen from the PE technique, DATA+ and DATA- together with their delayed copy DATA_D+ and DATA_D- feed the PE inputs. The PE modulation current ranges between 1 mA and 2.5 mA, thus obtaining 50% of pre-emphasis at maximum.

Transistors M_{PPE3}, M_{NPE3} and M_{PPE4}, M_{NPE4} have the same dimensions of the corresponding MD switches, i.e. M_{PD1}, M_{PD2}, M_{ND1} and M_{ND2} whilst transistors M_{PPE1}, M_{PPE2} and M_{NPE1}, M_{NPE2} are twice larger [43].

3.7 The Driver block

The second version of the pseudo-LVDS diver with pre-emphasis has been integrated in the Driver with some ancillary circuits to be integrated in the Data Transmission Unit (DTU). The DTU is a fast serial link containing a 600 MHz clock multiplier Phase Locked Loop (PLL), a fast serializer working in Double Data Rate (DDR) mode and the Driver block. lIn particular, the Driver block contains:

- A pseudo-LVDS driver (MD_{DTU});
- A ancillary pre-emphasis driver (PED_{DTU});
- Two 2 to 1 analog multiplexers (MUXs) for the signal selection at the driver inputs;

- Two single ended-to- differential (STD) blocks which convert the single ended multiplexers outputs to differential inputs for the MD_{DTU} and PED_{DTU};
- Two indipendent 4-bit-DACs for the main driver current and the pre-emphasis current settings.

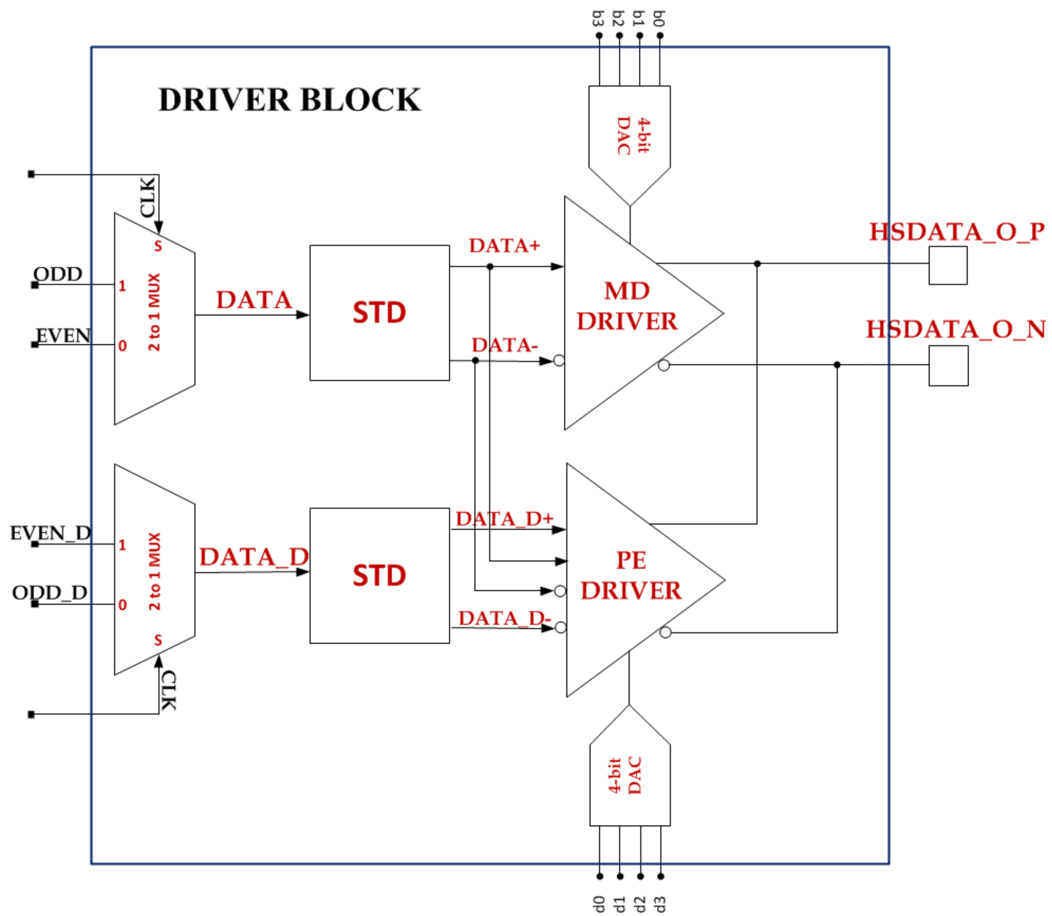


Figure 3.19: Block Diagram of the Driver block inegrated in the third ALPIDE chip prototype. In addition the the pseudo-LVDS driver and the pre-emphasis driver, it includes two MUXs and two STD blocks for the definition and the buffering of the two drivers input data stream.

With the exception of the MUX in which some standard cells are used, those circuits are fully custom made with the TowerJazz 0.18 μm CMOS technology and they work with nominal power supply of 1.8 V.

The Driver inputs are fed by the serializer output with data rates of 600 Mb/s and 200 Mb/s for the IB chips and OB chips respectively. However,

the select signal for the two MUXs is always a 600 MHz clock. What changes among the IB and OB chips is the way in which the data are encoded by the serializer.

While one MUX process the EVEN and ODD data to generate the DATA stream for the MD_{DTU} and PED_{DTU}, the other one deals with EVEN_D and ODD_D signals for the PE current activation.

The pseudo-LVDS and its ancillary driver have a differential inputs. For this reason the two STDs are placed in between the single ended MUXs and the two drivers. The purpose of this block is only to furnish the two phases of an input signal after its regeneration.

Finally, the pseudo-LVDS driver buffers the input data streams and drive the differential transmission lines. Depending on the characteristics of those data streams, the PED_{DTU} will add or subtract current to enhance the MD_{DTU} driver strenght, as foreseen by the PE technique (Sec. 3.5.1).

3.7.1 2 to 1 Multiplexers

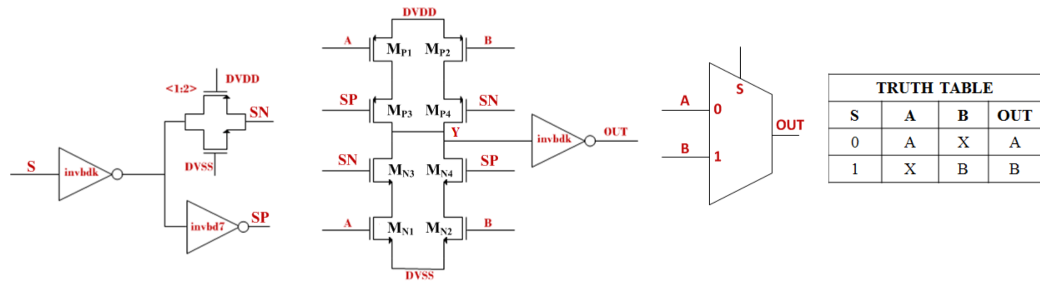
The 2 to 1 Multiplexer (MUX) is used to select one signal among the two inputs and outputs one among them, depending on the logic value of the select signal. The TowerJazz technology provides some MUX standard cells but they have not balanced outputs. This means that the rise time and the fall time of those cells are not equal and this fact gives a jitter component to the MUX outputs. For this reason an analog semi-custom circuit has been designed with the purpose to have a balanced output. The output load is a STD cell which has an input capacitance of 64 fF.

The MUX scheme is shown in Figure 3.20. The circuit is made up of two identical branches controlled by the two input signals (A and B) and the select signal (SP and SN). To have a fast device, minimum channel length transistors have been chosen whilst to ensure a balanced output the width of the PMOS transistors is $\sim$ three times the one of the NMOS.

Signals SP and SN are the two phases of the same select signal that are nedeed to chose which inputs among A and B has to be transmitted at the output.

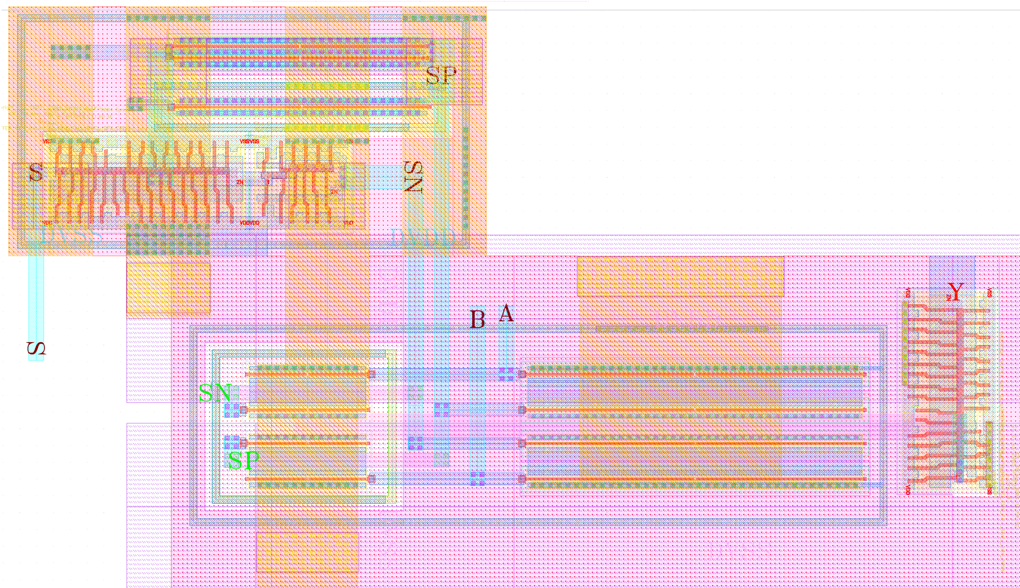
A dedicated circuit has been inserted to generate the controls SP and SN. Actually, the select signal S feeds the inverter standar cell *invbd7* with balanced output and then, it is transmitted by a transmission gate to generete the inverted signal SN and already inverted to generate the direct signal SP. The transmission gate has been designed taking in to account the delay due to the inverter standard cell. Indeed, the signals SP and SN have to have the same propagation delay from the input clock to minimize the output jitter .

The working principle of this block is explained in the table of truth reported in Figure 3.20. Whatever the B signal may be, when the S signal is at a logic 0, i.e. at 0 V, the MUX will output the A signal. Viceversa, the MUX output will be the B signal when S signal is at logic 1, i.e. 1.8 V, it does not matter which value the A signal is assuming.



TRUTH TABLE			
S	A	B	OUT
0	A	X	A
1	X	B	B

(a) 2 to 1 Multiplexer schematic view.



(b) 2 to 1 Multiplexer layout view.

Figure 3.20: 2 to 1 Multiplexer.

This MUX scheme is used to generate the 1.2 Gb/s or 400 Mb/s data streams for the MD_{DTU} and the PED_{DTU}. It has an output rise time of (75.0±9.8)ps and a fall time of (77.5±21.1) ps. A greater value of the fall time is due to the fact that there are some differences in the rising and falling time depending on the process corners.

Looking to the Driver Block Diagram reported in Figure 3.19, the EVEN

signal is selected when the clock is stable to its low level whilst the ODD signal will be output when the clock is at its high level, i.e. 1.8 V. Instead, the opposite is true for EVEN_D and ODD_D. In this way, whether the transmission is at 1.2 Gb/s or 400 Mb/s, the time shift between the EVEN and ODD data and their delay will be always half clock cycle of the 600 MHz clock.

3.7.2 Single Ended to Differential Block

The Single Ended to Differential (STD) block links the MUXs outputs and the driver inputs. It simply regenerate the singnal at its input by reproducing it in direct and inverted phases.

The STD schematic is illustrated in Figure 3.21. It has been designed to drive a load capacitance C_{Load} = 400 fF for each branch, considering that it has to drive the MD_{DTU} and PED_{DTU}. The non-inverting STD branch DATA+ and the inverting one DATA- have to have the same number of gates to ensure the same signal delay from the DATA input. For this reason the non-inverting branch is realized putting in series a transmission gate and two inverters whilst the inverting branch is implemented with a three inverters chain. The number of stages has been derived by computing the overall effective fanout F of the circuit considering the input capacitance of the minimum inverter C_{inv} = 11 fF and the drivers input capacitance C_{Load} = 400 fF.

$$F = \frac{C_{Load}}{C_{inv}} = 36.36 \tag{3.4}$$

Then, the minimum delay through the inverter chain has been minimized by the number of stages N:

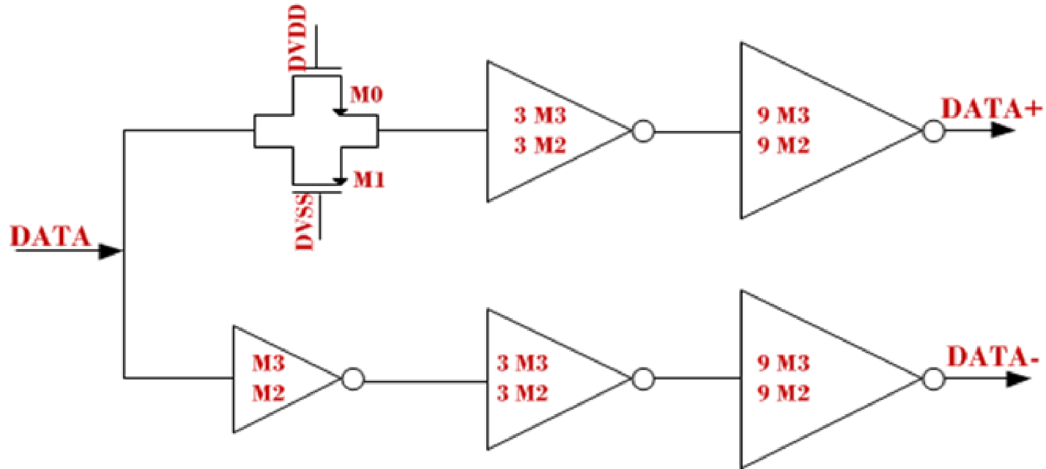
$$\frac{\partial t_p}{\partial N} = \frac{\partial}{\partial N}[N \cdot t_{p0} \cdot (1 + \sqrt[N]{F}/\gamma)] = \; = \gamma + \sqrt[N]{F} - \frac{sqrt[N]F \ln F}{N} = 0 \tag{3.5}$$

Here, t_p is the inverter chain delay, t_{p0} is the intrinsic inverter delay and $\gamma = \frac{C_{inv}}{C_g}$ is a factor between the intrinsic output capacitance of the inverter C_{inv} and the input gate capacitance C_g [44]. When the self-loading is neglected, $\gamma = 0$. However, in this case the value of $\gamma = 1$ has been adopted to take into account the inverter intrinsic output capacitance. Then, the number of inverters in the chain is established as

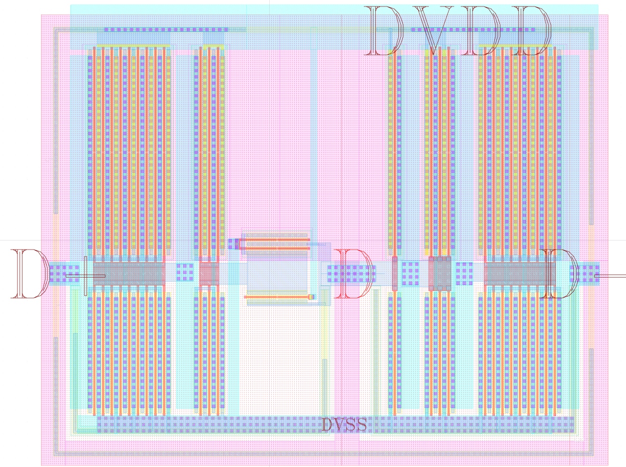
$$N = ln(F) - 1 = 2.6 \sim 3 \tag{3.6}$$

The effective fanout f of each inverter, i.e. the ratio between the capacitance of the inverter load and its input capacitance is defínined as $f = \sqrt[N]{F}$. With

the value computed above, an effective fanout of ∼3 has been obtained. Then, those factor has been used as multiplicity factor to scale the inverters in the chain. Minimum length transistors has been used for the transmission



(a) Schematic view.



(b) Layout view.

Figure 3.21: Single ended-to-differential block.

gate and the inverters to not affect the transmission speed. Concerning the transistors width, the inverter PMOS as well as the transmission gate PMOS are two times wider than the NMOS to guarantee a symmetric inverter characteristic and the same channel resistance respectively. Furthermore, the transistor width in the inverters and in the transmission gate have been optimized to have the same propagation delay on the two branches together

with the same rise time and fall time, thus allowing DATA+ to cross DATA- at DVDD/2. The timing characteristics of the STD block are resumed in Table 3.3.

Table 3.3: Timing Characteristics of the three stages single ended-to-differential block.

	DATA+		DATA-		
Parameter	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{pLH}	120	245	134	254	ps
t_{pLH}	182	237	182	237	
t_{fall}	61.6	90.18	61.6	90.18	
t_{rise}					
	Min		Max		
Intersection point	684		921		mV

As will be expleined in the next Chapter, it was found that this STD block consumes too much power driving the MD_{DTU} and PED_{DTU}. Actually, a non optimized dimensioning of the inverters entails that the PMOS and NMOS could be both in conduction depending on the value of the input signal. When this happens, a short circuit current is produced consuming power. This unwanted power consumption contribution has to be added to the power needed to switch the Driver input capacitances.

As it is possible to see from the block diagram, one of the STD drives four inputs, two for the pseudo-LVDS driver and two for the pre-emphasis. From the calculations and the simulations, the load capacitance at the input of each branch of this STD turns out to be 1.5 pF. Furthermore, those capacitance has to switch every 1.2 Gb/ in the worse case. Then, it has been modified by considering that the inverter at the MUX output has a capacitance of C_{invbdk}= 0.087 pF. By repeting the procedure explained before, the effective fanout f is equal to 4, then a big reduction of the load capacitance for each internal node of the STD block is foreseen. This block still maintains the structure of the previous version but the DATA+ branch is implemented with a two stages inverter chain whilst the DATA- branch is realized with a transmission gate in series to an inverter. The schematic of the revised STD is illustrated in Figure 3.22 together with the previous scheme of this block.

3.7.3 pseudo-LVDS driver and pre-emphasis driver

For the integration in the DTU chain, and then in the third ALPIDE prototype, a second version of the the pseudo-LVDS driver scheme with the

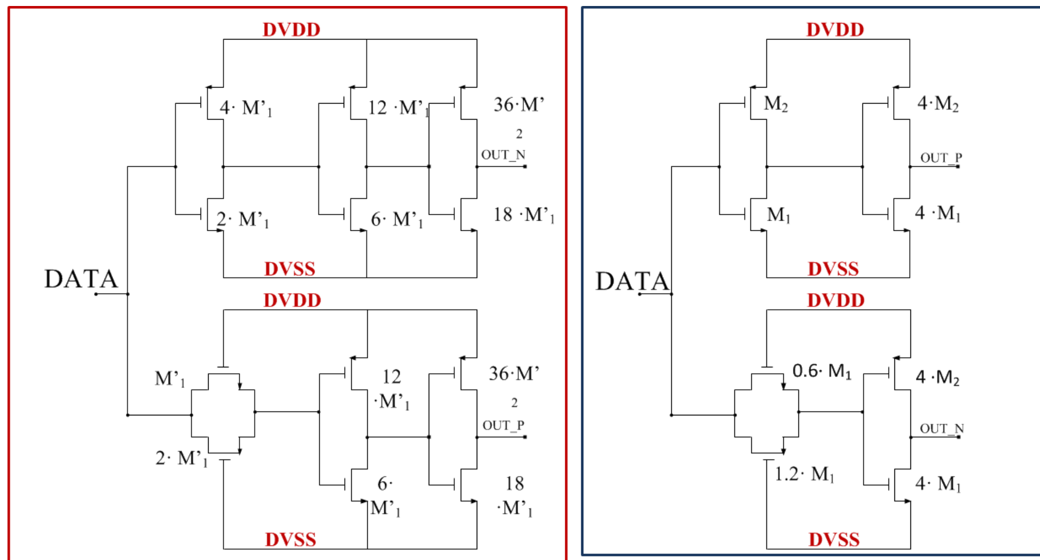


Figure 3.22: Modification to the Single Ended to Differential Block (STD). Red rectangle: first implementation of the STD block. Blu rectangle: power optimized STD block.

pre-emphasis driver has been designed . Indeed, the first driver prototype illustrated in 3.6 has been modified to eliminate the slew rate control transistors, as shown in Figure 3.23. A high driver strength is necessary when

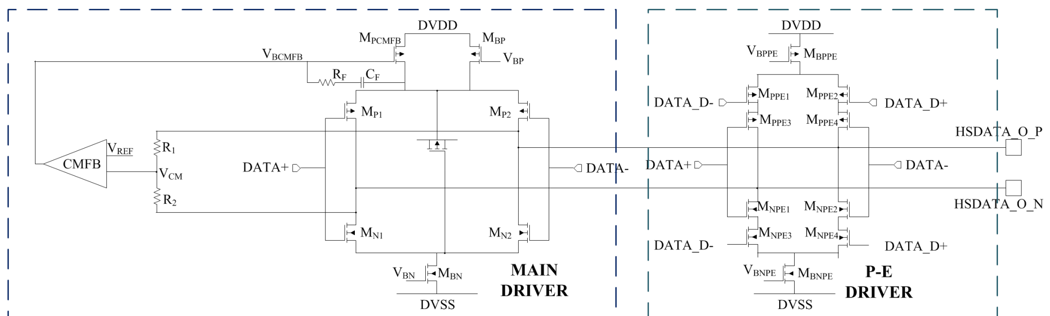


Figure 3.23: Second implementation of the pseudo-LVDS driver with pre-emphasis.

a fast bit transition starts. Then, the main driver has to deliver its total current from the beginning. Furthermore, the pre-emphasis driver will release an amount of additional current depending on the pre-empasis level. In the first driver scheme the slew rate circuit was added to slowly deliver the total driver current in the line, thus controlling the impedance mismatch effects. There, even a pre-emphasis driver was added but its effect turned to

be minimized by the slew rate control.

The second pseudo-LVDS driver circuit has the typical four switches configuration. Transistors have minimum length to maintain the speed performance but the PMOS are one and half wider than the NMOS, the output crossing point being at 1.1 V. Here, one tenth of the total driver current flows in the common mode feedback circuit and with a suitable mirroring ratio the transistor M_{PCMFB} provides half of the total MD_{DTU} current.

The pre-emphasis driver implements the same XOR logic as in the case illustrated in section 3.6.2. However, transistors here have been sized up with the same principle adopted for the second version of the main driver.

The main driver current and the pre-emphasis current are set using two indipendent 4-bit DACs, with the same operating principle of the first driver implementation.

In the next Chapter the study on the power consumption will be reported. After the integration in the third ALPIDE prototype, further studies have been done to reduce the power consumption of the second version of the HSO. Actually, because of the high transmission rate this is one of the most power hungry circuits in the pixel chip. To solve the power consumption issue, one of the solution could be to move the output common mode from 1.1 V to 0.9V, at center between the power supply and ground. This can be beneficial since entails a reduction of MD_{DTU} and PED_{DTU} input transistors size, thus reducing the input capacitance of those blocks. However, it has to be pointed out that this power optimized driver is still matter of study.

3.8 Data Transmission Unit: the PLL and the serializer circuits

A said before, the Data Transmission Unit is a series three circuits, namely, the 600 MHz clock multiplier PLLoop, the fast serializer and the high speed driver. The PLL and the serializer receive the 40 MHz clock and a parallel data stream respectively from the digital periphery whilst the driver buffers at its output HSDATA_O_P and HSDATA_O_N the serialized data to the RU.

The 600 MHz clock multiplier PLL shown in Figure 3.25 is a full custom circuit consisting of a Voltage Controlled Oscillator (VCO), a ×15 Frequency Divider, a Phase-Frequency Detector (PFD), a Charge Pump (CP), a RC filter and a DAC which is used to set the current in the CP.

The VCO is implemented using four stages of a differential ring oscillator like the one shown in Figure 3.26(a) which is based on [41] and [42] and

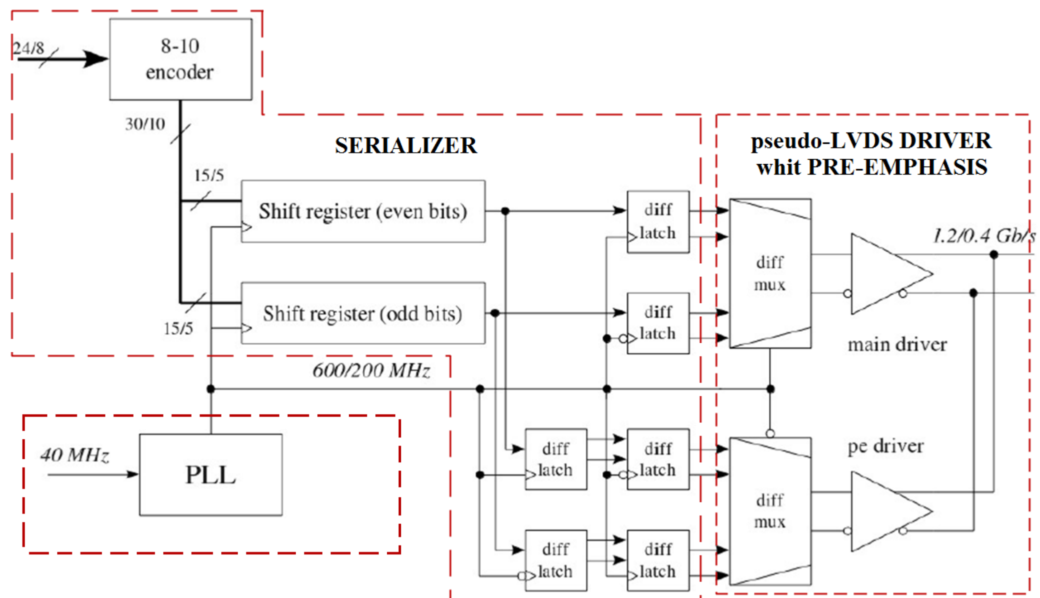


Figure 3.24: DTU Block Diagram. The PLL multiplies the 40 MHz LHC clock to feed the serializer inputs with a 600 MHz or 200 MHz clocks, the difference bing on the chip location (IB or OB). The serializer works in Double Data Rate and outputs the two phases of the data streams for the pseudo-LVDS driver.

it has a tuning range between 450-750 MHz. The top and bottom current sources provide the same current to the circuit and the current value can be suitably adjusted by varying the gate voltages Vcp and Vcn. The ring oscillator input is a PMOS differential pair loaded with diode connected transistors in parallel with two transistors with an external gate voltage.
This architecture has two advantages with respect to a single ended current limited inverter. Indeed, it is less sensitive to the noise and it allows to have an even number of stages in the VCO and hence dividing the phase by an even factor. The diode connected transistors are used to load the input differential pair instead of fixed resistors. These diode connected transistors in parallel with two transistors with external gate voltage give the possibility to adjust the output resistance of the VCO simply changing the current in the circuit. In this way, it is possible to control the overall circuit delay which depends on the value of the VCO output resistance and on the capacitance of its load [43].

The output of the VCO feeds the fully digital Divider circuit. It consists of a divider by 3, which provides the 200 MHz clock, followed by a divider by 5. The output of this last divider is compared with the 40 MHz input clock by the phase frequency detector (PFD). The entire circuit is SEU protected

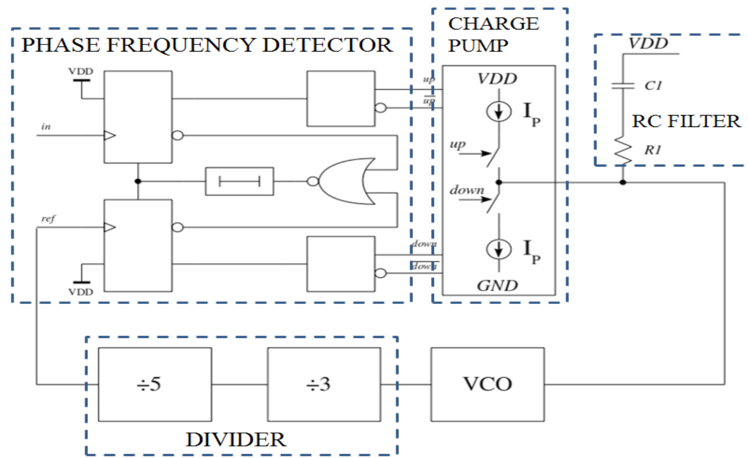


Figure 3.25: Block Diagram of the PLL circuit. In the image the constituents circuits of the overall apparatus are shown.

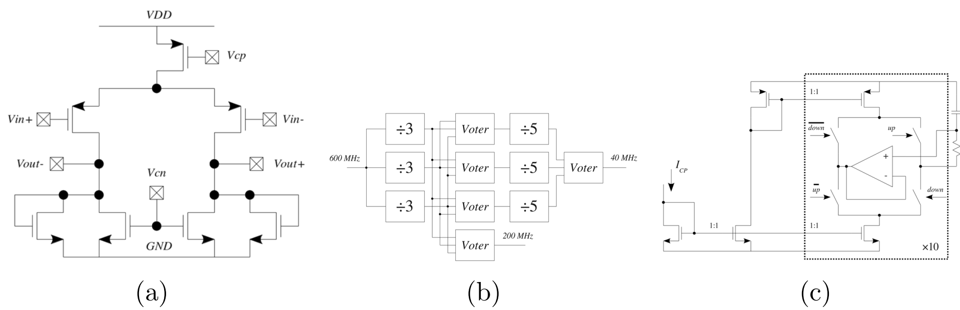


Figure 3.26: PLL components: (a) Ring Oscillator scheme; (b) ×15 Divider; (c) Charge Pump circuit.

to avoid bit flip and bit error propagation using a the Triple Modulator Redundancy (TMR) technique for each division stage, as shown in Figure 3.26(b). Four voters are implemented after the divider by 3 in order to guarantee the same load for each of the voter which generate the 200 MHz clock [43].

The outputs *up* and *down* of the PFD feed the Charge Pump circuit shown in Figure 3.26(c) in order to convert the phase difference value in a voltage value. The four switches are opened and closed alternatively to allow both current sources to provide the same current and let the current to flow in clockwise or counterclockwise direction. A careful design of the CP current sources is needed to reduce the static phase error and for this reason they have been designed with high output impedance transistors. Furthermore, the system has a unity gain amplifier feedback for voltage equalization. A

mismatch between the two currents in the loop will generate a phase difference to compensate the discrepancy [43].

A first order RC filter is added to guarantee the stability of the entire PLL system. By referring to Figure 3.25, the voltage in the middle point between the CP current sources is controlled by two switches. In this way it is possible to add or subtract an amount of charge in that point to change the C_L voltage drop. It can be shown that this system is not stable without the load resistor R_L. Indeed, with only C_L the transfer function of the circuit has two poles in the origin, the second coming from the VCO. In order to stabilize the overall circuit is thus needed to introduce a zero by means of the load resistance R_L. Sometimes, a second order filter is used which foreseen to add a capacitor in parallel to the previous RC filter to better control fast variation of the voltage in the middle point. Even if this technique helps the PLL stability, it slows down the circuit. After detailed simulations, it turned out that for this scheme the voltage spikes are not so relevant and then the first order filter was preferred [43].

The Double Data Rate (DDR) serializer (see Figure 3.27) has two 15 bit shift registers since the even and odd data from the 30 bit input are serialized on two different clock edges, thus implementing the DDR data transmission. The load of the shift registers is synchronized between the 40 MHz and the 600 MHz clock domains.

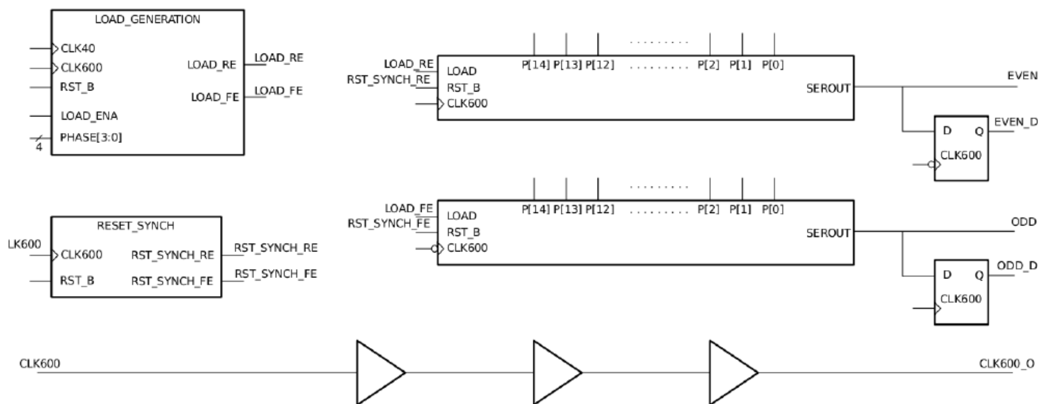


Figure 3.27: The Double Data Rate serializer scheme. This is a fully digital circuit which serializes data parallel data coming from the digital ALPIDE periphery. (This image is courtesy of Dr. G. Aglieri Rinella.

For sake of comprehensibility, the timing diagram of the 1.2 Gb/s transmission from the serializer to the driver is shown in Figure 3.28. Since the serializer has to drive the pseudo-LVDS driver and the ancillary pre-emphasis

driver, it outputs the signals EVEN, ODD and their delayed copies, EVEN_D and ODD_D with a time delay of half clock cycle. Furthermore, the serializer produce at its output the select signals for the driver multiplexers. Basically, those signal are two 600 MHz or 200 MHz clocks shifted by half cycle of the fastest clock.

The entire design has been done by using the TowerJazz standard cells, with a power supply of 1.8 V. Since this is a totally digital system it has been protected against SEU events. With this purpose a Triple Modular Redundancy (TRM) for the Flip Flop with SEU self correction has been used.

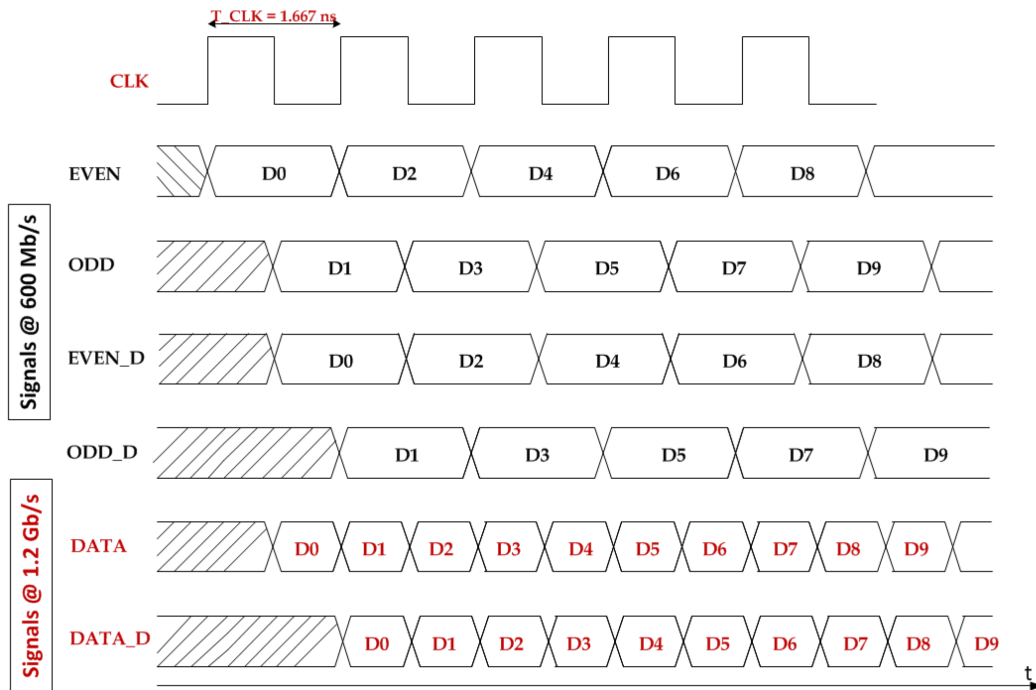


Figure 3.28: Timing diagram of the transmission from the serializer outputs to the driver inputs. Here the CLK is a 600 MHz clock whilst EVEN, ODD and their delayed copies are 600 Mb/s streams.

3.9 Overview on the ALPIDE 3 chip prototype.

The block diagram of the ALPIDE 3 pixel chip prototype is illustrated in Figure 3.6 and the chip pinout is illustrated in Figure 3.29. This chip consists

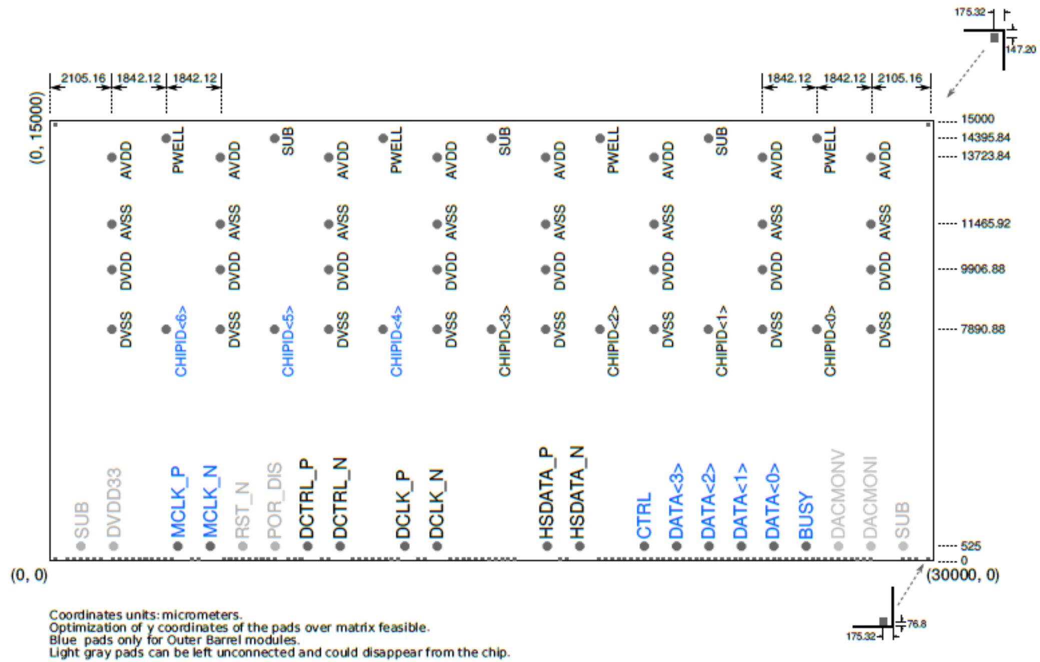


Figure 3.29: Pinout oof the ALPIDE 3 prototype

of two main parts, the pixel matrix and the chip periphery.

The pixel chip matrix is made up of 512 rows and 1024 columns, for a total of circa 500 k pixels and a sensitive area of 14.3 $\times$ 28.7 mm^2. Each pixel has an area of 28$\times$28 μm^2 which contains the sensor and the in-pixel discrimination circuit. This last circuit provides a binary information on a hit/not hit pixel and the addresses of the hit pixels are handled by the priority encoder, as already explained in section 2.4.2. The data thus obtained are sent first to the digital periphery and then to the data transmission blocks located in the pad ring.

Looking at Figures 3.6 and Figure 3.29, the pad ring groups the input/output interfaces (I/Os) of the ALPIDE 3 prototype.Those interfaces are the well know differential transmission block, as the M-LVDS transceiver and the LVDS driver, whilst the remaining are the CMOS (single ended) intefaces as the **CHIPID**[**6:0**], the **DATA**[**7:0**], or the control **CTRL** inputs.

It has to be pointed out that each port listed above allows the communication between the RU and the chip itself. Some of the port, like the differential **MCLK_P** and **MCLK_N**, are used only as chip inputs, i.e. a chip receives CLK or a CTRL signal from the RU. In the same way, the differential ports **HSDATA_P** and **HSDATA_N** or the single ended **DACMONV** and **DACMONI** output the signals toward the RU. However, the

remaining ports are bidirectional ports allowing the chip-to-chip communications and data exchange in both directions between the RU and a pixel chip. Inside the chip, the digital periphery encodes the data from the pixel matrix or receives the settings from the RU to allow a chip to work properly.

In this Chapter the control interfaces, as the M-LVDS transceiver as well as the HS output were extensively described. The periphery of the ALPIDE 3 prototype contains three of those M-LVDS transceiver corresponding to the differential ports **MCLK_P** and **MCLK_N**, **DCLK_P** and **DCLK_N**, **DCTRL_P** and **DCTRL_N**. However, it is worth to note that the differential input **MCLK_P** and **MCLK_N** are necessary to the clock forwarding only for the OB chips. Indeed, they correspond to the inputs of the receiver in the M-LVDS transceiver in which the driver is always disabled whilst the receiver is active and forward the signal to the inputs **DCLK_P** and **DCLK_N**.

The differential ports **HSDATA_P** and **HSDATA_N** correspond to the output of th unique high speed driver with which the chip is equipped. As explained prevoiusly, this driver is the last part of the high speed serial link named DTU which send out of the chip the signals coming from pixel matrix and which are handled in the digital periphery.

The ALPIDE pixel chip family, and in particular the ALPIDE 3 prototype, is very versatile since it has to be used as an IB chip as well as an OB chip. Since the ALPIDE pixel chip will equip the entire upgraded ITS, it has to be configured as an IB chip or Master/Slave OB chip. Furthermore, a Master can become a Slave and viceversa. To set the operation mode of each chip, a signal is applied to the **CHIPID[6:0]** port. Those inputs are subdivided as follow:

- **Module Identifier - bit CHIPID[6:4]**. The pixel chip inside the new ITS will be distinguished by the values of those 3 bit. Indeed, an IB chip is indicated by the code b000 whilst an OB chip has to have at least one of those bit different from 0. As an example, let's consider a Middle Layer pixel chip. Since the Module in these layers host four pixel chips, each of them will be identified with the code b001, b010, b011, b100. The same principle is adopted for the Outer Layers pixel chips, bearing in mind that, in this case a Module hosts seven of them.

- **Position and role inside a Module Identifier - bit CHIPID[3:0].** Once identified the Module at which a chip is belonging to, the role and the position inside the detector have to be assigned. In this case there is a difference between the IB and OB chips respectively. As reported in the description of the Stave layout, the IB Layers host a row of nine chips whilst a Module in an OB layer is made up of two

rows of seven chips. Then, for the IB chips any combination of 0 and 1 can be set with the exception of the b1111 which is used for broadcast addressing. For the OB chips the bit **CHIPID[3]** indicates the row in which a chip is located whilst the bit **CHIPID[2:0]** are set to identify a Master and a Slave. Indeed, the bit code b000 is associated to the Master chip whilst any combination of 0 and 1 labels a Slave. Even for an OB chip the combination b111 is forbidden since it is used for broadcast addressing.

The remaing CMOS I/O interfaces, as the **CTRL**, the**DATA[3:0]** and the **BUSY** ports are set for the OB chips only.

The **CTRL** is a bidirectional single ended port for the half duplex transmission between the Master and the Slave in the OB Module.

Even the bits **DATA[7:0]** are CMOS bidirectional data ports for the implementation of a shared parallel data bus between the OB Slave chips and their Master chip. The chips can be configured to work in Double Data Rate mode or Single Data Rate mode in the lowermost lines. In the firts case, at every clock cycle there is one complete byte transfer whilst in the second case one byte is sampled at every rising edge of the clock.

With the Single ended **BUSY** port the BUSY state between the OB Slaves and the associated Master chips is communicated by wiring in parallel all their BUSY ports.

The power supply, the ground, the substrate as well as the **DACMONV**, **DACMONI**, the **RST_N** and **POR_DIS** are utilized for both the IB and OB chips. The monitoring of the DACs inside the chip is done trhough the CMOS ports **DACMONV** and **DACMONI**. The first is a voltage monitoring output used to control the voltages generated by the internal DACs (see Figure 3.6) or to override the internal voltage DACs. The second port is a current monitoring output used to control each currents generated by the DACs, to ovveride the on-chip current DACs or to override the internal current DACs [25].

It has to be pointed out that every signal from the pixel matrix to the pad rings as well as the one in the opposite direction are handled by the digital periphery. A detailed description of every features of the digital periphery can be found in [25]. However, it is worth to note here that this unit turns to be essential for the pixel chip since it is in charge to encode data from the pixel matrix before to send them to the DTU and to distribute the trigger and settings to the entire chip.

Chapter 4

Simulations Test Bench and Test Results on the ALPIDE Data Transmission Circuits

In this chapter I present the results of the simulations on the M-LVDS transceiver and the drivers described previously in this thesis and the test measurements on the high speed circuits. The entire ALPIDE pixel chip is designed in 0.18 μm Qwell CMOS technology by TowerJazz powered by a 1.8 V power supply, since it allows to satisfy the requirements of the ITS upgrade, including the reduction of the power consumption and the minimization of the material budget. Simulations and test measurements aim to verify that the designed interfaces are suitable solutions for the ITS upgrade data transmission. In particular, the signal integrity along the hybrid transmission lines and at the ends of them was investigated by using the eye diagrams. Actually, this is a key tool which gives an idea of the transmission quality at firts glance and allows to intervene on the circuits to optimize the data transmission link.

A deeper analysis was done for the M-LVDS transceiver with the purpose to study the performance of this interface for the Module-to-Module and chip-to-chip communications in the IB and mainly OB chips arrangements.

The two pseudo-LVDS drivers with pre-emphasis were studied to verify that a suitable signal integrity is obtained at the end of the long e-links at the rate of 400 Mb/s and 1.2 Gb/s with the help of the pre-emphasis technique. Furthermore, the full DTU link have been tested to check the SEU hardness.

In the following, also the power consumption of the two transmission systems is illustrated. As said in the previous chapter, to minimize the ITS power consumption is one of the ALPIDE pixel chip design goal. For this reason the blocks have been simulated in the typical working conditions and

the results pushed for the circuit modifications shown before.

4.1 Simulations and Measurements

The circuits presented in the previous Chapter were designed and optimized by using the Cadence tools which allows to follow the design from the schematic to the circuits layout. Those tools help in having a precise idea of the circuits behavior before they are produced and eventually to take precautions to guarantee the circuits to work properly. In particular, with the Analog Design Environment (ADE) simulations can be done taking into account most of the variations which can modifies the system operations. Those variations are due to the mismatches between the circuits components or to the temperature and process corners. Actually, these two causes are considered with Monte Carlo simulations and corner simulations respectively. With the corner simulations a circuit undergoes to the temperature, power supply and process variations as listed in Table 4.1. Indeed, a correct circuit behavior has to be guaranteed in a range of temperatures which accounts for the characteristics of the chip working environment. Generally, the temperature range is [-40÷125] °C, but in the design of the ALPIDE pixel chip a narrower range between [-40÷85]°C was used since those high temperature will not be reached in a realistic case. In the same way, a check is done to study if the voltage drop along the power supply lines affects the circuit perfomance. In particular a ±10% variation around the nominal value represents the worst and the best cases. To have a complete picture of the situation, also the process variations are considered which account for a change in the circuit components characteristics due to the fabrication steps.

Table 4.1: Corners Definitions.

Corner	Temperature (°C)	Power Supply
Fast	-40	1.98
Nominal	27	1.8
Slow	85	1.62

At the end of the schematic optimization, the layout is done to draw the circuits as it will be fabricated on a silicon wafer. Usually the layout is done by following the design rules of a foundry to guarantee a good circuit production. The layout together with the post-layout simulations are the most important design steps. Those design phases reproduce the true circuit performance since here most of the parasitic effects introduced by the routing or the circuit components placement are considered in the simulations.

As can be argued, there is a long way to fabricate an ASIC (Application-Specific Integrated Circuit) and the last step is the test measurements on it to confirm the circuit performance after the production phase.

The high speed circuits described in the previous chapter were tested in the Electronics Laboratory of the Instituto Nazionale di Fisica Nucleare (INFN) hosted in the Physics Department of Turin University. Essentially the test measurements reproduce the analysis done during the simulations. To send a clock or a Pseudo Random Binary Sequence (PRBS) an Agilent 3.35 GHz Pulse Pattern Generator was used since it has a large selections of signals and input frequencies. A low jitter buffer clock was used to obtain a delayed copy of an input signal to test the pre-emphasis technique whilst the drivers output signals were analysed with a Tektronix oscilloscope able to acquire 25 GSamples/s in a range of frequencies up to 6 GHz.

4.2 Data Transmission Analysis: Eye Diagram and Timing Jitter

Many analysis have been done on the binary data transmission quality for the sign-off of the slow speed and high speed circuits for the ALPIDE data transmission by using the same arrangement foreseen for the IB and OB chips. The purpose was to check the signal integrity along the transmission lines for the M-LVDS transceiver and the pseudo-LVDS drivers. Many factors can affect the transmission quality such as the goodness of the broadcast signal, the impedance mismatches, the transmission line attenuation, the termination scheme and every kind of disturbances caused by the presence of the transmission line.

The most common way to check the signal integrity and to recognize the transmission issues is to use the *eye diagram* similar to the one shown in Figure 4.1. This is a tool characterized by some parameters, like the horizontal and vertical apertures, which reveal the signal degradation in time and amplitude. A Pseudo Random Binary Sequence (PRBS) is generally used as a signal to check the transmission qualitity. Indeed, this is a data stream randomly generated which contains the largest combination of bit sequencences.

Whatever the transmission protocol, for a good transmission quality one has to guarantee that the signal broadcast by a transmitter is recognized by a receiver. Indeed, a definite voltage swing at the driver output characterizes a logic 1 and a logic 0. If the signal degradation along the link is low, the voltage swing at the receiver inputs is large enough for the transmission of

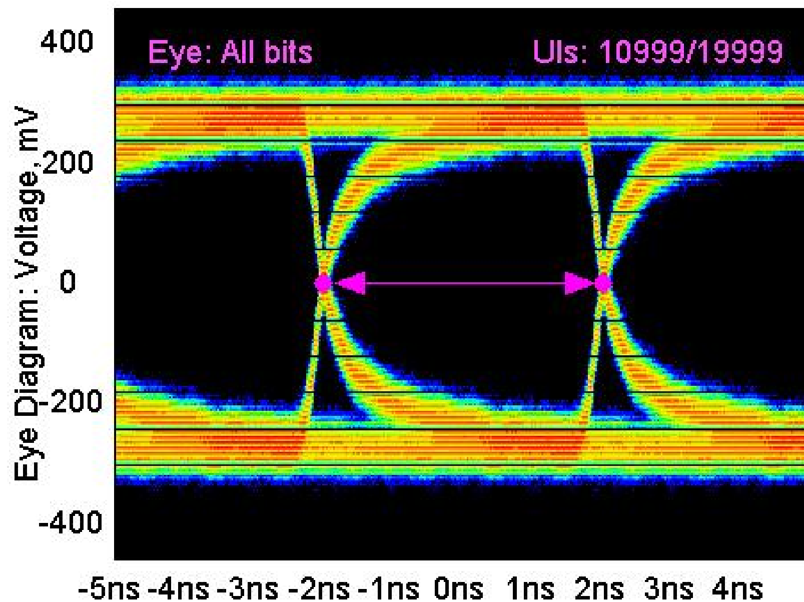


Figure 4.1: Example of an eye diagram obtained for a transmission in a 0.3 m Cu Flex Cable @ 250 Mb/s.

the appropriate logic value.

An ideal eye diagram should be nearly square, but the effect of the propagation of an electromagnetic wave in a medium modifies the eye shape. To obtain the eye diagram for a binary signal, the full data stream is subdivided in samples having the same time duration which depends on the transmission speed. By overlapping the samples, it is possible to generate an envelope having the typical eye-shape shown in Figure 4.1. That envelope contains the complete information on the transmitted data stream and thus it allows to inspect the overall signal integrity.

Depending on the features of the designed circuit and on the transmission line, the eye diagram can be more or less open in the horizontal or vertical direction. The parameters which characterize the eye openings are usually determined statistically, by using the histograms obtained from the envelops. Figure 4.2 illustrates the procedure to describe an eye diagram.

The key quantities describing the vertical eye aperture are [45]:

- **One Level.** Given a determined transmission protocol, the one level is the voltage value which is recognized as a logic one by a receiver. A one level is computed from measurements made between the 40% and 60% regions of the bit period. The histogram shows the statistical processing of the numerical "1" level data.

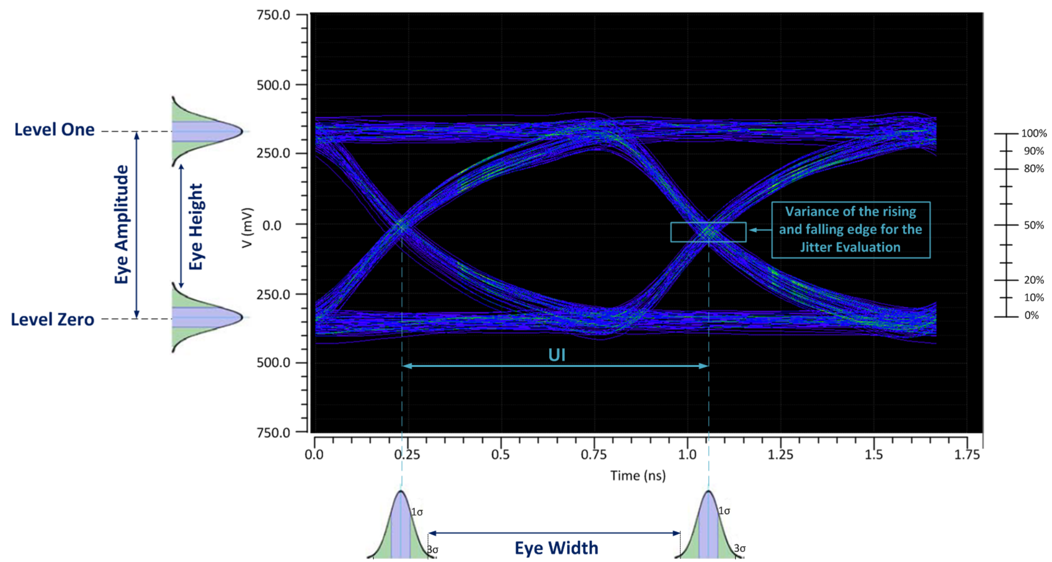


Figure 4.2: Eye Diagram Analysis. Eye amplitude and eye height on the vertical axis give insight on the attuenuation on the cable and on the bit error during a transmission. In the horizontal axis the eye width and the UI quantify the timing error during the transmission.

- **Zero Level.** The zero level is defined similarly to the one level. It is the voltage value which is identified as a logic zero by a receiver within a transmission protocol. The zero level is computed from measurements made between the 40% and 60% regions of the bit period. The histogram shows the statistical processing of the numerical "0" level data.

- **Eye Amplitude.** Figure 4.2 shows the graphical meaning of this voltage parameter. Actually, once that the logic one and zero are determined, the difference between those logic levels determines the eye amplitude. A receiver will react to those difference by transmitting a logic level depending on the eye amplitude. Actually, the eye amplitude gives a feedback even on the attenuation due to the presence of the transmission lines.

- **Eye Height.** The histograms which determine the voltage logic levels are characterized by the standard deviation. By taking the difference between the inner 3 σ voltage points towards the eye crossing, the eye height is determined. From this value it is possible to identify the Bit Error Rate (BER), i.e. the ratio between the wrong received bit and those transmitted. Actually, a wrong transmitted bit will populate the

histogram beyond the 3 σ points shutting off the eye in the vertical axis and thus revealing a transmission error. For the LVDS case a BER $\leq 10^{-12}$ is required.

In the same way as the vertical direction, there are some quantities which characterize the horizontal aperture of an eye diagram:

- **Unit Interval (UI).** This is a common metric used to define the eye horizontal aperture and the other parameters which characterize the eye opening in the time scale. From Figure 4.2, the Unit Interval (UI) is defined as the length of a bit pulse, i.e. the distance between the two eye crossing points. As an example, for a transmission speed of 1 Gb/s the UI is 1 ns whilst for a 5 Gb/s the UI is 200 ps.

- **Eye Width.** The two eye crossing point are located through the histograms in the horizantal axis. The distance between the inner 3 σ points of those histograms identify the eye width.

- **Rise time $\mathbf{t}_r$.** The rise time is a measure of the mean transition time in the upward slope of an eye diagram. Even this parameter is determined by using the histograms in the horizontal axis at 20% and 80% levels or, very often, at the 10% and 90% levels.

- **Fall Time $\mathbf{t}_f$.** The fall time is a measure of the mean transition time in the downward slope of an eye diagram. For the t_f definition, histograms are located at 80% and 20% levels or, correspondly, at the 90% and 10% levels.

- **Jitter.** This quantity characterizes the spread of the eye crossing point in the horizontal axis. It is defined as "the short term variation of significant instants of a digital signal from their ideal positions in time" [47]. Hence, timing jitter is the time deviation from the instant at which the signal transition between two logic levels should be .
  The total jitter (TJ) is the sum of two components:

  $$TJ = DJ + \alpha \times RJ \quad (4.1)$$

  DJ is the peak-to-peak deterministic jitter. It is due to specific problems of the examined system, as the electromagnetic interference, the intersymbol interference (ISI), crosstalk, etc. This is the jitter component which can be minimized by acting on the system and taking precautions during the circuit design. Viceversa, RJ is the unavoidable random jitter component. It is generated by thermal noise, shot noise,

etc... Generally, we assume that the random jitter follows a Gaussian distribution characterized by the width σ and the mean value μ. This Gaussian distribution describes the probability that the eye edges cross the sampling point which is situated in the center of the eye. σ represents the contribution of the random jitter to the total rms jitter, i.e. RJ $= \sigma$ [36].
In absence of deterministic jitter, RJ determines the time position of the eye edges [48]. It can be reduced by decreasing the transition time.

Equation 4.1 is valid under the assumption that the two jitter components are detrmined by indipendent processes. The factor α is linked to the BER required for the link and its value is listed by the Fibrechannel Methodologies for Jitter and Signal Quality (MJSQ). In the ALPIDE pixel chip case a BER $\ll 10^{-12}$ is reqired, then α has to be 14.069 [49].

- **Eye Opening**. This parameter is a way to describe the horizontal eye aperture in function of the BER when the total jitter is extimated. A UI is then defined as: 1 UI = Eye Opening + TJ.

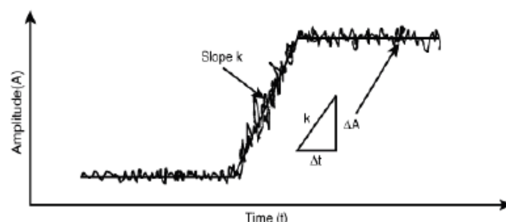


Figure 4.3: The Jitter fenomenon.

The noise and the jitter affect the bit transmission because they move along the t-axis the eye edges whilst the amplitude varies only along the voltage axis.
More generally, if A is the amplitude of a generic physical quantity which is a function of the time characterized by the amplitude A_0 and the noise amplitude ΔA(t), the total waveform can be described as: $A(t) = A_0 + \Delta A(t)$. The noise amplitude sometimes moves up the actual signal whilst sometimes moves it down: in this manner, $\Delta A(t)$ affects the crossing of the ideal signal by the actual signal (Fig.4.3) determining an error in the crossing time. The timing jitter corresponding to ΔA can be calculated by using the linear small-signal perturbation theory [47]:

$$\Delta t = \frac{\Delta A}{\frac{dA_0}{dt}} \tag{4.2}$$

In the equation 4.2, $\frac{dA_0}{dt}$ is the slope or the slew rate of the waveform. Hence, it can be argued that in order to minimize the timing jitter effects, the speed of the system has to be optimized to have very fast rise time as well as fall time. Indeed, the higher the slope the less is the timing jitter [47].

Generally speaking, a way to define how good a device is in transmitting a certain data stream is to look at the amount of jitter introduced. Since any commercial devices are characterized by a jitter amount less than 0.3 UI, this value is taken as a reference to qualify the drivers performance along the thesis.

4.3 Transmission Lines

The connections between the drivers outputs and the receiver inputs and the output pins of the ALPIDE chip with the Read-Out unit, are modeled by real transmission lines. In particular the FPC has been modeled with coupled microstrip line by using a multi-conductor transmission line (mtline) followed by some capacitances and inductances which represent the parasitic effects of the packaging included in the line model. The same is valid also for the twinax that has been associated to a 2-port device.

The mtline has a characteristic differential impedance of Z_0= 100 Ω and its properties are summarized in Tab.4.2 for the FPC used in the IB (Al) and the one used in the OB (Cu). The twinax cable has the same differential charateristic impedance, as reported in the manual [46].

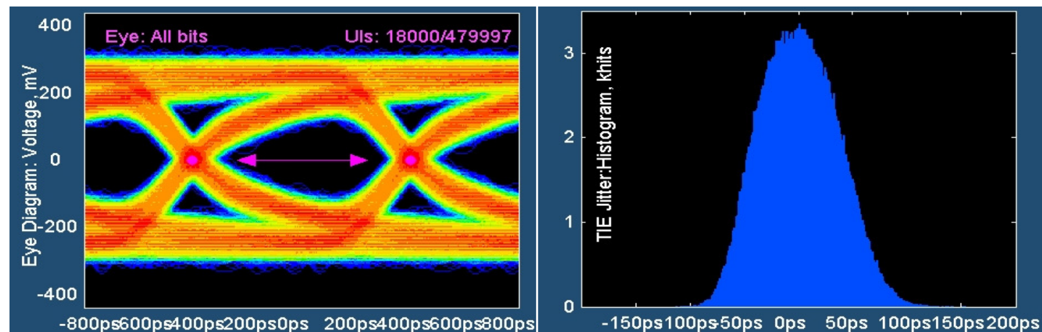
Table 4.2: Mtline Properties

Parameter	**Aluminium**	**Copper**
Numb. of lines	2	
Physical length (mm)	300	250
Multiplicity factor	1	
Rel. dielectric constant of layers (er)	3.4	
Dielectric layer thickness (μm)	50	
Signal line width (μm)	100	
Signal line thickness (μm)	25	18
Signal line height (μm)	25	
Signal line spacing (μm)	25	
Ground plane Thickness (μm)	25	
Signal line conductivity ($\times 10^7$ /m)	3.54	5.96

The FPC metal tracks are deposited on a flexible Kapton®layer. This model for the inner and outer layers FPCs takes into account the geometrical

parameters of the transmission line and reproduces the real physical behavior of the line during the data transmission. Indeed, they introduce the series resistance and inductance per unit length and the parallel capacitance and and conductance per unit length (RLGC model). It has to be pointed out that the geometrical parameters of those line have been carefully set in order to obtain a differential characteristic impedance of Z_0 ±10 % and they are based on the study conduced by the team in charge to develop the FPC.

The Twinax Coaxial cable has been simulated as a 2-port device for which the S-parameters data from the line measurements were available. This cable was characterized in the laboratory since it has to show a good radiation tolerance for the ALICE environment. Furthermore, the electrical characterization of the line allowed to include in the simulations the exact behavior of the line, thus reproducing correctly the attenuation along the cable and as a function of the transmission frequency. Figure 4.4 shows the eye diagram obtained at 1.2 Gb/s when the series between one FPC and the Twinax cable is driven by a standard LVDS signal from the Low Jitter Buffer Clock. Despite of the fact that the eye is well open, the amount of jitter is 0.4



FLEX + TWINAX		
Parameter	**Value**	**stdev**
Eye Height (mV)	352	40
Eye Width (UI)	0.663	0.014
t_r (UI)	0.33	0.05
t_f (UI)	0.34	0.06
Bit Period (UI)	1.0	$2 \cdot 10^{-4}$
TJ (UI)	0.4	

Figure 4.4: Eye diagrams at the ends of the 5.3 m long differential line when the line is driven by the low jitter buffer clock and none pre-emphasis current is added.

UI. Then, the aim in using the pre-emphasis technique is to enhance those jitter value.

4.4 Power Consumption

One of the issue in designing the high speed circuits is the overall power consumption. This is a sum of the static and dynamic dissipations as expressed in the equation 4.3,

$$P_{tot} = P_{stat} + P_{dyn} \tag{4.3}$$

where the second term generally dominates the chip power consumption since it depends on how fast a circuit has to switch by charging and discharging a capacitive load.

In a CMOS logic, where the circuit ouputs perform a full CMOS swing[1], the static power dissipation is given by the product between the circuit output voltage swing and the current which flows from the power supply to ground when there are no transitions between two logic levels. In the ideal case this contribution has to be zero, but the transistors leakage current due to the subthreshold conduction and to the non perfect gate isolation can dissipate power. For a LVDS circuit a current flows continuosly from DVDD to DVSS thus consuming a power given by the product of I^2_{OUT} and the value of the termination resistor R_T.

The dynamic power consumption depends on the short circuit current and on the number of transitions between two logic levels that a determined load C_L has to accomplish. The effect of the short circuit current is indicated as the direct-path contribution and it can be explained easily taking the CMOS inverter as an example (see Figure 4.5) [44].

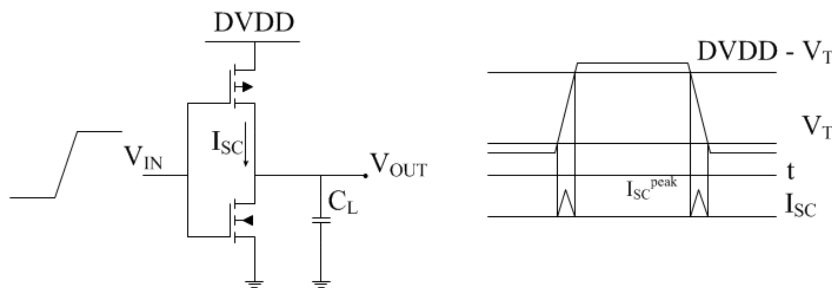


Figure 4.5: Generation of the short circuit current.

A PMOS transmits a strong logic 1 level when its gate is at 0 V whilst a NMOS gives a strong logic 0 level when its gate is at DVDD. In an ideal case, the input transistions of a CMOS inverter between two logic levels happen with zero rise and fall time, thus ensuring that only the PMOS or the NMOS

[1]Full CMOS swing means that the an inpiut or an output of a circuit swings from DVSS to DVDD

is in conduction and respectively charges and discharges a capative load. Unfortunatly, in the real case the non zero slope of an input signal causes both CMOS transistors to be in conduction at the same time, thus allowing a small amount of current I_{sc} to flow from the power supply to the ground. The power dissipation due to this undesired current contribution depends on the circuit switching activity and on the time interval t_{sc} in which the PMOS and the NMOS are in conduction simultaneously [44]:

$$P_{dp} = t_{sc} \cdot DVDD \cdot I_{sc}^{peak} \cdot f = C_{sc} \cdot DVDD^2 \cdot f \tag{4.4}$$

The short circuit current is determinated by the transistor sizes because of the saturation current. Furthermore, the non zero rise and fall time allow the PMOS and NMOS to be in conduction simultaneously. Generally speaking, the design of a CMOS inverter is optimized to have the same rise and fall time. In this case the average power dissipation produced by the direct path is described by [44]:

$$P_{dp} = t_{sc} \cdot DVDD \cdot I_{sc}^{peak} f \tag{4.5}$$

This formula states that this undesired power dissipation is a function of the switching activity (f) as well as the time the PMOS and NMOS are both in conduction, t_{sc}. Furthermore, with reference to Figure 4.5, I_{sc}^{peak} depends on the ratio between the input and output rise and fall time. The inverter input transition has to be faster than the output one to minimize the the direct-path contribution. If the input slope is less steep than the output slope, the short circuit current is maximum for a long time since the PMOS output stays at the high logic level longer than to the low logic level, thus consuming a great amount of current. In the opposite way, if the input slope is steepest than the output one, the CMOS inverter spends a major amount of time in the low logical state than in the higher one, thus minimizing the short circuit current [44]. This fact is explained in Figure 4.6.

The switching power does not depend on the transistor size but only on the transition frequency and on the capacitive load as:

$$P_{sw} = C_L \cdot DVDD^2 \cdot f_{0 \to 1} \tag{4.6}$$

Then, a way to minimize this power contribution can be to reduce the power supply when it is possible or, more easily, to lower the capacitive load.

4.5 M-LVDS Transceiver

The M-LVDS transceiver (see Section 3.4) is used to distribute the clock and broadcast the slow signals as the chip settings and triggers. It will work at

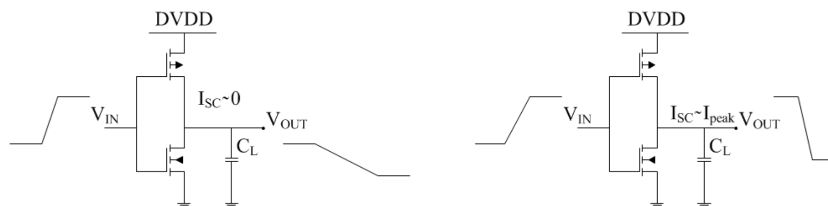


Figure 4.6: Power consumption optmization with a proper choice of the input/output signals slopes. On the left the input slope is steeper than the output one, then the short circuit current is at minimun. On the right, the input signal is slowest than the output and the short circuit current is at maximum.

the frequency of 40 MHz or at a bit rate of 80 Mb/s.
This system is used in chip-to-chip or in Module-to-Module communications. Although the transmission speed here is not an issue, the broadcast along the full hybrid transmission line is worth looking into. As it is already known, the FPCs are connected in series along the Stave/Half Stave. Furthermore the full flex cable has at one end the Twinax cable for the data exchanging with the read-out unit. Each connection between two consecutive flex cables as well as the link with the Twinax represent a point of weakness for the transmission since it can suffer of reflections if the impedance matching is not guaranteed. Furthermore, it has to be taken into account that more than one transceiver loads the transmission line, thus contributing to increase the capacitive load.

The pseudo M-LVDS driver together with the receiver have been fully simulated during the link optimization, before and after the circuit layouts, across process and temperature corners. In particular, the timing and the output voltage characteristics have been determined for the driver and the receiver separatly and they will be summarized in Table A.2. Furthermore, the eye diagram parameters at the driver outputs have been obtained to check the signal integrity along the full transmission line.

Unfortunatly, test measurements on chip-to-chip and Module-to-Module communication are not yet available since the Module is not yet ready at the time this thesis is completed. Indeed, the Module assembly is a delicated work which require a great effort to ensure a perfect result. The first results on the M-LVDS communications are expected in 2016.

4.5.1 pseudo-M-LVDS driver electrical characteristics

The test bench to assess the enable and disable times for the driver is shown in Figure 4.7. To determine them, simulations were done by fixing the input

Table 4.3: Custom pseudo M-LVDS Driver and Receiver Characteristics

Driver Characteristics					
Param.	**Min**	**Max**	**Param.**	**Min**	**Max**
V_{IS} (V)	DVSS	DVDD	t_{pZH}(ns)	0.35	8.4[2]
V_{OS} (SS) (mV)	980	1209	t_{pHZ}(ns)	0.85	1.3
ΔV_{OS} (SS) (mV)	-20	20	t_{pLZ}(ns)	0.85	1.35
ΔV_{OS} (PP) (mV)		150	t_{pZL}(ns)	0.25	0.7
I_{OUT} (mA)	2	8			
Receiver Characteristics					
V_{IS} (V)	DVSS	DVDD			
V_{OUT} (V)	0	DVDD			
t_{pENH}(ns)	0.25	0.55			
t_{pHEN}(ns)	0.7	2.6			

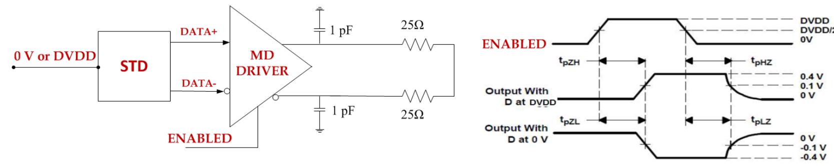
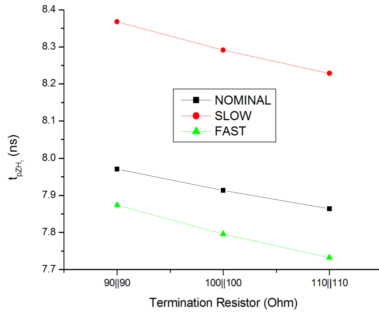


Figure 4.7: Determination of the enable and disbale time for the pseudo M-LVDS driver with their definitions.

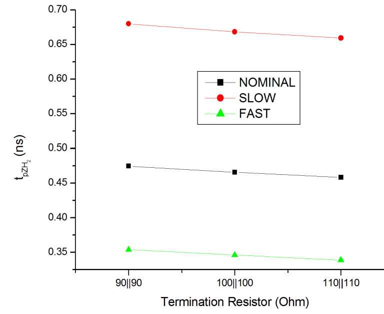
levels at the voltage value of DVDD or 0 V which correspond to a trasmission of a logic 1 and a logic 0 respectively. A square wave was used for the ENABLED signal. Studies were carried out changing the driver output current I_{OUT} and the termination resistor value to study how the driver behavior modifies when the driver strenght and the resistor load change. The value of the termination resistor was varied in the range [90 | | 90 ÷110 | | 110] Ω since the resistive load has a tolerance about 10% around the nominal value of 100 | | 100 Ω. Furthermore, the power supply changes across corners, as shown in Table 4.1.
Those simulations take into account that the enable and disable inputs will be transmitted from the digital periphery to the driver. Therefore, the influence of the connection wires was modeld as delay lines by using the distributed RC model.

Figures 4.8 and 4.9 illustrate the results on the enable time (t_{pZH} and t_{pZL}) and disable time (t_{pHZ} abd t_{pLZ}) when the driver output current is ∼ 8 mA. Here the ENABLED signal is a CMOS square pulse with a rise and fall times of 100 ps. The results show that t_{pZH} and t_{pZL} as well as t_{pHZ} and t_{pLZ} slightly vary around the value obtained with the typical 100 | | 100

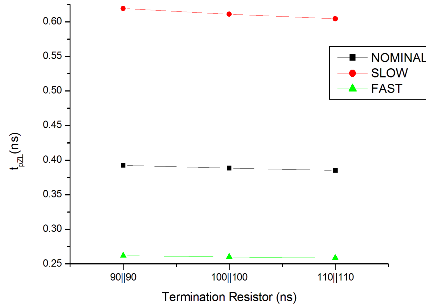
Ω resistor. Furthermore, those parameters show the same behavior across corners. It has to be noted that when the driver is turned on for the first time it needs more time to be enabled since each capacitance in the driver has to be charged on. For this reason in the Table of characteristics a maximum value of 8.4 ns is reported.



(a) High impedance to high level output t_{pZH_1} - First turn on.



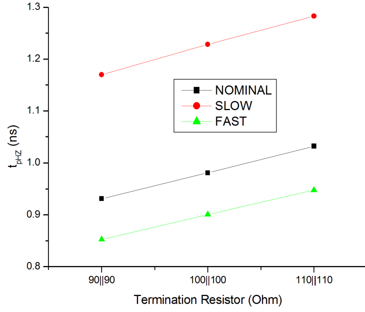
(b) High impedance to high level output t_{pZH_2}- Second turn on.



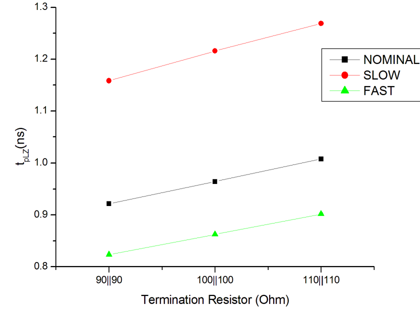
(c) High impedance to low level output t_{pZL}.

Figure 4.8: Enable time obtained by the simulations across corners with the resistive termination load ranges between (90 | | 90 ÷110 | | 110) Ω. Here the driver output current is ∼ 8 mA.

Conversely, it does not matter if the driver is turned off for the first or the second time, since it will need the same time interval to be switched off. As it is shown in Figure, the variation of t_{pHZ} abd t_{pLZ} is more evident here than the enable time but it still remains in the range of ±10% around the typical value of 0.95 ns. In the same way, the delay from the driver input to the receiver output has been assessed at variuos driver output current



(a) High level to high impedance t_{pHZ}.



(b) Low level to high impedance output t_{pLZ}.

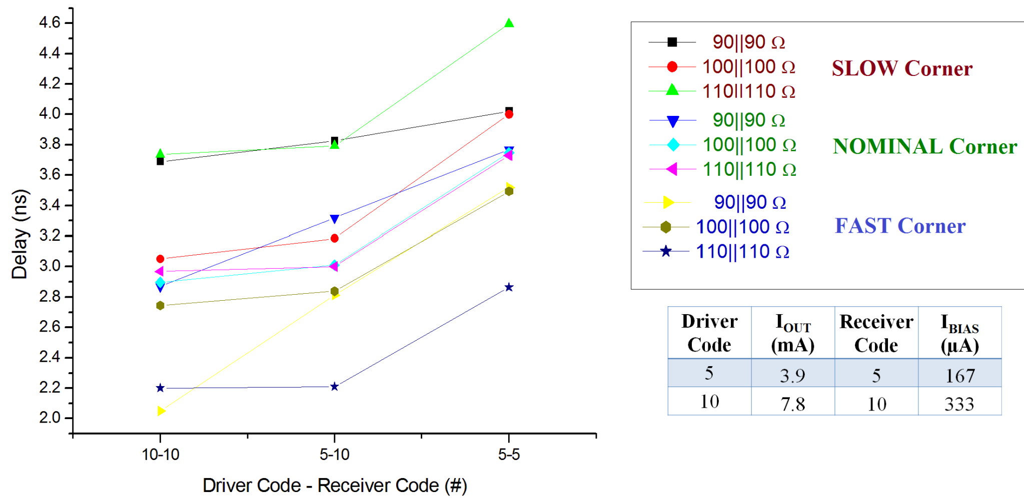
Figure 4.9: Disable time obtained by the simulations across corners with the resistive termination load ranges between 90 | | 90 ÷110 | | 110 Ω. Here the driver output current is ∼ 8 mA.

and receiver bias current. Figure 4.10 illustrates the simulation results when the output driver current varies from 4 mA (Driver DAC Code 5) to 8 mA (Driver DAC Code 10) and the receiver bias current varies from 167 μ A (Receiver DAC Code 5) to 333 μA (Receiver DAC Code 10). Since a 4-bit DAC selects the receiver current for the PMOS and the NMOS input differential pair, when a receiver code is fixed the same amount of current will flows in the two branches (see Figure 3.14). Furthermore, the effect of the termination resistor mismatch has been investigated. What it is possible to learn from those simulations is that, the greater is the termination resistor, the larger the time needed to transmit a logic voltage value at the receiver output and the situation is worse at low driver strength. All the electrical driver characteristics were determined taking into account the variation of process and mismatch. For the sake of semplicity, the results are summarized in Table 4.3.

4.5.2 pseudo-M-LVDS electrical receiver characteristics

The second block of the pseudo M-LVDS transceiver was characterized in a similar way to the driver, across corners and process and mismatch variations. The results are summarized in Table 4.3. Here the results on the receiver time response are shown.

Figure 4.12 illustrates the set up for the determination of the enable and



Driver Code	I_{OUT} (mA)	Receiver Code	I_{BIAS} (μA)
5	3.9	5	167
10	7.8	10	333

Figure 4.10: Signal delay from the driver input to the receiver output across corners. Simulations have been done by varying the driver output current I_{OUT} and the receiver bias current I_{BIAS} together with the termination resistor.

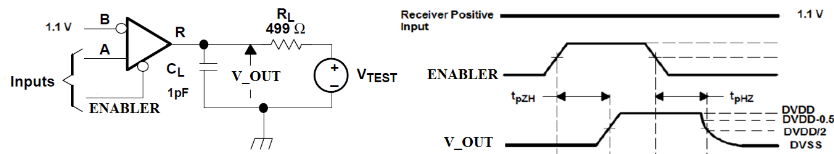
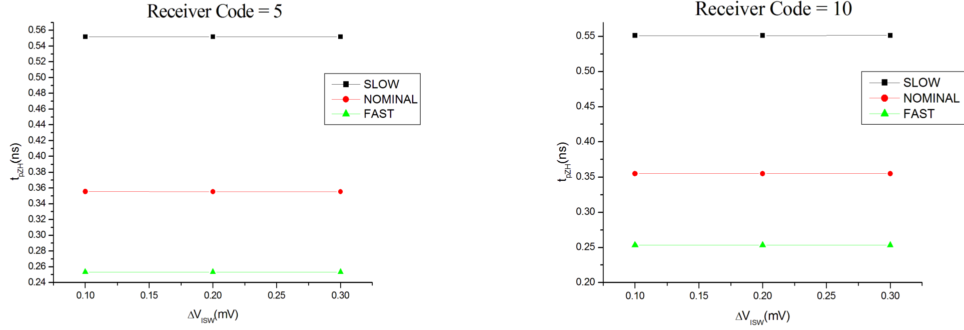


Figure 4.11: Test bench for the determination of the receiver enable and disable time.

disable time for the receiver and the values definition are illustrated. The same square wave used for the driver was used for the ENABLER to check the receiver speed response. As said in the previous chapter, it has to be pointed out that this M-LVDS receiver is not a three-state buffer. Indeed, this architecture takes advantage of an AND logic at the receiver output to fix it at 0 V (logic 0), thus avoiding the indesirable switching activity of the circuit in case of an idle bus condition. Then, what is called here enable time t_{pZH} is the time needed to the receiver output to transmit a logic 1 when the ENABLER swings from 0 V to DVDD. In the same way, the disable time t_{pHZ} is the time taken from the receiver to restore the logic 0 value at its output.

Simulations were carried out by varying the receiver input voltage swing to take into account that the voltage swing across the differential transmission line depends on the driver strength. Even in this case the connection between the digital periphery and the receiver enable circuit has been taken into

account with the same distributed RC model set up for the driver.



(a) Receiver Code = 5, i.e. the receiver bias current is $\sim$ 167 μA.

(b) Receiver Code = 10, i.e. the receiver bias current is $\sim$ 333 μA.

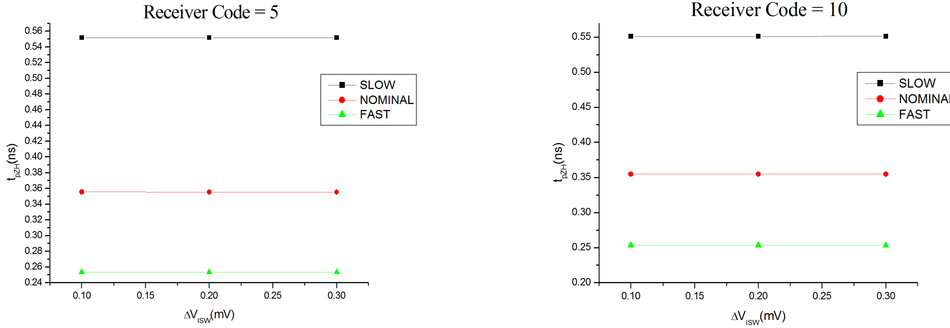
Figure 4.12: Receiver enable time for different bias currents. The behavior of t_{pZH} is constant with the receiver input volge swing ΔV_{ISW} but it show a big variation across temperature and process corners.

The results in Figure 4.12 display that t_{pZH} and t_{pHZ} are almost constant with the receiver input voltage swing. To make a difference is the receiver bias current across corners. Actually, the highest value for the enable and disable time correspond to the slow corner. Investigations on those discrepancy across corners on t_{pZH} and t_{pHZ} shown that the receiver has a slow time response when the actual bias current is less than its nominal value, as in the slow corner case. Fortunately, to solve this issue it is possible to change the 4-bit DAC settings to select a suitable current value which guarantees a fast time response.

4.5.3 M-LVDS transceiver performance on slow speed data transmission.

The M-LVDS transceiver behavior was fully simulated before and after the layout of the blocks. Indeed, in the last case all the parasitics effects, like the additional capacitances and the resistances due to the physical routing and the placement of the circuit components, were taken into account to study the M-LVDS transmission in a more realistic situation. Furthermore, to account for the manifacturing process, simulations across corners were carried out even to account for the tolerance on the termination resistor value.

Since the transceiver block is used for Module-to-Module and chip-to-chip communications, the test benches with the IB and the OB chips arrangements



(a) Receiver Code = 5, i.e. the receiver bias current is ~ 167 μA.

(b) [Receiver Code = 10, i.e. the receiver bias current is ~ 333 μA.

Figure 4.13: Receiver disable time for different bias currents. t_{pHZ} has the same behavior as t_{pZH}.

have been adopted to verify the signal integrity along the full transmission line. Furthermore, simulations were executed to ensure that the slow signals are accurately broadcast at different driving strength and receiver bias current.

The test results obtained with the Outer Barrel arrangement are presented in the following to show that this M-LVDS transceiver can be a suitable solution for the ITS upgrade. Indeed, the OB arrangement is the most challenging situation in which the transceiver has to work. As illustrated in Section 3.2.2, the outermost layers consist of a Half Staves made up of seven Modules for a total length of 1.5 m. Indeed, each Module consists of two rows of seven chips soldered on a 250 mm Cu FPC. Furthermore, one Half Stave is linked to the patch panel through the 5 m Twinax Cable. Then, any slow speed signal which is broadcast from the RU to the Modules or viceversa has to be transmitted with a good signal quality at a total distance of 6.5 m, in the worse case.

The set up arranged for the simulations is shown in Figure 4.14. In this test the connections between adjacent Modules were made by wire bonds. This solution represents the worst case from what concerns impedance variations. Here, only the slow speed driver of the Master chip in the Module 0 is enabled to transmit data (ENABLED = DVDD) whilst every receiver linked to the transmission line can get the message (ENABLER = DVDD).

To test the signal integrity, a 80 Mb/s Pseudo Random Binary Sequence (PRBS) was used as a data stream to simulate a slow control signal whilst a 40 MHz clock was adopted to analyze the clock transmission. It has to be pointed out that in the test bench the models of the pads over logic neverthe-

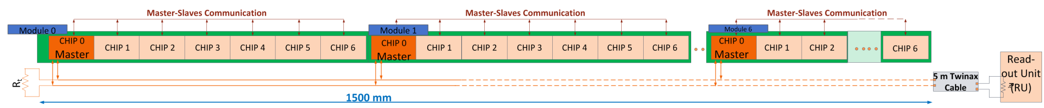


Figure 4.14: Outer layers arrangement. This is an example of the test bench adopted to check the signal integrity along the transmission line.

Table 4.4: List of outputs at which the signal integrity has been checked. D = Driver, R = Receiver, E = Enabled, D = Disabled.

Module	**D**	**R**	**Output**	**Line Segment**
0	E	E	(DCTRLP-DCTRLN)<0>	Module 0 - Module 1
1	D	E	(DCTRLP-DCTRLN)<1>	Module 0 - Module 2
2	D	E	(DCTRLP-DCTRLN)<2>	Module 0 - Module 3
3	D	E	(DCTRLP-DCTRLN)<3>	Module 0 - Module 4
4	D	E	(DCTRLP-DCTRLN)<4>	Module 0 - Module 5
5	D	E	(DCTRLP-DCTRLN) <5>	Module 0 - Module 6
6	D	E	(DCTRLP-DCTRLN)<6>	Module 0 - Module 7
–	D	E	(OUTTWINAXP-OUTTWINAXN)	Module 0 - RU

less the wire bond between the FPCs were taken into account together with the geometrical parameters of the FPC and the S-parameter of the Firefly Twinax Cable. Table 4.4 list the segment of the FPC or the Twinax at which the signals were sampled.

Figure 4.15 shows the eye diagrams captured along the transmission line when the termination resistor is 100 | |100 Ω, the driver output current I_{OUT} is ∼ 8 mA whilst the receiver bias current is ∼ 333 μA. Since the M-LVDS is a differential transmission, those eye diagrams represent the quality of the differential signal (DCTRLP-DCTRLN). Then, in an ideal case with 8 mA of current on the line and with a overall 50 Ω termination resistor, the voltage swing at the receivers inputs should be 400 mV, i. e. 800 mV peak-to-peak of differential voltage. Since the PRBS signal is transmitted at 80 Mb/s, the UI should be 12.5 ns.

Clearly, the case illustrated before is not ideal. Actually, the presence of the transmission lines, the attenuation along the cables and the not perfect impedance matching affect the signal transmission in the vertical and horizontal axis. In particular the effect of the reflections is evident in the eye edges.

The simulation results are summarized in Figure 4.16 where the behavior of the vertical and horizontal aperture nevertheless the total jitter along the full transmission line are presented.

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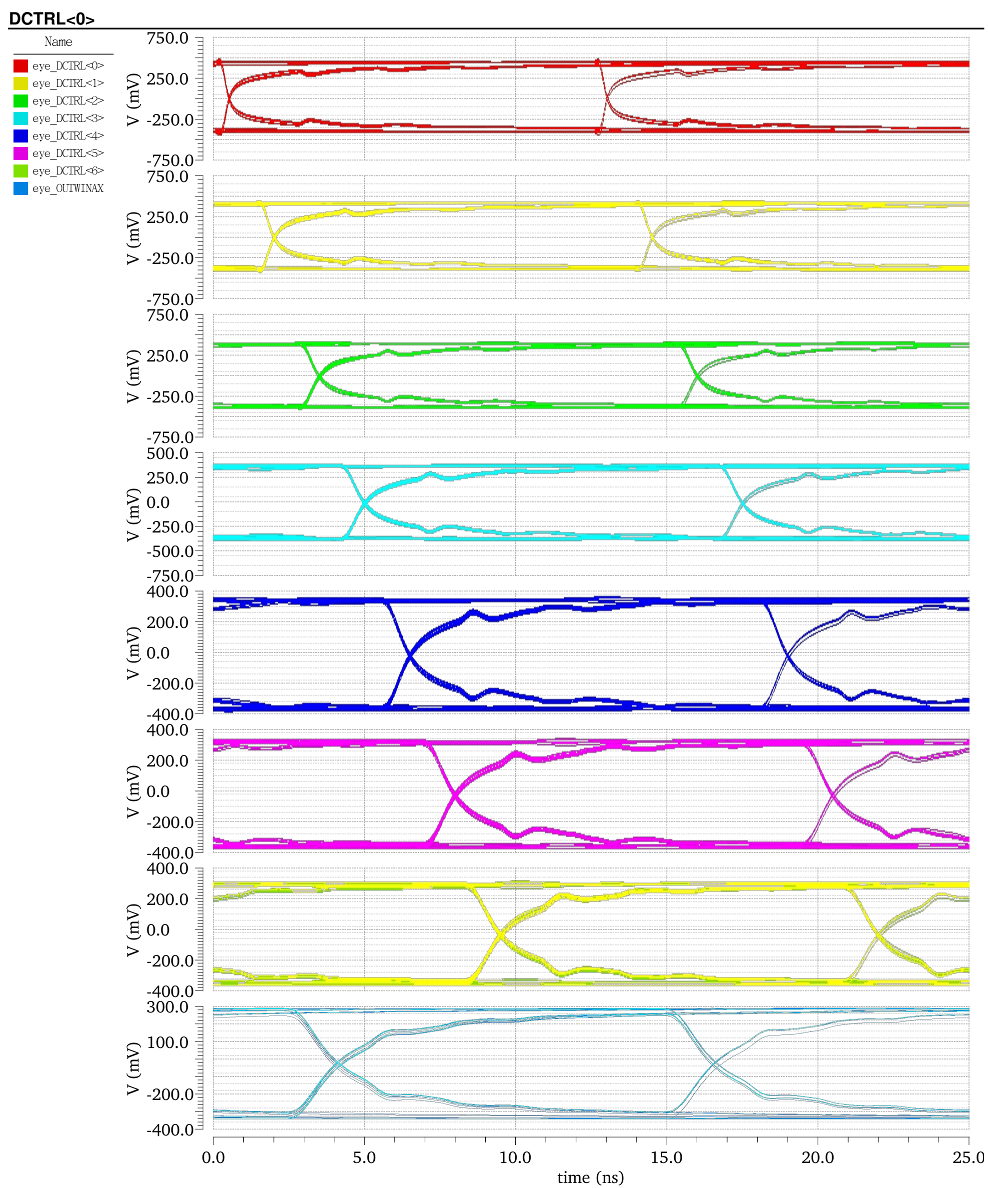

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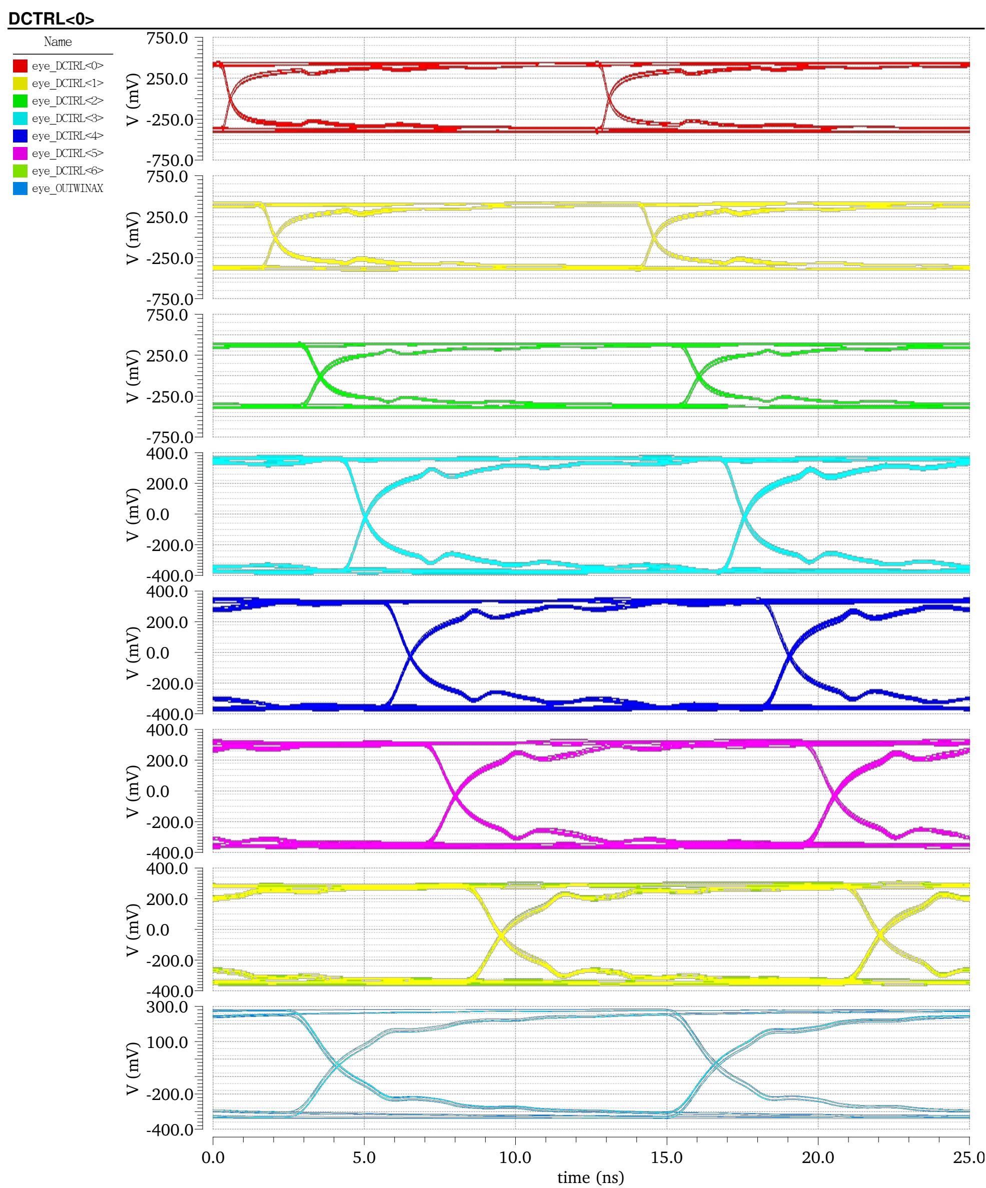
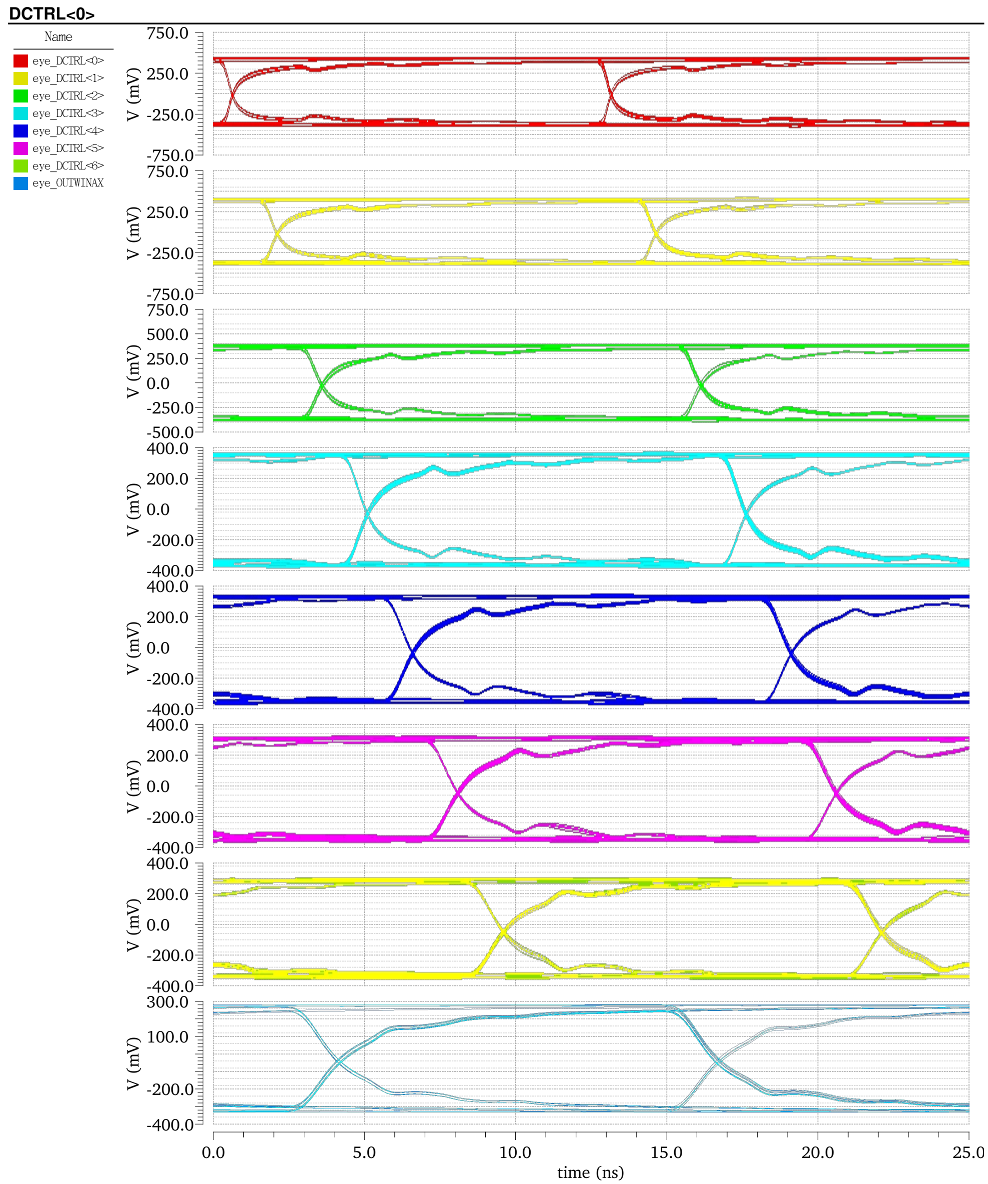
(a) Fast Corner.



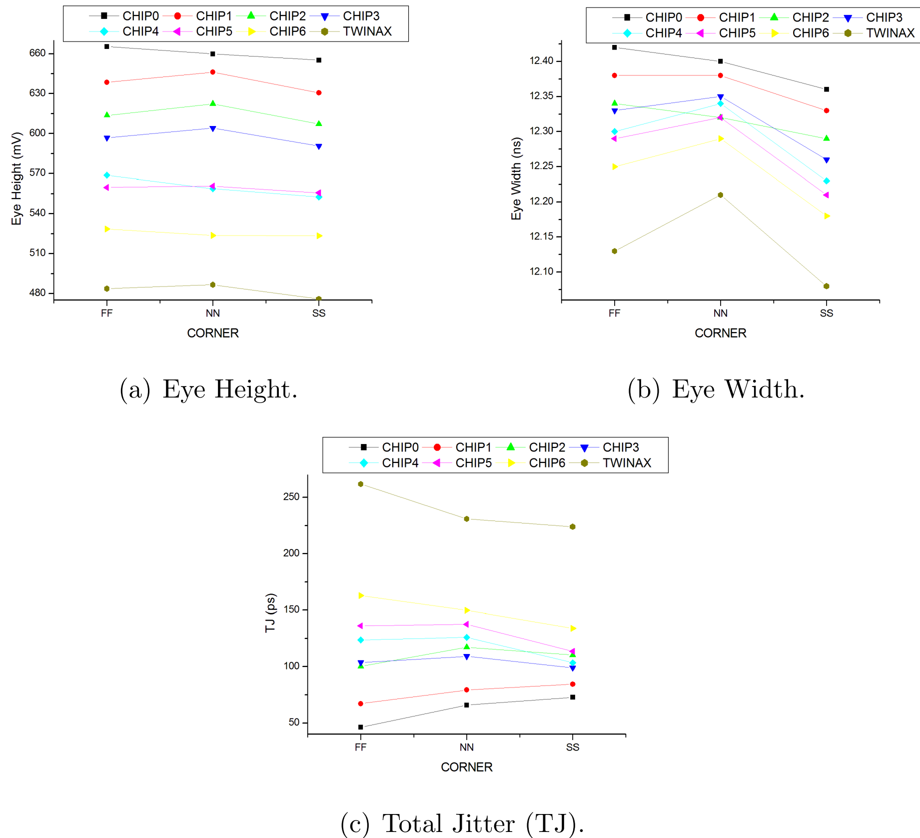
(b) Nominal Corner.



(c) Slow Corner.

Figure 4.15: Eye diagram across corners along the line.

Because of the propagation in a medium, the eye height decrease along the flex cable and mainly along the Twinax cable. However, those voltage difference at the receiver inputs allows the transmission of the correct bit stream at the receiver output as it was verified by checking the receivers outputs. The variation on the eye width is not really crucial for the transmission quality. In the worse case the eye width is 12.05 ns in view of a UI of 12.5 ns. This is due to the total jitter which increases moving toward the RU because of the signal reflections. Along the varius segments of the differential transmission line, the FPCs and the the Twinax cable, the TJ is well below the value of 0.3 UI. Actually, even at the input of the RU, i.e. at the output of the Twinax, the jitter value is about 250 ps corresponding to 0.02 UI. Then, this M-LVDS transceiver is a good candidate to be used for the clock and slow control distribution for the ALPIDE pixel chip.



(a) Eye Height.

(b) Eye Width.

(c) Total Jitter (TJ).

Figure 4.16: Transceiver performance on signal transmission. The output driver current is $I_{OUT} \sim 8$ mA, the receiver bias current is ~ 333 μA and the receiver termination resistor is $100 \,||\, 100$ Ω.

Table 4.5: ID of the receivers outputs. D = Driver, R = Receiver, E = Enabled, D = Disabled.

Module	**D**	**R**	**Output**	**Line Segment**
0	D	E	OUT 0	RU - Module 0
1	D	E	OUT 1	RU - Module 1
2	D	E	OUT2	RU - Module 2
3	D	E	OUT3	RU - Module 3
4	D	E	OUT4	RU - Module 4
5	D	E	OUT5	RU - Module 5
6	D	E	OUT6	RU - Module 6

The clock distribution to the Modules and to the Slave chips was investigated by varying the driver strenght and the receiver bias currents. As already said, to have a fast response of the receiver, a suitable current has to be set in this device. With the same test bench as before, a 40 MHz clock signal has been sent from the RU to the Half Stave.

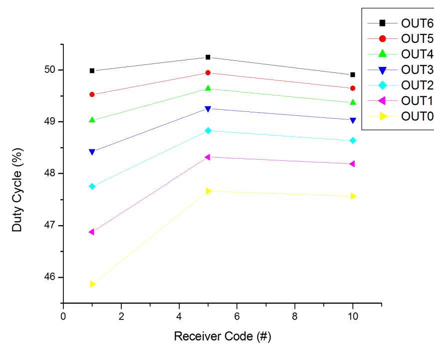
In Table 4.5 the ID of the outputs are listed. Simulations shown that the duty cycle varies in the range (45-50)%. As an illustrative example, the duty cycle of each receiver connected to the transmission line at different receiver bias current is illustrated in Figure 4.17 in the worst case condition. Actually, the driver strength in the RU is fixed to 5.5 mA and the termination resistor is the lowest one, 90 Ω (i.e. an overall resistance of 90 | | 90 Ω).

4.5.4 Transceiver Power Consumption

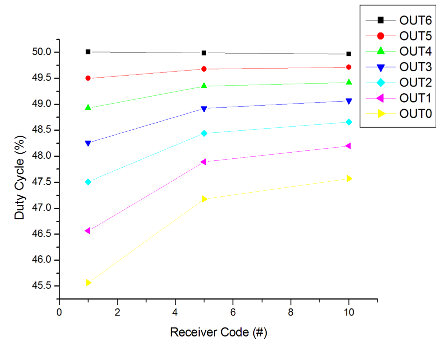
The transceiver power consumption has been simulated in detail since the ALPIDE pixel chip contains three of those devices and they can affect the overall power consumption.

Simulations were done in variuos operating chip conditions to have a precise idea of how much power a Master chip and a Slave chip will consume . Actually, the difference between a Master and a Slave in this case is that the former has the driver and the receiver enabled whilst the second can only receive the signal. In the same way, in a Module-to-Module communication only one of the Master chips has both of the two transceiver components enabled. The other Master in a Stave/Half Stave will have only the M-LVDS receiver enabled until one of them will be in charge to broadcast a signal.

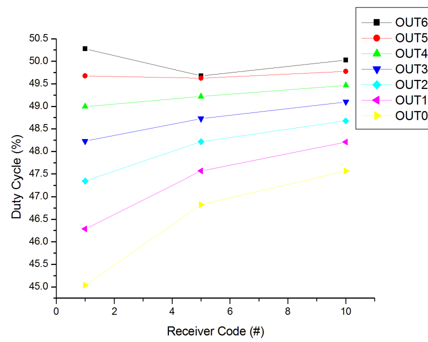
For a chip which has both the driver and the receiver active and which works at a well defined data rate, the overall power consumption depends on the driver strength and on the switching activity of the circuits. Actually, the



(a) Fast Corner.



(b) Nominal Corner.



(c) Slow Corner.

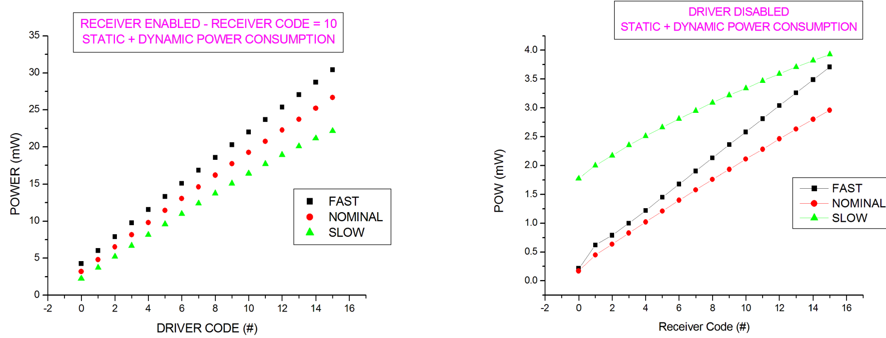
Rec. Code	$I_{BIAS,Fast}$	$I_{BIAS,Nominal}$	$I_{BIAS,Slow}$
1	31.17	31.7	31.3
5	157	155	152
10	320	306	297

(d) Receiver Bias current values.

Figure 4.17: Clock distribution. In the plots the duty cycle of the receivers connected to the transmission lines.

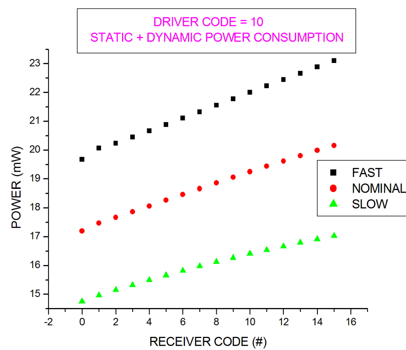
larger is the current steered by the driver, the greater is the power consumed by the transceiver. In the same way, the greater is the switching activity, the bigger is the dynamic power consumption.

Figure 4.18 shows the total power consumption (static+ dynamic) needed to the M-LVDS transceiver when the driver drives a single receiver which has the bias current of ∼333 μA (receiver code = 10) and the power consumption when only the receiver is enabled.



(a) Driver Enable - Receiver Enabled (Bias current ∼ 333 μA.)

(b) Driver Disabled - Receiver Enabled.



(c) Driver Enabled (I_{OUT} ∼ 8mA) - Receiver Enabled.

Figure 4.18: Static + Dynamic M-LVDS transceiver power consumption. The receiver code 10 corresponds to the bias current of ∼ 333 μA.

Here the transmitted data stream is a 40 MHz clock, which is the worst case condition since the switching activity of the driver and the receiver will be at maximum. As it is possible to argue from the graphics, the driver is the most power hungry circuit. In that regard, it has to be pointed out that in the power consumption of the transceiver even the power consumed by the

single ended-to-differential block (see Figure 3.7) is included when the driver is enabled. This block has the same switching activity of the driver but it drives a bigger load (the driver inputs) from 0 V to DVDD, thus contributing to consume power.

4.6 pseudo-LVDS driver

The two versions of the pseudo-LVDS drivers were fully simulated and tested. The first driver implementation was submitted with a dedicated test chip whilst the second one was integreted in the full DTU chain to be tested in a separated test chip and it was also integrated in the third ALPIDE prototype.

Simulations were done to verify the circuits performance across process corners and mismatches. Beyond the driver eletrical characteristics of the two drivers which are summarized in Table 4.6, it is fundamental to look at the signal integrity at the high speed rate to check if the drivers satisfy the ITS requirements. For this reason the eye diagrams have been captured along the

Table 4.6: Electrical characteristics of the first and second pseudo-LVDS driver with pre-emphasis.

	First Impl.		**Second Impl.**	
Parameter	Min	Max	Min	Max
V_{IS} (V)	DVSS	DVDD	DVSS	DVDD
V_{OS} (SS) (V)	1.00	1.20	0.96	1.21
ΔV_{OS} (SS) (V)	-50	50	-50	50
$\|V_T\|^3$ (mV)	268.5	410.5	268.5	454.8
|Short Circuit Current | (mA)	$\leq$14			

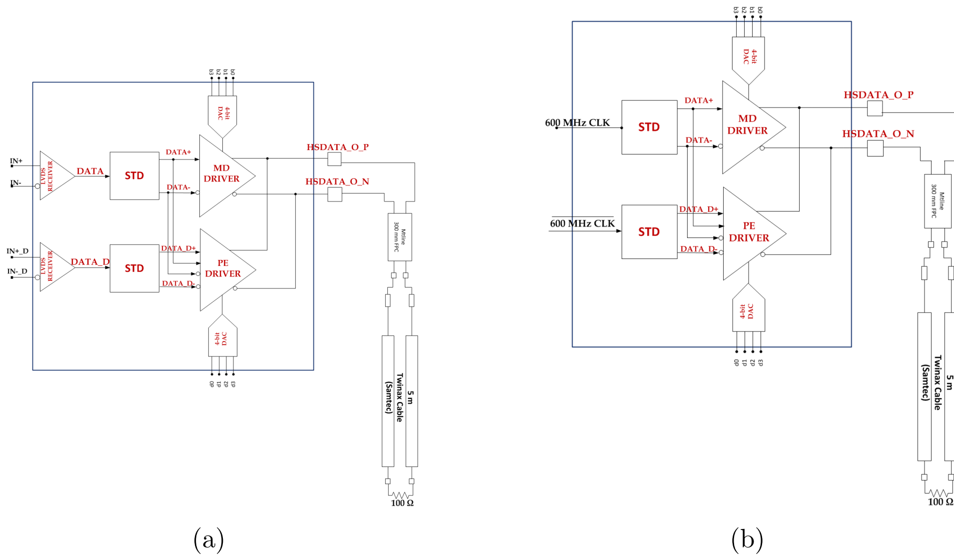
transmission line segments during the simulations and the lab measurements and the results are reported in the next paragraph.

4.6.1 Simulations on the first pseudo-LVDS driver implementation.

The purpose of the first driver implementation was to verify that this pre-emphasis technique works and that it guarantees a good signal quality at end of the Twinax cable. For this reason the test bench illustrated in Figure 4.19 has been used to control the signal integrity along the full transmission line.

The examples of the simulations reported above are executed by taking into account the parasitics effects. Indeed, undesired capacitances and resistances are introduced in the circuit layouts. Furthermore, a model for the

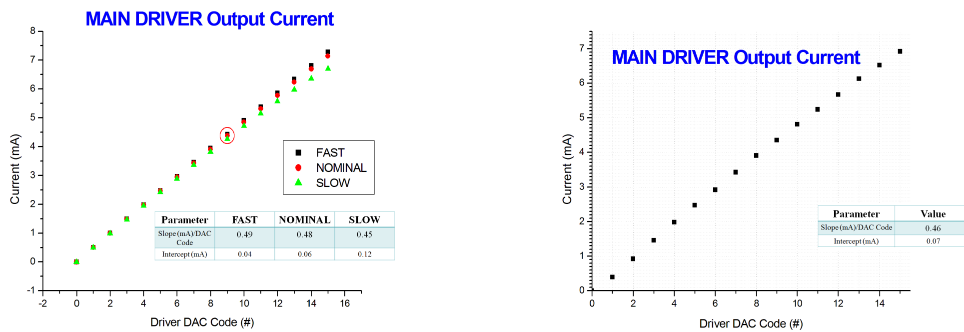
power, ground and substrate lines accounts for the voltage drop along those lines and the coupling between them.



(a) (b)

Figure 4.19: Test bench for the simulation of the first driver implentation with the pre-emphasis.

Figure 4.20(a) shows the Main Driver output current versus the driver DAC code. This DAC circuits will allow the driver to deliver a current up to 8 mA. Anyway, since this driver was designed to steer a maximum of 5 mA of current, the maximum DAC driver code which can be used is about 10.



(a) Simulated main driver output current versus DAC code.

(b) Measured main driver output current versus DAC code la figura non ha caption

Table 4.7 summarizes the parameters of the PRBS and the clock signals used for the circuits simulations to explore two different situations. A PRBS

Table 4.7: Input signals parameters for the simulation of the first driver implementation.

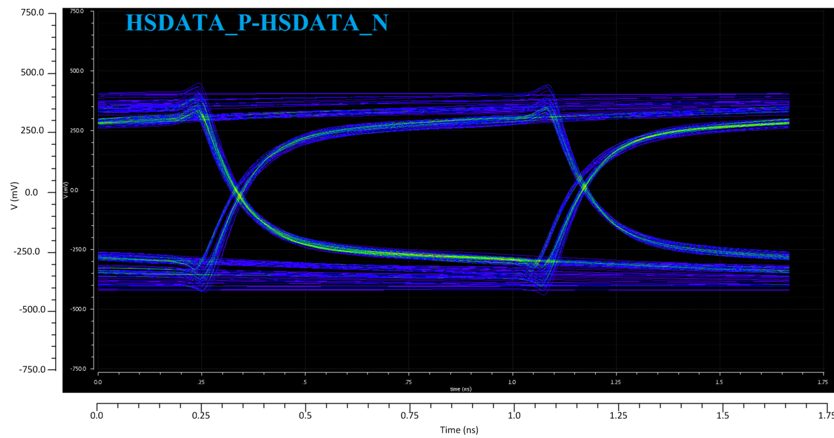
PRBS			CLK		
Parameter	DATA+	DATA_D+	Parameter	CLK	$\bar{CLK}$
V_{HIGH} (V)	DVDD	DVDD	V_0(V)	DVSS	DVDD
V_{LOW} (V)	DVSS	DVSS	V_0(V)	DVDD	DVSS
Bit Period (BP) (ps)	833.3	833.3	T_{CLK}	1.667	1.667
t_r(ps)	70				
t_f(ps)	70				
Delay (ps)	0	BP-10	Delay (ps)	0	$T_{CLK}/2$

will activate the pre-emphasis current randomly, since this data stream is randomly generated. In case of a clock signal, a bit transition happens twice in a period since each period consists of a logical 0 and a logical 1. Thus, the pre-emphasis circuit will add or subtract the I_{PED} at each half period. Furthermore, by using a clock waveform it is possible to nullify the Intersymbol Interference (ISI).

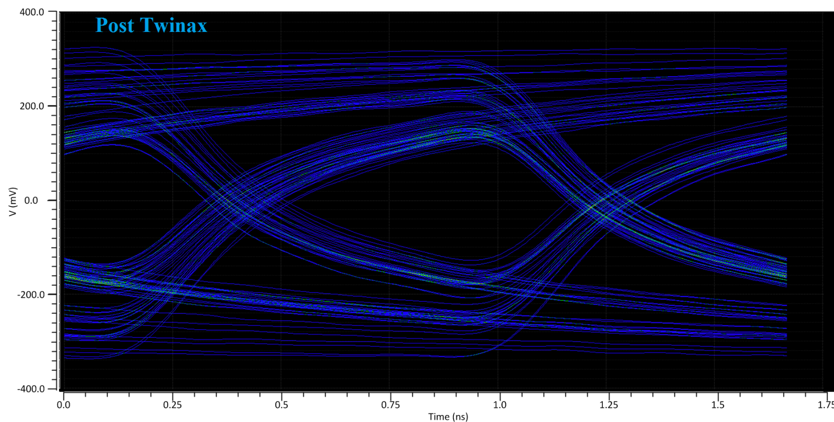
Figure 4.20 shows how appear in the nominal case the eye diagrams of the differential signals at the driver output and at the end of the Twinax cable when the MD steers a current of ∼4.4 mA (Code D = 9) and no pre-emphasis current is added (PE DAC Code = 0). Here, the termination resistor is 100 Ω.
As it is possible to see, even if the eye diagram at the direct driver output is well open, after the 5.3 m long transmission line it is difficult to distinguish between two different logical values since the envelops are spread along the entire vertical and horizontal axis. Actually, the bandwidth limitations introduced by the Twinax cable do not allow to properly reconstruct a signal.

The use of the pre-emphasis technique improves the transmission quality, as illustrated in Figure 4.21. These eye diagrams represent the same outputs as before, in the nominal case, when 50% of pre-emphasis current is added. Here the current steered by the MD is 4.4 mA whilst the pre-emphasis current is ∼ 2.2 mA.

As it is shown, the eye diagram at the far ends of the Twinax cable is still well open and the high and low logical levels are well separated. The presence of the reflections inside the transmission lines is revealed by the spread of the rising and the falling edges at the driver outputs. In any case, this effect does not limit the driver performance since the total jitter (TJ) is well below the 0.3 UI commercial value. Figure 4.22 shows the waveforms of a transmitted clock at the end of direct driver ouput and at the end of the



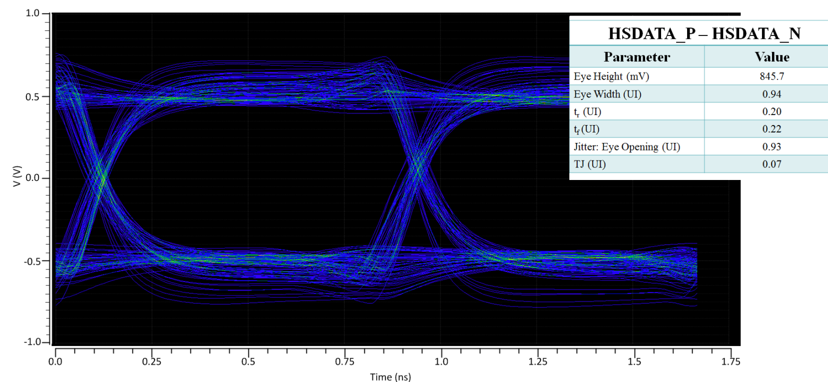
(c) Differential signal at the driver output.



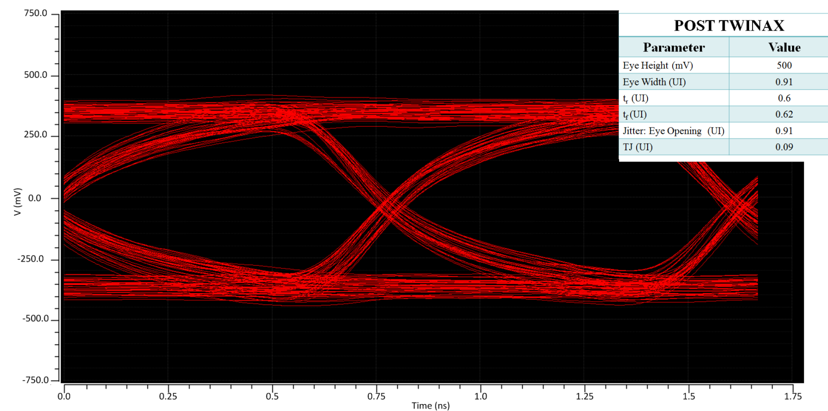
(d) Differential signal at the Twinax output.

Figure 4.20: Eye diagrams captured at the input and at the ouptut of the full 5.3m long differential transmission line.

Twinax cable. Here an I_{PED} of 2.2 mA helps the driver output current of 4.4 mA to drive the full line. As it is possible to see, the clock signal travels for $\sim$ 22 ns before reaching the end of the 5.3 m cable. 1.56 ns of this delay comes from the Al FPC which is 0.3 m whilst the biggest contribution of 21 ns is provided by the Twinax cable. The Post-Twinax eye diagram in Figure 4.23 shows that the eye is well open despite of the fact that the signal is attenuated by the propagation along the transmission line. Even in this case the TJ introduced by the driver and the transmission line is well below 0.3 UI, then allowing the chip submission.



(a) Differential signal at the driver output.



(b) Differential signal at the Twinax output.

Figure 4.21: Eye diagrams captured at the input and at the ouptut of the full 5.3 m long differential transmission line @ 1.2 Gb/s

4.6.2 Test measurements on the first pseudo-LVDS driver implementation.

The test chip submitted for the pseudo-LVDS driver with the pre-emphasis is shown in Figure 4.24. The purpose of this test chip is to verify or reject the simulation results and to see at what extent this driver prototype is a suitable option for the ALPIDE pixel chip. For this reason the test chip contains:

(a) two single ended LVDS receivers which feed the driver and the pre-emphasis inputs. In this way it is possible to send the data stream DATA and the delayed copy DATA_D to study the circuit behavior with a PRBS since it represents a typical data stream for this kind of pixel chip.

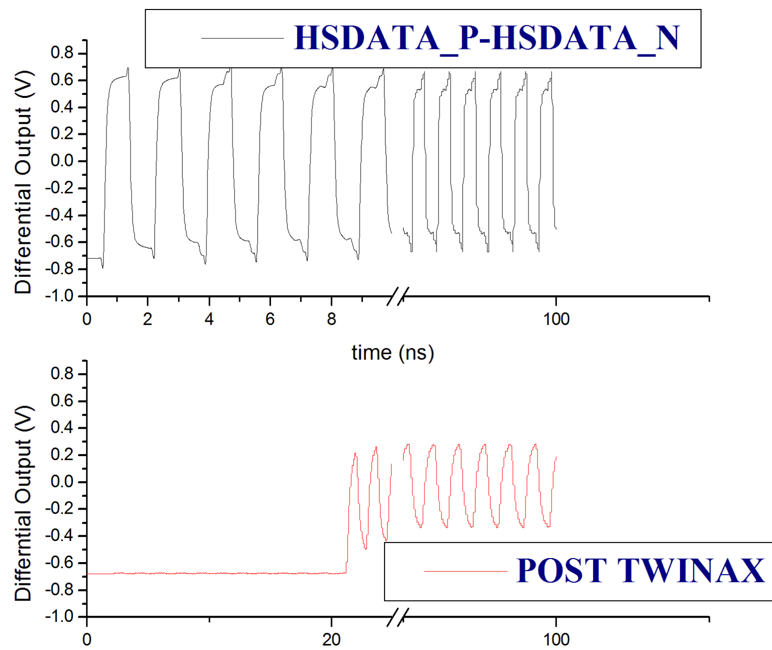
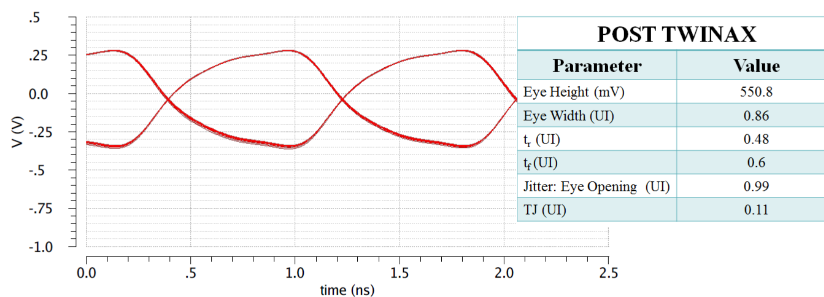


Figure 4.22: Transmission of a 600 MHz clock along the full 5.3 m long differential line.

(b) a PLL with a custom delay line and the driver with pre-emphasis to study the driver response to a 600 MHz clock.

During the test measurements the effective current I_{MD} flowing out from the MD has been obtained from a measure of the driver output swing. Actually, it is not possible to add a current probe to measure I_{MD} directly since a break of the link between the driver outputs and the trasmission line degrades the output signals. The driver current versus the DAC code is shown in Figure 4.20(b). As it is possible to see, in this way the maximum current provided by the driver is 6.9 mA. This is a non optimal situation for the circuit since



POST TWINAX	
Parameter	**Value**
Eye Height (mV)	550.8
Eye Width (UI)	0.86
t_r (UI)	0.48
t_f (UI)	0.6
Jitter: Eye Opening (UI)	0.99
TJ (UI)	0.11

Figure 4.23: Eye diagram of the clock signal at the end of the Twinax cable.

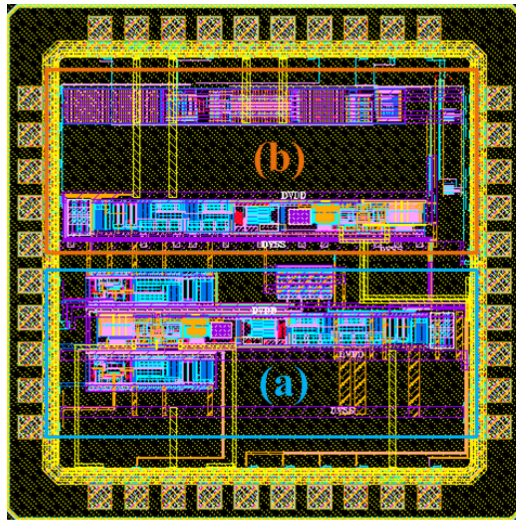


Figure 4.24: First implementation of the pseudo-LVDS driver with pre-emphasis. (a) The driver and the pre-emphasis circuits inputs are feed by the output of the two receivers. (b) The output clock of the PLL feeds directly the driver and the pre-emphasis circuit and the custom delay line.

the transistors are not guaranteed to work properly. For this reason, the test measurement were executed with driver code under 10.

A low jitter buffer clock was used to feed the receiver inputs since it replicates the signal at its differential inputs (see Figure 4.25). Then, two custom delay lines were made in the lab by using two Cu coaxial cable to obtain a delayed copy of those replica. The delay of the short lines is (844

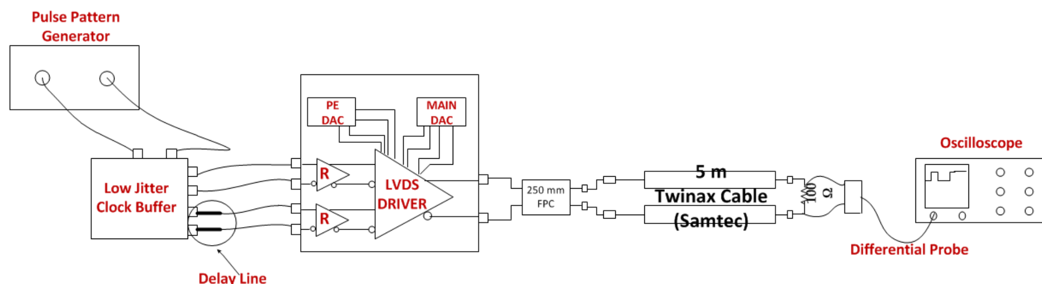


Figure 4.25: Test set-up with the full transmission line.

±15) ps, larger than the desired value corresponding at a data rate of 1.2 Gb/s. In any case, since it was not possible to have a more precise value of this delay, the two hand made short cables were used as well, bearing in mind that they can provide a jitter component.

The driver was tested with various driver and pre-emphasis DAC codes,

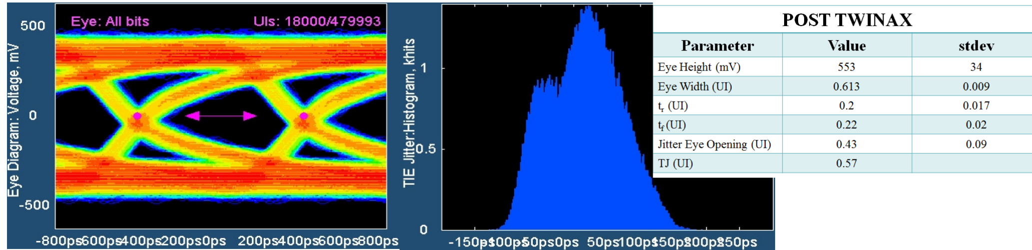
by using a 2^{31}-1 PRBS and the clock coming from the PLL. In the following the test results of the measurements executed with the settings summarized in Table 4.8 are presented. It has to be remembered that the total jitter

Table 4.8: Settings.

	(a)	(b)
Input Signal	2^{31}-1 PRBS	PLL Clock
Transmission Speed	1.2 Gb/s	600 MHz
Transmission line	25 cm Cu FPC + 5 m Twinax cable	
MD DAC Code	8	
PE DAC Code	4	

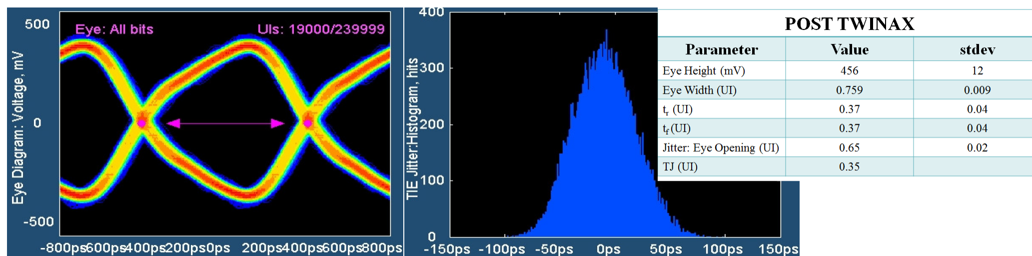
introduced by the series FPC and Twinax is 0.4 UI, as shown in Figure 4.4. Thus, the pseudo-LVDS driver with the pre-emphasis has to enhance the transmission signal quality.

The eye diagram obtained at the end of the full transmission line with a driver DAC code 7 and a pre-emphais code 0 are shown in Figure 4.26.



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	553	34
Eye Width (UI)	0.613	0.009
t_r (UI)	0.2	0.017
t_f (UI)	0.22	0.02
Jitter Eye Opening (UI)	0.43	0.09
TJ (UI)	0.57	

(a) PRBS @ 1.2 Gb/s - TJ 0.57 UI



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	456	12
Eye Width (UI)	0.759	0.009
t_r (UI)	0.37	0.04
t_f (UI)	0.37	0.04
Jitter: Eye Opening (UI)	0.65	0.02
TJ (UI)	0.35	

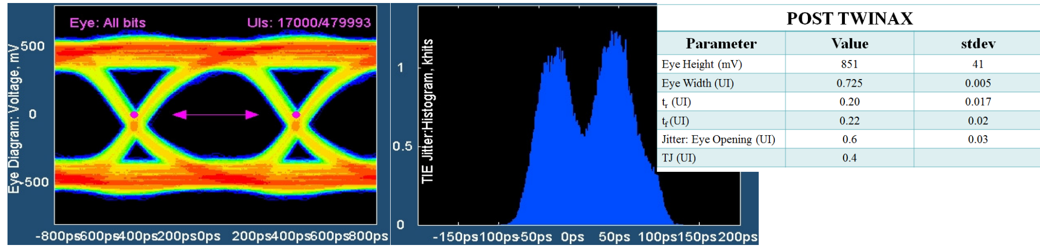
(b) Clock @ 600 MHz - TJ 0.35 UI

Figure 4.26: Eye diagrams at the ends of the 5.3 m long differential line when no pre-emphasis current is added.

In the PRBS case the envelops are reduced along the vertical axis, demonstrating that 3.4 mA of current are not sufficient to overcome the RC limitations of the entire 5.3 m long transmission line, as seen in simulation. The

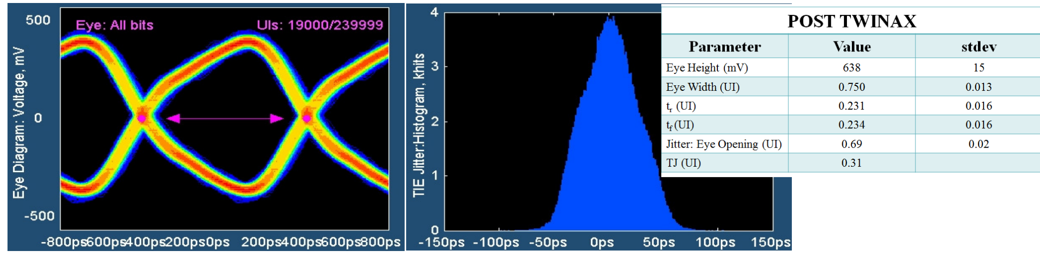
TJ ranges between 0.35 UI and 0.57 UI, out of the commercial standards. However, it has to be noted that when a PRBS is transmitted, the crossing points are not well centered at 0 V. Indeed, there is a shift of 70 mV which worsens the signal quality.

When a pre-emphasis current of $\sim$ 2 mA is added, the obtained eye diagrams result clearly open even if the jitter amount ranges between 0.31 UI and 0.4 UI as shown in Figure 4.27. By increasing the driver DAC code



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	851	41
Eye Width (UI)	0.725	0.005
t_r (UI)	0.20	0.017
t_f (UI)	0.22	0.02
Jitter: Eye Opening (UI)	0.6	0.03
TJ (UI)	0.4	

(a) PRBS @ 1.2 Gb/s - TJ = 0.4 UI



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	638	15
Eye Width (UI)	0.750	0.013
t_r (UI)	0.231	0.016
t_f (UI)	0.234	0.016
Jitter: Eye Opening (UI)	0.69	0.02
TJ (UI)	0.31	

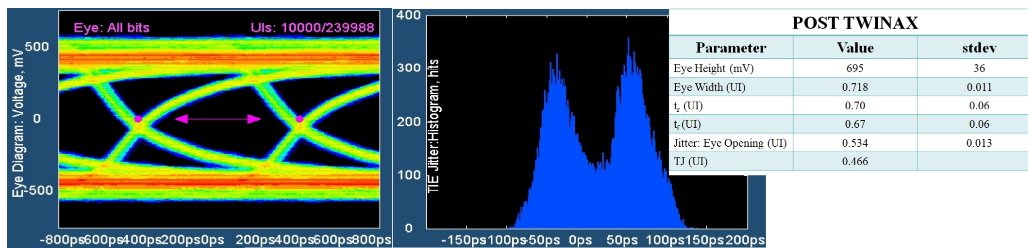
(b) Clock @ 600 MHz - TJ = 0.31 UI

Figure 4.27: Eye diagrams at the ends of the 5.3 m long differential line when $\sim$ 2 mA of pre-emphasis current is added.

to 9, i.e. with a driver output current of 4.3 mA, the eye diagram at the end of the series FPC and TWINAX transmission line shows that the parasitics effects of the line limit the rise and the fall time of the signal. Nevertheless, by making a comparison with the previous case without pre-emphasis, an increase of 1 mA of current allows an eye width of 0.71 UI and the TJ reduction down to 0.47 UI.

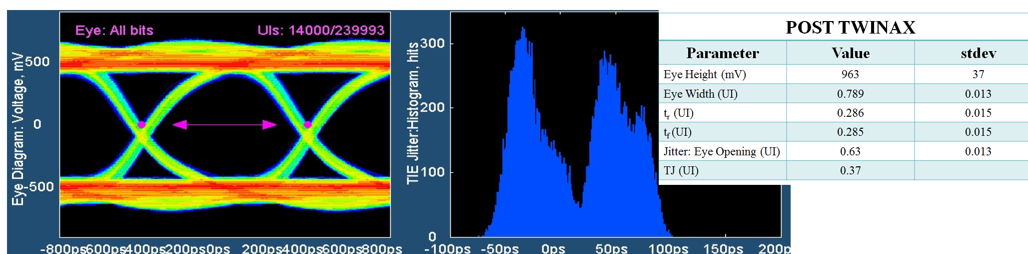
With the 50% of pre-emphasis current, which correspond to a PE driver DAC code of 4, the rise and fall time of the system are sensibly reduced as well the TJ. Unfortunately, the total jitter amount is still out of the commercial limit of 0.3 UI (see Figure 4.29).

Some interesting lessons can be learned from the measurements. In the two cases in which the pre-emphasis current is added, it helps the MD to overcome the bandwidth limitations of the transmission line. Indeed, the



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	695	36
Eye Width (UI)	0.718	0.011
t_r (UI)	0.70	0.06
t_f (UI)	0.67	0.06
Jitter: Eye Opening (UI)	0.534	0.013
TJ (UI)	0.466	

Figure 4.28: Eye diagrams at the ends of the 5.3 m long differential line with a MD DAC Code of 9 and none pre-emphasis - TJ = 0.47



POST TWINAX		
Parameter	Value	stdev
Eye Height (mV)	963	37
Eye Width (UI)	0.789	0.013
t_r (UI)	0.286	0.015
t_f (UI)	0.285	0.015
Jitter: Eye Opening (UI)	0.63	0.013
TJ (UI)	0.37	

Figure 4.29: Eye diagrams at the ends of the 5.3 m long differential line with a MD DAC Code of 9 and PED DAC code 4.

rising and falling edges of the eyes are steeper and the high and low logic levels are well defined. However, the total jitter amount is still high.

Various inspections were done to find a cause of those measured jitter values which are higher when a PRBS stream is transmitted. Indeed, a shift between the eye crossing points from zero is evident and largerly affects the timing error whenever the driver strenght is. Coming back to the simulations, a cause was found in the receivers output signals. Actually, those outputs do not have the same rising and falling time and then the inverters in the STD, which are controlled by the receivers outputs, do not switch properly and propagate the shift at the driver outputs. This effect was not so relevant during simulations but it turned out to be important after the chip production.

4.6.3 Simulations on the second pseudo-LVDS driver implementation.

The second prototype of the Driver block is different from the previous one. Indeed, what is called Driver block here consists of the MD, the PED, two single ended-to-differential (STD) blocks and two multiplexers (see Figure 3.23). Even in this case the Driver has been fully simulated with the test

Table 4.9: Input signals parameters for the Driver block.

Parameter	EVEN	ODD	EVEN_D	ODD_D
V_{HIGH} (V)	DVDD			
V_{LOW} (V)	0			
Bit Period (BP) (ns)	1.6667			
t_r(ps)	70			
t_f(ps)	70			
Delay (ps)	0	BP-10	BP	

bench shown in Figure 4.30 before and after the block layout, thus including the parasitic effects due to the placement and routing of the various components and the parasitics in the transmission line. The purpose here is to verify the signal quality at the end of the full 5.3 m long transmission line when the full chain MUXs, STDs and drivers are assembled together. It has

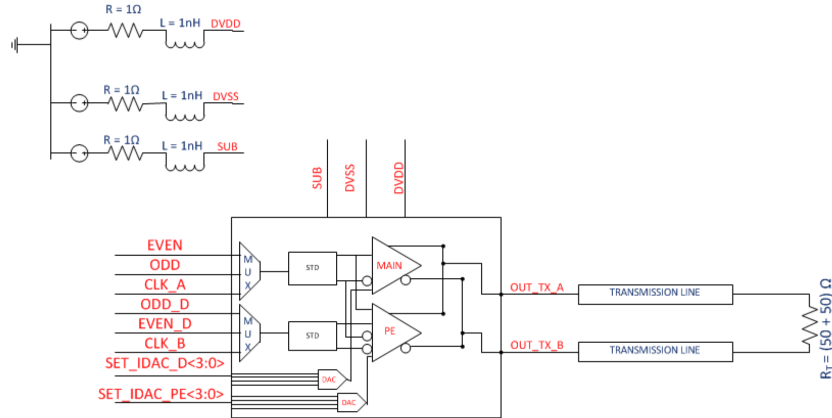


Figure 4.30: Test Bench for the secon driver implementation.

to be noted that, for this Driver prototype the DACs which control the MD and the PED circuits have been modified to include a bias current generator inside the chip, thus avoiding a further external pin. However, a drawback is that the current value is not the same across corners, when the same codes have been set (see Figure 4.31).

The MUXs input signals are used to simulate the serializer outputs and they have the characteristics reported in Table 4.9. An example of the eye diagrams obtained at the input and at the outputs of the transmission line are plotted in Figure 4.32. Here the I_{MD} selected current is 4.3 mA whilst I_{PED} is $\sim$ 2.2 mA, thus applying a 50% of pre-emphasis. The effect of the reflections at the driver outputs is outlined by the spread in the vertical axis of the two

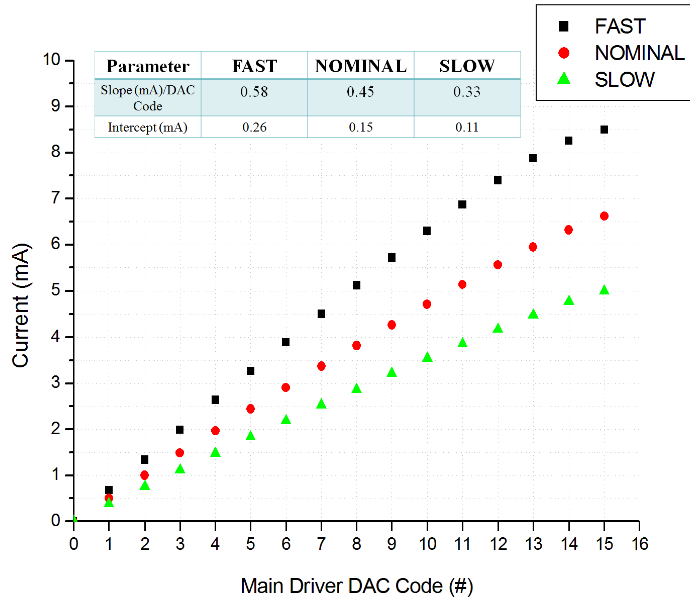


Figure 4.31: Main driver current versus main driver DAC code across corners.

logical levels and by the shift of about 70 mV from 0 V of the two crossing points. Despite of this, the eye diagram at the end of the transmission line is quite open and the two eye crossing point are well centered at 0 V, then allowing to a receiver to buffer a data stream correctly.

4.6.4 Test measurements on the second pseudo-LVDS driver implementation.

This Driver block has been integrated with the entire DTU in a dedicated test chip and in the ALPIDE 3 prototype. Concerning the test measurement on the dedicated test chip, very prelimanary results were produced on the electrical characteristics of the DTU chain and on its resistance to the SEU events.

The set-up to test the DTU chain is very similar to the one used to test the first driver prototype. However, here the low jitter buffer clock is used to feed the PLL input. The output driver current is plotted in Figure 4.33 versus the driver DAC code. As it is possible to see, after the test chip production, a driver DAC code of 11 has to be set to obtain 4 mA of current.

The test set-up have to be completed to check the signal quality at the end of a 5.3 m transmission line. In Figure 4.34 we can see the eye diagram of the differential driver output when it is directly linked to the oscilloscope,

without any transmission line.

At the speed of 1.25 Gb/s, and a MD current by half range, the eye is well defined even without any pre-emphasis current. Unfortunately, the total jitter reaches the 0.3 UI commercial limit. One of the causes which produce those jitter values has been tracked down in a not negligible random jitter component, mainly due to the fact that the set up has to be optimized.

Concerning the SEU test, it was done in the INFN Legnaro ion beam facility by using three different ions and two angles of incidence to study the SEU event probability by varying the Linear Energy Transfer (LET).

To carry out the test, a 30 bits pattern at the speed of 1.2 Gb/s was continuously sent to the DTU while an external FPGA monitored the incoming data stream to check if an error in the transmission occured. The measurements were not easy to do, since many stops were done to allow one of the operators to reset manually the FPGA since a loss of synchronization between the DTU and the FPGA occurred. However, even if the PLL lost the lock, this was not correlated to the loss of lock of the FPGA. Furthermore, the SEU events resposible for the loss of synchronization of the PLL were correctly collected and no latch-up event was occurred.

4.6.5 High speed drivers power consumption.

In the first design steps of the high speed drivers block a great effort was made to guarantee a good signal integrity during the transmission instead to save the power consumption.

After the second pseudo-LVDS driver implementation in the Driver block for the DTU, the reduction of the power dissipation of the high speed circuits has been the subject of an intense study. The same test benches used to check the signal integrity has been used to analyse how much power the high speed drivers needs to send data at 1.2 Gb/s with a good signal quality.

To reproduce a realistic situation, the PRBS signals with the same characteristics listed in Table 4.7 has been used for the corners simulation and the overall power consumption of the entire Driver block has been considered.

For sake of clarity, let me recall that this high speed block consists of a main pseudo-LVDS driver with its 4-bit DAC, a pre-emphasis driver with another 4-bit DAC, two single ended-to-differential blocks (STD) and two multiplexers (MUX). The power consumption of this block is then the sum of the single contributions.

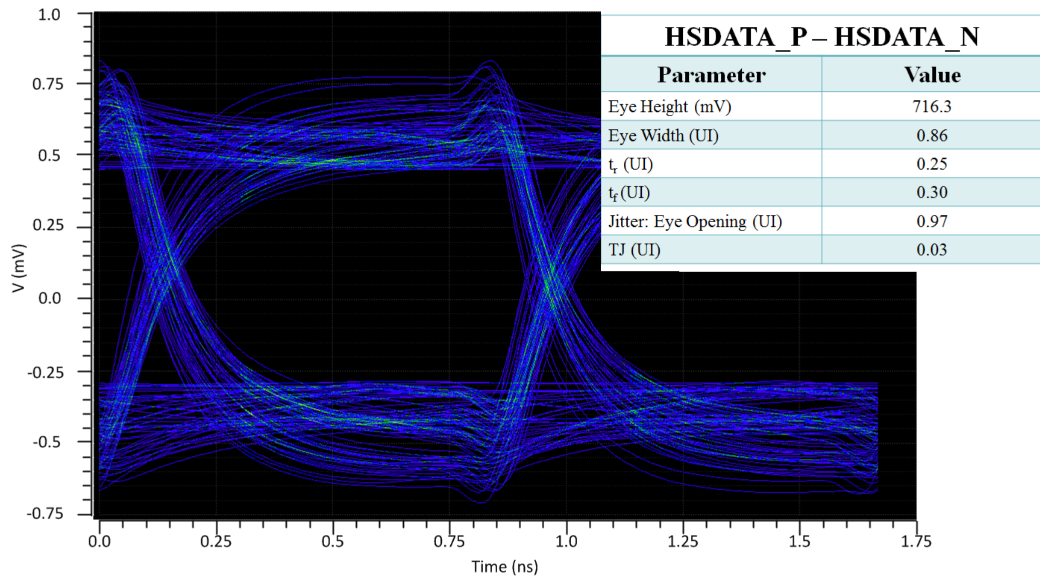
From the first power estimation of this block it turned out that with a MD current of $\sim$ 4.3 mA and a 50% pre-emphasis the total (static + dynamic) overall power consumption of the Driver block ranges between 26mW and 38mW. Looking for the cause of this unexpectedly high power dissipation,

it was found that the single ended-to-differential blocks are the most power hungry circuits. Despite the fact that they have a negligible static power consumption, the high switching activity consumes a noticeable amount of power. In particular, the STD which drive the two MD and two of the PED inputs has a power consumption ranging between 12 mW and 16 mW. Actually, those circuit works at the frequency of 1.2 Gb/s by driving a capacitve load of few pF with a 1.8 V voltage swing. Furthermore, it has to be considered that another power contribution of this block comes from the internal power dissipation. Actually, a STD circuit is made up using a 3 stages and a 2 stages inverter chains which swing at 1.2 Gb/s between 0 V and 1.8 V driving the internal (load + parasitc) capacitances. Furthermore, a not perfect ratio between the input and output signals slopes of the STD worsen the situation.

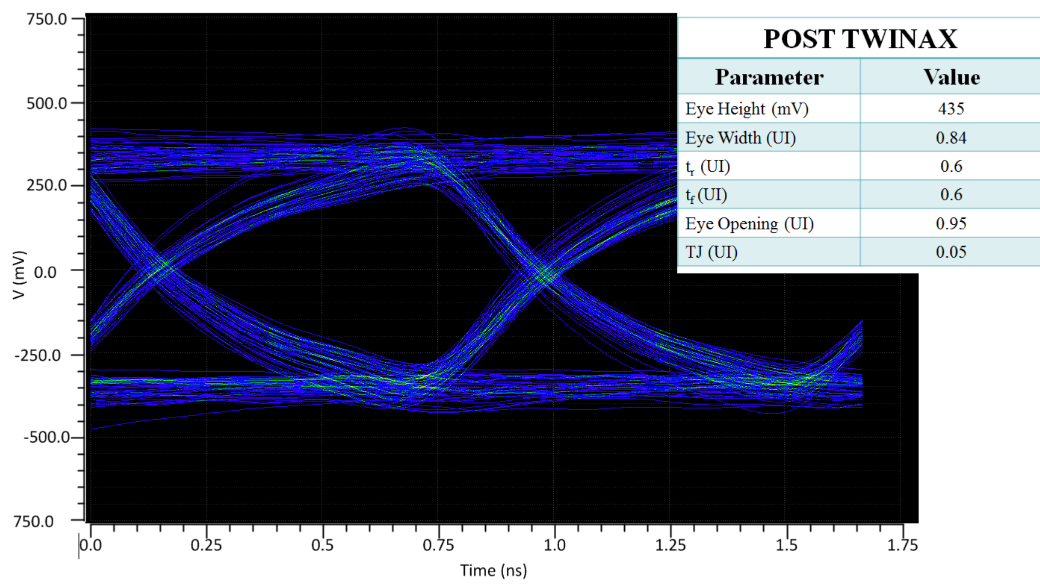
To reduce the power consumption of the entire Driver block and reduce the capacitive load, still maintaing a good signal quality at the end of the 5.3 m long transission line, the STD has been modified as shown in Section 3.7.2. The inverters chains now consist of only two stages and the transistor size have been reduced, thus minimizing the internal capacitive load. With this modification, the overall total power consumed by the Driver block is sensibly reduced and ranges between 15 mW and 25 mW where the STD block gives a contribution in the range 2.2 mW and 4.2 mW.

Other solutions are now under study to limit the power dissipation of the entire Driver, as to reduce further the pseudo-LVDS driver output common mode from 1.1 V to 0.9 V by using the same circuit of the second driver implementation. Indeed, by moving down the common mode by 200 mV and resizing the MD and PED transistors it is possible to reduce the input capacitance of those circuits to help the reduction of the current needed to drive them. From the schematic simulations it comes out that with this expedient it is possible to reach a further reduction of 6 mW in the overall total power consumption.

It has to be noted that, whatever the Driver modifications will be, to guarantee the system to work properly a compromise will be done between the power saving and the signal integrity at high speed with long transmission line. The simulations and test results show that, independently from the chosen driver scheme, there is a clear trade-off between power consumption and signal integrity over long transmission line. Therefore, given the different cable lenght for the 7 ITS layers, a wide range of programmability is required for the driver.



(a) Differential signal at the driver output.



(b) Differential signal at the Twinax output.

Figure 4.32: Eye diagrams captured at the input and at the ouptut of the full 5.3 m long differential transmission line @ 1.2 Gb/s.

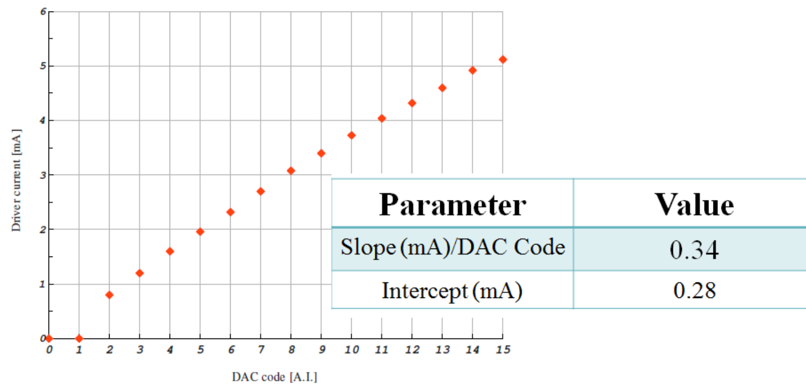


Figure 4.33: Driver current versus driver DAC Code.

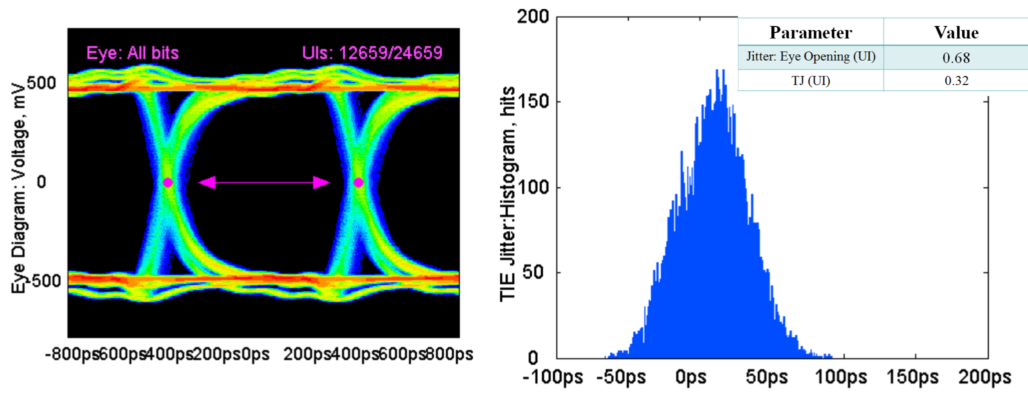


Figure 4.34: Driver current versus driver DAC Code.

Chapter 5

Architectural study of a monitoring ADC for the ALPIDE pixel chip

A component of the ALPIDE pixel chip is a monitoring Analog to Digital Converter (ADC) to control some voltage levels which are essential for the correct chip operation, as the bias voltage of the current mirrors or the power supply. Since digital signals are easier to elaborate from the computer point of view and they are more robust to the noise than the analog signals, very often data in the digital form are preferred to the analog ones.

The monitoring ADC inside the pixel chip will complete the features of ALPIDE. It will be used to control voltage values not variable with time, therefore the conversion speed will not be an issue as well as the power consumption.

Despite of the success of the most popular ADC scheme ([44], [50]), as the Pipeline ADC, the Successive Approximation (SAR) ADC or the Sigma Delta ADC ($\Sigma\Delta$), a novel architecture was studied which takes the advantage of two principle, the 2-steps conversion and the successive approximation [44]. In the following, the architectural study on the implementation of this ADC will be illustrated to show that this new principle works.

5.1 Study on a 11-bit monitoring ADC

Various architectures were explored for the implementation of a monitoring ADC, for which a resolution of 11-bit was required.

A 2-steps architecture was studied to obtain this moderate resolution, in which the Most Significant Bit (MSB) and the Less Significant Bit (LSB)

are determined respectively by a coarse and a fine conversion. In this way, it is possible to reduce the number of components, and thus the power consumption and area, needed for the entire system. In order to save power, the proposed architecture is asynchronous with the pixel chip clock and no digital steering signal is foreseen since the conversion process start only if the analog voltage reference V_{REF} is greater than the analog monitored voltage V_{IN}, as it will be described in the following sections.

The block diagram of the studied ADC architecture is implemented as shown in Figure 5.1.

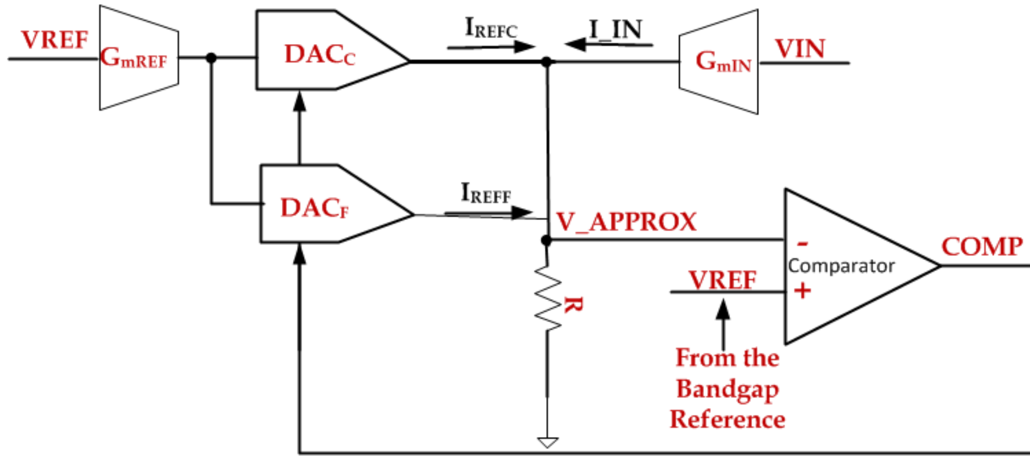


Figure 5.1: Proposed ADC block diagram

The entire system consists of:

- a 1 bit ADC, i.e. a differential comparator consisting of a pre-amplification stage and PMOS input symmetrical OTA. This circuit outputs a logic 0 (0 V) or a logic 1 (DVDD) depending on the difference between its inputs and controls both the DACs [51].

- a 6 bit DAC (DAC_C) for the coarse conversion. It is made up of 63 current cell, each steering a current of I_{REF_C} ~160 nA;

- a 5 bit DAC (DAC_F) for the fine conversion. It has the same structure of the DAC_C but it consists of 34 current cells each steering a current of $I_{REF_F} \sim 5$ nA. Actually, when 32 current cells of this DAC are active, the total current contribution is equal to I_{REF_C} and it accounts for 2 redundant bit.

- a high gain transconductor G_{mREF} fed by the reference voltage V_{REF};

Table 5.1: Estimated area and power consumption for the 11-bit ADC components

Block	Area (μm^2)	Power (μW)
G_{mREF}	18200	26
G_{mIN}	18000	26
Comparator	1120	38
Current cell DAC_C	531.6	0.288
Current cell DAC_F	286.9	0.009
34 DAC_F + 63 DAC_C latches	16507	ND

- a second high gain transconductor G_{mIN} fed by the voltage V_{IN} which has to be monitored.

The transconductors G_{mIN} and G_{mREF} are implemented with a rail-to-rail Operational Amplifier (R2R opamp, [51]) previously designed for another circuit of the ALICE ITS upgrade. The output of the R2R opamp in the G_{mIN} is proportional to V_{IN} and it bias the current mirror responsible for the I_{IN} generation. In the same way, the output of the R2R opampam in the G_{mREF} is the bias voltage for the DACs current cells.

The area and the power consumption needed to each block are resumed in Table 5.1.

5.1.1 Principle of operation

The principle of operation of this converter is based on the double conversion from the monitored voltage into a current value and again this current is converted in the voltage V_{APPROX}.

The reference voltage comes from the Bandgap Reference, inside the ALPIDE pixel chip, and it has the maximum value of 1.2 V. What is measured with this ADC is how far is V_{IN} from V_{REF}.

When the voltage V_{IN} has to be measured, it feeds the input of G_{mIN} to be converted in the current I_{IN}. This current flows in the the resistor R generating the voltage drop V_{APPROX} at one of the comparator input. Until now, the DACs do not steer any additional current and the first comparison takes place among V_{APPROX} and V_{REF}. Then, the two DACs will be driven to add current or not depending on the comparator output COMP, as follows:

(i) IF $V_{REF} < V_{APPROX} \rightarrow$ COMP = 0 $\rightarrow$ STOP TO COMPARE

(ii) IF $V_{REF} > V_{APPROX} \rightarrow$ COMP = 1 $\rightarrow$ ADD CURRENT

When the condition (i) is not satisfied, the DACs will continue to add current until V_{APPROX} will overcome V_{REF}. Indeed, the currents flowing out from

the DACs are added to I_{IN} and the total current thus obtained will generate a new value for V_{APPROX} until the gap between V_{IN} and V_{REF} is filled.

The value of V_{APPROX} will approach V_{REF} growing up as a staircase and the fine and coarse DACs will output a thermometer code. Indeed, any time a logic 1 displays in the DAC_C thermometer code, an amount of current is added to I_{IN} which generates the voltage drop:

$$V_{LSB,C} = \frac{V_{REF}}{2^6} = \frac{V_{REF}}{64} = \frac{1.2V}{64} = 18.75mV \tag{5.1}$$

In the same way, the corresponding voltage drop generated by a single current contribution from the DAC_F is:

$$V_{LSB,F} = \frac{V_{LSB,C}}{2^5} = \frac{V_{LSB,C}}{32} = \frac{18.75}{32} = 0.585mV \tag{5.2}$$

In a further development step, those thermometer codes have to be converted in two correspondent binary codes. However, for this demonstrative implementation, V_{APPROX} will be obtained multiplying $V_{LSB,C}$ and $V_{LSB,F}$ respectively for the number of 1s in the fine and coarse thermometer codes and adding up the two contributions.

Basically, the two DACs perform a kind of zooming, as illustrated in Figure 5.2. Indeed, the DAC_C is used to find the range in which the monitored voltage lays. Then, the value of V_{APPROX} which is the nearest to V_{IN} is found in this range with the fine conversion by DAC_F.

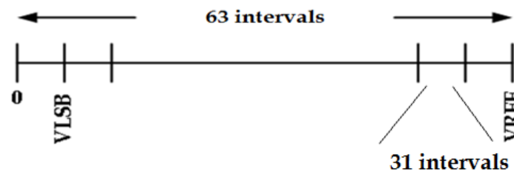


Figure 5.2: ADC full range partitioning.

5.1.2 Thermometer Code generation

It is well known that a thermometer code is a unary code populated by a number of logic 1s equals to the number which has to be represented [52]. An example of a 4-bit thermometer code with its corresponding binary code is illustrated in Table 5.2.

It has to be noted here that the number of 1s in the thermometer code grows linearly with the number that has to be represented. To understand the basic principle for the thermometer code generation with the designed

Table 5.2: Representation of a natural number N with a 3 bit binary code and a 7 bit thermometer code.

Number	**Binary Code**			**Th. Code**						
	$\mathbf{b}_2$	$\mathbf{b}_1$	$\mathbf{b}_0$	$\mathbf{m}_7$	$\mathbf{m}_6$	$\mathbf{m}_5$	$\mathbf{m}_4$	$\mathbf{m}_3$	$\mathbf{m}_2$	$\mathbf{m}_1$
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

converter, let's focus on a single step of this ADC. For the sake of simplicity, let's take the one which is made up of the 5-bit ADC.

Before the conversion in a binary code, the thermometer code generated by the DAC for a 5-bit ADC consists of 32 bit. Let's suppose that after 13 comparison steps the code is the one represented in Table 5.3:

Table 5.3: Example of a 32 bit thermometer code after 13 steps of conversion.

0	0	0	0	0	1	1	1	1	1	1	1
Q_{31}	Q_{30}	Q_{29}–Q_{15}	Q_{N+1}	Q_N	Q_{N-1}	Q_{11}	Q_{10}	Q_9	Q_8	Q_1–Q_7	Q_0

Then, bearing in mind the linear growth principle of the number of 1s in a thermometer code, the n-th bit is written by taking into account the sign of the comparator, the value of the Q_{N-1} bit and the Q_{N+1} bit as described in Table 5.4:

Table 5.4: Truth table for the thermometer code generation

Q_{N-1}	Q_{N+1}	COMP	Q_N
0	0	X	0
0	1	NP	Keep State
1	0	0	COMP
1	1	X	1

This truth table states that when every bit before and after Q_N is set to a logic 0, then Q_N will be fixed to 0 whatever the comparator output is, meaning that no additional current has to be steered by the DAC. In a

similar way, if $Q_{N-1} = Q_{N+1} = 1$, then Q_N has to be set to one and an additional current contribution will be output by the DAC. The situation in which $Q_{N+1} = 1$ and $Q_{N-1} = 0$ is not allowed since the number of 1s in a thermometer code increases with the number that has to be represented, then one imposes the system to keep the state. Finally, the comparator output COMP plays a role when every bit before the n-th is at logic 1 whilst the Q_{N+1} is at logic 0. Indeed, a further current contribution will be added or not depending on how far V_{APPROX} is from V_{REF}.

5.2 DAC circuits

The block diagram of the coarse and the fine DAC cells is represented in Figures 5.3 and 5.4. The two DACs have the same structure consisting of a latch and a current cell. The latch drives the current cells to steer the current depending on the value of the n-th bit, as stated by the truth table. Furthermore, it is even responsible for the bit value storage.

A DAC current cell circuit consists of the current source $M_{G_{C,F}}$ and a pair of switches implemented with the two PMOS transistors M_L and M_R. The current source is biased by a voltage proportional to the G_{mREF} output, thus ensuring that each current cell furnishes a current I_{REF_C} and I_{REF_F} respectively. Those currents are steered toward ground or to the resistor R, depending on the n-th bit value and its negative phase. Actually, the PMOS switches are paired, thus allowing the current to flow always in a well-defined path.

For the sake of clarity, a remark has to be done at this point on the code generation. It has been stated before that when Q_N is at logic 1 a current contribution is output by the DAC. Indeed, the PMOS switch controlled by Q_N is open whilst the one controlled by $\overline{Q_N}$ is in conduction. In this way the current is steered toward the comparator input producing a desired voltage drop.

5.2.1 Full Latch structure for the fine DAC

When the condition (i) (see Section 5.1.1) is not satisfied, the P_i bit of the fine DAC starts to be switched from a logic 0 to a logic 1, correspondingly to the voltage value which has to be converted.

At the beginning of the comparison process each P_i bit has to be reset at a logic 0. For this reason an external reset signal RST is mantained at a logic 1 (logic 1 = DVDD) and only when RST switch to a logic 0 each P_i can be written at its correct value.

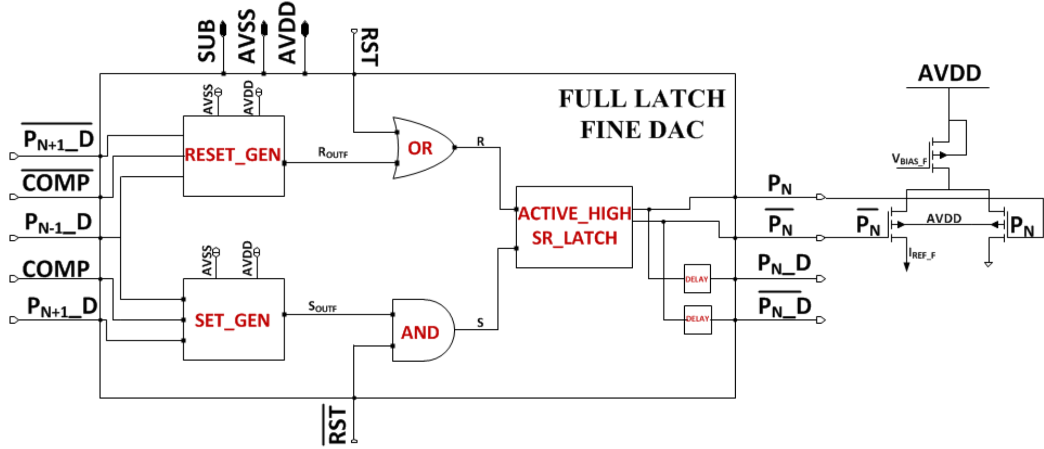


Figure 5.3: Fine DAC cell. The full latch contains the logic to store the bit values and control the current cell.

As said before, the latches are in charge to drive the DACs current cells and to latch the bit values. For this reason the outputs of the n-th latch are the two phases of the n-th bit, P_N and $\overline{P_N}$, and a delayed copy of those signals P_N_D and $\overline{P}_N$_D. The delay turned out to be necessary to compensate the time the comparator needs to perform a comparison. In this way, each bit is written only when the comparison is ended.

The circuit for the n-th full latch is illustrated in Figure 5.3. The inputs of this block are fed by the bit P_{N-1}, P_{N+1}, $\overline{P}_{N+1}$ and by the comparator outputs COMP and $\overline{COMP}$. This fact comes from the need to drive an active high SR latch inside the full latch block but bearing in mind the truth table.

The set (S) and reset (R) signals at the SR latch inputs are produced by combining the outputs of the dedicated RESET_GEN and SET_GEN blocks with RST. Those dedicated block are controlled by the bit values and comparator output COMP, as illustrated in Figure 5.3.

The output signal S_{OUT} of the SET_GEN block is obtained from the combinatorial logic circuit described by:

$$\begin{aligned} S_{OUT_F} &= (P_{N-1} \wedge P_{N+1}) \vee (P_{N-1} \wedge COMP) = \\ &= \overline{\overline{(P_{N-1} \wedge P_{N+1})} \wedge \overline{(P_{N-1} \wedge COMP)}} \end{aligned} \tag{5.3}$$

The RESET_GEN outputs R_{OUT} is produced with the combinatorial logic circuit described by:

$$R_{OUT_F} = \overline{P_{N-1}} \vee (\overline{P_{N+1}} \wedge \overline{COMP}) \tag{5.4}$$

Finally, the inputs S and R for the n-th SR latch are determinated combining S_{OUT} and R_{OUT} with $\overline{RST}$ and RST respectively, as follows:

$$\begin{aligned} S &= \overline{RST} \wedge S_{OUT_F} \\ R &= R_{OUT_F} \vee RST \end{aligned} \tag{5.5}$$

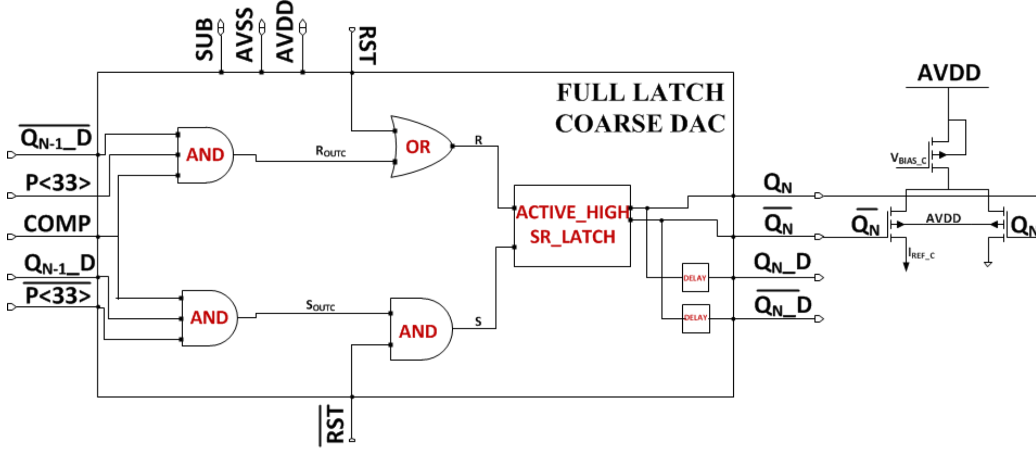


Figure 5.4: Coarse DAC cell. This DAC cell is similar to the one of the fine DAC but here the full latch is controlled by the fine bit P_{33} that allows the coarse DAC to participate at the conversion.

5.2.2 Full Latch structure for the coarse DAC

When every P_i bit of the fine DAC is at a logic 1 and the condition (i) is not yet satisfied, the current contributions from the coarse DAC have to be activated. Then, the latch logic has to account for the saturation condition of the fine DAC which will allow the coarse DAC to steer an amount of current, despite of the fact that the coarse bit Q_i are determined with the same principle explained in the truth table.

As well as the full latch illustrated above, the inputs of those n-th latch implemented for the coarse DAC are fed by the bit Q_{N-1}, the comparator output COMP and the fine bit P_{33} with their negative phases. Then, the equivalent signals S_{OUT} and R_{OUT} are produced by:

$$S_{OUT_C} = P_{33} \wedge COMP \wedge Q_{N-1} \tag{5.6}$$

$$R_{OUT_C} = \overline{P_{33}} \wedge COMP \wedge Q_{N-1} \tag{5.7}$$

Again, those values are combined with the external reset thus determining the S and R signals for the SR latch as before:

$$\begin{aligned} S &= \overline{RST} \wedge S_{OUT_C} \\ R &= R_{OUT_C} \vee RST \end{aligned} \tag{5.8}$$

5.3 An illustrative example

Preliminary studies were done to check that the operating principle of this ADC is working. Actually, simulations across corners were carried out to verify that the comparator stops to compare when the condition (i) (see Section 5.1.1) is reached, that its output does not start to oscillate and that the number of bit set to 1 corresponds to the value which has to be converted.

For example, consider that the voltage V_{IN} = 547 mV has to be monitored. As said before, this ADC measures how far V_{IN} is from V_{REF} and then the thermometer codes are produced to account for this discrepancy. In this case,

$$V_{DIFF} = V_{REF} - V_{IN} = (1.2 - 0.547)V = 0.653V \tag{5.9}$$

By considering a coarse voltage drop V_{LSB_C}, V_{DIFF} is obtained if in the coarse thermometer code the number of bit set to one is:

$$\frac{V_{DIFF}}{V_{LSB_C}} = \frac{653mV}{18.75mV} = 34.82 \sim 34 \tag{5.10}$$

or, alternatively, if the the bit Q_0 - Q_{34} in the coarse DAC are set to the logic 1 as well as all bit in the fine DAC. In any case, the comparison process will stop if V_{APPROX} overcomes V_{REF}.

Figure 5.5 shows the simulation result in the nominal case when the value V_{IN} = 547 mV and V_{REF} 1.2 are set. As it is possible to see, the comparator output switches from the logic 1 (DVDD) to zero when V_{APPROX} reaches a value of circa 1.23 V and the convergence is thus obtained in 3 μs. By looking at thermometer codes in Figures 5.6(a) and 5.6(b) obtained for the coarse and fine converters one has:

- All bit in the fine converter, P_0 - P_{33}, are set to the logic 1. In this way, an overall current contribution of 34×I_{REF_F} is added to I_{IN} and the coarse comparator can start to add current.
- The bit Q_0 - Q_{34} are set to the logic 1. Then, their negative phases are set to a logic 0 and they allow the PMOS switches to be open in conduction, thus steering the current overall 34×I_{REF_C} toward the resistor R.

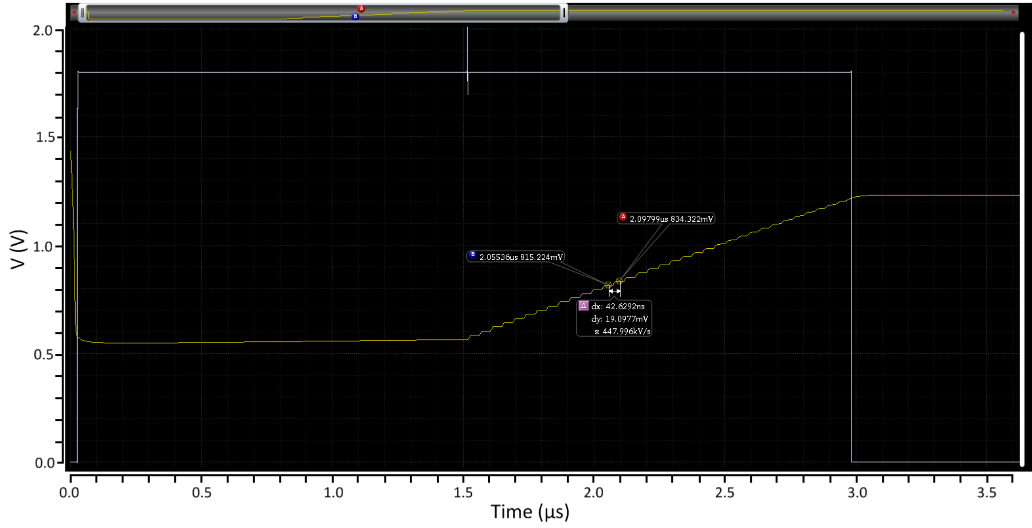
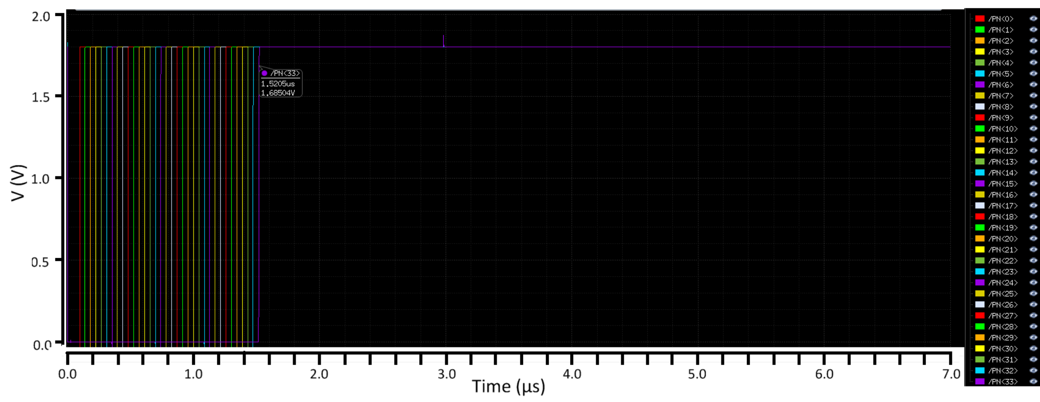


Figure 5.5: Convergence of the ADC. The value of V_{APPROX} at which the conversion stops is 1.23 V.

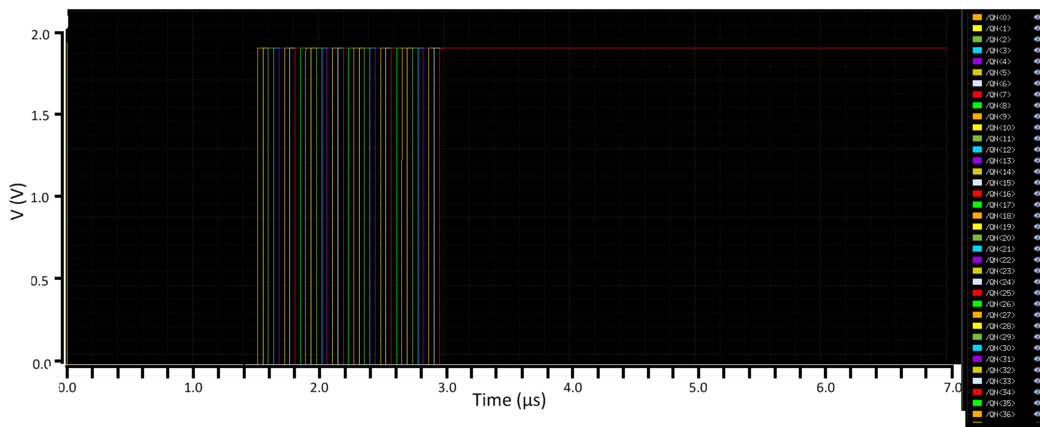
5.4 Conclusion

To fully equip the ALPIDE pixel chip an ADC has to be included to monitor some voltage values which are essential for the correct operation of the system. For this reason, an 11-bit ADC based on the two steps conversion technique together with the successive approximation principle has been designed. The monitored voltage V_{IN} generates a current I_{IN} producing the voltage drop V_{APPROX} at one of the input of a comparator whilst the other comparator input is connected to the reference voltage V_{REF}. This ADC measures the difference between V_{IN} and V_{REF} and fills this gap steering an additional current from the DACs to update the value of V_{APPROX}. Actually, the comparison will stop only when $V_{APPROX} > V_{REF}$ and the results are two thermometer codes, for the coarse and the fine DAC respectively, in which the number of 1s is linearly proportional to the difference which has to be converted.

Very preliminary studies have been carried out on this ADC demonstrating that the principle of operation is working. Then, this architecture can be the basis of a further development for an improved converter. In this way, the overall system could be optimized in terms of area and power consumption to guarantee the best performance. Furthermore, the algorithm to obtain a binary code from the DACs thermometer codes could be added with the purpose to manage less bit than the present 96 at the converter output, thus simplifying its read-out.



(a) Fine DAC Thermometer Code.



(b) Coarse DAC Thermometer Code.

Appendix A

Differential Transmission Standard Specifications

A.1 ANSI/TIA/EIA-644 and -899 LVDS standard protocol

The Table below describe the electrical characteristics on the point-to-point (ANSI/TIA/EIA-644) and on the Multipoint LVDS (ANSI/TIA/EIA-899)transmission protocols.

Table A.1: ANSI/TIA/EIA-644 and -899 Driver Electrical Specifications [32].

Parameter	**TIA/EIA-644 (LVDS)**	**TIA/EIA-899 (M-LVDS)**
Driver Characteristics		
Offset Voltage: $V_{OS}(max)(V)$	1.375	2.1
Offset Voltage: $V_{OS}(min)$ (V)	1.125	0.3
Differential output voltage: V_{OD} (max)	454 (100 Ω)	650 (50 Ω)
Differential output voltage: V_{OD} (min) (mV)	247 (100 Ω)	480 (50 Ω)
Offset Voltage variation: V_{OS}(PP) (mV)	150	150
Short circuit current: I_{OS} (mA)	12/24	43
Differential voltage change: ΔV_{OD} (mV)	50	50
Offset Voltage change: ΔV_{OS} (mV)	50	50
Transition time: t_r/t_f (min) (ps)	260	1000

A.2 Electrical Characteristic custom M-LVDS transceiver.

The Table below summarizes the electrical characteristics of the custom M-LVDS transceiver.

Table A.2: ANSI/TIA/EIA-644 and -899 Receiver Electrical Specifications [32].

Parameter	**TIA/EIA-644 (LVDS)**	**TIA/EIA-899 (M-LVDS)**
Receiver Characteristic		
Ground potential difference: V_{gpd} (V)	±1	±1
Input leakage current: I_{in} (μA	20	20
Differential input leakage current: $I_{id}\mu A$	NS	4
Input voltage range: V_{in} (V)	0 to 2.4	-1.4 to 3.8
Input threshold: V_{ith} (mV)	100	50

Table A.3: Custom pseudo M-LVDS Driver and Receiver Characteristics

Driver Characteristics					
Param.	**Min**	**Max**	**Param.**	**Min**	**Max**
V_{IS} (V)	DVSS	DVDD	t_{pZH}(ns)	0.35	8.4[1]
V_{OS} (SS) (mV)	980	1209	t_{pHZ}(ns)	0.85	1.3
ΔV_{OS} (SS) (mV)	-20	20	t_{pLZ}(ns)	0.85	1.35
ΔV_{OS} (PP) (mV)		150	t_{pZL}(ns)	0.25	0.7
I_{OUT} (mA)	2	8			
Receiver Characteristics					
V_{IS} (V)	DVSS	DVDD			
V_{OUT} (V)	0	DVDD			
t_{pENH}(ns)	0.25	0.55			
t_{pHEN}(ns)	0.7	2.6			

Bibliography

[1] H. Hillemanns *et al.*, *Radiation hardness and detector performance of new 180 nm CMOS MAPS prototype test structures developed for the upgrade of the ALICE Inner Tracking System*, 978-1-4799-0534-8/13, **IEEE**.

[2] The ALICE Collaboration. *Letter of Intent of A Large Ion Collider Experiment*, CERN/LHCC/93-16, LHCC/1 4, 1March 1993.

[3] https://cds.cern.ch/record/2025215.

[4] Massimiliano Marchisone. *Probing the Quark-Gluon Plasma from bottomonium production at forward rapidity with ALICE at the LHC* PhD thesis, 2013.

[5] The ALICE Collaboration. *The ALICE Experiment at the CERN LHC. JINST*, 3 (08), 2008

[6] The ALICE Collaboration. *Technical Design Report of the Inner Tracking System (ITS)*. CERN/LHCC 99-12, ALICE TDR 4, 18 June 1999.

[7] http://alipub-dev.web.cern.ch

[8] The ALICE Collaboration. *Upgrade of the ALICE Experiment. Letter of Intent*. CERN-LHCC-2012-012/LHCC-I-022, September 8, 2012.

[9] The ALICE Collaboration. *Conceptual Design Report for the Upgrade of the ALICE ITS*. CERN-PH-EP-2012-XXX, March 6, 2012.

[10] The ALICE Collaboration. *Upgrade of the Inner Tracking System. Thecnical Design Report*. CERN-LHCC-2013-024, ALICE-TDR-017, December 2, 2013.

[11] The ALICE Collaboration. *Alignment of the ALICE Inner Tracking System with cosmic-ray tracks.* JINST 5 (2010) P03003.

[12] G. Contin, *Performance of the present ALICE Inner Tracking System and studies for the upgrade.* JINST 7 (2012) C06007.

[13] L. Musa, *Topical Workshop on Electronics for Particle Physics.*

[14] W.R. Leo, *Techniques for nuclear and particle physics experiments.*

[15] Low-Power High Dynamic Range Front-End Electronics for the Hybrid Pixel Detectors of the PANDA MVD, PhD thesis, T. Kugathasan, 2010.

[16] S. M. Sze. *Physics of Semiconductor Devices.*

[17] H. Spieler,*Semiconductor Detector Systems.*

[18] www.optique-ingenieur.org/

[19] L.Rossi, P- Fischer, T. Rohe, N. Wermes *Pixel Detectors. From Fundamentals to Applications.*

[20] J.A. Ballin et al., *Monolithic Active Pixel Sensor (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels.* Sensors **2008**, 8.

[21] W. Snoeys, *Monolithic pixel detectors for high energy physics.* Nuclear Instruments and Methods in Physics Research A 731 (2013) 125-130.

[22] W. Snoeys, *CMOS monolithic active pixel sensors for high energy physics.* Nuclear Instruments and Methods in Physics Research A 765 (2014) 167-171.

[23] M- Deveaux et al., *Development of CMOS Monolithic Active Pixel Sensors for the ALICE-ITS Outer Barrel and for the CBM-MVD*, PoS (VERTEX 2015) 045.

[24] C. Cavicchioli et al., *Design and characterization of novel monolithic active pixel sensors for the ALICE ITS upgrade*, Nuclear Instruments and Methods in Physics Research A 756 (2014) 177 - 182.

[25] ALICE ITS ALPIDE development team, *ALPIDE-3 Operations Manual.*

[26] P.Yang et al., *MAPS Development for the ALICE ITS Upgrade*, 2015 JINST 10 C03030, doi:10.1088/1748-0221/10/03/C03030.

[27] A. Collu, *Development and characterisation of Monolithic Active Pixel Sensor prototypes for the upgrade of the ALICE Inner Tracking System*, PhD thesis 2015.

[28] L. Greiner et al., *A MAPS based vertex detector for the STAR experiment at RHIC*, Volume 650, Issue 1, 11 September 2011, Pages 68–72.

[29] P.Yang et al., *Low-Priority Address-Encoder and Reset-Decoder data-driven readout for Monolithic Active Pixel Sensors for tracker system*, Volume 785, 11 June 2015, Pages 61–69.

[30] P. Giubilato, ALICE Read-out Elcetronics Overview. Engineering Design Review.

[31] Hazem W. Marar, Khaldoon Abugharbieh, Abdel-Karim Al-Tamimi, *A 1.8 V low power 5 Gbps PMOS-based LVDS output driver with good return loss performance*, Analog Integr. Circ. Sig. Process. DOI 10.1007/s10470-013-0224-6

[32] Michael Peffers, *Introduction to M-LVDS (TIA/EIA-899)*, Application Report, SLLA108 - February 2002.

[33] ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS, TIA PN-4584 - Revision 1.2.

[34] C. Watterson, *LVDS and M-LVDS Circuit Implementation Guide*, **AN - 1177 Application Note**

[35] A. Tajalli, Y. Leblebici, *A Slew Controlled LVDS Output Driver Circuit in 0.18 μm CMOS Technology.*, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, **VOL. 44**, NO. 2, FEBRUARY 2009.

[36] A. Lattuca, *Development of ntegrated Electronics for Monolithic Detectors in Q-well CMOS Technology*, Master Thesis, 2012.

[37] Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits. TIA PN-4584.

[38] M. Chen, J. Silva-Martinez, M. Nix, M.E. Robinson, *Low-Voltage Low-Power LVDS Drivers*, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, **VOL. 40**, NO. 2, FEBRUARY 2005.

[39] G. Mazza *et al.*, *The GBLD: a radiation tolerant laser driver for high energy physics applications, JOURNAL OF INSTRUMENTATION, vol. 8, ISSN: 1748-0221*, doi: 101088/1748-0221/8/01/C01033

[40] W. Park, S. C. Lee, *Design of LVDS Driver Based CMOS Transmitter for a High Speed Serial Link.* 2010 International Conference on Electronics and Information Engineering (ICEIE 2010)

[41] J.G.Maneatis and M.A.Horowitz, *Precise Delay Generation Using Coupled Oscillators*, *IEEE JSSC* Dec 1993.

[42] D.A.Badillo and S.Kiaei, *Comparison of Contemporary CMOS Ring Oscillator*, IEEE RFIC Symposium 2004.

[43] A. Lattuca, G.Mazza et al. *A CMOS 0.18 μm 600 MHz clock multiplier PLL and a pseudo-LVDS Driver for the high speed data transmission for the ALICE Inner Tracking System front-end chip.*, Preprint JINST_112P_1115

[44] Jan M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits. A design perspective*, Second Edition.

[45] *Understadanding Eye Pattern Measurements*, Application Notes, **Anritsu**

[46] http://www.samtec.com

[47] Mike Peng Li, *Jitter, Noise, and Signal Integrity at High-Speed.*

[48] Agilent, **Jitter Analysis Techniques for High Data Rates**, Application Notes 1432.

[49] **LeCroy**, *LeCroy Jitter Seminar.*

[50] R. Schreier, G. C. Temes, *Understanding Delta-Sigma Data Converters.*

[51] P. E. Allen, D. R. Holdberg, *CMOS Analog Circuit Design, Second Edition*, **OXFORD University press**

[52] www.ee.ucla.edu/ brweb/teaching/