Development of the readout for the IBL Upgrade Project of the ATLAS Pixel Detector

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by

Nina Krieger

The LHC luminosity is upgraded in several phases until 2022. The resulting higher occupancy degrades the detector performance of the current Pixel Detector. To provide a good performance during the LHC luminosity upgrade, a fourth pixel layer is inserted into the existing ATLAS Pixel Detector. A new FE-I4 readout chip and a new data acquisition chain are required to cope with the higher track rate and the resulting increased bandwidth. Among others, this includes a new readout board: the IBL ROD. One component of this board is the DSP which creates commands for the FE-I4 chip and has to be upgraded as well.
In this thesis, the first tests of the IBL ROD prototype are presented. A correct communication of the DSP to its external memory is verified. Moreover, the implementations for an IBL DSP code are described and tested. This includes the first configuration of the FE-I4 with an IBL ROD. In addition, a working communication with the Histogrammer SDRAM and the Input FIFO on the IBL ROD are demonstrated.

Contents

1 Introduction

During the last century a physics model was developed which explains the basic processes of elementary particle physics. This so called Standard Model made predictions which could be verified with measurements by detectors at high energy particle accelerators. A lot of parameters of this theory are already well described. However, there are still some open issues. One of the main challenges is the question about the origin of mass which is described by the Higgs mechanism. An evidence for the existence of this mechanism is the Higgs particle which is one of the main focusses of the today's high energy particle physics experiments.

To improve the precision of the Standard Model and find hints for physics beyond the Standard Model the Large Hadron Collider (LHC) was built at the CERN[1] research facility in Geneva, Switzerland. Here, two proton beams are collided at a nominal centre of mass energy of presently $\sqrt{s} = 7$ TeV. In these collisions new particles are produced which are detected by high energy particle detectors. One of the main experiments to measure these particles is the ATLAS[2] Detector. It consists of subdetectors which are specialised to give information about the different types of particles.

The innermost subdetector is the ATLAS Pixel Detector. It is made up of an on-detector part which measures the hit information of traversing particles and an off-detector part which is used to transmit the data off the detector and processes it further.

To extent the physics potential the LHC luminosity is upgraded in several phases until 2022. This leads to an increased track density which in particular influences the performance of the innermost ATLAS Pixel Detector layer. Furthermore, radiation damages and detector failures which occurred during operation degrade the Pixel Detector. A fourth detector layer is inserted into the current Pixel Detector to guarantee a good detector performance during the upgrade. This Insertable B-Layer (IBL) is planned to be installed in the first phase of the LHC luminosity upgrade in 2013.

The distance of the IBL to the interaction point is smaller than the distance of the current innermost Pixel Detector layer. This and the higher luminosity lead to an increased track rate which requires a new sensor with higher granularity. In addition, a new readout chip has to account for the increased amount of hit data. To cope with the higher bandwidth which is necessary to transmit the hit data off the detector, a new readout chain is required as well. As a baseline the Read Out Driver (ROD) of the current Pixel Detector is used. This board histograms and analyses the hit data when the detector is calibrated. It also contains a Digital Signal Processor (DSP) which communicates with the readout chips when they are configured or scanned. For the IBL a new enhanced ROD is developed to fulfil the requirements of the IBL.

One improvement of the IBL ROD is the capability to handle four times the data processed by the ROD. Furthermore, the bandwidth of the interface which is used to send the analysed hit information off the ROD has to be increased. On the IBL ROD a Gigabit Ethernet link is used to send the data to an external PC where it is further processed.

To account for the changes in communication with the new readout chip the software of the

[1] Conseil Européen pour la Recherche Nucléaire
[2] A Toroidal LHC Apparatus

DSP has to be changed as well. New configuration streams and an adjusted scan procedure have to be implemented into the IBL DSP software. In addition, the host software which sends commands to the IBL DSP to control the detector has to be adapted.

This thesis gives a short introduction about the Standard Model and physics beyond the Standard Model in Chapter 2. In Chapter 3 is explained how particles interact with matter. An overview of the LHC and the ATLAS Detector is given in Chapter 4.

In Chapter 5 the Pixel Detector is introduced, specifying the relevant physics processes which require a good performance of the B-Layer. Then the ATLAS Pixel Module and the readout chain are described. Moreover, an introduction about the DSP is given. In Chapter 6 the IBL upgrade project is explained.

Chapter 7 is dedicated to the IBL DSP. First, the IBL DSP software code is described, followed by the challenges experienced during the development. Finally, the necessary implementations are pointed out which were done with the IBL DSP code. First hardware tests carried out with an IBL ROD prototype board are described in Chapter 8. Moreover, the implementations of the first version of the IBL DSP code are tested. A conclusion and an outlook are given in Chapter 9.

2 The Standard Model and beyond

Although in every day life people are rarely faced with the field of high energy particles physics this part of science seeks to answer one of the most exciting questions of physics:
What is today's matter and why is it like that?

To answer this question the ancient Greek philosopher Demokrit started in 400 B.C. with the postulation of the atom. Many years later in 1897, Joseph John Thomson discovered the electron and in the 1920s Quantum mechanics was developed by Erwin Schrödinger, Werner Heisenberg, Max Born and many other physicists. Among the latter, Max Planck proposed the Planck constant to define discrete energy values and Wolfgang Pauli introduced the spin of a particle as a new Quantum number. At the same time Quantum Field Theory was developed to describe the elementary particles and their interactions.

While these discoveries have been made by a handful of people, nowadays experiments are made by collaborations of thousands of people organised by research facilities like CERN or KEK[1]. More than 20,000 people from all over the world joined in large groups to discover more and more about particle physics[2], building huge detectors to discover the properties of the smallest particles.

To come to a deeper understanding of how the world is made up a theory was developed which explains the basics of elementary particles. This so called Standard Model (SM) is further explained in Section 2.1. Although the SM was verified many times and led to the prediction and discovery of new particles the model has reached its limits which are listed in Section 2.2.

2.1 The Standard Model

The Standard Model (SM) combines the electroweak and strong force into one theory. It explains the elementary particles as well as the interactions between them. All particles can be categorised by their properties like electric charge, colour charge, spin or mass. These properties define the individual behaviour of each particle. Furthermore, conservation laws such as energy, spin or charge conservation are predicted by the SM which characterises the decay of particles into other particles. All SM particles are listed in Figure 2.1.

The individual force carriers are gauge bosons with integer spin: the photon γ is the interaction particle for the electromagnetic force; the Z^0- and $W^{\pm}$-boson mediate the interactions of the weak force and the gluon g for the strong force. They all have spin 1.

The photon is massless and therefore the range of the electromagnetic force, acting on all charged particles, is infinite. The force carriers of the weak force are massive and thus the weak interaction has a finite range of 10^{-18} m. Both, the electromagnetic and the weak interactions are unified within the electroweak theory.

[1] High energy accelerator research organisation located in Tsukuba, Japan.

[2] Just to mention the members belonging to the CERN Experiments of ATLAS, CMS, ALICE and LHCb (15,600 members) [1], as well as the institutes of Fermilab (2,000 members) [2], Brookhaven National Lab (3,000 members) [3] and KEK (600 members) [4]. The list is not complete because larger collaborations are mentioned only.

The strong interaction is the force which binds quarks into hadrons. It acts on all particles carrying a colour charge: quarks and gluons. Quarks carry one of three possible colour states. Gluons are one of eight different linear combinations of two of three possible colour states. The range of this force is about 10^{-15} m. If the distance between bound quarks increases due to external interactions the energy in the field of the strong force gets so strong that new quark-antiquark-pairs are generated. This effect is called confinement.

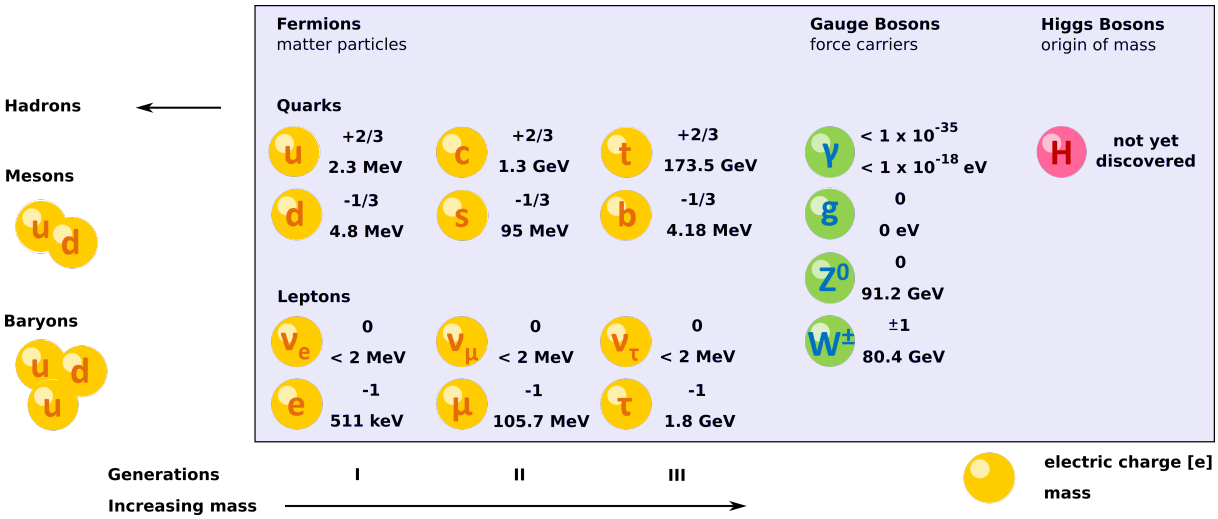

Figure 2.1: The elementary matter particles (yellow) and their interaction particles (green) with their electric charge and mass [5]. The fermions and gauge bosons are already measured particles of the SM. The higgs boson (pink) is still a hypothetical particle to complete the list of elementary particles in the SM.

The particles interacting through these forces are the matter particles of the SM. They are fermions with half-integer spin. The matter particles can be categorized into three generations with increasing mass. For each particle there is an identical partner with opposite electrical charge which is called its antiparticle. Fermions can also be separated into quarks and leptons.

Quarks interact via the strong, electromagnetic and weak force. They carry a so called "colour" which can be one of three states or their anti-states. As there are only colour-neutral particles in nature they never exist as single particles but in colourless compound states which are called hadrons. Hadrons can be separated into mesons and baryons. Mesons contain a quark-antiquark pair with a colour and an anti-colour state, respectively. Baryons consist of three quarks. The three quarks are either the three colour states or the three anti-colour states in order to be colour neutral. Although they are all called matter particles only the u- and d-quarks and the electron e^- form the matter we see in every day life. The most common hadron seen in every day life is the proton, consisting of two u- and one d-quark, and the neutron, consisting of one u- and two d-quarks. The different type of quark is also called "flavour" which can only be changed via the weak force. As the t-quark has the highest mass with 173.5 GeV/c^2 it decays immediately after being produced [6, 7]. Therefore, it does not hadronise.

Leptons contain the electron, the muon and the tau particle and their chargeless neutrinos. The first three interact through the weak and the electromagnetic force. Because neutrinos carry no electric charge they only interact by the weak force and have a very low cross section. Thus, they rarely interact with matter.

Basic parameters of the SM could be verified at the LHC after the first years of data taking. In the following some examples are listed. The full range of measurements cannot be stated here as it would go beyond the scope of this thesis.

At CMS, the W^+W^- production cross section in pp collision data at $\sqrt{s} = 8$ TeV was measured to be $\sigma_{ww} = 69.9 \pm 2.8\,(\text{stat.}) \pm 5.6\,(\text{syst.}) \pm 3.1\,(\text{lumi.})$ pb with an integrated luminosity of 3.54 fb^{-1}. This result is consistent with the SM prediction of $\sigma_{ww} = 57.3\ (^{+2.4}_{-1.6})$ pb [8].

With an integrated luminosity of 2.9 pb^{-1} and an assumed t-quark mass of 172.6 GeV, a $t\bar{t}$ cross section of $\sigma_{t\bar{t}} = 145 \pm 31^{+42}_{-27}$ pb could be measured at the ATLAS Detector in pp collisions at $\sqrt{s} = 7$ TeV [9]. This is as well in agreement with the SM predictions of $\sigma_{t\bar{t}} = 164^{+11.4}_{-15.7}$ pb [10].

Furthermore, the LHCb detector measured the CP-violating phase ϕ_s, the B_s^0 decay width Γ_s and the decay width difference $\Delta\Gamma_s$ of the heavy and light mass eigenstates of the $B_s^0 - \bar{B}_s^0$ system in $B_s^0 \to J/\Psi\phi$ decays at 0.37 fb^{-1} of pp collisions at $\sqrt{s} = 7$ TeV [11]:

$$\begin{aligned}
\phi_s &= 0.15 \pm 0.18\ (\text{stat.}) \pm 0.06\ (\text{syst.})\ \text{rad},\\
\Gamma_s &= 0.657 \pm 0.009\,(\text{stat.}) \pm 0.008\,(\text{syst.})\ \text{ps}^{-1},\\
\Delta\Gamma_s &= 0.123 \pm 0.029\,(\text{stat.}) \pm 0.011\,(\text{syst.})\ \text{ps}^{-1}.
\end{aligned}$$

These results also agree with SM predictions [12, 13].

2.2 The limits of the Standard Model

In an energy range of up to several TeV the Standard Model describes physics very well as was shown in Section 2.1. Particles like the t-quark could be predicted and have been discovered[3]. Still there are many open questions which show the limits of the SM. Some examples are listed in the following.

The SM cannot explain the origin of the masses of the particles. One possibility which is not yet proven is the higgs mechanism. It describes how particles interacting with the higgs field obtain their masses. A hint for the validity of this mechanism is the higgs boson, an excitation of the higgs field. First measurements of a possible candidate of the higgs boson have been undertaken by the CDF and DØ collaborations with an excess around 120 GeV/c^2 in July 2012 [14]. Furthermore, the ATLAS and CMS collaborations could also substantiate the theory of the higgs mechanism in July 2012. As a preliminary result for a possible higgs boson the ATLAS collaboration showed an excess at a mass of 126.5 GeV/c^2 [15]. A new boson with a mass of 125.3 GeV/c^2 was also observed by the CMS collaboration [16]. To prove that this new boson corresponds to the higgs boson, further measurements have to be accomplished in the next years of LHC data taking.

Another example for the incompleteness of the SM is the matter-antimatter asymmetry. According to the model of the Big Bang the universe contained an equal amount of matter and antimatter. This is based on the theory that fermions are always produced in particle-antiparticle pairs. Evidence for a deviation in matter-antimatter symmetry is the fact that we see matter in the universe. This excess of matter with respect to antimatter requires the violation of charge and parity conservation also known as CP-violation within the SM. In this theory particles and antiparticles do not decay in the same manner. But CP-violation within

[3] 1973 Makoto Kobayashi and Toshihide Maskawa predicted the t-quark and 1995 it was discovered at Fermilab at the CDF and DØ experiment [17, 18] .

the SM appears not to be large enough to explain the complete matter-antimatter imbalance. To explain the full asymmetry, physics beyond the SM has to be considered.

The observed flavour oscillations of neutrinos are also not described by the SM. This transmission stems from a very low but non-zero mass and is in conflict with the SM prediction where neutrinos are massless.
As explained in Section 2.1, three of the four fundamental forces, the electromagnetic, the weak and the strong force, are described by the SM. Only gravity is not included in the SM.
Furthermore, dark matter and dark energy cannot be explained by the SM. As it is estimated that most of the universe is made up of dark energy and dark matter and only 4% of visible matter there is still a high discovery potential in particle physics.

A possible theory of new physics which would also include the SM particles is Supersymmetry (SUSY). If realised it would provide a better unification of the couplings of the electromagnetic, weak and strong interaction and could give a dark matter candidate. The fundamental particles of SUSY do not only include the SM particles but also their SUSY-partner which are called sparticles. As these super-partners have a much higher mass than the SM particles discoveries of these are more likely to happen with much higher centre of mass energies than $\sqrt{s} = 8$ TeV.

3 Particle interaction with matter

To measure particles they have to interact with matter in a certain way. Depending on the type of particle, being charged or neutral, very heavy, light or even massless, it generates different signals in the detector material. The measured hits in tracker systems and the deposited energy in calorimeters can be used to reconstruct particle tracks and thus find the point of origin and the properties of the particles. The following chapter describes how particles interact with matter, see Section 3.1, gives an overview about detectors used in high energy physics, see Section 3.2, and leads to the use of silicon material as detector material, see Section 3.3. Finally, it describes the effects of high irradiation to silicon in Section 3.4.

3.1 Fundamental interactions

To measure an incident particle it has to interact with the medium it traverses. This can be via bremsstrahlung, elastic and inelastic scattering or pair-production.

A particle is deflected from its original path by the electric field of a nucleus while traversing close by to it. Due to this deflection it radiates bremsstrahlung. The effect is proportional to the square of the inverse of the particle's mass:

$$\sigma \propto \left(\frac{e^2}{mc^2}\right)^2 . \tag{3.1}$$

Elastic scattering deflects the particle's track without energy loss inside the detectors. This leads to multiple scattering and is an unwanted effect in track reconstruction. To achieve as little energy loss by multiple scattering as possible it is very important to reduce this effect and as a consequence to avoid dense material inside the detector.

For particle detection the inelastic scattering is more relevant. Through this interaction the atoms of sensitive detector materials can be ionised and thus create electron-ion pairs. These charge carriers can move through the material. With an external electric field the initial charges can generate secondary charge carriers and thus enhance the number of ionised atoms. This can be measured by detector electrodes. The mean energy loss during ionisation and as a function of particle momentum is described by the Bethe-Bloch formula [19, 20]:

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2} \cdot \left[ln\left(\frac{2m_e\gamma^2 v^2 W_{max}}{I^2} - 2\beta^2 - \delta - 2\frac{C}{Z}\right)\right], \tag{3.2}$$

with the values described as follows:

N_a	$= 6.022 \times 10^{23}$ mol^{-1}	: Avogadro's Number
r_e	$= 2.817 \times 10^{-13}$ cm	: classical electron radius
m_e	$= 511$ keV	: electron mass
ρ	$= 2.33$ gcm^{-3}	: density of absorbing material silicon
I	≈ 173 eV	: average effective ionisation potential
Z	$= 14$	: atomic number of absorbing material silicon [e]
A	$= 28$	: atomic weight of absorbing material silicon [u]

z	$\propto$ e	: charge of incident particle
β	$= v/c$	: speed of incident particle
γ	$= 1/\sqrt{1-\beta^2}$	: Lorentz factor
δ		: density correction
C		: shell correction
$W_{max} \approx 2m_e c^2\beta^2\gamma^2$		: maximum energy exchanged during a collision of particles with $M \gg m_e$

The Bethe-Bloch formula is not valid for electrons as here the main energy loss due to bremsstrahlung has to be taken into account. This is not the case for particles with higher mass than the electron mass. Here bremsstrahlung has to be considered at much higher energies. For muons for example at an energy of about 1 TeV.

The functional behaviour of the Bethe-Bloch formula can be separated into three parts, see Figure 3.1. For the low energetic part the formula is dominated by the term $1/\beta^2$ and leads to

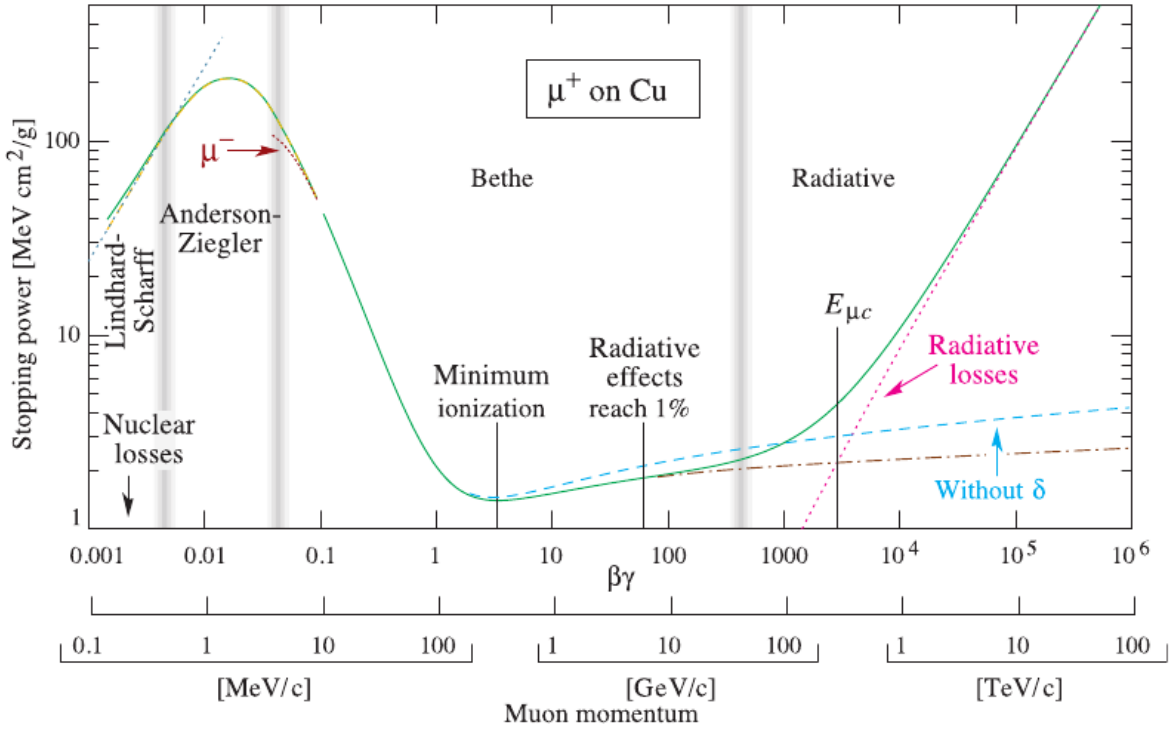

Figure 3.1: The mean energy loss or stopping power of antimuons in copper described by the Bethe-Bloch formula as a function of $\beta\gamma$ (solid curve). Additionally, the ranges for very low and very high stopping power where the Bethe-Bloch formula is not valid anymore is shown [6].

a decrease of the mean energy loss until a minimum for ionisation at $v \approx 0.96\ c$ with a mean energy loss or stopping power of 1.5 MeVcm^2/g is reached. Particles having such velocity are therefore called minimal ionising particles (m.i.p.). The position of the minimum is dominated by the charge of the particles rather than the mass. This leads to the fact that most particles are considered as a m.i.p. At even higher energies the logarithmic part dominates and leads to a slow increase of energy loss.

The density effect δ considers the polarisation of the atoms inside a material along the path of the incident charged particle. The electrons of the atom which have a higher distance to

the charged particle are thus shielded and do not feel the full charge of the incident particle. The shielding is even more effective if the material is denser. Therefore, the correction is called density effect. This decreasing energy loss is especially important for relativistic energies as the range of the transverse electric field increases as well. The density correction also leads to the saturation of the Bethe-Bloch formula at relativistic energies.

The shell correction C becomes effective if the velocity of the incident particle is very small. For the Bethe-Bloch formula without any corrections it was assumed that the electrons of the material's atoms are stationary with respect to the incident particle. This is not valid anymore if the incident particle has a velocity which is smaller than the velocity of the bound electrons of the atom.

At very low and very high values of $\beta\gamma$ the Bethe-Bloch formula is also not valid anymore. A particle in the low energy range temporarily captures electrons on its way through the material. The particle then acts as a neutral particle. This effect of a changing charge of the incident particle is not taken into account in the Bethe-Bloch formula [21].

In a range of $0.01 < \beta\gamma < 0.05$ the phenomenological description by Andersen and Ziegler predicts the mean energy loss quite well [22, 23]. For particles moving slower than $v \approx 0.01c$ the gradient of the mean energy loss is explained by Lindhard-Scharff and is proportional to β. For even lower energies the main energy loss is caused by nuclear recoil [24].

The μ^- in Figure 3.1 denotes the Barkas effect which points out the difference in stopping power between positive and negative muons [25].

At $\beta\gamma > 1,000$ radiative losses mainly caused by e^+e^--pair production and bremsstrahlung become dominant [26].

High energetic charged particles also lose energy due to Cherenkov-radiation and transition radiation. As only the latter effect is used in the frame of this thesis the Cherenkov-effect will not be described here. Transition radiation occurs as soon as a high energetic charged particle crosses the boundary between two media of different dielectric constants. The charged particle polarises the first medium while traversing it and thus produces an electromagnetic field. As soon as the particle reaches the next medium the field from one to the other medium has to change. To compensate for the continuous change of the electric field x-rays are emitted at the boundary layer of the two media [27].

As already stated, the Bethe-Bloch formula describes the mean energy loss of an incident charged particle. However, the functional behaviour of the actual energy loss is described by the Landau distribution. It takes the additional energy loss produced by the statistical fluctuations of further collisions into account. The latter is provoked by high energetic electrons which are knocked out of the atom due the initial incident particle. These δ-electrons have such a high kinetic energy that they are able to ionise other atoms and evoke so called secondary ionisation [20]. To account for all energy losses except ionisation, for example phonon excitation, the Fano factor F is introduced. It determines the deviation of a fixed value of Energy E needed for creating N electron-hole pairs [28]. The fluctuation of the number of generated electron-hole pairs is described as

$$< \Delta N^2 >= FN = F\frac{E}{w} \quad . \tag{3.3}$$

For semiconductors and gases $F < 1$ is obtained [20, 29].

Due to energy loss electrons cover a certain distance through matter which is dependant on the number of nucleons inside a material and its density. After this so called radiation length X_0 the energy of the particle is reduced to 1/e due to radiation and can be described by the

following formula:

$$X_0 = \frac{716.4\ \mathrm{g\,cm^{-2}}\ A}{Z(Z+1)\ln(287/\sqrt{Z})} \quad . \tag{3.4}$$

Z and A are the atomic number and nucleon number, respectively. High energy photons can loose their energy by pair-production in creating an e^+e^--pair or due to the photoelectric effect and Compton scattering. The mean free path for such a photon is defined by:

$$\lambda = \frac{9}{7} X_0 \quad . \tag{3.5}$$

A corresponding relation for hadrons, for instance a proton, can be described by the nuclear interaction length:

$$\lambda_n = 35\ \mathrm{g\,cm^{-2}} A^{1/3} \quad . \tag{3.6}$$

3.2 Particle detection

Tracking Detectors

On the basis of the particle interactions with matter, described in Chapter 3.1, properties like mass or momentum of the particles can be determined.

The momentum of charged particles can be measured by their bent trajectory inside a magnetic field $\vec{B}$. This can be done by calculating the sagitta of the curve. An explanation of this relation can be seen in Figure 3.2. The particle path can be described by connecting two points of the curve with a straight line of length L. The curve is a sector of a circle with an opening angle of θ and a radius R. The deviation of a charged particle with momentum p flying in z-direction is thus sensitive to the y-component of the magnetic field B_y [30]:

$$s = \frac{eB_yL^2}{8p} \quad . \tag{3.7}$$

To measure the curved trajectory of the charged particle a tracking detector is needed which is placed inside a magnetic field.

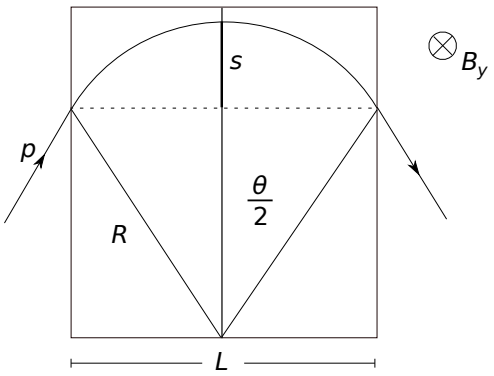

Figure 3.2: The curved track of a charged particle with momentum p in a magnetic field. The deflection angle θ, the radius R, the length L and the sagitta s are shown.

Tracking detectors in current experiments are mainly made of solid state material, for example silicon, see Chapter 3.3. With such a sensor it is possible to gain a high granularity which leads

to a good position resolution. This is particularly important if the particle flux is high which is the case close to the interaction point. The resolution of the position x of a traversing particle can be calculated by

$$\sigma = \left[\frac{1}{d}\int_{-d/2}^{+d/2} x^2 \,\mathrm{dx}\right]^{1/2} = \frac{d}{\sqrt{12}} \ , \tag{3.8}$$

with d being the pitch of the sensor. In this formula a homogeneous distribution of the particle flux between $-d/2$ and $+d/2$ is assumed. If not only the hit information of the single hit is used but the additional charge distribution within a cluster is available, the resolution can even be increased.

A magnet surrounding the tracking detector can be used to deflect a charged particle by the Lorentz force:

$$\vec{F} = \pm e(\vec{E} + \vec{v} \times \vec{B}) \ . \tag{3.9}$$

With measuring this curved trajectory the momentum p can be determined.

Calorimeters

The energy of particles is measured in so called calorimeters. Electrons, positrons and photons are measured in electromagnetic calorimeters, whereas hadrons are measured in hadronic calorimeters. Both are explained in the following.

Electrons have to penetrate a material with high atomic number to highly interact with it. A sequence of e^+e^--pair-production and bremsstrahlung induced by a high energetic particle initiates an electromagnetic shower. Finally, only low energetic electrons and photons are left which mainly loose their energy due to ionisation and are thus fully absorbed by the calorimeter. A scintillator directly placed at the absorbing material measures the energy of all shower particles which is equal to the energy of the primary particle. Photons are measured in a similar way.

Knowing the radiation length X_0 for charged particles, see Equation 3.4, the optimal size of such a calorimeter can be determined. Two possible setups are used in high energy physics: a sampling and a homogeneous calorimeter. A sampling calorimeter consists of alternating layers of a dense material with high atomic number, lead or steel, and a sensitive material like a scintillator. A homogeneous calorimeter consists of crystals with a high atomic number which serve as absorber and sensitive material at the same time. To receive a measurable quantity, photomultipliers convert the energy of the photons received by the scintillator or the crystal into a current.

The longitudinal distance of electromagnetic showers is dominated by the high energy of the initial particle. To determine the transversal behaviour the Molière radius is used:

$$R_M = 21 \text{ MeV} \, \frac{X_0}{E_c} \ , \tag{3.10}$$

with E_c as the critical energy which defines the energy at which the ionisation loss per radiation length is equal to the initial electron energy [27].

To fully absorb hadronic particles with a calorimeter a denser absorber material than in the case of an electromagnetic calorimeter is needed. This can be explained by the longer hadronic radiation length λ_n stated in Equation 3.6. Charged hadrons can ionise the absorber nuclei or interact with it through the strong interaction. If an inelastic scattering process occurs secondary particles like charged or neutral pions or η-mesons are produced. The final state products are again photons and charged particles which can be measured in a similar way as it is done at electromagnetic calorimeters. Because of excitation and spallation processes inside the absorber

material some of the energy of the original particle stays inside the absorber and thus cannot be fully measured by the sensitive material. Iron and copper are suitable for the absorber material. The sensitive material may be scintillators or liquid ionisation chambers.

With the energy E deposited in calorimeters the particle's mass m can be calculated according to

$$E = \sqrt{(mc^2)^2 + (pc)^2} \ . \tag{3.11}$$

Muon detector

A common particle detector consists of several layers of subdetectors so that a generated particle first traverses a tracker system and deposits its full energy inside the calorimeters. Only muons and neutrinos are able to traverse both tracker and calorimeters completely due to their low interaction cross sections. As the neutrino is not even charged it also traverses the Muon detector without being measured. As the muon is charged tracking detectors are used to detect the muon's track via ionisation loss at this part of the detector. Muon chambers are often made up of drift chambers. These consist of a gaseous volume, mostly argon, containing an anode wire. At the outer region the cathode wires are arranged.

Particle identification

With the above mentioned detectors energy, momentum and as a result the mass of a particle can be determined. Because particle detectors are often built as a 4π-detector the collision point of two colliding particles can be completely surrounded. Thus, all final state particles of one collision event have to penetrate through the detector layers and can be measured. As the neutrino is not directly measured by any of the described detectors only its missing energy after a full event reconstruction can be calculated. Due to momentum conservation the sum of the transversal momentum $\sum \mathrm{p_T}$ of all measured particles in a 4π-detector has to be zero. A deviation from this value therefore indicates that a particle traverses the detector without being measured. This is the case for a neutrino.

With a complete event reconstruction the physics processes occuring during such a collision can then be determined. An example of a 4π-detector is the ATLAS Detector explained in detail in Chapter 4.2.

3.3 Silicon as sensitive detector material

Crystal silicon is a good material used for tracking detectors. It has a small band gap and is a semiconductor which can therefore be depleted. Hence, it is suitable for detecting traversing charged particles as explained in the following. The sensor is made up of two differently doped areas. An n-doped area has implemented atoms with one more electron than silicon which are called donors. In case of silicon a donor would be phosphorus or arsenic. In contrast a p-doped area has an implemented atom with an electron less which is called acceptor. In case of silicon an acceptor would be boron. To establish an equilibrium state the free charge carriers drift to the oppositely doped area and built a space charge region, see Figure 3.3. In addition, an electric field opposite to the field between the doped areas arises. This zone is also called depletion zone because no free charge carriers are present.

If an external reverse voltage is applied to this pn-junction the space charge region expands. Is the reverse bias high enough, the doped areas are fully depleted and do not contain any free

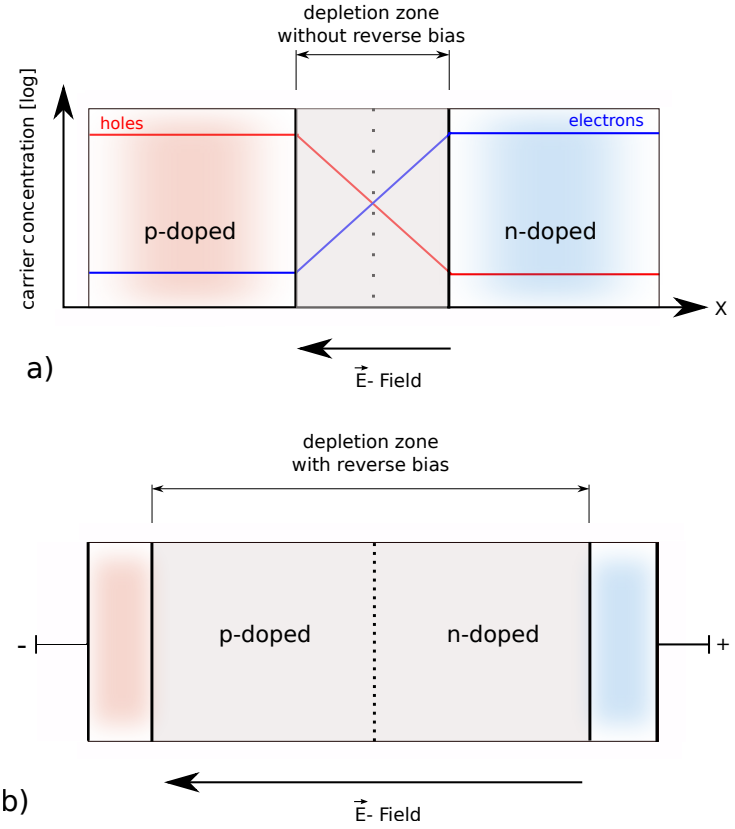

Figure 3.3: a) The pn-junction without a reverse bias voltage. The coloured areas indicate the particular doped area in a non depleted state. They grey area is the depletion zone and contains no free charge carriers. b) The pn-junction with reverse bias voltage and increased depletion zone.

charge carriers. This bias voltage is called depletion voltage. The n- and p-doped areas together with an applied external electric field behave similar to a reverse-biased diode.

If a charged particle traverses this depletion area electron-hole pairs are created along the path of the incident particle and the generated free charge carriers can be measured. If no electric field is applied the electron-hole pairs would recombine immediately and thus do not contribute to the detector signal.

To determine the average number of electron-hole pairs N the absorbed energy E has to be divided by the average energy needed to create one electron-hole pair w which is 3.62 eV in silicon[1]. This is much higher than the band gap of silicon which is 1.12 eV. The excess of energy is transformed in lattice oscillations or phonons inside the silicon material and heats up the sensor. The fluctuation of the number of generated electron-hole pairs N is described by Formula 3.3. An electron or hole generated this way can be assumed to be a free charge carrier which can travel through the medium due to different effects. Diffusion occurs if there is a local excess of charge carriers inside the silicon material. This disequilibrium is compensated by moving charge carriers from one to the other excess region.

[1]The creation of one electron-hole pair inside a gaseous detector is in the order of 20 eV.

More important for the detection of signals in silicon is the effect of charge drift. An external electric field accelerates the electrons and holes along the direction of the electric field $\vec{E}$ and leads to a current per unit area:

$$\vec{J}_{n,drift} = -en\mu_n\vec{E} \ , \qquad \vec{J}_{h,drift} = en\mu_h\vec{E} \ . \tag{3.12}$$

μ_n and μ_h are the mobilities for electrons and holes, respectively. n is the carrier concentration and e the electron charge. The mobility depends on the temperature and the doping and impurity concentration of the material. Inside a high electric field the free charge carriers are accelerated until a saturation velocity is reached. The latter just depends on the mean free path or the mobility μ inside the material. The applied voltage U_{bias} for particle detectors depends on the doping concentration and the sensor thickness and is slightly higher than the depletion voltage U_{depl}. This is done to establish a non-zero electric field at the electrodes which then can be reached by the drifting charge carriers. A common value for unirradiated sensors is $U_{bias} = U_{depl} + U_a \approx 150$ V, in which U_a is the increase relative to the depletion voltage of about 30-50 V. While the charges are drifting due to the external electric field simultaneous diffusion causes a spread of the charges which is perpendicular to the direction of the electric field. This leads to charge sharing in which signal charges do not induce a charge on one pixel segment but on several ones.

In the presence of a magnetic field the carriers are deflected according to the Lorentz force described in Equation 3.9. The resulting deviation angle, or Lorentz angle θ_L, can then be described via the Hall mobility μ_{Hall}:

$$tan\ \theta_{L,n} = \mu_{Hall,n}B_\perp \ , \qquad tan\ \theta_{L,h} = \mu_{Hall,h}B_\perp \ . \tag{3.13}$$

$B_\perp$ is the magnetic field perpendicular to the velocity of the charge carriers. The Hall mobility can be described with the before mentioned mobility $\mu_{Hall} = r\mu$, with r being the Lorentz factor[2]. Due to the Lorentz angle, the charge sharing effect is increased. Thus, the Lorentz angle has an impact on the spatial resolution and the cluster size [31].

To realise a particle detector, n^+-doped pixel implants are placed in the n-type bulk of the sensor, see Figure 5.3. As a result, an incident charged particle creates electron-hole pairs with the electrons being accelerated in the direction of the higher n^+-doped implants on top of the sensor. The implants act as electrodes and measure an electrically induced signal according to Ramo's law while the electrons are moving towards them [32]:

$$i = E_v ev \ . \tag{3.14}$$

i is the current measured at the implant due to a single electron, e is the electron charge, v the velocity of the electron and E_v is the weighting field. A sensor with an n-bulk and n^+-doped implants is called n^+-in-n sensor and is used as sensitive material for the Pixel Detector discussed in this thesis. n^+-doped implants provide a still n-doped area while the original n-doped bulk changed to a p-doped bulk at a certain radiation dose, see Section 3.4. A possibility to isolate the n^+- and n-type zones from each other is the implementation of a p-doped zone called p-spray which is brought up between the two n-type zones [33]. Thus the implants are isolated in case the reverse bias is applied. Using such implants the granularity of a pixel detector can be very high. This is especially important for b-tagging as described in Chapter 5. Taking Equation 3.8 into account the resulting small distances, which are in the order of several µm, between the n^+-doped implants yield a very good spatial resolution of charged particle's hits.

[2]The Lorentz factor r is measured to be 1.15 for electrons and 0.72 for holes at a temperature of 0°C.

Electron-hole pairs can also be generated by thermal energy at the surface of the material or within the depleted bulk. This leads to a leakage current and is observable as noise when measuring a particle signal.

Applying a very high reverse bias voltage causes a so called breakdown in which a high leakage current occurs so that the sensor is badly damaged and signal detection is not possible anymore.

3.4 The effects of radiation on silicon

Silicon has a crystalline structure which determines the behaviour of the material. This lattice structure as well as additional doping can be affected by a high radiation dose and hence change the behaviour of silicon. Due to these lattice defects of the material the efficiency in detecting particles decreases. The main effects causing such damages inside the silicon structure are explained in the following. Damages due to radiation can occur inside the sensor bulk and at the surface of the sensor. As the first is more crucial regarding the efficiency of particle detection merely defects inside the bulk are considered here.

A not reversible bulk damage is the displacement of a single silicon atom. For this a minimum energy of 25 eV is needed. This can be achieved by an electron with a minimal energy of 260 keV or a proton or neutron with a minimal energy of 190 eV. If the incoming particle has even more than the minimal energy the recoiling atom can induce further damage inside the sensor. With an energy of the silicon atom of more than 2 keV it can even damage a complete region inside the lattice and thus produce a cluster defect [28].

Point defects which come from radiation are for example silicon vacancies and interstitials. The latter are atoms inside the material which are not included inside the lattice structure but in between. Vacancies describe a missing atom inside the regular lattice structure. Depending on the temperature both defects can move through the lattice and may recombine with other defects. Still they can have an effect on the space charge inside the depletion region: They produce additional energy levels. If these are located inside the band gap of silicon the defects act as generation-recombination centres and increase the leakage current.

Another side effect of defects is charge trapping in which a signal charge is kept for a longer time than the usual charge collection time needed to produce the full signal. As a result, the final signal height measured at the electrodes is smaller than in an unirradiated sensor. After a dose of 10^{15} n_{eq}/cm^2 the effect becomes relevant as about 50% of the signal will be lost due to charge trapping.

Moreover, charge defects have an impact on the reverse bias. To fully deplete the sensor after irradiation, a higher operation voltage is necessary. Hence, the leakage current increases and therefore the power dissipation is higher as well. This heats up the sensor which in turn leads to a higher leakage current. As a consequence, a higher operation power is needed which would again increase the leakage current. This cycle which further increases the operation voltage and the leakage current is called *thermal runaway* and makes the cooling of silicon inevitable.

Radiation also impacts the effective doping concentration. The ratio of donor- and acceptor-like states changes due to defects. Inside an n-type doped bulk the majority charge carriers are electrons which can be removed easier than holes inside a p-type bulk. Radiation damages thus alter the original n-type bulk to a p-type one. As a consequence of this type inversion the pn-junction moves to the n^+-segmented pixel side and the growth direction of the depletion zone changes.

To describe the radiation damages independent of the particle type all deposited energy except the energy used for creating electron-hole pairs can be expressed by *Non-Ionising Energy Loss*

(NIEL). The NIEL caused by a certain flux of an arbitrary type of particle is normalised to the NIEL caused by 1 MeV neutrons. The unit is the neutron equivalent fluence n_{eq}/cm^2.

Due to thermal energy defects are able to move through the sensor. To prevent this the sensors are cooled down in normal detector operation. If the sensor is exposed for several hours to higher temperature of about 30 to 60°C the annealing effect is increased. Differently charged defects can recombine due to thermal energy and become inactive. This is observable as the effect of trapping is decreasing after that time. In contrast, a longer annealing time of several weeks increases the effects of radiation damages. In this case the impact of defects in combination with higher temperature changes the crystal lattice in a more complex way. This effect is called reverse annealing [34]. Even in periods during which the sensor is not exposed to high radiation cooling is needed to avoid reverse annealing.

The described radiation damages have to be considered during detector operation with high irradiation and silicon as sensor material and lead to a necessary upgrade of the detector which is further explained in Chapter 6.

4 Experimental setup

4.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is a proton-proton collider with a nominal centre of mass energy of 14 TeV and is located at CERN[1] in Geneva. A schematic drawing of the ring can be seen in Figure 4.1. The LHC is located inside a tunnel which is about 100 m underground and

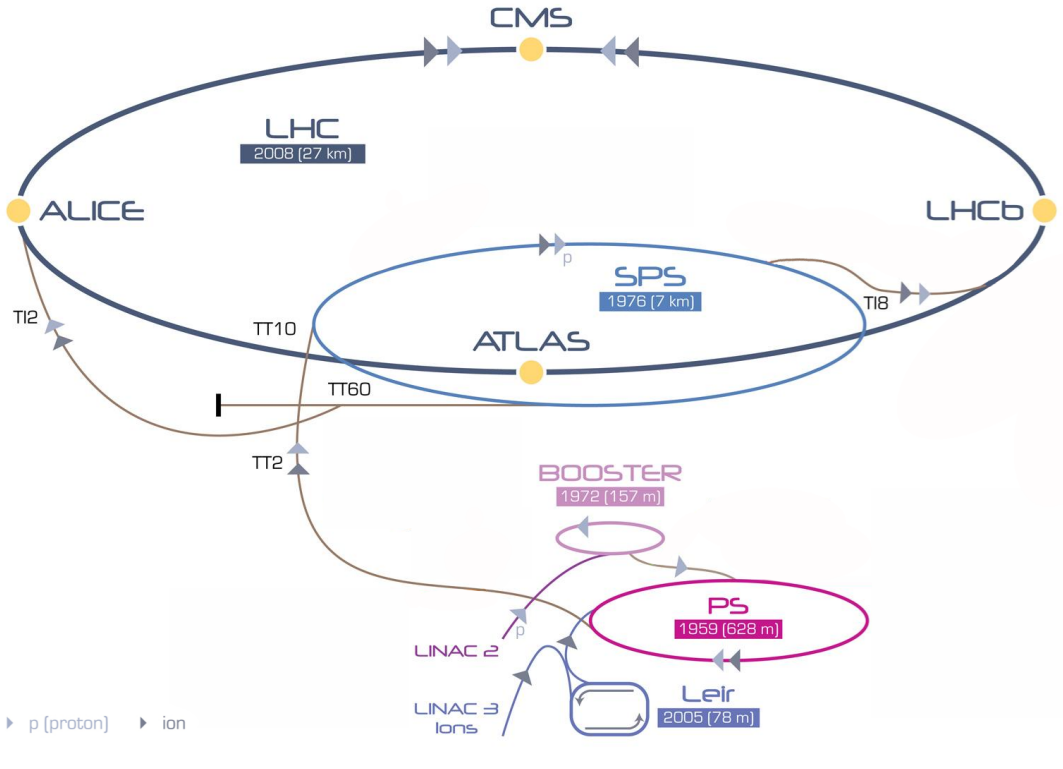

Figure 4.1: A schematic of the LHC ring [35]. Shown are the pre-accelerators, the two proton injection points and the four main experiments ATLAS, LHCb, CMS and ALICE.

has a circumference of 27 km. It is built inside the former tunnel from the previous accelerator machine Large Electron-Positron (LEP) Collider which was in operation from 1989 until 2000.

With a complex system protons are injected into a subsequent order of different machines to accelerate the particles up to 7 TeV. The protons themselves are taken from a hydrogen bottle. After stripping off the electrons from the hydrogen the protons are accelerated up to an energy of 50 MeV by the 30 m long linear accelerator 2 (LINAC2). From there they are injected into the Proton Synchrotron Booster (PSB) and brought up to an energy of 1.4 GeV. In the following Proton Synchrotron (PS) and Super Proton Synchrotron (SPS) they are further accelerated to

[1] Conseil Européen pour la Recherche Nucléaire

an energy of 25 GeV and 450 GeV, respectively. All three synchrotrons are circular accelerators with increasing circumferences of 50 m, 628 m and 7 km [36].

Finally, the protons are injected as bunches in two opposite directions into the LHC ring at the injection points TI 8 and TI 2 [37]. If the LHC is completely filled up each beam consists of 2808 bunches. Each bunch contains 1.5×10^{11} protons. With this setup every 25 ns a collision between two bunches takes place. This leads to a bunch crossing frequency of 40 MHz and determines the clock frequency for detector readout.

In the LHC the protons are accelerated by 16 cavities and focused with 858 quadropole magnets to counteract their electromagnetic repulsion. To keep the bunches on a circular track 1,232 dipole magnets are used. All these magnets are superconducting and have to be cooled down to temperatures of about 1.9 K. A drawing of a dipole magnet is shown in Figure 4.2.

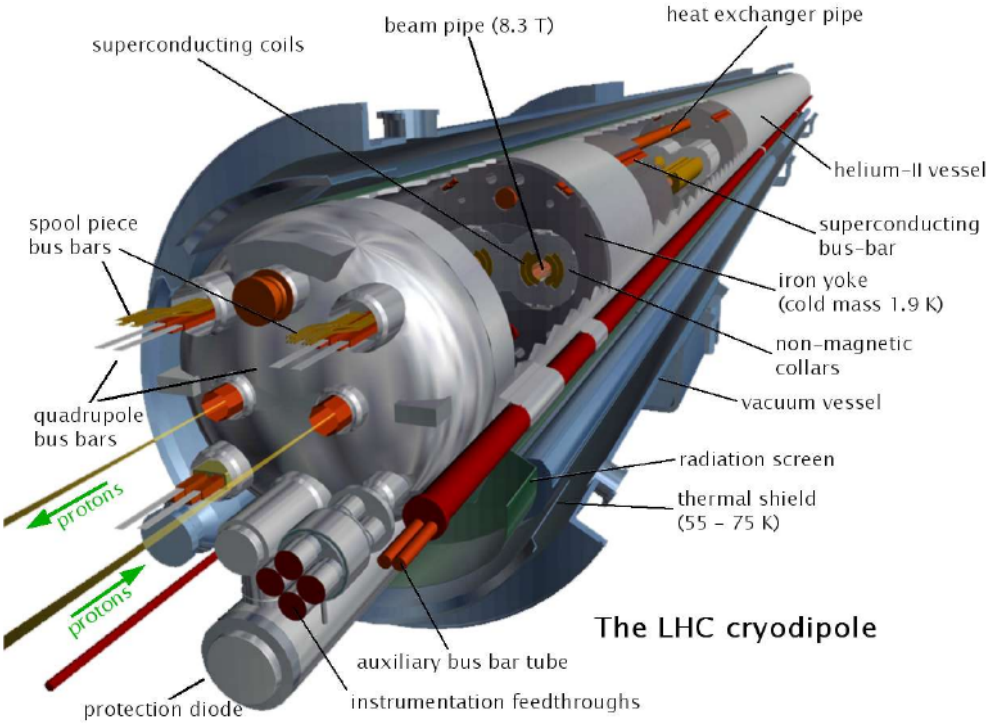

Figure 4.2: A drawing of an LHC dipole [38]. The main elements are the two beam pipes which are enclosed by superconducting coils, a non magnetic collar and an iron yoke to gain a magnetic field of 8.3 T. To cool the superconducting magnets down to 1.9 K a helium-II vessel is used. An additional vacuum vessel surrounds the magnet and keeps an insulating vacuum [39]. Additionally, a heat exchanger and a thermal shield provide temperature compensation. Several bus bars interconnect the individual magnet elements.

The four main experiments making use of the collisions of the LHC are the ATLAS[2]-, CMS[3], LHCb[4]- and ALICE[5] detectors. The first three mentioned record the data of proton-proton collisions.

[2]A Toroidal LHC Apparatus
[3]Compact Muon Spectrometer
[4]Large Hadron Collider beauty
[5]A Large Ion Collider Experiment

ATLAS and CMS are built as discovery machines: Both are 4π-detectors which are sensitive to all detectable particles independent of their direction of flight. With up to 30 proton-proton collisions per bunch crossing ATLAS and CMS gain a high luminosity. The peak luminosity of both detectors is about 6×10^{33} cm^{-2}s^{-1} in August 2012 [40]. Having a flexible trigger system the produced particles and their decays can be analysed individually. These properties enable ATLAS and CMS to detect and analyse particles in different topics of high energy particle physics. More details about the ATLAS Detector can be found in Section 4.2.

The LHCb Detector only analyses one proton-proton collision per bunch crossing and thus has a better spatial resolution. Its main task are precise measurements in the field of b-quark physics.

Besides protons, also lead ions are collided inside the LHC which are especially analysed by the ALICE Detector. The aim of these heavy-ion collisions is the production of a quark gluon plasma and hence the generation of matter as it is thought of to be present in the early stages of the universe [41].

On 10th September 2008 the first proton beam circulated inside the LHC. Due to a mechanical damage which occurred during this event a long technical stop followed. The first proton-proton collisions took place on 23rd November 2009 with a centre of mass energy of 450 GeV. On 30th March 2010 the LHC started for the first 7 TeV collisions. Finally, the first 8 TeV collisions took place on 5th April 2012 and result in an already large amount of data.

A quantity to obtain the amount of data is the integrated luminosity. It is defined as the integration of the luminosity:

$$\mathcal{L}_{int} = \int \mathcal{L}\,\mathrm{dt} = \int \frac{N_a\, N_b\; j\, v}{A\, U}\,\mathrm{dt}, \tag{4.1}$$

with N_a and N_b being the number of particles inside the storage ring, j the number and v the velocity of bunches, U the circumference of the storage ring and A the cross section of the beam during collision [42]. In 2011 the ATLAS Experiment reached an integrated luminosity of 5.6 fb^{-1} with a centre of mass energy of 7 TeV. In 2012 the total integrated luminosity has already reached ~ 10 fb^{-1} after the first half year of data taking with a centre of mass energy of 8 TeV.

4.2 The ATLAS Detector

With a size of 42 m in length and 22 m in diameter the ATLAS Detector is the biggest of the LHC detectors. It is a 4π-detector, meaning that the full solid angle surrounding the interaction point is completely covered by detector material. Thereby, it can be ensured that particles traversing from the interaction point towards the outer region are detected in any case. The detector consists of several subdetectors arranged in an onion-like structure as can be seen in Figure 4.3.

The Tracking Detectors

The innermost detector is the Inner Detector (ID) which is made up of the Pixel Detector, the Semi-Conductor Tracker (SCT) and the Transition Radiation Tracker (TRT). The complete ID is shown in Figure 4.4. All subdetectors of the ID are made for particle tracking purposes and as a consequence have a high spatial resolution. It is enclosed by a solenoid magnet with a central

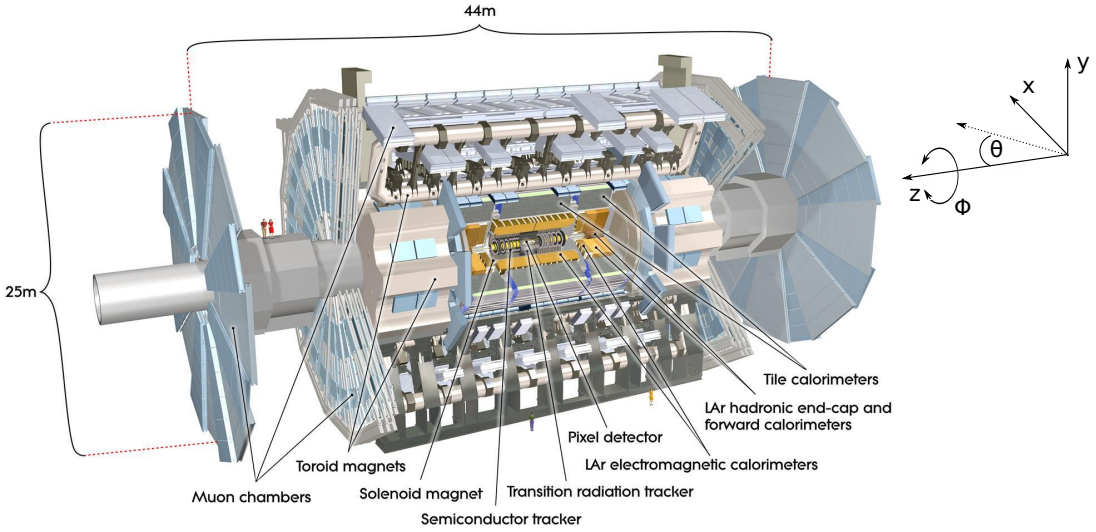

Figure 4.3: The different layers of the ATLAS Detector [43]. The subdetectors and the ATLAS reference coordinate system are described. Two humans standing on the ATLAS radiation shield between the end cap Muon chambers give an imagination of the proportions of the ATLAS Detector.

magnetic field of 2 T. The outer radius of the ID is 2.1 m with a length of 6.2 m. The individual subdetectors are explained in the following in more detail.

The Pixel Detector is explained in Chapter 5 as this belongs to the main topic of this thesis.

The SCT consists of silicon elements which are segmented into stripes with a size of 80 µm × 12.6 cm. Four barrels with radii of 30, 37.3, 44.7 and 52 cm cover a region[6] of $|\eta| < 1.4$. Two end caps each consisting of nine disks cover the region of $1.4 < |\eta| < 2.4$. In total there are 2,112 barrel modules and 1,976 end cap modules containing p-in-n stripe sensors [44]. Similar to the Pixel Detector the SCT experiences radiation damages due to an estimated flux of 2×10^{14} n_{eq}/cm^2 after 10 years of operation [45].

The TRT is composed of drift tubes in which 52,544 axial tubes with a length of 150 cm are used for the barrel part and 319,388 radial tubes with a length of 39 cm to 55 cm build the end caps [46]. Each tube has a diameter of 4 mm and is filled with a gas mixture which mainly contains xenon and carbon dioxide. It consists of a 30 µm gold-plated tungsten wire as anode as well as 60 µm thick multi-layer film of carbon-polyimide as cathode [47]. The drift tubes are embedded inside a 15 µm diameter polypropylene/polyethylene fibre radiator. A high energetic charged particle crossing the boundary between carbon dioxide and the polypropylene fibres or traversing the radiator itself then emits transition radiation as explained in Chapter 3.1. Besides the transition radiation, charged particles also directly ionise the gas inside the drift tubes. Measuring the time the produced electrons and holes drift from the point of ionisation towards the anode or cathode the path of the originating particle can be reconstructed. With these two effects traversing particles in an area of $|\eta| < 0.7$ and $0.7 < |\eta| < 2.5$ can be measured by the TRT barrels and end caps, respectively. A complete overview of the Inner Detector and its covered area is shown in Figure 4.4.

[6]The pseudorapidity η is a spatial coordinate commonly used in 4π-detectors and depends on the polar angle θ: $\eta = -\ln[\tan\theta/2]$.

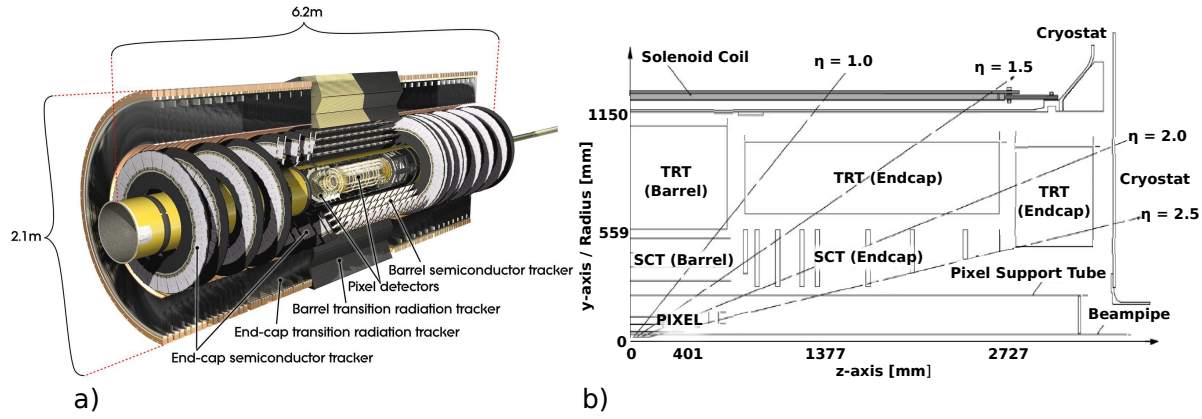

Figure 4.4: a) A drawing of the three subdetectors of the ID [38]. b) The ID subdetectors Pixel Detector, SCT and TRT. Shown are the different layers and end caps of the detectors in the yz-plane of the ATLAS coordinate system. In the outer region the solenoid magnet coil is indicated. See Figure 4.3 for a description of the ATLAS coordinate system. Additionally, the corresponding pseudorapidity η and radius are shown [45].

As already mentioned the ID is surrounded by a superconducting solenoid magnet, see Figure 4.4 b), providing a magnetic field of 2 T. The size of the bore is 2.3 m and the length is 5.3 m. To ensure that the solenoid interacts as little as possible with traversing particles it is made up of 44 mm thin high-strength aluminium [48]. Thus, a radiation length of 0.63 X_0 is achieved [49]. To return the magnetic flux of the solenoid the Tile Calorimeters are used, see Figure 4.5.

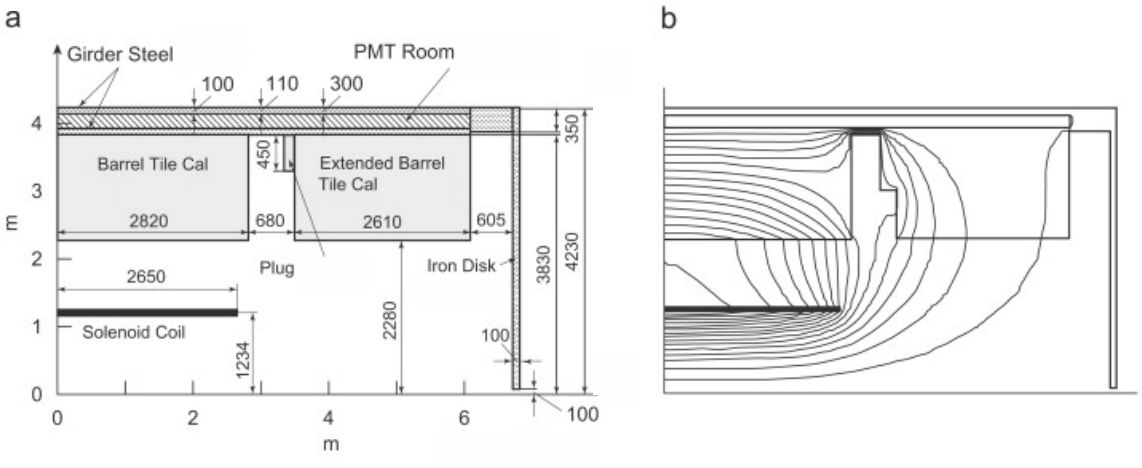

Figure 4.5: a) The solenoid magnet and the Tile Calorimeter. The ID and LAr Calorimeter are not shown in this drawing. The Tile Calorimeter is acting as return yoke for the magnetic field within the ATLAS xy-coordinate system. Further details of the Tile Calorimeter structure are explained in the text. b) The magnetic field lines within the detector components described in a) [50].

The Calorimeters

While the ID is mainly built for tracking the following calorimeters are important for measuring the energy of the particles. Right outside the solenoid the Liquid Argon (LAr) Calorimeter is placed. It consists of the LAr Electromagnetic Barrel and two end caps each containing the LAr Forward Calorimeter, the LAr Electromagnetic end cap and the LAr Hadronic end cap, see Figure 4.6. The barrel consists of 1.9 mm thick lead absorber layers with liquid argon as detecting medium in between [49]. The lead layers are arranged in an accordion structure to allow signal detection independent of the particle's incident angle. The barrel is 6.8 m long and covers a radius of 1.15 m $< r <$ 2.25 m. It is placed inside an aluminium alloy with vacuum insulation. The end cap LAr Electromagnetic Calorimeter consists of an accordion structure, too. But here the amplitude of the accordion waves scales with the radius. Similar to the barrel an aluminium cryostat with vacuum isolation surrounds the end cap. The complete end cap has a length of 3.17 m and an outer radius of 2.25 m. The radial coverage of the complete electromagnetic LAr detector is $|\eta| < 3.2$.

The two wheels of the LAr Hadronic Calorimeter end caps have an outer radius of 2.03 m. They consist of two parallel copper plates as absorber which enclose Kapton electrodes. The spatial detection capability of the LAr Hadronic Calorimeter is $1.4 < |\eta| < 4.8$.

The LAr Forward Calorimeter is exposed to a high level of radiation and is therefore recessed by 1.2 m compared to the beginning of the LAr Electromagnetic end cap.

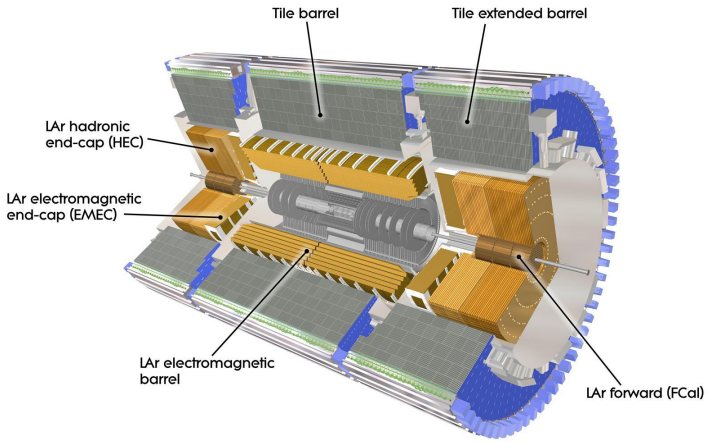

Figure 4.6: The complete calorimeter system of the ATLAS Detector. The grey area in the centre is the Inner Detector. Further out the LAr Calorimeter followed by the Tile Calorimeter are shown [38].

To measure hadronic particles the Tile Calorimeter builds the next subdetector layer. It uses steel plates as absorber. Due to its structure it is also called "girder steel" as referenced in Fig 4.5. As active material scintillating tiles placed in between the steel structure are used. Optical fibres transmit the light to photomultiplier tubes at the end of the calorimeter structure. The Tile Calorimeter is arranged in a 5.6 m long central barrel structure with an inner and outer radius of respectively 2.3 m and 4.2 m. In addition, there are two 2.9 m long extended barrels. The gap between the central and the extended barrel is used to lead the cabling of the ID and LAr Calorimeter out of the detector. The coverage of the central barrel is $|\eta| < 1.0$ and for the extended barrels $0.8 < |\eta| < 1.7$ [51].

The Muon Detector

The outermost layer of the ATLAS Detector is the Muon Detector. At this point all particles except for muons and neutrinos already lost their energy within the previous detector layers. The Muon Detector consists of several subdetectors which use the detection principle of gas ionisation by charged particles. As a result, only muons are measured here. The subdetectors are especially built to provide a precise spatial resolution for track reconstruction or a precise time resolution for the trigger system.

The barrel region of the Muon Detector is built-up of three layers of Monitored Drift Tubes (MDTs) which are placed inside a toroidal magnetic field, see Figure 4.3 and Figure 4.7. The MDTs consist of drift tubes filled with a gas mixture mainly composed of argon. As anode a gold-plated tungsten wire is used. Three layers of MDTs are also placed inside the end cap. Thus they cover the main part of the Muon Detector with a pseudorapidity of $|\eta| < 2.7$ and are mainly used for track reconstruction [52].

The MDTs are enclosed by Resistive-Plate Chambers (RPCs) which are used as a trigger unit. An RPC is made up of two parallel-plate electrodes which enclose a volume filled with tetrafluoroethane gas. To detect a signal metal strips with a width of 30 and 40 mm are placed orthogonal to each other on each plate [53]. The pseudorapidity coverage is $|\eta| < 1$.

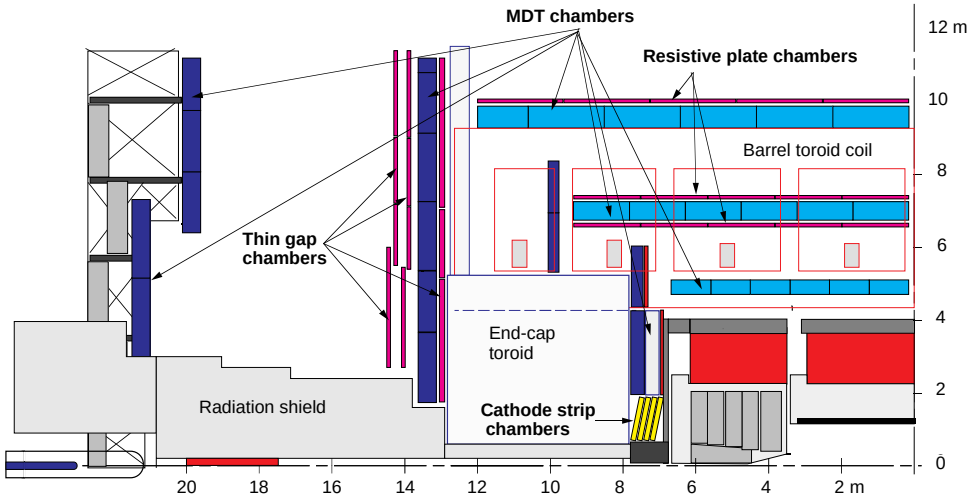

Figure 4.7: A side view of one quadrant of the Muon Detector. The four subdetectors MDT, RPC, CSC and TGC can be seen as well as the area where the toroid coil is placed. The horizontal axis refers to the z-axis and the vertical axis to the y-axis of the ATLAS coordinate system, respectively [52].

The end cap layers consist of MDTs and Thin Gap Chambers (TGC). The latter is made up of two parallel graphite cathodes which enclose a gas volume of carbon dioxide and n-pentane (C_5H_{12}). Multiple gold-plated tungsten wires between the two cathodes act as anodes. TGCs are used as triggering system similar to the RPCs and cover a region of $1 < |\eta| < 2.4$.

Close to the beam pipe the MDTs are replaced by Cathode Strip Chambers (CSC) to deal with the high radiation dose. The sensitive gas mixture contains argon and carbon dioxide. Anode wires of gold-plated tungsten and lithographically segmented cathode strips are used to measure the induced charge. The pseudorapidity range of the CSCs is $2 < |\eta| < 2.7$.

The magnet system of the muon spectrometer consists of three air-core superconducting toroids producing a magnetic field in the region $0 < |\eta| < 2.7$. The Barrel Toroid has a

length of 25 m and an inner and outer radius of 9.4 and 20.1 m, respectively. Its magnetic field peaks at 3.9 T. The two End Cap Toroids have a length of 5 m and an inner and outer radius of 1.65 and 10.7 m, respectively. Each of them has a magnetic field peak at 4.1 T. The complete magnet can be seen in Figure 4.3 and is also indicated in Figure 4.7 [54].

4.2.1 The ATLAS trigger system

The LHC bunch crossing frequency is 40 MHz. Together with up to 30 possible proton-proton interactions per bunch crossing the event rate is about 1 GHz. To store the collision data on disk this event rate has to be reduced to a rate of 200 Hz. This can be achieved by a trigger system with three trigger levels.

The first-level trigger system uses information from the calorimeters and the Muon Detector to mark an event as special. Such a special event could for example be a higgs particle decaying into two Z-bosons: $H \rightarrow ZZ \rightarrow 2e + 2\mu$. In this case the final decay products are two electrons and two muons. Thus two particle showers inside the electromagnetic calorimeter and two tracks inside the Muon Detector are detected. The first level trigger has a decision time of 2.5 µs to reject or accept such an event and therefore reduces the event rate from 40 MHz to 75 kHz.

If an event is accepted a so called LV1 Accept signal is sent to all ATLAS subdetectors and the read out data is stored inside the buffers of the Read Out Subsystem (ROS). A more detailed description of the ROS can be read in the Data Acquisition hardware part of Section 5.5.

The second level trigger uses the data stored at the ROS. To decide if an event is rejected or accepted the second-level trigger uses limited information of so called regions of interest of all subdetectors. If an event is accepted it is further processed by the Event Builder which combines the fragments of the ROS to one event and sends it to the Event Filter. The event rate at this stage is 2 kHz.

Finally, an Event Filter reduces the data to a rate of 200 Hz so that it can be stored on disk. It uses the full detector information beyond the region of interests mentioned in context with the second-level trigger.

5 The current ATLAS Pixel Detector

The Pixel Detector is the innermost layer of the ATLAS Detector and is shown in Figure 5.1. It consists of 1,744 Pixel Modules arranged in three barrel layers at radii of 5.05 cm, 8.85 cm and 12.25 cm and three end cap disks at z = 49.5 cm, 58 cm and 65 cm on each side. It covers a pseudorapidity region of $|\eta| < 2.5$ [55].

Each Pixel Module is a hybrid assembly made up of a particle detecting sensor area and an electronic readout area and is further described in Chapter 5.1. If a charged particle traverses the Pixel Detector a three dimensional hit information is recorded by measuring the z-position along the beam axis and the rϕ-position[1].

Due to its close proximity to the interaction point, especially the innermost layer is very important in vertex reconstruction for b-quarks, see Section 3.2 and below. This decay vertex is important to be measured as precisely as possible as it is used for b-tagging and is thus called "Layer 0" or "B-Layer". The central barrel layer is called "Layer 1" followed by "Layer 2" as the outermost layer.

To receive the hit information of each single pixel, roughly 80 million channels are handled by the ATLAS Pixel readout chain as explained in Chapter 5.2. A special role in data distribution and data handling is taken by the Read Out Driver (ROD) which is explained in more detail in Chapter 5.3. For communication with the front-end chip of the module the Digital Signal Processor (DSP) placed on the ROD is important. A general description of the DSP and its tasks is given in Chapter 5.4.

To integrate the Pixel Detector into the ATLAS Detector software environment the Pixel Detector specific software PixelDAQ is connected to the ATLAS Trigger and Data Acquisition (TDAQ) software. Using this software framework the whole Pixel Detector can be controlled and configured. More details can be found in Chapter 5.5.

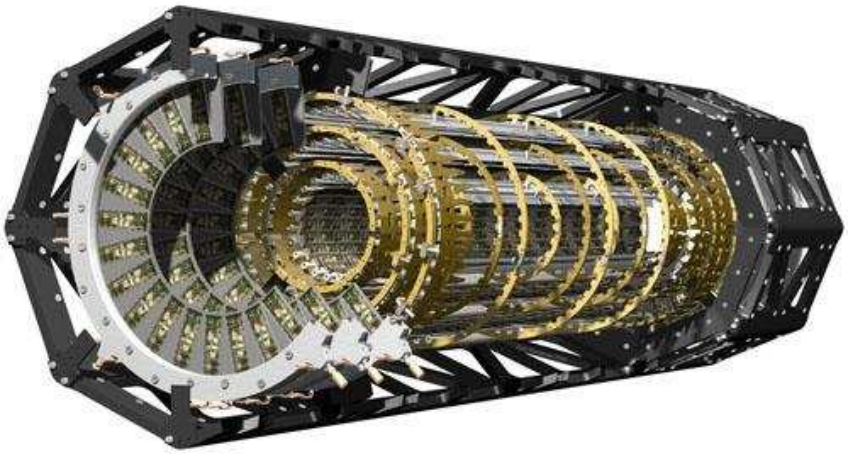

Figure 5.1: Schematic view of the ATLAS Pixel Detector [56].

[1] For an explanation of the ATLAS coordinate system see Chapter 4.2.

B-tagging

Quark transitions due to the electroweak interaction are described by the Cabibbo-Kobayashi-Maskawa-mechanism (CKM-mechanism). The probability of the transformation between the different quarks is described by the CKM-matrix [6, 57]:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} = \begin{pmatrix} 0.97 & 0.23 & 4.15 \times 10^{-3} \\ 0.23 & 1.01 & 40.9 \times 10^{-3} \\ 8.4 \times 10^{-3} & 42.9 \times 10^{-3} & 0.89 \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix}. \quad (5.1)$$

The probability of one quark decaying into another one is proportional to $|V_{ij}|^2$. The diagonal terms of the matrix are $V_{ii} \approx 1$. Thus the transition between quarks of the same generation is higher than between quarks of different generations.

The b-quark is the second heaviest quark with a mass of 4.91 GeV [58]. Its decay into the lighter u- or c-quarks is suppressed by the CKM-mechanism. As the t-quark is approximately 35 times heavier than the b-quark this transition is suppressed as well. Hence it follows, that the lifetime of mesons containing at least one b-quark is in the range of ps [59]. This leads to a distance of flight of up to ~ 7 mm from the collision point and can be measured by particle detectors which are located close to the interaction point [60].

The measurement of the decay vertex of the b-quark is called b-tagging and is important for e.g. jet-reconstruction or general b-physics. This requires precise tracking detectors which are located as close as possible to the interaction point.

5.1 The ATLAS Pixel Module

Each module consists of a particle detecting sensor and an electronical readout part, the so called front end (FE) chip, as can be seen in Figure 5.2. The sensor has a total size of 63 mm $\times$ 18.6 mm, a thickness of 250 µm and is subdivided into several pixels. It is further described in Chapter 5.1.1. The electronical readout part is made up of 16 Front End-I3 (FE-I3) chips, one of each keeping 46,080 electronical readout circuits. With this setup almost each pixel cell of the sensor material is connected to its own electronical cell via a lead-tin bump bond connection and the analogue signal of the silicon material can immediately be digitised on the module, see Figure 5.3. The Front End chip is described in more detail in Chapter 5.1.2.

The signals of all 16 FE-I3 chips are fed into the Module Control Chip (MCC) which transmits them to the off-detector side. To connect FE chips and MCC a flexible Kapton foil with wire-bonds, a so called "Flex-Hybrid" is used. The Kapton pigtail directs power and signal lines from the Type-0 connector to the Flex-Hybrid [61]. There are power supplies for the on-chip analogue and digital electronics which both are filtered by ceramic capacitors at the entry points of the external power lines. Local Decoupling Capacitors (LDC) are used for each supply between every FE pair.
To connect the HV[2]-line from the top of the Flex-Hybrid to the backside of the sensor a HV-Hole via with wirebond is used. A HV-Guardring surrounds the HV area to isolate this voltage lines from the remaining part of the Flex. Finally, an NTC[3] ceramic thermistor measures the temperature of the module.

[2] High Voltage
[3] Negative Temperature Coefficient

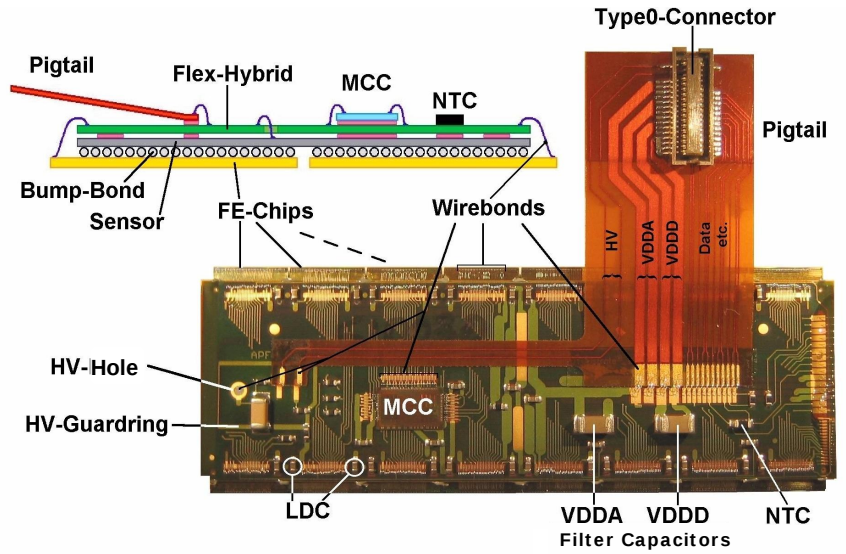

Figure 5.2: The ATLAS Pixel Module.

5.1.1 The sensor material

The Pixel sensor is an n-in-n type sensor as described in Chapter 3.3. It is made up of 250 µm thick diffusion-oxygenated float-zone silicon to improve the radiation hardness [62]. The sensor

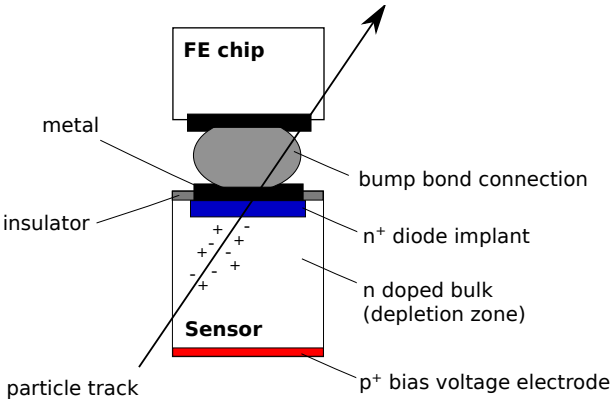

Figure 5.3: A schematic of the sensor pixel cell connected to the FE chip with a bump bond connection. If a reverse bias voltage is applied the sensor is completely depleted.

is subdivided into 47,232 pixels. 41,984 pixels have a size of 50 µm × 400 µm, whereas 5,248 pixels are a bit longer with a size of 50 µm × 600 µm [63]. This is to cover the gap between the long sides of the FE-I3 chips. To have sensitive material between the short sides of the FE chips pixel cells are placed here, too. As there is no underlying FE chip such a pixel is connected to a bump bond connection of another pixel and is therefore called “ganged pixel”. If two pixel share the same bump bond connection and thus the digital readout part, an incoming charge cannot clearly be assigned to one or the other pixel sensor. To avoid this every other of the last eight bump bonds of the last row is connected to one of the ganged pixels. Thus, the origin of a charge occurring from a shared bump bond can be determined by the charge sharing effect measured in the neighbouring pixels. The pixels lying between the ganged pixels and not sharing their bump

bonds are called "inter-ganged pixels". With this pixel segmentation and a pitch of 50 µm a space-point resolution of about 12 µm in rϕ and about 115 µm in z is achieved.
As the edges of the sensor are damaged by the cutting process, this area is prone for short-circuits which increase the leakage current. Thus the applied sensor field has to be decreased in this area. This is done with 17 "guard rings". These rings with decreasing voltage from the inner to the outer part of the sensor edge provide a slow field drop and close off the edges from the remaining part of the sensor. Therefore, the active area of each sensor is 1.8×6.2 cm^2.

5.1.2 The FE-I3 chip

The FE-I3 readout chip has a size of 10.8 mm $\times$ 7.6 mm and is divided into 2,880 pixel cells arranged in 18 columns and 160 rows as can be seen in Figure 5.4. Each pixel cell is directly connected to its own sensor cell via a bump-bond connection and consists of an analogue and a digital part.

The analogue part

An incoming signal reaches the analogue part and charges a capacitor C_{FB}. It is amplified in the first stage amplifier Amp I, see Figure 5.5. A defined feedback current IF discharges this capacitor. This current has to be high enough, such that the capacitor is free of charge for the next incoming signal. At the same time it has to be low enough to not significantly decrease the charge before it is fully loaded onto the capacitor which would cause a loss of the signal height. As there is an optimal working point for the individual analogue cell this value has to be tuned for each single pixel. The variable to be tuned is the Feedback DAC[4] value stored in the Pixel Register which is further described in the configuration section of this chapter. The charging and discharging of the capacitor leads to a triangular signal shape in charge versus time which is shown in Figure 5.6. The rising slope depends on the charge and the falling slope is defined by the feedback current.

After a second amplification in Amp II the analogue signal is transformed into a digital signal by a discriminator. The threshold of this discriminator can be adjusted globally for all discriminators on the chip via a 5-bit DAC value called GDAC and locally for each single pixel cell via a 7-bit value called TDAC.

Expecting a signal of 24,000 e induced by a m.i.p. a nominal value for the discriminator threshold is about 4,000 e. The last threshold is determined by the fact that the induced charge by a particle crossing the sensor plane in an 90° angle can be shared between four pixels. This leads to a minimum charge of 6,000 e which has to be detectable by a single pixel [64]. The noise of a pixel cell is about 200 e [63].

To tune the discriminator threshold of the sensor or for detector scans it is possible to inject a test charge inside the analogue part. This is done by two capacitors with 7 fF and 40 fF. The amplitude of this test charge can be set by a DAC value which is called VCAL.

If an incoming charge exceeds the discriminator threshold a logical one is transmitted to the digital part of the readout cell.

[4] Digital to Analog Converter

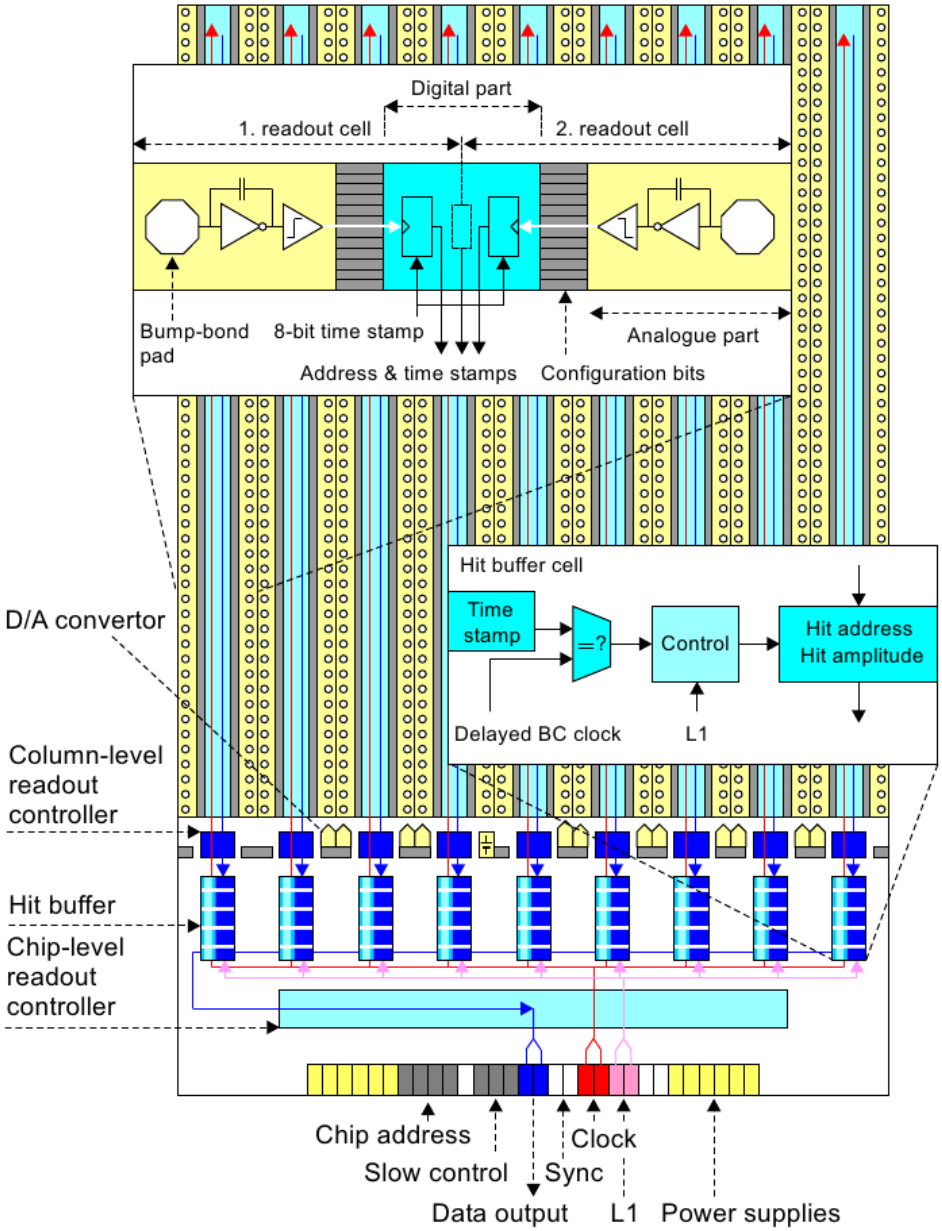

Figure 5.4: Functional representation of the ATLAS Pixel readout chip [65].

The digital part

The time the input signal exceeds the discriminator threshold is called Time Over Threshold (ToT). It is proportional to the amount of charge the incident particle deposites inside the silicon sensor. Thus, by assigning a time stamp to the leading and to the falling edge of the discriminator output the ToT can be measured in units of 25 ns. This information together with the pixel address is shifted out towards the column-level readout controller which transmits the hit information of a complete double-column unit to the hit buffer [64, 66]. Both, ToT value and the address of a pixel cell detecting a particle hit, are stored here. As 8 bits are foreseen for the ToT it can have a maximum value of 255 times the bunch crossing rate of 25 ns.

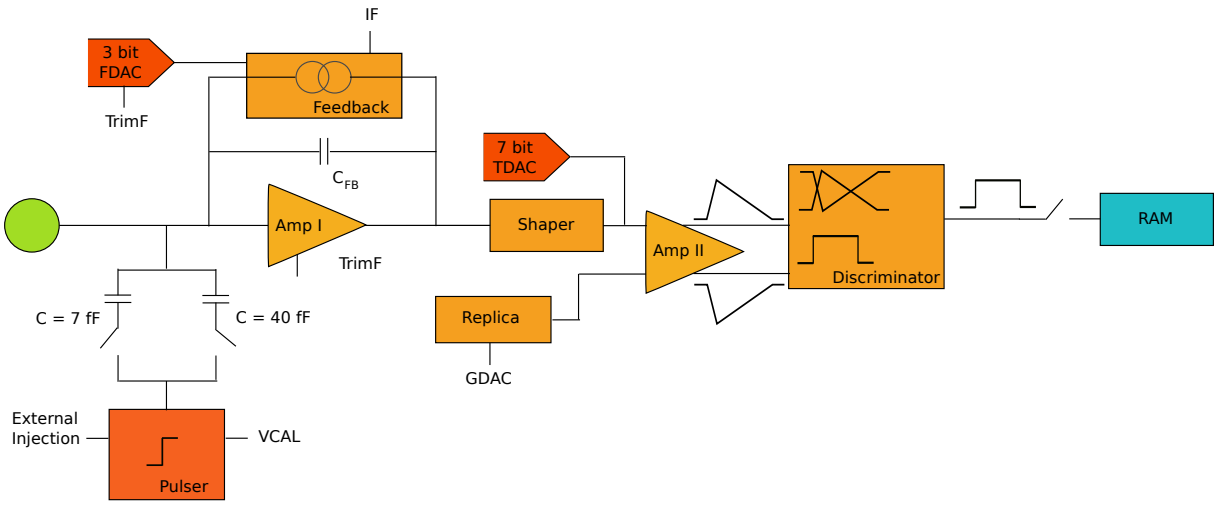

Figure 5.5: The analogue readout cell of the FE-I3 chip.

As soon as a Level 1 trigger signal occurs the ToT and its address information are packed into a data frame and sent out via the chip-level readout controller through the data output lines of the FE chips. In addition, lines for Slow Commands, see Chapter 5.3, the chip address, the reset signal "Sync", power supply and the clock are foreseen, see Figure 5.4.

Finally, the data is transmitted to a Module Control Chip (MCC). This chip combines the data of the 16 FE chips of one module and sends the data to the off-detector electronics.

Configuration and timing

To be synchronous with the LHC bunch crossing frequency the FE chip receives the 40 MHz clock from the off-detector part [66]. Control is done via three registers: the Command Register, the Global Register and the Pixel Register which are clocked with the slower 5 MHz Command Clock.

Incoming commands are stored and processed inside the Command Register. It reads the chip address and detects if configuration data comes together with the received command.

The Global Register is 231 bit long and stores configuration parameters valid for the whole

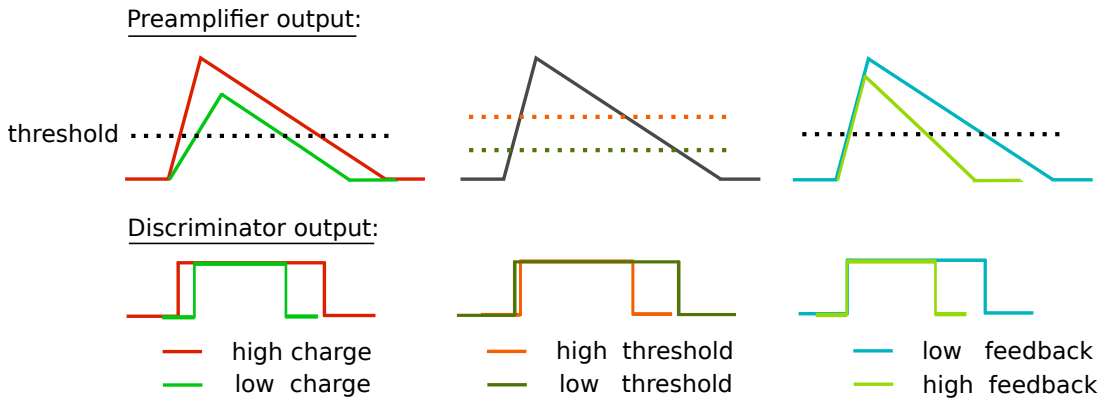

Figure 5.6: Output of the first preamplifier and discriminator output of the FE-I3 digital part. The dependence on the injected charge, the threshold and the feedback current are shown.

chip. As the chip is exposed to a high radiation dose, single event upsets (SEUs) can occur which lead to undesired bit flips of the configuration values. Thus, to have a preferably SEU-tolerant environment each bit is stored in latches using a shadow register. The shadow register is used to shift the configuration variables bit by bit into the FE. A received strobe signal will then write the values at once into the latches. Through a majority decision a single bit flip in one of the three latches can be detected and the value of the two other latches is taken. Another way of detecting an SEU can be achieved by computing the parity of the 231 Global Register bits. With this method the corrupted value cannot be restored as it is unknown which bit has flipped. The whole configuration has then be marked as damaged.

Each pixel cell contains its own 14 bit wide Pixel Register. It is written and read by a 2,880 wide Pixel Shift Register. All pixels on one FE are divided in nine double columns (DCs). Each DC contains 320 bits which can be individually enabled or disabled. Similar to the Global Register configuration the content of the Pixel Shift Register is stored simultaneously inside the pixel latches to preferably avoid SEUs using a strobe.

Commands sent to the FE chip are divided into Trigger, Fast and Slow Commands and are all received and processed by the MCC and then further distributed to the 16 FE chips on the module [67]. Trigger and Fast Commands are only accepted if the chip is in Run Mode, meaning the chip is in data taking mode. If the chip is in Configuration Mode it is able to receive Slow Command signals. The Trigger Command just contains a LV1A trigger command. It can be sent by the ATLAS Trigger System during data taking or is generated locally by the DSP on the ROD during scans. The Fast Command is used to send timing signals like the calibration strobe, a SYNC signal or the ECR and the BCR, see Chapter 5.3 for explanation. The calibration strobe activates for example the time of the injection of test charges within the pixel cells. The SYNC signal initiates a reset on the chip. To configure the chip a Slow Command is sent which immediately sets it into configuration mode and stops data taking. All kind of chip configurations are done with such commands: writing and reading of the Global and the Pixel Register, reset the MCC or the FE or enable data taking to be able to send Fast and Trigger Commands again.

5.2 The Pixel Detector readout chain

The Pixel Detector consists of 1,744 modules, each of them providing data on 46,080 readout channels. Thus a total of 80,363,520 channels have to be handled by the ATLAS Pixel readout chain. The radii of the three layers of the Pixel Barrel decrease towards the interaction point and the hit rate per area increases. To account for that the modules closer to the interaction point have to send out the data with a higher bandwidth. The modules placed on the outermost Layer 2 send data on one link to the off-detector part using a bandwidth of 40 Mb/s. The central Layer 1 modules use one data link with a bandwidth of 80 Mb/s. The B-Layer modules send the data out using two links with each 80 Mb/s per module and thus have a total bandwidth of 160 Mb/s per module.

The data is sent off a module via the Type-0 cable. The Type-0 cable is connected to an Optoboard, see Figure 5.7. It consists of an 8-way VCSEL[5]-array transforming the electrical data signal into an optical signal. Thus, the distance of 80 m between detector and counting room can be covered fast and without significant signal loss via optical fibres. For transferring signals in the opposite direction the optical signal is converted into an electrical one using an

[5]Vertical Cavity Surface Emitting Laser

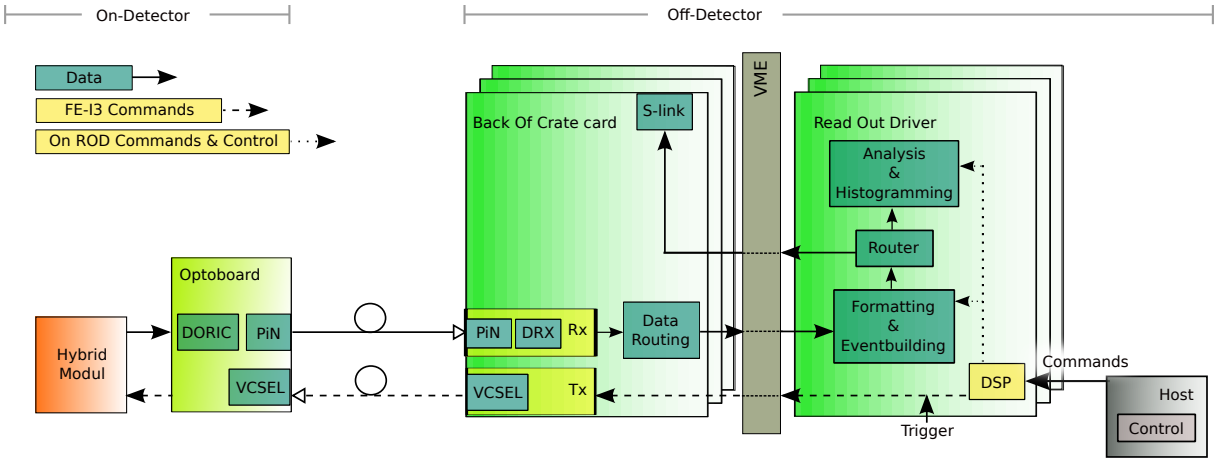

Figure 5.7: The ATLAS Pixel readout chain.

8-way PiN[6]-diode-array. As the signal is Bi-Phase Mark (BPM) encoded, containing clock and signal in one line, a Digital Opto-Receiver IC (DORIC) decodes the encoded signal. One DORIC receives four channels. Thus one Optoboard handles the data of up to eight modules coming from Layer 2, Layer 1 or the Disks. To deal with B-Layer modules a special type of Optoboard is equipped with two VCSEL-arrays to provide the transmission of double the bandwidth.

The data receiving part on the off-detector side is a printed circuit board called Back Of Crate card (BOC) converting the optical into electrical signals. Similar to the Optoboard Rx plug-ins, each receiving eight data channels, they contain PiN diodes and serve as optical-electrical interface. A Data Receiver IC (DRX) is used to amplify the signal and converts it into an LVDS[7] signal. All electrical signals and clocks are transmitted as LVDS reducing the noise sensitivity in high data transmission using a lower logic level than the standard 3.3 V or 5 V signals. To send signals from the off- to on-detector part an 8-way VCSEL Tx plug-in is used [68].

Another task of the BOC is the multiplexing of the data signals. As the Read Out Driver (ROD) is just able to process 40 Mb/s streams the BOC multiplexes an incoming 80 Mb/s stream into two 40 Mb/s streams.

Depending on the run mode of the Pixel Detector the ROD either analyses the incoming data (Configuration Mode) or sends it to the BOC's S-Link (Run Mode) after having formatted it. In the first case commands have to be sent to the FE for configuration or executing scan loops. This is done by the Digital Signal Processor, which is further discussed in Chapter 5.4 and 7. More details about the ROD can be found in Chapter 5.3.

To send the data to the ATLAS Read Out Buffer an S-Link is used [69]. It is placed on a HOLA[8] card mounted on the BOC and transmits 32 bits in parallel. The functionality of the general ATLAS Data Acquisition as a key element is further explained in Chapter 5.5.

One ROD-BOC pair serving for Layer 2 modules can read out the data of 26 modules. Likewise it serves for 12 or 13 Layer 1 and Disk modules as well as six B-Layer modules. In total 132 BOC-ROD pairs are needed to read out the complete ATLAS Pixel Detector. Both cards are inside a standard 9U VME crate where a maximum of 16 pairs can be placed. Thus, nine such crates are used to keep all readout cards needed for the Pixel Detector.

[6] Positive-intrinsic-Negative
[7] Low Voltage Differential Signal
[8] High Speed Optical Link for ATLAS

To be able to control the ROD-BOC pairs a Single Board Computer (SBC) is placed inside the VME. This and the corresponding software framework is further explained in Chapter 5.5.

Timing, trigger and control (TTC) signals are received by one TTC Interface Module (TIM) placed in each VME crate. The TTC signal is transmitted to the ROD and then further to the modules. The TTC signal includes trigger commands like the Level 1 Accept trigger, test and calibration triggers. A LV1A is generated by using the information of the calorimeters and the muon chambers and is the trigger signal sent during data taking. Besides the trigger signal, the TTC signal also includes the LHC bunch crossing clock and synchronisation signals: the Bunch Counter Reset (BCR) and the Event Counter Reset (ECR) [70].

5.3 The Read Out Driver

The Read Out Driver (ROD) is the main board within the ATLAS Pixel readout chain. It is able to reformat and monitor the incoming data if the Pixel Detector is in data taking mode. In configuration mode the ROD receives commands from the host and creates FE commands on its Digital Signal Processor (DSP). This is used to configure the chip and control scans. The main ROD peripherals are several Field Programmable Gate Arrays (FPGAs) and DSPs. The primary function of the FPGAs are transmitting and reformatting the detector data towards the S-Link and having an overall control of the tasks being executed on the ROD. Regarding the DSPs they have two functionalities executed by one Master and four Slave DSPs. The Master DSP processes commands, scan loops, and controls the Slave DSPs which are responsible to process and analyse the incoming data, see Chapter 5.4.

The ROD Controller FPGA (RCF) controls the overall tasks on the ROD and receives the TTC signal sent by the TIM, see Figure 5.8. This signal contains the L1ID[9] and a BCID[10] information. Every time such a signal arrives an internal L1ID counter is incremented by one and at the same time a BCID counter is stored into a register such that it can be used in the event header as the event BCID. The BCID counter is incremented by one at each LHC-clock cycle and can be reset to zero by a BCR [71]. The L1ID counter can be reset by sending an ECR. In total there are 48 command links from the ROD to the BOC but only 26 are used. Each single command link connects to one module. A mask determines which module links are active. The trigger or command signal are then sent to active modules only.

The ROD Formatter FPGAs receive the data coming from the modules on one, two or four data links. This is due to the fact that data can be sent out in 40 Mb/s, 80 Mb/s and 2×80 Mb/s, as explained in Chapter 5.2. But the ROD is only capable of receiving data in 40 Mb/s streams. Each of the eight Formatters thus receives data on 12 serial input links. An event header has to be detected to decode the following data and trailer of the data bit package. Module errors, stored as an error flag inside the bit stream, can be detected and a direct connection with the ROD Controller FPGA (RCF) permits real-time monitoring of the link occupancy. The serial data is transformed into 32 bit words and stored in the internal FMT FIFO[11]. For debugging purposes the incoming data can be directly stored inside the FMT Input FIFO and read out by the Master DSP for example.

The Event Fragment Builder (EFB) receives the data coming from the FMTs. It collects the data of the modules of one event and forms an event data fragment out of it. This is stored

[9] Level 1 Identification
[10] Bunch Crossing Identification
[11] First In First Out Buffer

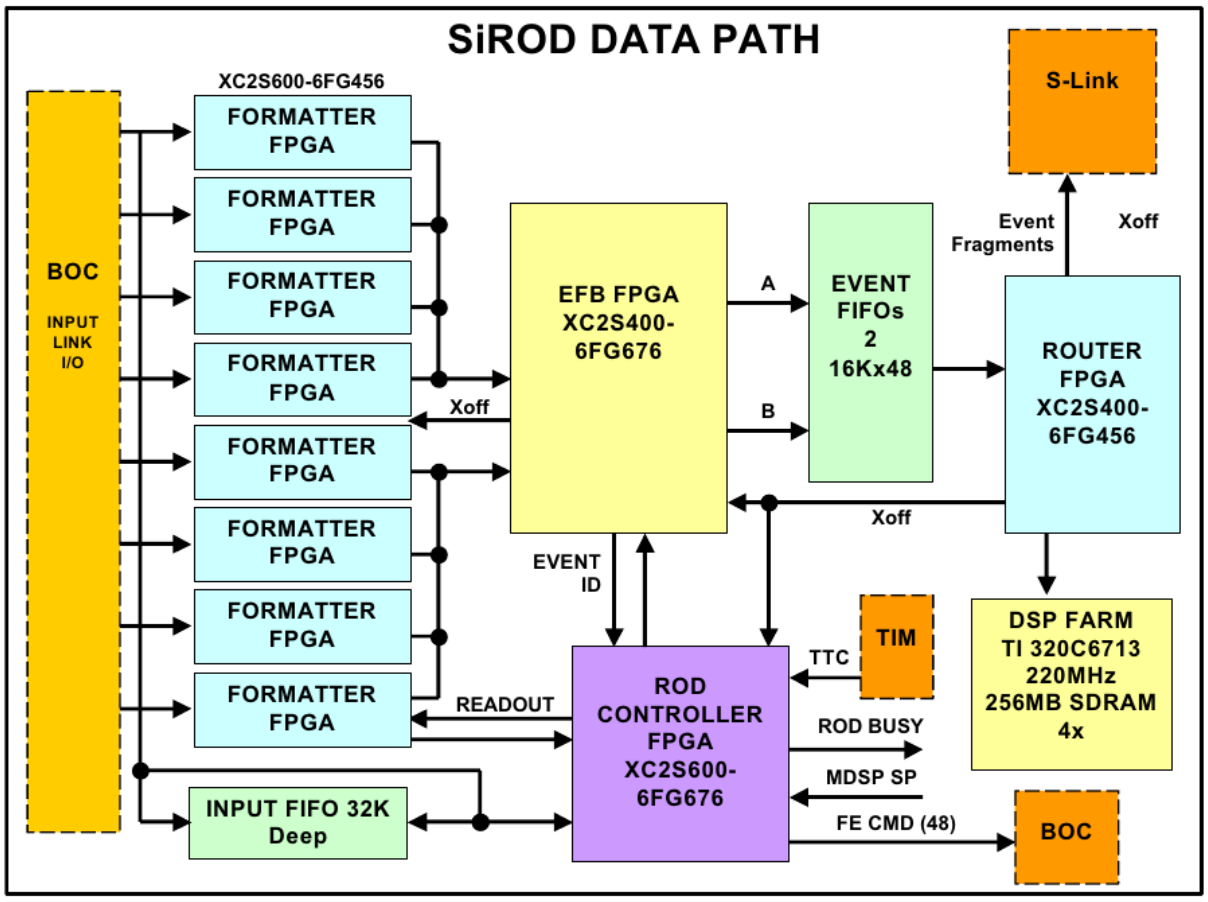

Figure 5.8: The data and control path of the Read Out Driver [71].

inside a FIFO which can keep up to 16,000 32 bit words. Furthermore, the EFB checks L1ID and BCID module information against the ATLAS L1ID and BCID. Then the bit stream is checked for errors. These errors are counted and stored in the internal EFB FIFO. In addition, the number of 32 bit words is counted and written to the Event FIFO. The complete event fragment can be sent to the Router FPGA. The Router decides if the data is sent out to the S-Link or whether the data is sent to the four Slave DSPs (SDSPs) depending on the ROD being in data taking or calibration mode. In the latter case direct memory access (DMA) is used to store the data into the SDRAM[12] of the SDSP. As the data transfer from Router to SDRAM is twice as fast as the data transfer from the EFB FIFO to the Router the SDSP has time enough to shift the data into its internal memory before the next data fragment of 256-words arrives.

The four SDSPs are used for monitoring, histogramming and analysing the data [72]. They are directly connected with the Master DSP (MDSP) via the Host Port Interface (HPI), which is explained in more detail in Chapter 5.4. Thus the MDSP can access the complete memory range and all registers of the SDSPs for control and status requests. To monitor the event data during data taking the SDSPs display for example timeout, link header bit, L1ID or BCID errors.
The main task of the SDSPs is histogramming and analysis of the data taken during scan procedures. There are two different scan types: “normal” and “special” scans. In the former case data words are always sent back from the detector. Special scans are all other scans.

[12]Synchronous Dynamic Random Access Memory

Normal scans are either based on measuring the number of hits above threshold, occupancy scans, or on measuring the mean and root-mean-square values of the ToT per pixel after several charge injection steps [72]. An example is the digital scan in which a pulse is injected after the discriminator of every pixel cell. As the FE-I3 chip has not enough memory to store the data of all pixels at the same time, the scan is divided into several mask steps. Normally 32 mask steps are used such that 90 pixels are tested at the same time. A successful scan result would show a FE chip map in a histogram with all pixels having fired by a defined number of injections.

As an example of a special scan the Register Test can be mentioned. Here, a known bit pattern is written into the chip's registers and then read back. The sent and received bit patterns are compared and if equal the scan is declared as successful.

Finally, the Program Reset Manager (PRM) FPGA connects the peripherals on the ROD with the VME interface. Thereby, all FPGAs and the MDSP can be programmed and a global reset on the ROD can be executed.

Back-pressure occurs if the data cannot be handled fast enough by the S-Link or the SDSPs. This information is transmitted to the RCF and the data transmission from the EFB towards the Router FPGA stops immediately. Meanwhile the incoming data is stored in the Event FIFOs of the EFB. If even the Event FIFOs are full the ROD is set into a ROD Busy state by the RCF. In that case the ROD is not capable of processing module data anymore and sends a ROD Busy signal to the TIM. Another situation for the ROD being in ROD Busy is during device configuration and reset.

5.4 The Digital Signal Processor on the ROD

A Digital Signal Processor (DSP) is a type of microprocessor. It processes data very quickly as it contains more complex algorithms which are needed for fast digital signal handling. On the ROD two types of DSPs are used. The Master DSP (MDSP) is a TMS320C6201 fixed-point DSP running at 200 MHz with two 64 kB blocks of internal memory [72]. A DSP-special external memory interface (EMIF), a bus protocol for communication, connects it to its external devices. In the case of the MDSP these devices are an external SDRAM and Flash memory as well as the Rod Register Interface (RRIF). Through the EMIF the MDSP has read and write access to all registers on the ROD and on the BOC.

Another DSP specific property is the Host Port Interface (HPI), a memory interface through which other devices can access the DSP's memory. It is used to program the MDSP via the PRM FPGA, the interface to the VME crate. The PRM can thus load an appropriate MDSP firmware onto its Flash memory and as a consequence the MDSP can be programmed via the VME interface. At the same time the PRM sets the appropriate MDSP bootmode such that the MDSP can directly load the firmware and boot from it. Besides the firmware, all commands received via VME interface are transmitted through the HPI as well. To send out the chip commands as a serial data stream the Multichannel Buffered Serial Ports (McBSP) are used. Moreover, a timing interface for clock signals, an interrupt interface for external interrupts and a general purpose input/output interface are used for MDSP communication. The latter can be used to control the LEDs on the ROD's Front Panel. To store data in memory the DSP uses a 32-bit word alignment. Hence it follows that there are always unused bits between two variables having a size which differs from a multiple of 32 bit.

All four Slave DSPs are TMS320C6713 floating-point DSPs running at 220 MHz and containing 256 kB of internal memory. They have an EMIF and an HPI as well. Through the EMIF one SDSP connects to the Router to receive data for monitoring during data taking and for analysis

and histogramming during calibration. Furthermore, the SDSP connects to its two external 128 MB SDRAM sections to store event histograms. The HPI is connected to the MDSP which can load the firmware of the SDSPs and boot it.

5.4.1 The tasks of the Master DSP

The Master DSP receives commands from the host via the VME interface [71]. These can be "Primitives" or "Tasks". A Primitive is a command sent between host and MDSP or between SDSP and MDSP. It can contain data and is executed once [72]. The module configuration parameters for example can be read from the database on the local host computer and sent to the MDSP together with the appropriate Primitive. The MDSP then stores the configuration data into its memory, creates a serial bit stream and sends this bit stream via its serial ports to the modules.

A Task is an execution which is processed until it is finished or which runs until it is stopped by an appropriate Primitive. An example is a Scan Task which controls and executes a Digital Scan, explained in Chapter 5.3. In this case the scan parameter is just the mask step. While executing the mask steps one after another the host waits for its completion. Simultaneously, the host gets informed about the scan status from the MDSP. The Scan Task itself uses Primitives, for example it tells the SDSP to analyse scan data or requests scan results from it. To control tasks on the four SDSPs from the host all commands have to be sent via the MDSP using the HPIs. The MDSP can send Primitives to the SDSP as well to initiate a certain Task.

With the MDSP's EMIF it has access to all registers on the ROD. Thus it can read status registers and pass this information to the host or it can prepare the ROD for a coming task with writing into certain register addresses. This is important for the overall ROD configuration during calibration.

To react on commands sent by the host the MDSP runs an endless polling loop after being booted. Within this loop it waits for Primitives and Tasks and can immediately recognises them if being sent. For debugging purposes the MDSP has a text buffer which is frequently read out by the host.

5.5 Data Acquisition

The ATLAS Pixel data acquisition can be separated into a software and a hardware part. The hardware part is made up of a ROD-BOC pair, an S-Link and the Read Out System (ROS), explained later in this chapter.

The software part consists of a common ATLAS Trigger and Data Acquisition (TDAQ) software and a Pixel Detector specific DAQ software called PixelDAQ and is further described in the following.

The TDAQ and PixelDAQ software framework

The PixelDAQ software is embedded inside the ATLAS TDAQ software, which combines all ATLAS subdetectors [73]. With this software the complete detector can be prepared for a proton-proton collision run. This is done by starting a so called "partition" which interfaces the individual ATLAS subdetectors with the TDAQ environment. Among others, TDAQ contains the configuration and condition database, an expert system which performs the analysis of errors, an information service which allows software applications to exchange user-defined information

and a process manager which performs the basic job control and creates, controls and monitors the status of all processes in the TDAQ system.

Using the PixelDAQ and TDAQ framework gives access to the Configuration and Calibration Data Base such that module configuration parameters can be read and written from and to the database. PixelDAQ interfaces between the common TDAQ software and the Pixel Detector hardware and implements all functions needed to configure and control the detector. An overview of the functional blocks can be seen in Figure 5.9.

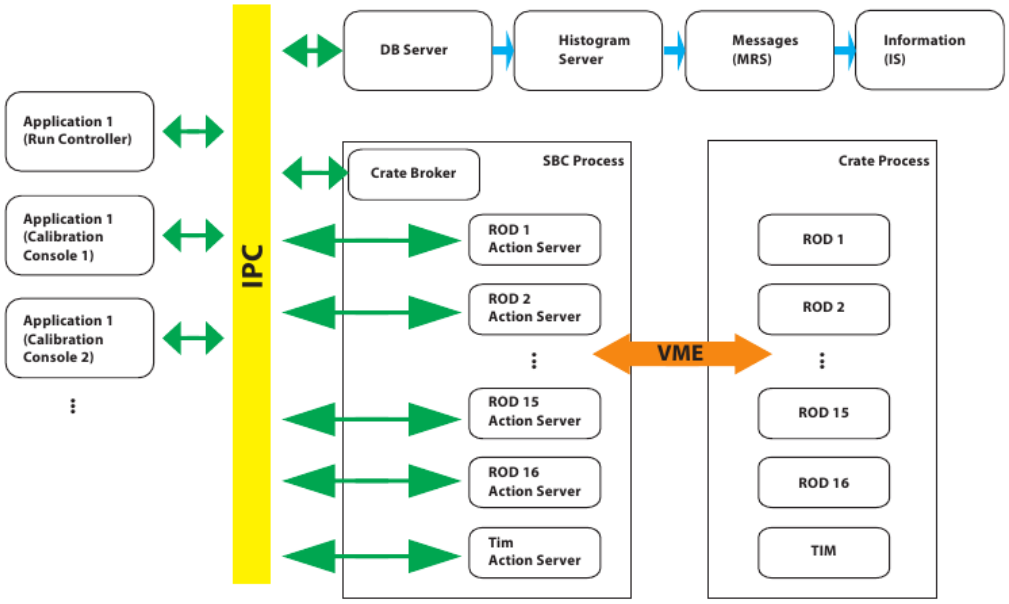

Figure 5.9: The functional blocks of the TDAQ and PixelDAQ data acquisition software [74].

The described interface structure is hidden behind different applications to send commands or analyse calibration data and thus provides a user friendly environment having a complex software framework in the background. The different applications can be started and controlled via a user friendly GUI[13].

When starting the TDAQ GUI a detector partition can be booted which starts the *Run Controller*. Here, all functional blocks are connected with each other. These are connections to several servers like the Database (DB) server, Histogram Server, Message Server (MRS) and the Information Server (IS). As indicated by their names, these are the interfaces to the configuration database, store and load histograms and handle message and information requests. As the overall communication between the different blocks is very complex several threads have to be processed at the same time which is done vie inter process communication (IPC).

After the TDAQ partition is started and all interconnections have been done the application *Calibration Console* can be used to configure modules, run scans and follow the scan status during execution and finally to see the results of scans. All these tasks are called “Actions” and are handled by so called *Action Servers*. While the *Run Controller* and *Calibration Console* are executed on the user’s host PC the *Action Servers* run on the Single Board Computer (SBC) which is the interface between the host and the VME crate. The SBC in turn connects to the actual hardware components located in different slots inside the VME crate, for example the

[13]Graphical User Interface

ROD. The coordination of the commands and request sent via the VME interface are handled by the *Crate Broker*.

When configuring a module *Calibration Console* connects to the DB Server via IPC and loads the specific configuration data from the database. Similarly, *Calibration Console* connects to the Histogram Server to store histograms after a scan has been executed. *Calibration Console* also connects to the ROD MDSP text buffers via the PixelDAQ framework. Although they have a limited storage space, the frequent readout is essential for debugging purposes while the ROD is processing.

While TDAQ provides the general communication between the servers, individual detector components are implemented into the TDAQ framework with PixelDAQ. In Figure 5.9 this is indicated by the *Action Servers* which control the commands sent to the detector component, for example the ROD.

To implement the ATLAS Pixel readout system into the DAQ software a virtual interface to the hardware is used which is represented by C++ classes. The ROD-BOC specific *ROD-PixController* class inherits from this class and contains all basic functions needed to control the detector. To implement hardware details of the ROD-BOC system, for example memory mapping, a *RodModule* class and a *VMEInterface* package translate the functions of *ROD-PixController* and write the passed arguments and configuration parameters directly into the memory of the ROD.

Besides using the connection between host, SBC and ROD, the user can also directly connect to the SBC without an explicit application like *Calibration Console*. As the ROD register structure is known in the PixelDAQ framework, direct commands to the ROD can for example dump the content of the MDSP memory, the HPI or other registers. This interface is also used if new FPGA or DSP firmware has to be loaded onto the ROD.

Due to a flexible and complex DAQ software other readout hardware can be used within the PixelDAQ framework, as well. An example is the USBPix readout system which is used for first tests with the new FE-I4 chip. This system provides the readout for a FE-I4 Single Chip Card (SCC) and can be connected to a PC using a USB plug. Another example is the new IBL ROD-BOC chain, explained in Chapter 6.

The Detector Control System (DCS) is accessed as well by the PixelDAQ software. It permits direct control and monitoring of the voltages, currents and temperatures of each module. Last but not least an interface to the TIM is provided to manage the trigger setup.

The Data Acquisition hardware part

As explained in Section 4.2.1 an incoming LV1 Accept signal gives notice of an interesting event. The trigger signal is sent to the TIM and from there handed over to the ROD-BOC cards and the modules. The event data temporarily stored inside the FE chips is then transmitted from the modules back to the ROD-BOC chain. The data sent by the off-detector readout chain ROD-BOC is then sent optically from the S-Link to the Read Out Buffer Input Stage (ROBIN) with a bandwidth of 160 Mb/s.

The ROBIN is the main interface between 1,600 detector front end links and the higher level trigger farm and is included in the ATLAS Read Out Subsystem (ROS) PC [75]. It buffers the incoming detector data such that the second-level trigger farm decides within 10 ms if an event is interesting or if it should be rejected. The ROS PC communicates with the second-level trigger farm and manages the data delete and request commands for the ROBIN.

One ROS PC contains four ROBINs[14] and in total there are 160 such ROS PCs. Each ROBIN is connected to three ROD-BOC pairs with one optical link each. On the ROS PCs the basic handling of the Pixel Detector data is similar to the handling of the data of all other ATLAS subdetectors.

[14]Depending on the bandwidth five or three ROBINs are mounted on one ROS PC.

6 The Insertable B-Layer Upgrade

To increase the potential in high energy particle research it is foreseen to upgrade the LHC accelerator. Some examples which show the physics potential are described in Section 6.1. The upgrade comprises an increase of the luminosity of the LHC until 2022 to the so called High-Luminosity-LHC (HL-LHC) [74]. The current accelerator is designed for a luminosity of $L = 10^{34}$ cm^{-2}s^{-1} and a centre of mass energy of $\sqrt{s} = 14$ TeV. With an upgrade of the LHC a luminosity of up to $L = 5 \times 10^{35}$ cm^{-2}s^{-1} can be achieved.

This upgrade has an impact on the detection sensitivity and the data readout of the experiments. Especially the detectors which are placed close to the interaction point have to bear an environment with a higher particle rate. This is in particular true for the current innermost layer, the B-layer, of the Pixel Detector. To compensate the expected decrease in detection performance a new B-Layer, the Insertable B-Layer (IBL), is placed into the current Pixel Detector as explained in Section 6.3. Due to the requirements of the IBL, adequate sensor and readout components come along with the newly layer. Improved sensor components are explained in Section 6.4.1. A new developed front-end chip is described in Section 6.4.2. Furthermore, a readout chain and especially a new Read Out Driver for IBL are described in Section 6.5 and 6.6, respectively.

6.1 Physics at the High-Luminosity-LHC

An upgrade of the LHC accelerator with higher luminosity enlarges the research potential in high energy physics especially on physics beyond the Standard Model or so called New Physics.

The major improvement is the gain of more statistics of rare decays.
One example is the decay of a higgs boson in a mass range of $100 - 160$ GeV/c^2 into a Z-boson and a photon: $H \rightarrow Z\gamma$. The Z decays into either two electrons or two muons. This channel can be observed with $\sim 3.5\sigma$ and 600 fb^{-1} of data [76]. The rare decay $gg \rightarrow H \rightarrow \mu^+\mu^-$ produced by gg-fusion cannot be observed better than 3.5σ at the LHC. For a higgs mass between $100 - 160$ GeV/c^2 a significance of 5σ is expected at an upgraded LHC. Furthermore, the higgs decays can be measured more accurately.

The number of produced t-quarks decaying via flavour-changing neutral currents (FCNC) is limited. These decays can be $t \rightarrow q\gamma$, $t \rightarrow qZ$ or $t \rightarrow qg$ with q being a u- or c-quark. To achieve a higher number of events an upgrade of the luminosity and the provision of the current detector performance for the HL-LHC are necessary. Hence, the measurement of these decays may lead to physics beyond the Standard Model.

Another topic of New Physics which promises more discovery potential with an upgrade on the LHC is a higher mass reach for the discovery of supersymmetric sparticles in which the mass range can be extended from 2.5 TeV/c^2 to 3 TeV/c^2.
Furthermore, other topics of New Physics like extra-dimensions benefit from the upgrade.

6.2 ATLAS Detector upgrades for the High-Luminosity-LHC

To prepare the individual experiments for the luminosity upgrade three LHC shutdown phases are intended. The first shutdown is the so called "Phase 0" which is planned to take place in 2013 and 2014. During this phase the Pixel Detector will be upgraded with an additional fourth Pixel Layer: the Insertable B-Layer (IBL).

The central beam pipe, the area of the beam pipe which is enclosed by the ATLAS Detector, will be replaced by a new beam pipe with a smaller diameter. This additional space between the beam pipe and the B-Layer is used to insert the IBL into the current Pixel Detector. Hence, together with the IBL a new beam pipe will be inserted.

Similar to the current central beam pipe the new central beam pipe consists of beryllium. The outer parts of the beam pipe are made of stainless steel which causes high multiple scattering background inside the Muon Detector. Thus, these parts have to be exchanged as well. The new beam pipe is made of aluminium which reduces the background by 10-20% [77, 78].

After Phase 0, the luminosity is increased from currently $L = 6.8 \times 10^{33}$ cm^{-2}s^{-1} to $L = 1 \times 10^{34}$ cm^{-2}s^{-1} and an integrated luminosity of 100 fb^{-1} is planned to be reached. The bunch spacing is decreased from 50 ns to 25 ns. Furthermore, the current centre of mass energy is raised from currently $\sqrt{s} = 8$ TeV to $\sqrt{s} = 14$ TeV.

The next upgrade phase is the "Phase 1" upgrade which is carried out during the long shutdown phase in 2018. The ATLAS upgrade in this phase ensures a good operation performance of the detector at a luminosity of $L = 2 \times 10^{34}$ cm^{-2}s^{-1} and an integrated luminosity of 350 fb^{-1} after 2018 especially due to improved trigger systems.

One of the main projects of this phase is the Muon Chamber upgrade. Within this project the innermost MDT wheel is replaced by a new smaller wheel. Hence, a good performance can be provided with the higher occupancy resulting from the LHC upgrade. This is especially necessary due to a high background of particles in this area [79]. With the new small muon wheel also the muon trigger is upgraded to stand the higher rate of tracks.

Similarly, the calorimeters need an upgrade to measure the energy in an environment with higher occupancy. The granularity of the LAr and Tile Calorimeter is partially increased. Furthermore, an upgrade of the front-end readout architecture is planned.

An improved trigger system is especially important for the Pixel Detector. This should be accomplished with the Fast Track Trigger (FTK). In the current setup hits are sent from the Pixel Detector and the SCT to the second level trigger. In contrast, the FTK delivers tracks of each L1A-event to the ROB [79]. The expected installation of the FTK is foreseen to take place before the shutdown in 2018.

Within the third upgrade phase "Phase 2" in 2022 the ATLAS Detector is prepared for a luminosity upgrade to $L = 5 \times 10^{34}$ cm^{-2}s^{-1} with an integrated luminosity of $3,000$ fb^{-1}. At this stage a new Inner Detector is needed. Due to the high radiation damages the current Pixel Detector and the SCT have a degraded performance. In addition, the higher occupancy exceeds the design parameters of the TRT. The Inner Detector is replaced by an all-silicon Inner Tracker (ITk) [78]. The ITk has to have a higher granularity and needs improved radiation-hard readout components. It is currently in an R&D phase. The present structural design is very similar to the Pixel Detector and the SCT after the IBL Upgrade. Four pixels and five silicon strip layers are foreseen for the barrel part. The end caps each consist of six pixel and five silicon-strip disks. The pixel size is planned to be 50×250 μm^2. The silicon strip size is not clear yet and may be 10×10 mm^2 or 97.5×97.5 mm^2 [80].

Besides the ID, the calorimeters need an upgrade, too. The replacement of the electronics inside the cryostat of the LAr Hadronic End Cap and the replacement of all on-detector readout electronics may be essential for all calorimeters. It is further considered to either replace the entire Forward Calorimeter (FCal) or to install an additional warm "Mini-FCal" calorimeter in front of the Forward Calorimeter.

Also the third upgrade phase needs a trigger upgrade similar to Phase 1 in which the muon trigger coverage should be enhanced and the full granularity of the calorimeters should be considered at the first stage trigger level.

With these improvements the ATLAS Detector is supposed to have a good performance with a luminosity of $L = 5 \times 10^{34}$ $cm^{-2}s^{-1}$ and collect up to $3,000$ fb^{-1} of data until 2030 to expand the range of research developments in high energy physics.

6.3 The Insertable B-Layer

The expected radiation dose of the current B-Layer at 300 fb^{-1} was simulated and estimated to 1.6×10^{15} n_{eq}/cm^2 [74]. Although this large radiation dose is not crucial for the full functionality of the B-Layer the performance will decrease before the end of the Phase 1 shutdown and especially until the full replacement of the Pixel Detector by the ITk. This is in particular disadvantageous for the efficiency in b-tagging. The IBL can compensate this loss.

Due to the higher luminosity and the smaller radius of the new pixel layer the track rate is increased. This leads to a higher occupancy which exceeds the bandwidths limits of the Pixel Detector. The current FE chip is not able to handle the higher amount of hit information. Furthermore, the maximal bandwidth to send the data of 16 FEs to the readout chain is 160 Mb/s. This exceeds the bandwidth limits of the current FE chip and the readout chain. Another effect caused by the higher particle fluence is an inefficiency of the Pixel Detector due to radiation damages at the sensors and the FE chip. Both effects, the higher occupancy and the higher fluence especially affect the Pixel Detector because of the small distance to the interaction point. Furthermore, the number of pile-up events is increased. This leads to a reduced vertex resolution and hence a poor b-tagging performance.

To keep the performance of the Pixel Detector during the LHC upgrade an additional Pixel Detector layer is inserted. This also minimises the affects of damages due to the past detector operation. Irreparable failures of the Pixel Detector occurred due to previous operation. Defects at single pixels, FE chips, modules or even a complete Optoboard lead to the loss of one to 300,000 readout channels per defect. Furthermore, the gained experience during detector operation can be taken into account and improve the detector layout to prevent some of the irreparable failures.

Because of the new beam pipe layout the IBL can be directly inserted into the current Pixel Detector. The upgrade of the LHC also includes a better focusing of the proton beams and hence the beam pipe radius was reduced by 4 mm. The new beam pipe has an inner radius of 29 mm in comparison to 24 mm of the previous beam pipe [74]. The IBL is installed at an inner radius of $r = 3.1$ cm. In total 14 staves are planned for the IBL, each containing 32 or 16 modules depending on the the type of sensor: 3D or planar, respectively. Due to little space the slightly tilted modules do not overlap as it is the case in the current detector layout. Thus, it does not have a full coverage in z as the Pixel Detector. The higher active area of the sensor partially compensates this deficit. The coverage of the IBL is $|\eta| < 3.0$.

The insertion of the IBL was originally foreseen for Phase 1 in 2015. An LHC failure led

to the reduction of the centre of mass energy from the nominal value of $\sqrt{s} = 14$ TeV down to $\sqrt{s} = 8$ TeV. As a consequence, Phase 0 was introduced to be able to repair that failure and Phase 1 was delayed to 2018. This also influences the insertion of the IBL which is now installed in Phase 0 in 2013.

The IBL also gives the opportunity to develop and test an improved Inner Detector layer under real conditions. The hereby gained experience can be taken to emend the development of the new Inner Detector ITk foreseen for the 2022 installation.

6.4 The ATLAS IBL Module

As the IBL is installed at a radius of r = 3.1 cm the estimated 1 MeV neutron fluence is even higher compared to the current B-Layer with a radius of r = 5.05 cm. At 550 fb^{-1} it is expected to be 3.3×10^{15} n_{eq}/cm^2. To have a safety margin the IBL is planned to stand a non-ionising dose of 5×10^{15} n_{eq}/cm^2 and an ionising dose of 250 Mrad [74, 81]. The higher number of collisions per bunch crossing as well as the number of pile-up tracks result in a higher occupancy for the current Pixel Modules. This is even increased for the IBL due to the vicinity to the interaction point. The high dose and the occupancy have influence on the sensor and the front-end electronics of the Pixel Module.

For the IBL more radiation hard sensors with higher granularity are required. In addition, the FE-I3 of the current Pixel Detector is replaced by a new FE-I4 chip which can cope with the new radiation hardness and data handling requirements of IBL.

The IBL Module is similar to the current ATLAS Pixel Module a hybrid assembly. The silicon sensors are fabricated in two different ways: 3D and planar sensors. The front-end chip is replaced by a new chip FE-I4 with increased radiation hardness and granularity.

3D IBL Modules are assembled as one-chip modules with a 3D sensor whereas planar IBL Modules contain two chips with planar sensors. Two FEs receive commands by one link at 40 Mb/s. Each FE has its own 160 Mb/s data-out link to ensure the required data bandwidth for IBL Modules. The module width in z-direction is $4,13$ cm and $2,05$ cm for planar and 3D modules, respectively [82].

6.4.1 The IBL sensor material

A quantity to measure the increase of radiation damage at the Pixel Detector is the leakage current of the sensors. Figure 6.1 shows the rising leakage current for the B-Layer and the Layer-1 after an integrated luminosity of 350 pb^{-1}, 1.3 fb^{-1} and 2.3 fb^{-1}. The current especially rises higher for the B-Layer due to the closer distance to the interaction point.

For the IBL more radiation hard sensors have been developed. These two different sensor types have to fulfil the requirements of the IBL: 3D and planar sensors which have to resist a fluence of 2×10^{15} n_{eq}/cm^2 and fit into the marginal space foreseen for the IBL. Both are made of silicon material. The choice of having two different sensors for IBL has been made after a longer development phase for increased radiation hard sensors compared to the current Pixel Module sensor. 3D and the improved planar sensor with a slim edge show individual advantages regarding high irradiation or operation experience and thus both of them have been chosen for IBL and are explained in the following.

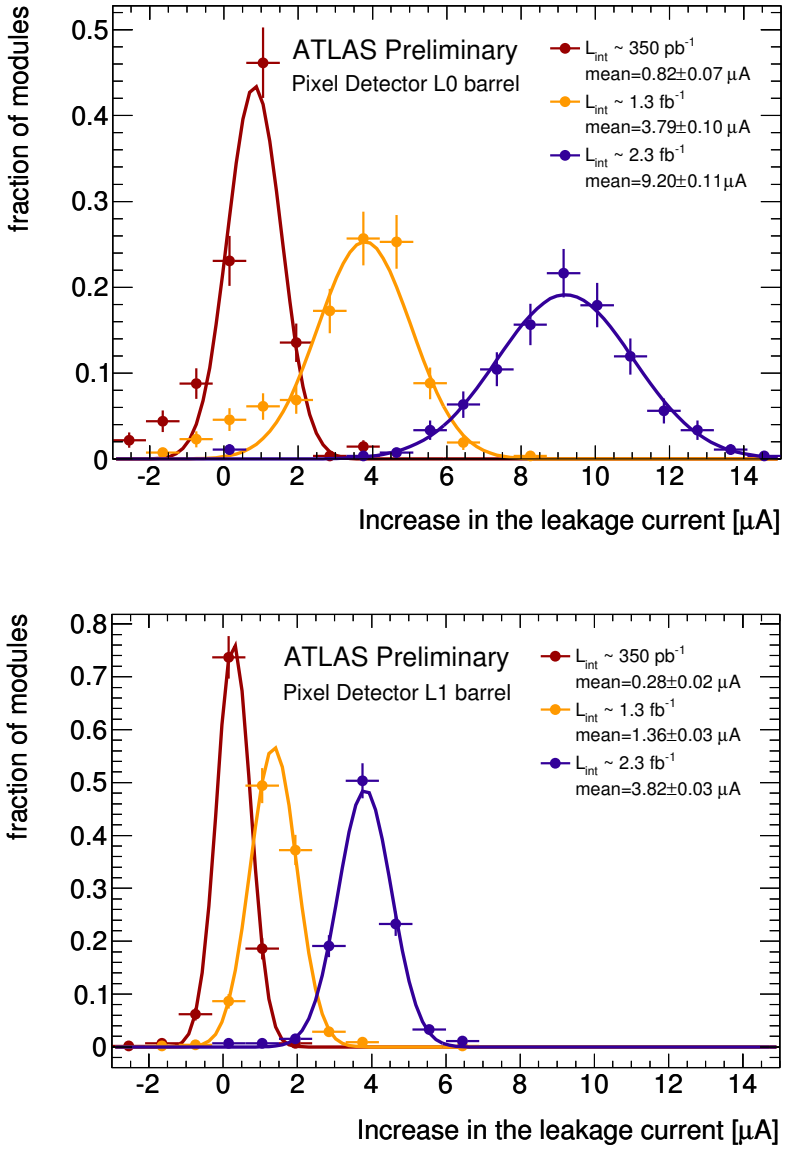

Figure 6.1: The increase of the leakage current for all modules in the B-Layer (top) and in Layer-1 (bottom) after an integrated luminosity of 350 pb^{-1}, 1.3 fb^{-1} and 2.3 fb^{-1}. It can be seen that the current increases higher for the B-Layer as it is closer to the interaction point [38].

The planar silicon sensor

The planar sensor is based on the current Pixel Detector sensor. It is an n-in-n sensor made of diffusion-oxygenated float-zone silicon. The pixel size is 50×250 μm^2 and thus the granularity is increased compared to the old sensor layout.

The thickness of the sensor was reduced down to 200 μm compared to the FE-I3 module sensor. Thus, a higher electric field at the same bias voltage and a higher charge collection after irradiation are achieved [82]. This is an advantage as the bias voltage is limited to 1000 V due to the insulation of the cabling [83]. Besides the sensor, the FE-I4 chip has a reduced thickness, too. This comes along with a bowing of the material and is especially unfavourable during

the chip-flip process while bump bonding. To reduce the bowing, a carrier board is needed as support structure which complicates the production process [81].

Due to the marginal space foreseen for the IBL there is no overlap in z-direction between the modules like in the current layers of the Pixel Detector. Hence, insensitive detector material at the edges of the modules has to be avoided. Developments have been undertaken to receive smaller inactive edges than present in the former sensor design. The resulting "slim-edge" sensors have a reduced inactive edge of 225 µm by moving the guard rings partially underneath the pixels. Therefore, these outermost pixels have a length of 500 µm and are longer than the common pixels.

The temperature of the sensor is $\sim -15°C$ to avoid the thermal runaway after irradiation and is a requirement for the successful operation of the planar sensors.

An advantage of this type of sensor is the already gained experience in production and detector operation. Moreover, it is delivered by many vendors. The production process is simpler compared to the one for 3D sensors. As a result, the yield is higher and costs can be kept down.

The 3D silicon sensor

The 3D sensor type has a p-doped bulk with alternating n^+- and p^+-doped columns which are etched perpendicular to the sensor surface inside the bulk, see Figure 6.2 on the right. Thus, the electric field is parallel to the sensor surface and the depletion zone is generated laterally between

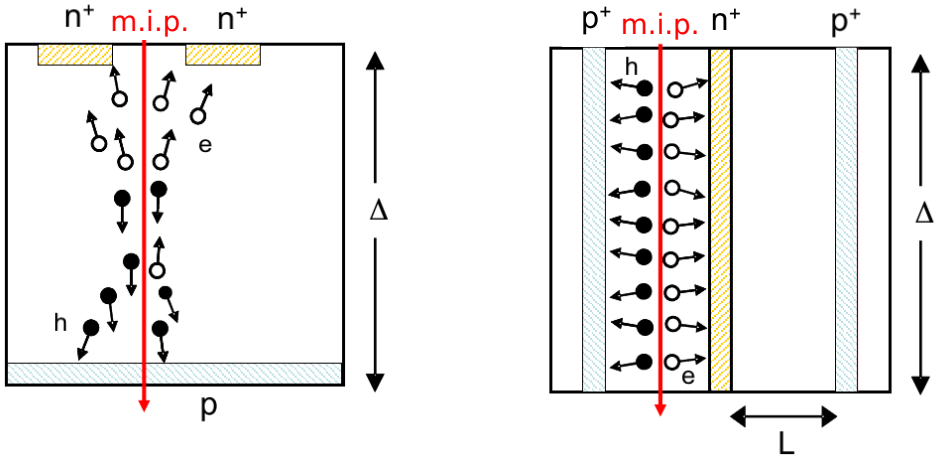

Figure 6.2: Difference of charge collection inside a planar (left) and 3D (right) sensor induced by a traversing m.i.p. In the planar case the drift distance of the charges depends on the bulk thickness Δ. In the case of 3D this distance is only dependant on the distance between the electrodes L but not on the bulk thickness Δ. The drift path thus decreases from $200 - 300$ µm in the planar case to ~ 50 µm in the 3D case [84].

the electrodes. With this method, electron-hole pairs induced by a m.i.p. have a shorter drift distance towards the electrodes. This reduces charge trapping and increases the charge collection time from several tens of ns to a few ns [84]. The reduced charge trapping is especially important after the sensor is irradiated. The major effect of the short distance between the electrodes is the low electric field needed to generate the depletion zone. 3D sensors only need a depletion voltage of < 10 V whereas the planar sensors need several tens of volts.

If a particle traverses the sensor along the electrodes no electron-hole pairs can be generated and thus the particle cannot be measured. In contrast at higher incident angles generated

electron-hole pairs drift to several electrodes. This charge sharing increases the spatial resolution. To take advantage of this effect the 3D modules are slightly tilted by an angle of 10 to 15°.

Two different versions of the 3D sensors are used. The "Full 3D" sensor consists of columns which are etched from one side and completely traverse the bulk. Here, an extra coating is needed to isolate the n^+-columns from the bias voltage on the back side of the sensor. Similarly, it is done for the p^+-columns. The second version is called "double-sided 3D" sensor. In this case the etching is done from both sides and stops immediately before the surface is reached. Hence, n^+-columns are etched from top of the sensor surface and p^+-columns from the backside. The bulk itself serves as isolation towards the opposed potential.

Both 3D sensors use a slim edge to prevent short circuits inside the bulk due to crystal-defects at the edge. This edge is realised by p^+-doped "guard fence" columns which steadily decrease the electric field towards the edge of the sensor [74]. The width of the inactive edge is 200 µm [84].

As there is no thermal runaway due to the low reverse bias voltage, sensor cooling is not as important as in the case of planar sensors. However, it prevents the movement of defects inside the material.

Although the 3D technology has many advantages, the production of the etched electrodes is difficult and a relatively new method compared to the reliable processing of planar sensors. Hence, a high production yield and a good uniformity has to be demonstrated to use them for the IBL [74].

The sensor partitioning on one IBL stave is not settled yet. It is either planned to have 75% planar and 25% 3D sensors or 100% planar sensors in case the fabrication of 3D modules is not fast enough. The 3D modules are placed in the forward region. In the central region planar modules are placed.

6.4.2 The FE-I4 Chip

The FE-I3 of the current Pixel Detector is not able to cope with the higher occupancy expected for IBL. One major issue is the limited transmission of the hit information from the pixel cells to the buffer inside the periphery. Furthermore, the bandwidth to read out the data of one module is 160 Mb/s. This is equivalent to 16 FEs and undermatches the requirements of IBL by far.

To cope with the higher particle flux at the IBL the FE-I3 is replaced by a chip which is more radiation hard and has a higher granularity. Thus, the newly developed FE-I4 chip has a reduced pixel size of 50×250 µm^2 [85]. The chip is 20 mm wide and consists of a 17 mm long sensitive pixel array and a 2 mm long periphery for digital data and command handling as can be seen in Figure 6.3. 26,880 pixels are aligned in 80 columns or 40 double columns and 336 rows. The covered area of the FE-I4 is bigger compared to the FE-I3. Hence, the area with pixel implants compared to the total area is larger which results in a higher active fraction. The chip is thinned down from 190 µm in the FE-I3 case to 90 µm in the FE-I4 case [81].

To increase the radiation hardness transistors are used which can cope with a dose of 300 Mrad [86]. For development purposes a prototype chip FE-I4A was produced. It contains some test features like different power supply options and different feedback capacitors of the double columns [86]. Thus, the best operation performances could be tested. The resulting optimisations were used to produce the FE-I4B chip which is the final version used for IBL. One specific power option, the redesign of the readout periphery and additional circuits, for example for leakage current measurements, are implemented into the FE-I4B.

The analogue circuitry is in its basic functionality very similar to the one of the FE-I3 described in Section 5.1.2 and is thus not explained in further detail. One of the major differences are the sizes of the DAC values. They are one reason why the configuration of the FE-I4 is changed

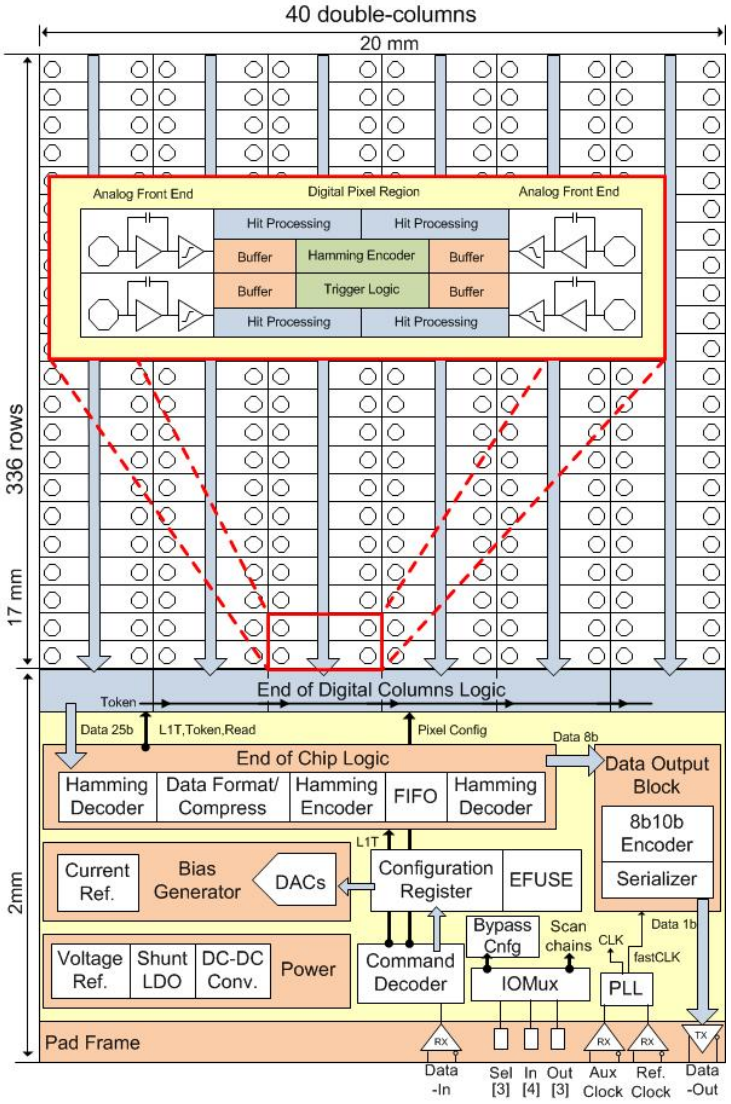

Figure 6.3: Schematic drawing of the FE-I4 layout. The top part shows the pixels aligned in a double column (DC) structure. The readout unit for four pixels is indicated as 'Digital Pixel Region' and shows the basic functionality. In the lower part of the chip the periphery is shown. It contains the digital circuitry for command and data handling [86].

compared to the one for FE-I3. The feedback current of the FE-I3 chip is adjusted with a 3-bit DAC whereas the FE-I4 has a 4-bit DAC. Similar, the DAC value to adjust the local pixel discriminator threshold has changed from 7-bit to 5-bit for FE-I3 to FE-I4. The ToT value contains 4-bit instead of 8-bits as in the case FE-I3 [74].

The digital part

Similar to the FE-I3, the FE-I4 uses a Global and a Pixel Register to store configuration values. In addition, it uses a Pixel Shift Register to move the configuration data inside the Pixel Register. The differences for the FE-I4 mainly consider the new requirements of radiation hardness and the higher occupancy needed for the IBL.

The FE-I4 uses an IBM 130 nm CMOS technology which leads to a higher integration density for digital circuits [86]. Therefore, a readout unit for four pixels at a time can directly be implemented inside the double column structure. This readout unit contains several digital blocks for buffering, hit processing, receiving triggers and hamming encoding. The latter is the transmission protocol used within the FE-I4 digital part to prevent SEU. The readout unit is directly located at the analogue part and thus the hit information of up to five bunch crossings for each pixel can be stored individually on the FE-I4 [74]. This was not the case for the FE-I3 chip where the hit information was shifted to the global shared memory in the periphery. This shift procedure was not able to transmit the hit information fast enough. Furthermore, the memory space for the hit information was not sufficient to store the information of all pixels on the chip.

Upon receiving a Level 1 trigger the hit information is transmitted to the End Of Chip logic and further sent to the Data Output Block within the digital readout periphery at the bottom of the chip. In the latter the hit information is 8b10b encoded, serialised and sent off the chip. Further digital blocks inside the FE-I4 periphery are used for power supply, Global Register storage, clock and command management. These are not explained in detail here as it is not relevant for this thesis.

8b10b encoding

The 8b10b encoded transmission protocol has been chosen to be able to detect single bit flips inside the serial data stream. Bit flips can occur during the transmission from the FE chip to the off-detector part. A specified encoding-decoding scheme can thus detect a single bit flip at the off-detector part. The appropriate bit stream is therefore rejected and not taken for further data handling. In addition, 8b10b can be used for clock recovery. In the following, both advantages are explained in more detail.

At the transmitter side the bit stream is grouped in 8-bit words. Each of these words is translated into a corresponding 10-bit word with a certain disparity. The disparity is the number of 1's minus the number of 0's of that word. In the 8b10b coding scheme for the FE-I4 a maximal disparity of $\pm$ 2 is used [86]. Hence, a 10-bit word can either have a disparity of $\pm$ 2 or 0 in case it has the same number of 0's and 1's. The disparity is used to properly align the 10-bit words one after another. After a word with a disparity of +2 either a word with disparity of -2 or 0 can be placed. This rule is also described by the so called running disparity. A bit word with a disparity of +2 or -2 changes the sign of the running disparity. If the disparity is 0 the running disparity is the same. The receiver checks the correctness of the running disparity. If after a word with disparity +2 another word with +2 follows this indicates a bit flip and the transmitted data is corrupted. Thus, the 8b10b encoder and decoder have to use the same coding scheme to handle the stream correctly and detect possible bit flips.

A property of this coding scheme are so called "comma words". These words are defined bit sequences which are used to control the transmission of the words. For the FE-I4 these are used to mark the start or end of a data frame for example. A special word is the so called "Idle comma" which is always sent in case no FE-I4 data is submitted. Hence, a continuous signal of

1's and 0's is provided which is aligned to the clock of the transmitting device. Similarly, the receiver device can use this signal to align its own clock and is thus synchronous to the clock of the transmitting device. This is also called clock recovery.

The aligned 1's and 0's ensure a direct current balanced bit stream. The direct current balanced serial stream avoids that capacities inside the digital circuitry are charged as it is the case in an unbalanced stream.

Moreover, the continuously submitted bit stream from the on-detector part to the off-detector part prevents data loss if a pixel hit data stream is transmitted. Due to the permanent usage of this laser-diode which sends the pixel hit data the turn-on process of the laser-diode is faster.

Encoding 8-bit words into 10-bit words increases the total data rate by 25%. Due to the sufficiently high bandwidth of the IBL of 160 Mb/s this is not affecting the data transmission. For the IBL a data bandwidth of 88 Mb/s was estimated. This value results from a simulation in which tracks of 75 events per bunch crossing at 40 MHz were read out by an unirradiated, planar sensor. This is far beyond the limit of 160 Mb/s [74].

Configuration

Each FE-I4 can be individually addressed via Slow Commands. The address of the FE-I4 is determined by the chip ID which can be set to a defined value by wiring three FE-I4 chip ID pads. The default address of the chip is 000 in case no wires are set. Trigger and Fast Commands are accepted independent of the address information. All three command types, Slow, Fast and Trigger Commands, have a similar meaning as in the FE-I3 case.

The configuration of the FE-I4 is done via a Global and a Pixel Register [86]. The Global Register configuration values are valid for the complete chip. They store for example enable bits which are used by the Pixel Shift Register to select the appropriate pixel latches. In addition, the Global Register keeps information how double columns are addressed and how the data is sent out. These parameters include the clock frequency, the bandwidth and if the data is 8b10b encoded or not.

Packages of 16 bits can be written with one Global Register write command and are accessed by an individual address. For layout optimisation of the circuitry some register values have the MSB[1]- and some the LSB[2]-value stored first inside the register field. The first 35 Global Register addresses are writable and readable via Slow Commands. The addresses 36-63 are readable only.

The Pixel Register contains 13 configuration bits for each individual pixel. These are for example the DAC values of the analogue circuitry or single bits to enable the injection capacitors. The Pixel Register bits are stored in latches which can only be written by a Pixel Shift Register. The latter writes the content of one pixel latch of a complete double column, see Figure 6.4. Thus, the content of a complete double column is first written into the Pixel Shift Register and then written into the individual pixel latches.

6.5 The IBL readout chain

As already mentioned in the previous sections the IBL requires a new data readout chain to be capable to transmit the increased data rate from the IBL modules towards the ROS. The current Pixel Detector readout chain is able to transmit the data of six FE-I3 Modules at a bandwidth of 160 Mb/s each. For the IBL the data of 16 FE-I4 Modules with a bandwidth of 160 Mb/s

[1]Most Significant Bit
[2]Last Significant Bit

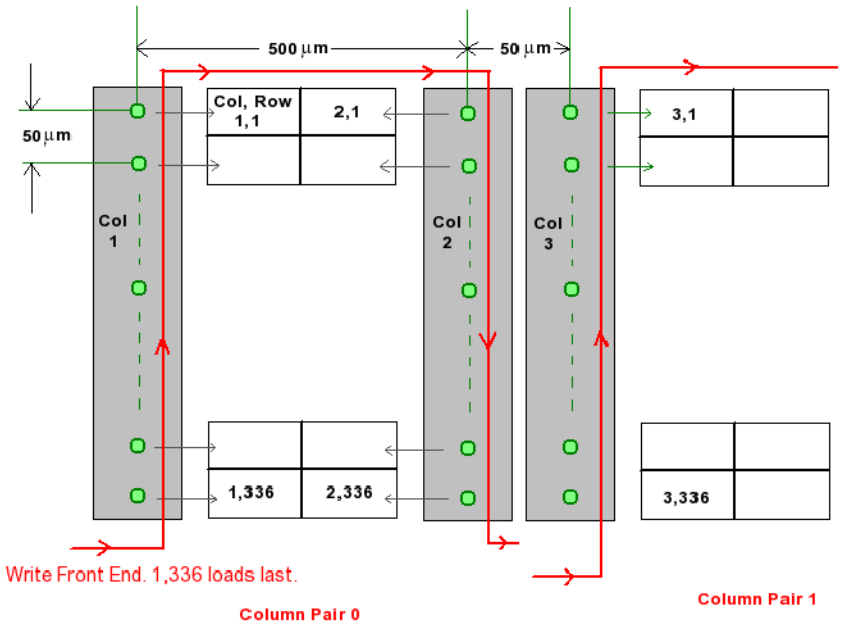

Figure 6.4: Schematic view of the Pixel Register. The Pixel Shift Register writes into one of 13 Pixel Register latches of a complete double column and in total into 672 latches. Thereby, the latch of the last pixel of the second column is written first and the latch of the last pixel of the first column is written last. The DCs to be written are selected by the Global Register configuration and the specified address within the "Write Front End" command [86].

each has to be handled and would exceed the capabilities of the current readout chain. Thus, a new readout chain is needed to fulfil the requirements of the IBL.

The Fast Track IBL schedule demands to have a fully integrated chain for the new detector layer before the Phase 0 shutdown in 2013. To accomplish the demands for IBL within the short time scale a readout chain similar to the one of the present detector was planned. With this decision basic board layouts, the firmware and also the gained knowledge of the previous detector operation can be used as a sophisticated starting point to develop a readout chain for the IBL. Furthermore, the necessary high level of backward-compatibility to the current Pixel Detector readout can be provided. This is done by a readout chain on the basis of the current ROD-BOC pair using VME interface communication.

It consists of a ROD-BOC pair inside a VME crate and an Optoboard followed by a hybrid module as sketched in Figure 6.5. Control and configuration of the IBL ROD and IBL BOC as well as the IBL Module are still done via VME interface and the corresponding SBC-host connection. The same TIM used for the current readout chain is also used for IBL. Hence, the VME pin-out to the TIM has to be exactly the same as before and was considered during the IBL ROD-BOC development. More details on how the individual parts are upgraded for the IBL are explained in the following. As the IBL ROD is the major topic of this thesis, more details on the upgrade can be read in Section 6.6.

The main tasks of the IBL BOC is the data preparation such that it can be handled by the IBL ROD. It receives the clock from the TIM and adjusts it for a proper clock delay and phase

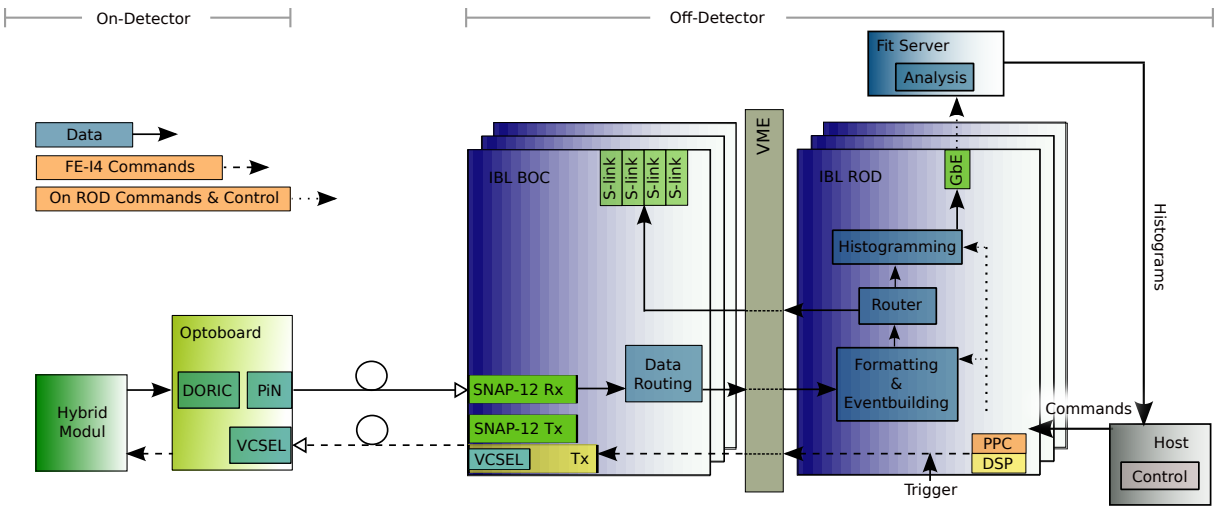

Figure 6.5: The IBL readout chain. The main components of the IBL readout chain are indicated. The analysis of the pixel hit data is done off-ROD by a new introduced Fit Server and the DSP tasks are carried over to a PPC. Optical transmission between the IBL BOC and the IBL Optoboard is done via SNAP-12 transceiver and transmitter.

to be synchronous to the global LHC bunch crossing clock of 40 MHz. This clock is further distributed to the IBL ROD and the on-detector readout parts. One major change of the IBL BOC is the 8b10b encoded module data which is decoded on the IBL BOC. While decoding the data the IBL BOC simultaneously checks the 8b10b stream for errors like disparity errors. This kind of error is specific for 8b10b coding and occurs if the predetermined sequence of 1's and 0's is not kept. During data taking such an error would cause the IBL BOC to discard the current event as the exact location of the provoking SEU cannot be determined.

The IBL BOC has to be upgraded to be able to satisfy the higher data throughput. Two equivalent data paths are implemented which each manage the data of 16 FE-I4 chips. To transmit commands within one data path one SNAP-12[3] transmitter (SNAP-12 Tx) is used. The commands are transmitted to two FE-I4 chips at a bandwidth of 40 Mb/s. To receive data two SNAP-12 Receiver (SNAP-12 Rx) per data path have been introduced onto the IBL BOC, see Figure 6.6. The two receivers handle the data of two FE-I4 chips at a bandwidth of 160 Mb/s each. The optical power of SNAP-12 was not sure to be enough in the first stages of the board development. Hence, a possibility to place additional Tx plugins from the current BOC design on the IBL BOC was given. Meanwhile, it was shown that the SNAP-12 plugins fulfil the requirements as stated in [87]. One SNAP-12 Rx receives twelve optical links: eight data channels, two address and two control channels. As the optical receiver automatically senses the average light level the best working point can be automatically determined to receive the incoming data without errors. This is an improvement as on the Pixel Detector BOC the best working point had to be determined regularly and an extra scan, the "BOC scan" had to be implemented. The data of one data path is handled by a Spartan6 "BOC Main FPGA" (BMF) where it is 8b10b decoded, multiplexed and further sent to the IBL ROD [88].

To be able to transmit the increased amount of data towards the ROS and to send a copy of the data to the future Fast Track Trigger four S-Links are used. The space consuming HOLA card used for the current BOC was removed and the protocol logic needed for the S-Links

[3] A SNAP-12 is a commercial Snap-On Plugin for twelve optical channels [90].

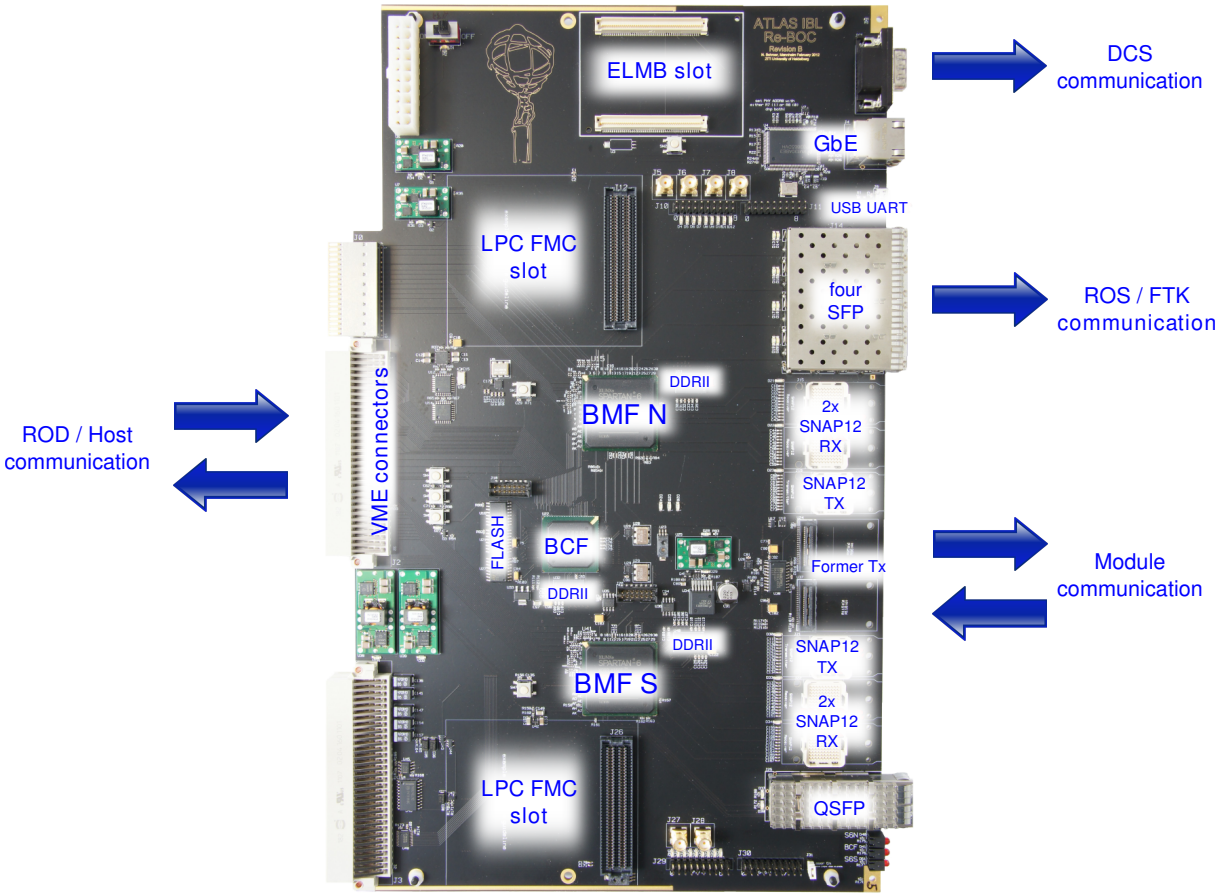

Figure 6.6: The second IBL BOC prototype with its main components and communications [91].

moved inside the FPGAs. As no final decision was made the first IBL BOC prototypes contain two different implementations of S-Links for evaluation. Four individual SFPs[4] and one smaller Quad-SFP (QSFP), which has the same functionality as the single SFPs but is less space consuming, were chosen to transmit the data to the ROS [89].
To control the data handling on the IBL BOC a Spartan6 "Board Control FPGA" (BCF) is used. It programs the individual FPGAs with the firmware stored inside the flash memories and manages the ROD-communication as well as the clock distribution. Moreover, all three FPGAs have their own 512 Mb DDRII memory. For a possible future upgrade the two BMF FPGAs each have a connection to an additional Low Pin Count FPGA mezzanine card (LPC FMC) [88]. For the DCS communication an Embedded Local Monitoring Board (ELMB) is foreseen such that PiN currents and voltages can directly be read out.

The IBL Optoboard serves as optical-electrical interface between the on-detector and off-detector components. It receives optical bit streams from the IBL BOC and transmits them into an electrical signal. Vice versa it converts the electrical signals from the FEs into an optical signal. The new board has eight command links and 16 data links and thus is connected to 16 FE-I4 chips. Due to failures present in the current Optoboard some urgent improvements

[4]Small Form-Factor Pluggable Transceiver

have to be implemented for IBL. One problem is the solder connection between the so called "opto-pack" which contains the VCSEL and the PiN diode and the PCB[5] and leads to problems in the transmission of signals [74]. This problem is solved for IBL by using a wire bond instead of a solder connection. Furthermore, the currently used custom made connector for the optical fibres is fragile and difficult to mount and dismount and hence replaced by a commercial one. During the past Pixel Detector operation the appearance of the Optoboard failures increased and led to configuration or readback problems in 1% of the modules [74]. So far, the source of the problem could not be figured out as the Optoboards are inside the detector and not accessible. The IBL Optoboards will be placed at the end caps outside the detector such that they can be accessed.

One IBL ROD-BOC pair processes the data of two half staves where each half stave has 16 FE-I4 chips. And one IBL Optoboard transmits streams of half a stave. Thus, in total there are 14 staves and 14 ROD-BOC pairs with 28 IBL Optoboards and 448 FE-I4 chips.

To be prepared for the IBL installation several testing phases for the IBL detector chain are foreseen in 2012 and 2013. These system tests are the first trial to check, validate and improve the interconnection between all readout components. This comprises the FE-I4 chips loaded onto a stave and connected to a readout system. Furthermore, cooling and the DCS system is implemented. Currently a readout board for test issues is used but it is planned to integrate the IBL ROD-BOC chain as soon as the major development steps are completed.

[5] Printed Circuit Board

6.6 The IBL Read Out Driver

As the IBL ROD is one major part of the topic of this thesis its layout is explained in further detail. Previous to that the demand of a new developed ROD for the IBL and its planning phase are described to give an overview of the complete development phase of that board.

The necessity for a new readout board for the IBL

As already stated in the previous section the time scale given by the Fast Track IBL project was limited and hence a board similar to the current ROD was foreseen. The reasons for the upgrade of the current ROD are explained in the following.
The increasing data throughput at the IBL affects the layout of the IBL ROD. The ROD of the Pixel Detector has to handle the data of eight modules, each with a bandwidth of 160 Mb/s. In contrary the IBL ROD is expected to process the data of 16 modules or 32 FE-I4 chips, respectively. This has impact on the complete data processing chain: the formatting of the received data from 32 FE-I4s with a bandwidth of 160 Mb/s each, the handling of raw data which has to be forwarded to the ROS via S-Links and the part in which the histogramming and analysis of the data takes place.
Especially the data throughput of the limited bandwidth of the VME interface of 7 MB/s makes the transmission of histogram data from the ROD to the host difficult. This limitation affects all RODs inside one crate as they share the same VME bus and can thus only be used by one ROD at a time [74].
Besides the increased data throughput, the hardware components on the current ROD can be replaced by modern FPGAs [92]. For the new readout board components are used which comply with the requirements of the new data rate.

Furthermore, parts of the Pixel Detector ROD firmware can be reused for the development of the board.

Planning phase

Two readout chains with a different interface have been proposed for IBL. One uses a VME interface communication and has a similar layout compared to the ROD-BOC readout chain of the Pixel Detector. The other is a new developed readout chain based on an ATCA[6] interface. Although the latter provides an interface with a higher bandwidth, the VME interface was chosen for the IBL. One of the main reasons for this decision is the backward-compatibility towards the Pixel Detector chain. Moreover, an already known system was preferred due to the critical time scale of the Fast Track IBL project. Using an IBL ROD-BOC pair the basic layout and firmware were already given by the current Pixel Detector readout chain.

The intensive planning phase for the IBL ROD started in 2009. First, the choice of the IBL ROD components were made in accordance with the bandwidth requirements of the IBL. This included modern chips and a method to bypass the VME interface if histograms have to be transmitted of the detector. For this reason, an external Fit Server PC was foreseen to analyse the histograms produced on the IBL ROD. The other basic functionalities were kept similar to the Pixel Detector ROD. One of the FPGAs, the Virtex5, includes a PowerPC. Hence, the functionality of the Master DSP on the Pixel Detector ROD was foreseen to be ported to this processor. For development purposes the first prototype boards still have a DSP mounted which

[6] Advanced Telecommunications Computing Architecture

is of the same type as the previous used DSP on the ROD. Similar, the adaptations of the DSP code towards an IBL DSP code were studied and presented.

The IBL ROD proposal has been presented in February 2010. A first prototypes of the IBL BOC and the IBL ROD were scheduled for the beginning of 2011 while the IBL installation was foreseen for 2016. This schedule was revised in February 2011 with the Fast Track IBL project.

Preparations of the DAQ system to include the IBL ROD into the existing data acquisition chain were done. Hence, the basic software environment was prepared for the new IBL ROD. In addition, the development to adapt the DSP code to the FE-I4 chip was started.

The fabrication of the first IBL ROD began in early summer 2011. The first prototype, the so called IBL ROD revision A, arrived in autumn 2011. At the same time, the firmware development for the IBL ROD was ongoing [93]. First tests which should proof the basic functionality were done. This included a correct power and clock distribution and the access to all components on the ROD. The IBL ROD was connected to the VME interface to test the communication between the host and the IBL ROD.

Furthermore, the basic functionality of the communication of the IBL ROD and IBL BOC prototypes was tested for the first time.

After primary tests, improvements for a new IBL ROD prototype were included in the IBL ROD revision B board which was produced in spring 2012. Since then, further tests have been done which also include the FE-I4 chip. Simultaneously, the firmware development of the IBL ROD FPGAs and the DSP proceeded.

The next revision of the IBL ROD is planned for the end of 2012.

Final assembly

The IBL ROD prototype B is shown in Figure 6.7. The main device on the IBL ROD is the Virtex5 FPGA which performs the tasks of the former RCF [94]. It additionally comprises a PowerPC (PPC), a processor which will be used to run the DSP code later on. As the IBL ROD development and especially the integration of the DSP software into the PPC is still ongoing the first two prototypes still contain a DSP chip with the SDRAM used as external memory and a flash memory device for the firmware [95]. For the final production board of the IBL it is planned to remove the DSP chip.

Like the DSP, the PPC has an external DDRII memory and a flash memory device. The other two main components are the Spartan6 “North” and “South” FPGAs. They replace the former FMTs, the EFB, the RTR and also the histogramming part of the SDSPs. The latter have completely been removed from the IBL ROD as only modern FPGAs are foreseen for the final IBL ROD and the histogramming had to be renewed in any case. Each Spartan6 is connected to two SSRAMs and one DDRII memory. The PRM is identical to the one of the Pixel Detector ROD. For clock generation and distribution a Lattice clock manager is mounted.
Besides these FPGAs, a “J6” connector directly connected to the Spartan6 North and South for debugging and a JTAG[7] “J9” connector for loading the FPGA firmware in one JTAG chain are implemented. With an adaptor a TTCrq mezzanine card[8] can be mounted on the IBL ROD to provide an additional timing, trigger and command interface.
The Virtex5 and the Spartan6 North and South are each connected to a Gigabit Ethernet (GbE)[9]

[7] The “Joint Test Action Group” (JTAG) communication defines an interface to FPGAs for debugging purposes.
[8] The TTCrq mezzanine card contains the TTCrx and the QPLL. The latter is used to provide a phase locked loop which acts as a jitter filter and a clock multiplier [97]. The TTCrx is a receiver card for Timing, Trigger and Control commands for LHC [98].
[9] Gigabit Ethernet is a defined standard to transmit high data rates.

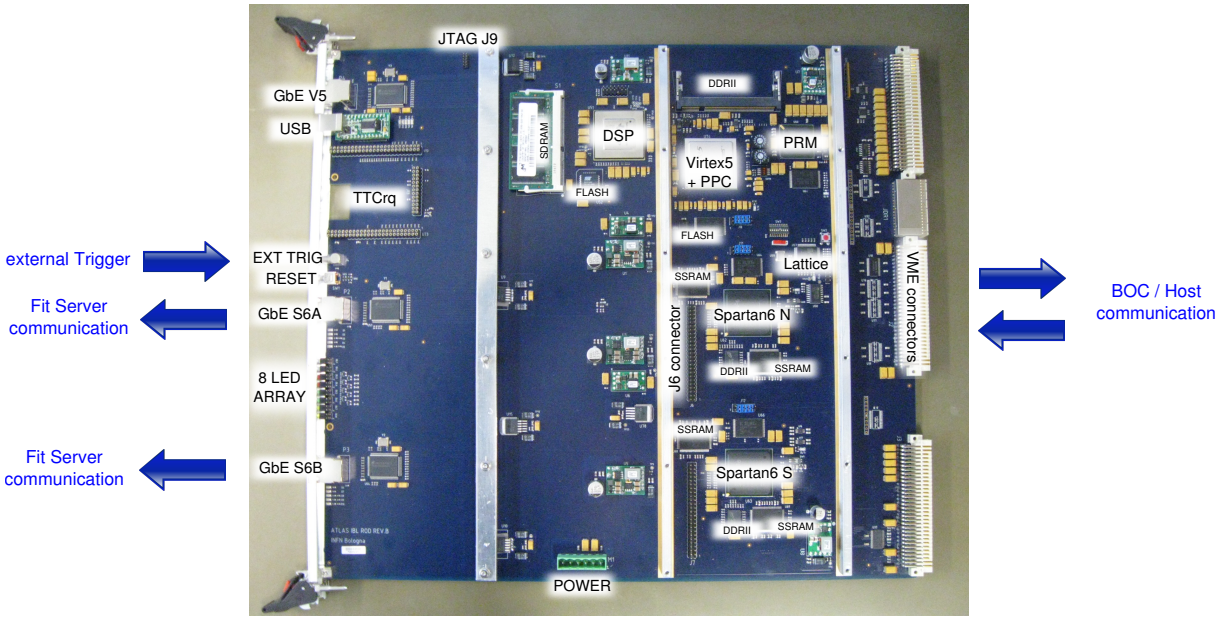

Figure 6.7: The IBL ROD revision B prototype with its main components and communication interfaces.

plug. The GbE connection of the Virtex5 provides an additional interface to an external PC such that the PPC is able to receive commands not only from the VME interface. Each GbE plug of the two Spartan6's connects the histogramming part of the FPGAs with the external Fit Server which takes care of the data analysis of the produced histograms.

Moreover, a USB interface, a connector for an external trigger, a reset button and eight LEDs[10] are accessible from the IBL ROD Front Panel. The VME connectors of the IBL ROD consist of the three connectors also used at the Pixel Detector ROD and one additional smaller "P0" connector. The latter provides additional links between the IBL ROD and the IBL BOC needed for the higher data throughput towards the S-Links.

Finally, an extra power supply connector gives the possibility to easily power the IBL ROD if it is not placed inside the VME crate as may be the case for debugging purposes.

A major change with respect to the Pixel Detector ROD is related to the histogramming and analysis part which is used at scans during detector calibration. The data analysis task is moved to an off-ROD Fit Server as can be seen in Figure 6.5. This is essential as the bandwidth of the VME interface is limited to 7 MB/s. Using the two GbE links a maximum bandwidth of 220 MB/s for sending the histograms off-ROD can be achieved [93]. For the Fit Server GHz processors are foreseen which reduces the time needed for a fit-operation with respect to the time needed by the SDSPs on the ROD. The Histogrammer inside the Spartan6 North and South FPGAs are able to accumulate occupancy and ToT values per pixel. To speed up the scan procedure parts of the histograms are already sent to the Fit Server although the scanning of one FE chip is not completed. Hence, the Fit Server can already analyse the pixel hit data. Simultaneously, the next part of the histogram of subsequent pixels are processed inside the Histogrammer [96]. Thus, histograms are stored on-the-fly which leads to a very fast histogram processing. To accomplish the new histogramming procedure the analysis part

[10]Light Emitting Diode

of the former SDSP firmware has to be ported to the GPU Fit Server farm. Furthermore, the transmission of the histogram data from the IBL ROD to the Fit Server has to be fast enough. An average data rate of 6.9 MB/s for a threshold scan and 17.1 MB/s for a ToT scan per IBL ROD is expected [99]. To achieve an adequate transmission in terms of speed and reliability the Transmission Control Protocol (TCP) is the most promising solution. As network address it uses an IP address and a port number. With a handshake between the Fit Server and the Spartan6 FPGAs a working connection can be verified before the actual histogram data is sent to the server.

Due to fabrication failures of the IBL ROD revision A, a second prototype had been built. The major issues of the revision A ROD are listed briefly in the following. The footprint of the DDRII memory of the PPC is wrong and thus no external memory is available for the PPC. This leads to restricted operations of the PPC and hence the IBL ROD revision A board is not able to process the complete DSP code. Another bug was the slight displacement of the P0 connector footprint. However, with a workaround the connector was mounted on one of the revision A boards such that the general connection and functionality of the links to the P0 connector could be tested and if necessary corrected. At the Virtex5 GbE connection additional termination resistors had to be mounted. Due to a failure during the first IBL ROD-BOC connection test one of the boards also lost a Spartan6 South FPGA which had to be dismounted. In addition, there had been smaller problems. Most of them could be directly fixed.

The second prototype, the IBL ROD revision B board, had no major problems. Due to small changes of the linking between the chips the revision A and revision B board have a slightly different Virtex5 pin-out which has to be taken into account within the firmware development of the FPGA.

6.7 The IBL Data Acquisition

The TDAQ/PixelDAQ software provides a complex and flexible framework to operate and control the Pixel Detector. This environment is also used to integrate the operation of the IBL in parallel to the current Pixel Detector. Major changes of the PixelDAQ code had to be made in the calibration part which uses scan and configuration methods for the FE chip.

The TDAQ/PixelDAQ system had to be provided for lab setups for the IBL ROD-BOC development phase. Hence, it was extended with an additional local and simplified database with respect to the complex database setup used to operate the complete ATLAS Detector. One simple database file was used to store scan processes and results. A local script was provided to generate controller and chip configuration files for different controllers and FE chips.
In addition, much effort went into the installation of TDAQ at a lab environment. So far, the software was just installed by two experts and first attempts of previous installations failed. With the urgent need of a TDAQ lab system for IBL this aim could finally be accomplished and several institutes engaged in the IBL project had an own TDAQ installation.

To implement the IBL in the PixelDAQ framework an extra development branch IBLDAQ was split from the PixelDAQ framework used for current detector operation. Since then, at the end of 2010, several developers have been working on the integration of the IBL into this framework. A necessary starting point was the restructuring of the class hierarchy. This included the disentanglement of classes and the removement of controller specific remnants in base classes. An example are FE-I3 and *RODPixController* related usages which had been partially spread

over classes which fulfil a rather controller independent task.

With these preparations new controllers could be implemented into IBLDAQ. For example, the *USBPixController* was introduced for test setups for FE-I4 tests. Furthermore, an *IBLRODPixController* on the basis of the *RODPixController* has been added and modified to be able to communicate with the IBL ROD and the DSP, respectively. To implement the new readout chip a FE-I4 class has been introduced.

Scan results are now directly downloaded from the Fit Server and not via the VME interface. A probable implementation to include this changes into IBLDAQ would be a request of the scan results via the *IBLRODPixController*. In that case the results have to be handed over to the appropriate classes for scanning. Another scenario is to directly download the results via the scan classes without a detour of using the *IBLRODPixController* class.

7 The Digital Signal Processor for the IBL ROD

7.1 Introduction

The Digital Signal Processor (DSP) is especially important if the detector is in calibration mode to configure modules and control scan processes. Within the IBL ROD development the software of the DSP has to be upgraded.

The code was originally written for the Master DSP of the Pixel Detector ROD. Several developers have designed this code. During the last years of detector operation it could be further improved and failures be eliminated. The DSP code has been developed to meet the requirements on the ROD. This includes a direct communication between the DSP and its environment. Through a continuously running loop the DSP permanently stays in contact with the host. The latter sends Primitives and Tasks which are executed on the DSP. Primitives are commands which are executed once. A Task is a process which can be stopped or runs until it finishes. At the same time the DSP sends back status information or data such that the scan procedure, which is executed on the host, can stop a running process if necessary. Furthermore, the DSP has access to all FPGAs and the four Slave DSPs on the ROD. Thus, it can write and read individual register values through which the DSP can control data path settings and request status information. These control mechanisms are needed while calibrating the detector and running scans.

The basic functionality of the DSP code on the IBL ROD and its main communication to the host and other on-ROD components stayed the same. Hence, it has been decided to use this code as a starting point for the IBL DSP code. This decision is supported by the fact that a successful functionality of the sophisticated and complex design of the current DSP code could already be shown in the past detector operations. As a result, adaptations regarding the properties of the new FE-I4 and the communication to the IBL ROD gives a fully functioning code for the IBL readout chain. Moreover, the time scale of the Fast Track IBL project does not permit the development of a completely new DSP design.

To start the DSP development for the IBL project the TDAQ and PixelDAQ environment had to be setup in the Göttingen lab. This is required as only with this software framework the module configuration can be read from a database and sent to the IBL ROD. Another example for the necessity of this environment are scan procedures which are only initiated by the TDAQ/PixelDAQ package. Hence, the existing PixelDAQ framework has to be extended to an IBLDAQ framework to be able to communicate with the IBL readout chain. These improvements are first integrated into the lab environment and are later used within the full operation of the ATLAS Detector.

At the time TDAQ was setup in Göttingen, only three existing installations had been present at CERN, SLAC[1] National Accelerator Laboratory and the University of Genoa, Italy, which

[1] Stanford Linear Accelerator

had been setup by two experts involved at CERN for a long time. A missing user-unfriendliness and, in addition, an upgrade of the SBC complicated the installation process[2].

7.2 The DSP code

As the DSP code is a very complex code grown during several years of development this chapter explains its fundamental functionality. Especially the basic architecture of the code and the principle of the host-DSP communication are described in Section 7.2.1. Furthermore, the main task of the DSP, the processing of scans, is explained in Section 7.2.2.

7.2.1 Basic architecture

The DSP code accesses several on-ROD components like FPGAs, Slave DSPs, buffers and the LEDs on the front-panel. Furthermore, it can also connect to the BOC and communicate with the host. The communications are done via request and command channels. To send command streams to the detector modules the DSP uses its serial ports. Each of these peripherals is represented inside the DSP code with a c-type "typedef struct" directive[3]. These structures build up an architecture in which a main structure represents the complete DSP. This structure is called *System*. It contains all peripherals of one IBL ROD which are used by the DSP. Each peripheral is also defined with "typedef struct" directives as can be seen in Figure 7.1. These sub structures contain variables and functions to describe the properties of the peripherals. An example is given with the *Module* structure. It contains an integer and a character variable which represent the ID number and the ID name of the detector module. Because each module consists of two FE-I4 chips it also contains a FE configuration array which keeps two individual configurations. The FE configuration is represented as a *FE Config* sub structure. Each FE has its own *address* variable by which it can be identified and a *feFlavour* variable such that the DSP is able to distinguish between the two FE-I4 prototypes: FE-I4A and FE-I4B. Furthermore, it stores a *Pixel Register* and a *Global Register* sub structure which contain the values for the corresponding registers on the FE chip. Besides values, also functions can be assigned to a specific peripheral. Hence, *Module* is able to call its own *configure()* or *readConfiguration()* function.

Another example is the *LED* structure to represent the eight LEDs at the IBL ROD front panel. An LED can be toggled and switched on and off. These functionalities are described by functions with the same denominator. Furthermore, the Input FIFO of the IBL ROD is described and contains a reset and a read function with which the register can be accessed. These functionalities are again represented as structure, functions and variables, respectively.

Until now, all described structures belong directly or indirectly to the *System* structure. In addition, there are also sub structures which are not part of the *System*. This is for example the *Comp FE Config* sub structure which is used to sent the FE configuration data from the host to the DSP. An extra compressed structure is introduced to pack the individual variables as close as possible because of the bandwidth limitation of the VME. For communication the host and the DSP exchange commands and requests. The latter are packed in so called Primitive structures which can contain integer values or a pointer to a data structure for example. This way, a command to turn on an LED on the ROD's front-panel or FE configuration values can be sent to the DSP. If a sequence of more than one Primitive is executed by the DSP, a so called

[2] https://twiki.cern.ch/twiki/bin/viewauth/Atlas/InstallAndOperatePixelDAQ

[3] A "typedef struct" directive defines a new structure type in c programming language which can contain variables and functions.

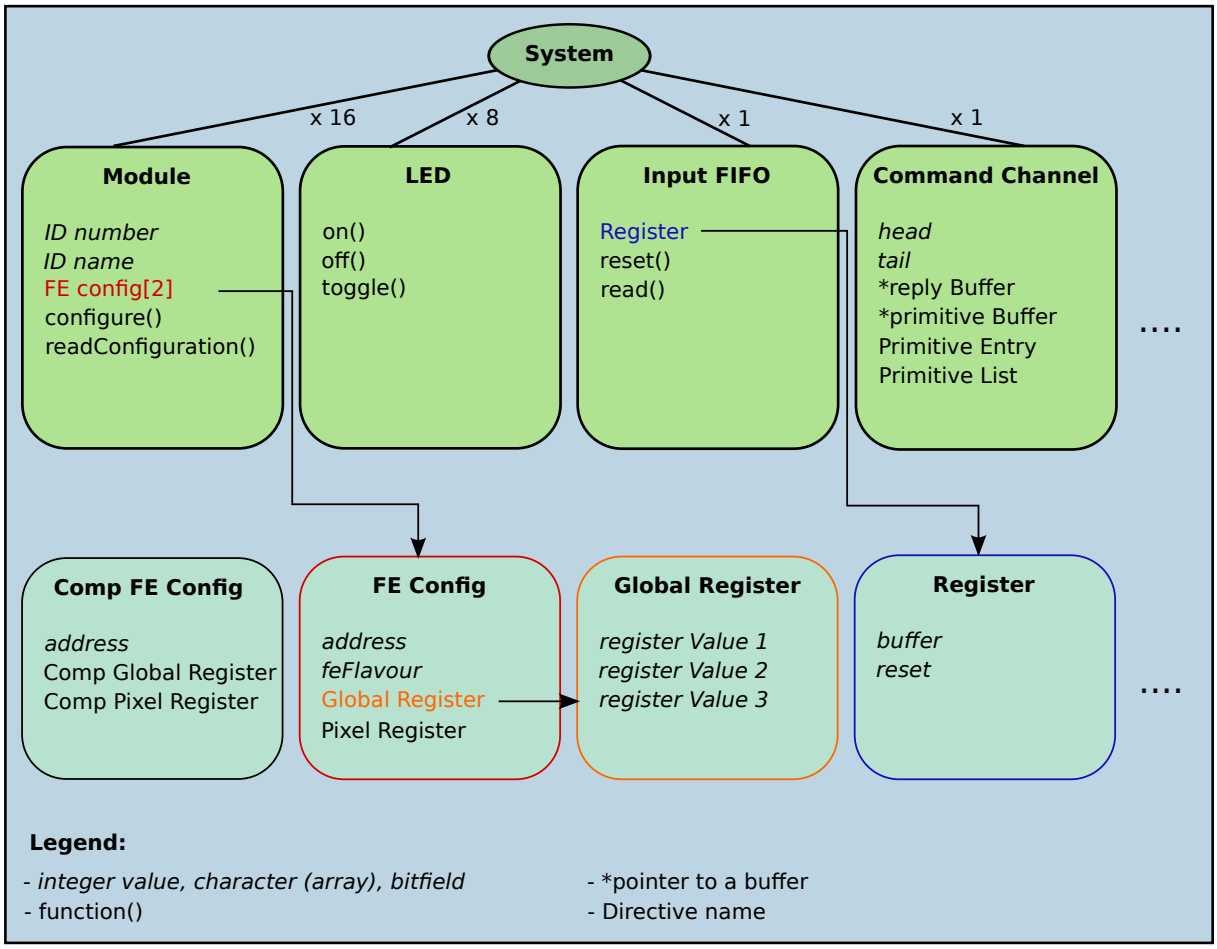

Figure 7.1: The DSP architecture contains a structure called *System* to which all peripherals (green boxes at the top) are connected. This connection is indicated by the black lines. Each peripheral contains variables of different type and are further explained in the text. Also shown are sub structures which only belong indirectly or not at all to the *System* (boxes at the bottom).

Primitive list is sent. Primitives are executed once on the DSP and if requested also send a reply back to the host. In contrast, a Task initiates a process on the DSP which runs until the process has finished or until it is stopped by the host. An example of a Task is a scan procedure.

To represent the command channel of the DSP the *Command Channel* sub structure is used. A Primitive is embedded inside a head and a tail and is stored inside a Primitive Buffer. To differ between the Primitives a Primitive Entry defines their name and hence the related function is called if the Primitive is sent to the DSP. A requested reply of the Primitive is written into the Reply Buffer which is then read by the host. As the command channel has to know about all the properties of a Primitive these are represented as variables, sub structures or pointer to a buffer inside the *Command Channel* sub structure.

After initialisation the DSP runs a polling loop to continuously check if commands or requests are written inside the Primitive Buffer by the host. This is done as no interrupt mechanism is used to sent information to the DSP. Upon receiving a Primitive the DSP first reads its identifier name and then calls the appropriate Primitive function. Depending on the Primitive, values or data pointer to a common sub structure are transmitted.

The *System* can be called from everywhere inside the code. As a result, also a *Module* assigned to the *System* and hence its properties can always be obtained. To retrieve a specific module it is identified by its ID number. Within *System* 16 *Modules* are created which represents the number of detector modules handled by one IBL ROD. Similar, eight *LEDs* and one *Input FIFO* and one *Command Channel* are used as indicated in Figure 7.1.

Host-DSP communication

An example for a host-DSP communication is shown in Figure 7.2. On the host side the user is able to configure modules using the GUI *CalibrationConsole*. Within IBLDAQ the *IBLROD-PixController* class is called. This class reads the module configuration from a database. The configuration values are then stored inside the compressed FE configuration *Comp FE Config*. The amount of transmitted data has to be reduced as much as possible because of the limited VME bandwidth. More details about this compression are explained in the Section *Compressed FE configuration* further down. The compressed FE configuration and additional information like the module ID are stored inside a Primitive and sent to the DSP.

The DSP's *Command Channel* receives the Primitive. Depending on the name of the Primitive the appropriate Primitive function is called. In the example *writeModuleConfig()* is executed first. This function acquires a *Module* from the *System*. The committed ID number from the host is written into the corresponding variable *ID number*. The compressed FE configuration is unpacked, stored inside the uncompressed FE configuration and assigned to the *Module*. Next, the *sendModuleConfig* command is sent in the same manner. Only knowing the newly transmitted module ID the DSP can acquire the correct module from the *System*. To finally configure the module the *configure()* function of *Module* is called. Here, a serial port is acquired from the *System* and individual registers on the ROD are written to prepare the command path on it. A bit stream buffer is created into which subsequent FE commands are written.

For each FE of the module a *writeGlobalRegister()* function is called. Within this function the previously created bit stream buffer is first filled with a Slow Command to set the FE in configuration mode. Then the bit stream buffer is filled with several Slow Commands to write the Global Register for each of the 35 addresses. For that the flavour of the FE, being a FE-I4A or FE-I4B, has to be checked to account for the two different Global Register setups and hence write the correct 16-bit packages into the Slow Command. At the end the Slow Command which sets the chip back into run mode is written into the bit stream buffer. Finally, a loop over all FE rows and columns accounts for the creation of a bit stream for the Pixel Register configuration.

The bit stream is then sent off the DSP via the serial port. Further details about the bit stream generation are described in the Section *Bit stream generation*.

Both DSP codes, for the ROD and for the IBL ROD, use the basic mechanisms indicated in Figure 7.2. They differ in the way how bit streams for the FE configuration parameter are created and hence mostly functions like *writeGlobalRegister()* or configuration structure are different.

Compressed FE configuration

The *Comp FE Config* sub structure contains *Global Register* and *Pixel Register* sub structures. Each of them keeps the configuration values in a different way. The *Global Register* stores the values in bit fields of the size of the configuration value itself. As a result, they are stored consecutively in memory consuming minimal memory.

The Pixel Register contains four mask bits and a 5-bit TDAC as well as a 4-bit FDAC. Hence, in total it only contains six different values which are available for each individual pixel on the

FE chip. The optimised way to store this configuration is with an array. The four 1-bit sized values are each stored as 32-bit words inside an array of eleven rows multiplied by the number of columns on one FE. With this segmentation eleven 32-bit words and hence 336 1-bit values are stored per column. As a result, the values for a complete FE chip can be written consecutively inside memory. The other two Pixel Register values are 5-bit and 4-bit values respectively. Thus, they are each stored in 8-bit packages in an array of 26,880 cells. As a consequence, this compression is not as effective as the one for 1-bit values.

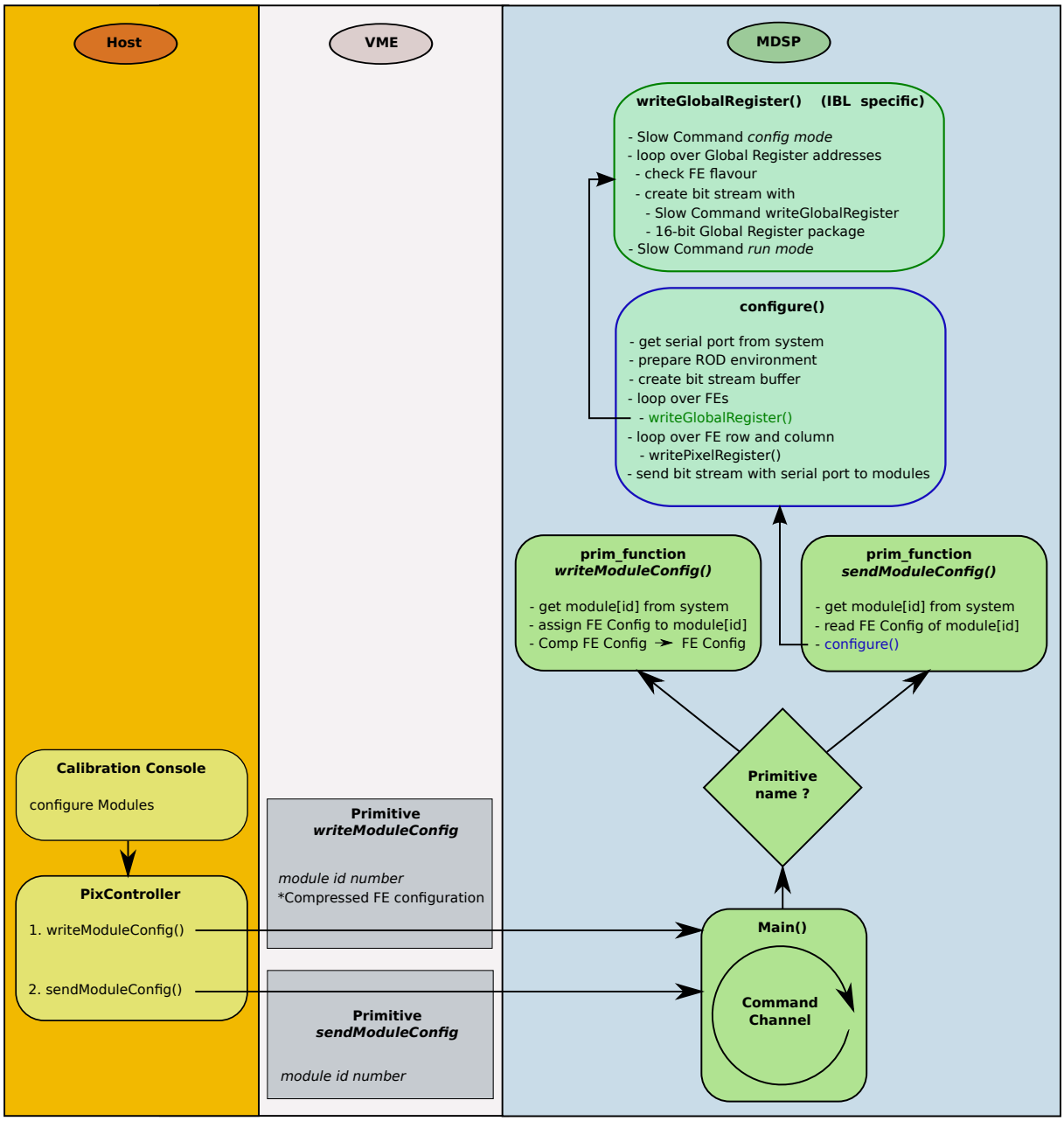

Figure 7.2: A simplified model of the communication between host and DSP using Primitives. As an example, the configuration of a module is shown.

Bit stream generation

The bit stream is a structure which is used each time a serial bit stream is created to send it to the modules. According to the DSP memory structure the buffer which stores the bit stream consists of several 32-bit words as shown in Figure 7.3. Using a pointer to that buffer a bit sequence can be written directly into it. The buffer index j determines the current location of the pointer and is used to set it to the beginning of a new 32-bit word after previous words have been filled. If a 32-bit word is not completely filled by a command sequence it is filled up with padding bits. This is especially important if more than two 32-bit words are used. In that case the bits of command sequence of the second word have to be shifted to the left to generate a sequence without a gap. The Slow Command and its individual bit fields are listed in Table 7.1. After a bit stream is completely filled it is sent via the DSP's serial port as a serial bit stream to the modules.

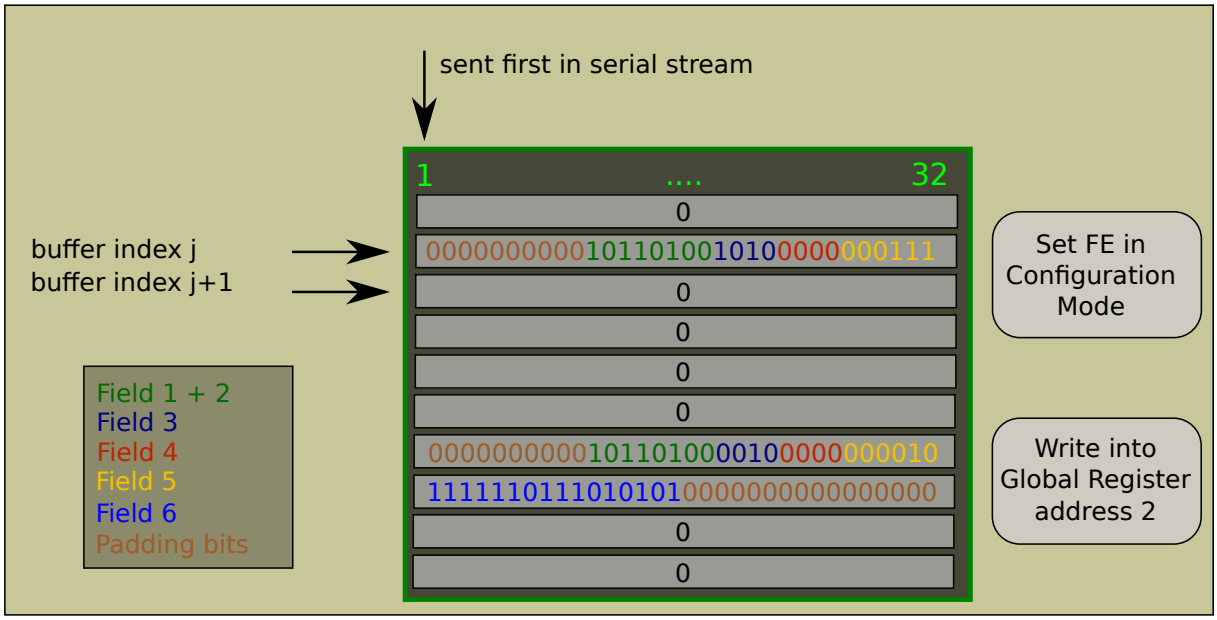

Figure 7.3: The bit stream generation on the DSP. Each command consists of several fields which are further explained in Table 7.1. The single zeros indicate a 32-bit word completely filled with zeros.

Command	Field 1+2	Field 3	Field 4	Field 5	Field 6
General	header	command	chip ID		
Number of bits	8	4	4	6	varied
FE chip config. mode	10110100	1010	0000	000111	not used
FE chip run mode	10110100	1010	0000	111000	not used
Write Global Register	101101001	0010	0000	address	16-bit data

Table 7.1: The definition of a Slow Command with three examples used in this thesis. The usage of Field 5 and 6 is dependant of the Slow Command type.

7.2.2 The scan procedure

The main task of the DSP is the processing of scans. This is done if modules have to be calibrated or their full functionality has to be tested. Scans are divided into normal and special scans. Most of the scans are normal scans which always measure the occupancy and the ToT of the individual pixels. A special scan is for example a register Test which writes a test bit pattern into the FE's Global Register or Pixel Register and then reads it back. By comparing the received data with the original test bit pattern the functionality of each Register bit can be checked.

An overview of a normal scan is given in Figure 7.4 and is in general equal for each different type of scan. The starting procedure contains a setup in which scan parameters from the host are implemented into the scan architecture. In addition, the scan is initialised. Here, the IBL ROD is prepared for a scan procedure and the data path for the returning FE data is setup. Then the actual scan loops are processed. Several nested loops with a specified amount of loop steps run one after the other. The first loop is the so called Mask Stage Loop which enables appropriate pixels on the FE chip. In the case of two Mask Stage Loop steps every second pixel is masked to be read out. Hence, two steps are needed to scan the complete FE. The FE chip is arranged in double columns (DC) which are the parameter of the second loop. A common value are ten DC Loop steps. Hence, in each loop step four DCs are written at the same time. The selected pixels of a FE chip after one Mask Step Loop step and one DC Loop step are shown in Figure 7.5. The next loop is the Parameter Loop which loops over the actual scan parameter followed by the Trigger Loop. The latter sends a trigger signal to the FE chip to read out the pixel hit information. After the loops have finished processing the hit data is histogrammed. Depending on the scan parameter the hit data is also further analysed. An example of a Threshold Scan is described in the following.

During a Threshold Scan increasing test charges are repeatedly injected into the analogue circuit of a pixel. At low test charge values the discriminator threshold is not exceeded and no hits are read back. At some point the test charge is above the discriminator threshold and a hit is recognised within the pixel cell. This behaviour corresponds to a step function in which first no test charges reach the discriminator threshold. After the threshold is exceeded all test charges are recognised by the discriminator. Due to electronic noise within the pixel cells this step is not well determined and the behaviour is described by an S-curve as shown in Figure 7.6. By reading back this pixel hit data the threshold of the discriminator can be measured. It corresponds to the VCAL value at which 50 % of the hits are above threshold. Simultaneously, the electronic noise for each pixel can be determined as the signal sometimes exceeds and sometimes undermatches the threshold although the same test charge was used. The details of how the Threshold Scan is processed on the DSP are further explained in the following.

The scan is a Task and started via a command by the user through *CalibrationConsole*. At that point the host takes control over the scan procedure. The FE configuration is read from the database and a loop which controls the scan status on the DSP is started. This is done by frequently reading an address on the DSP. During the scan procedure this address is written by the DSP to deliver information about the currently processing scan loop. This query is used to keep the user informed about the processing and, moreover, to send further instructions if needed. The latter can be for instance a Task to download the scan results in form of histograms.

Finally, a Scan Task is created by the *IBLRODPixController* class which is sent to the DSP and passes the scan configuration. Now the scan control is setup. Hereby, the scan configuration

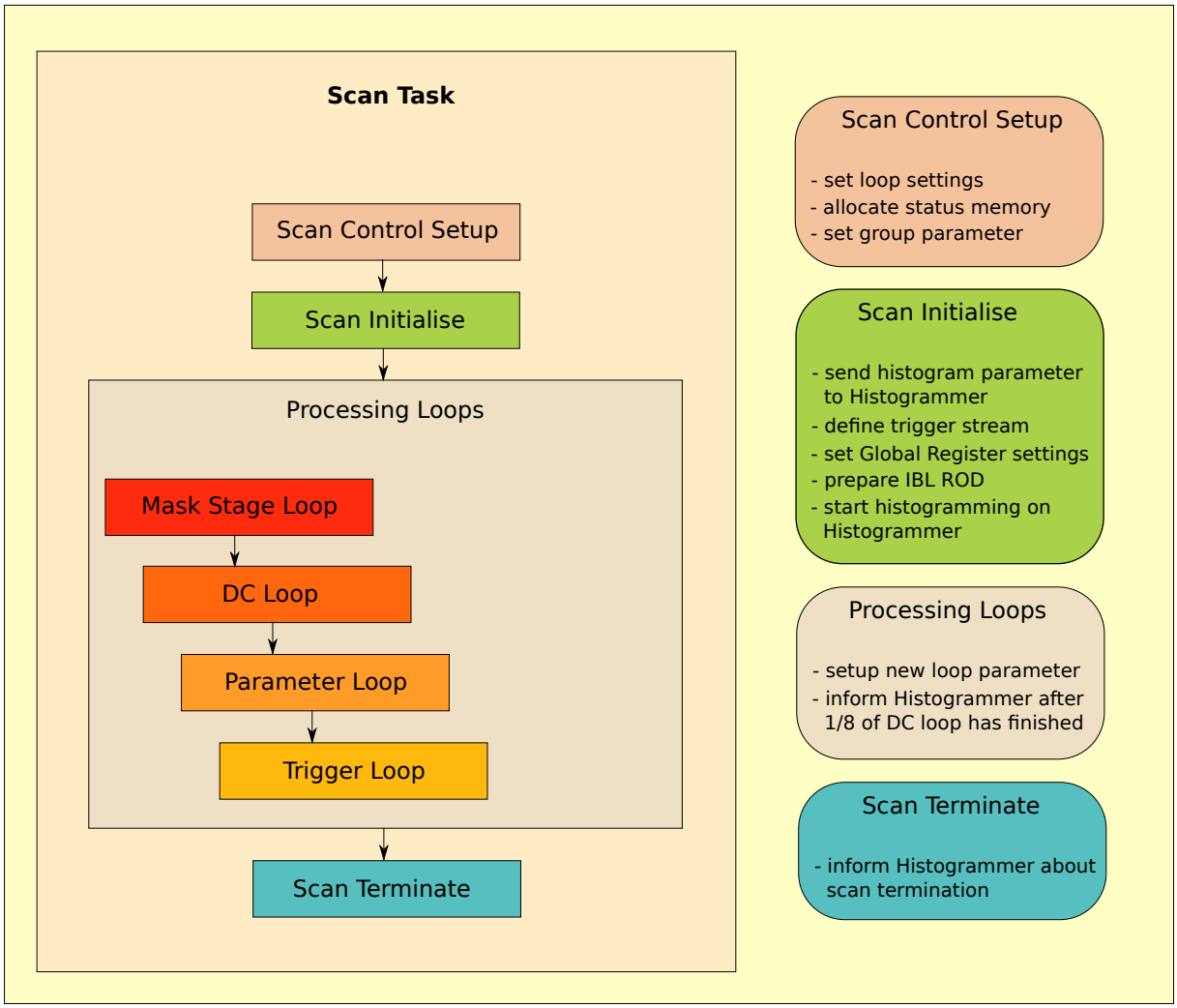

Figure 7.4: A simplified model of the DSP scan procedure. It consists of two methods to prepare the ROD for an upcoming scan, the actual processing loop and a termination method. The DC loop is only implemented for the DSP code of the IBL ROD.

is stored which includes the scan variables, the number of loops and the number of events per loop for example.

Besides the loop parameters, the group is set up. This parameter is needed for the IBL ROD Histogrammer which receives the data of one group of modules. Because four Histogrammer are on one IBL ROD, each Histogrammer processes the data of four modules or of one group.

After the scan control setup has finished the scan is initialised. The Global Register settings like the trigger latency, the enabling of digital injection and the value for external charge injection are written. In addition, the data path on the IBL ROD has to be prepared for readback with writing into the appropriate registers of particular IBL ROD peripherals. This includes for instance the enabling of the FMTs and their links. Finally, the Histogrammer have to be prepared for receiving and processing scan data. In this procedure, the histogram parameters are forwarded to the Histogrammer. Among others, these contain the number of steps of the scan parameter, the number of triggers or the number of mask steps.

After the IBL ROD is prepared for the scan procedure the scan loops start. Not all pixels are scanned at the same time. This is done as the pulser circuitry of the FE-I4 is not powerful enough to inject the test charges for all pixels simultaneously. Furthermore, the Histogrammer is optimised to process the hit data of one eighth of one FE chip.

The following loop is the Mask Stage Loop. This demands the configuration of the Pixel

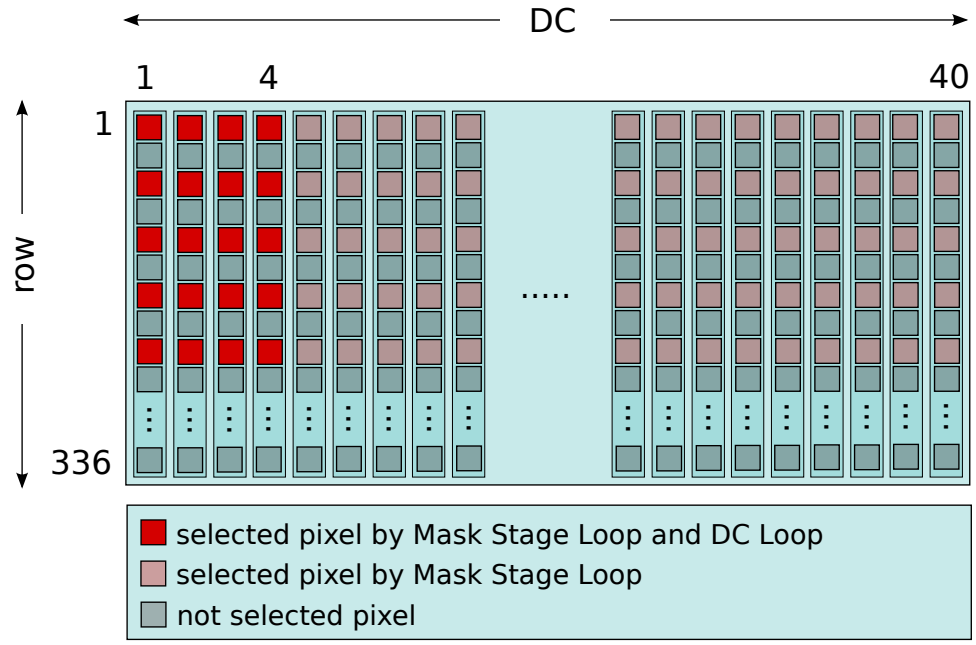

Figure 7.5: The selected pixels after the first step of the Mask Stage Loop and the DC loop. One eighth of the complete pixel array of one FE is chosen to receive triggers by the subsequent parameter and trigger loop.

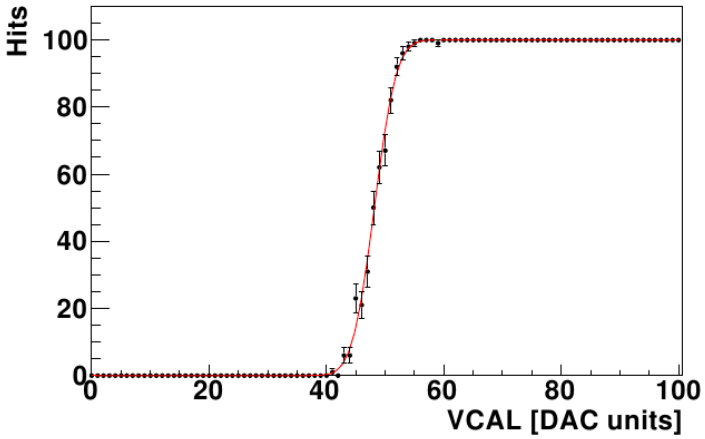

Figure 7.6: The result of a Threshold Scan with 100 test charge values which are each triggered 100 times. The number of hits as a function of an increasing test charge shows an S-curve. The test charge is plotted in VCAL units which corresponds to the FE-I3 terminology [100].

Register to enable or mask the selected pixels. As the configuration of the Pixel Register is time consuming it is not written again if the next mask step is reached. The most efficient way to reconfigure it is by shifting the Pixel Shift Register.

After the Mask Stage Loop the DC Loop is set up. Here the DC address has to be defined. Furthermore, the mode how many DCs are written at the same time is determined. This can be for instance every second DC or one single DC at a time. These parameters demand the reconfiguration of the corresponding Global Register addresses. After the first step of the Mask Stage Loop and the DC Loop the Histogrammer is informed about the current loop status. At this stage one eighth of the FE data is filled inside a histogram and can be forwarded to the Fit Server. Hence, the histogram data can already be analysed although the scan procedure is not finished.

The next loop is the Parameter Loop and demands the reconfiguration of the corresponding Global Register addresses to increase the scan parameter. For the Threshold Scan this parameter is the test charge. A common value for this loop are 200 steps for the increment of the test charge. The following Trigger Loop usually contains 100 steps. In each step the test charge value is injected into the pixel cell and then read out by a trigger bit stream.

If all scan loops have finished processing the scan is terminated.

7.2.3 DSP memory and address management

To program the DSP and create serial bit streams the memory alignment has to be taken into account. The DSP uses little-endian, meaning that the LSB is stored first in memory at the lowest address. This is important when a bit stream buffer is filled and sent to the modules via the serial port.

The alignment of structures and arrays plays an important role in dealing efficiently with the data. Both are aligned to the boundaries which is required by the largest type it contains [101]. On the DSP a 32-bit word alignment is used. Inside a structure it is therefore important in which order their properties are placed. An example for illustration is shown in Figure 7.7.

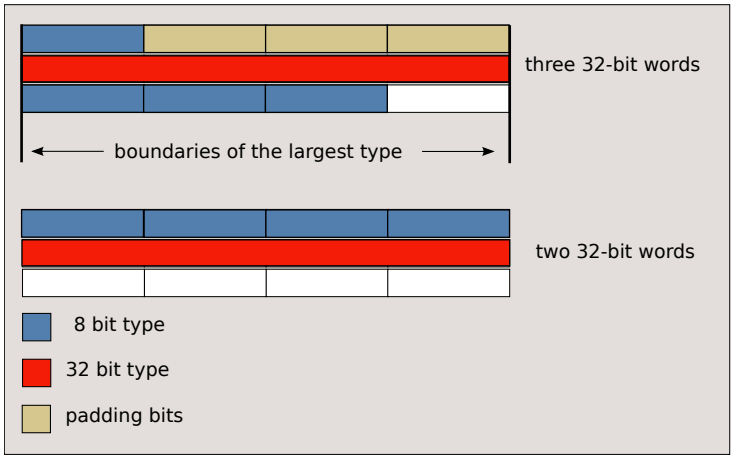

Figure 7.7: The word alignment to a 32-bit boundary as it is used on the DSP. In the upper example one 8-bit type, one 32-bit word and three 8-bit types are placed one after another inside memory. To fill the space between the first 8-bit type and the following 32-bit type padding bits have to be inserted and three 32-bit words are used to store the complete structure. In the bottom example the four 8-bit types are placed one after another inside a structure. Only two 32-bits and no padding bits are needed. The latter is thus the most efficient way for memory storage.

Bit fields do not use word alignment. Thus, all values are stored directly one after another inside memory. Hence, two bit fields of 3 bits each are written into one byte. Because bit fields do not use alignment they also do not have a size which can be queried. Nevertheless, it makes sense to pack them into 32-bit packages such that a bit field structure can be efficiently integrated into a higher level structure which does use 32-bit alignment. This is done for the compressed FE configuration which is part of the temporary module configuration and used to sent the data from host to the DSP.

Another characteristic of the DSP memory alignment are “pragma” directives. These are used to allocate functions and objects which are stored in memory. Within the DSP code two pragma directives are used. The CODE_SECTION directive is used to store executable code, like functions and constants, into either the internal or the external programme memory, which is the SDRAM. The DATA_SECTION directive stores variables into either the internal or external data memory.

To address an on-ROD component the DSP uses 20 bits which are sent in parallel to a receiving peripheral. For a correct transmission the actual address has to be shifted by two bits to the left. This is caused by the DSP EMIF which sends the bits 2 to 21 via the address bus [102]. This has to be considered in case the existing DSP code should be ported to a PPC or if new test code for the DSP is written.

7.3 The challenges of the DSP code development

The DSP code is a complex code which was originally written by a couple of developers over the course of several years. It was further developed during the last years of detector operation for debugging purposes and improvements. Within that time a note was written which so far is the only documentation about the DSP code on the ROD [72]. Although it gives a good introduction and overview, many details of the code itself have of course to be figured out by directly reading and running the code. Very few comments are made by the developers to help understand the code.

The most challenging task of the DSP development is the limited available debugging capability. The functionality of the code can only be tested in a fully working environment. This includes a running TDAQ partition with a working IBLDAQ and lab database interface as well as a fully implemented IBL ROD. This is needed as only within this complex framework Primitives and Tasks are sent to the DSP. As a consequence, TDAQ and IBLDAQ had to be maintained as basic software to establish an always working framework. Moreover, only with a fully implemented IBL ROD necessary requests to certain registers are possible which monitor the process flow. The IBL DSP code development was complicated by a not properly working communication with the external DSP components on the IBL ROD. Especially during more sophisticated processes like a scan procedure the DSP often reads individual IBL ROD registers. These actual needed implementations had to be located and removed to be able to have a simpler but first IBL DSP code.

Another limitation for debugging is the DSP text buffer. It is read out frequently by the IBLDAQ framework and contains the printout of statements inside the DSP code. The text buffer is limited in space and has a size of 4,096 32-bit words only. Incorrectly used its content is overwritten and no debug output is received. This happens in two cases: If the programmer inserts too many printout statements for debugging purposes or places them inside a function which is called very often. This is very disadvantageous since many functions are frequently called by the main processing loop of the DSP. The first challenge in DSP coding therefore was where to put meaningful printout statements and where not.

A common and more sophisticated debugging tool for integrated circuits like FPGAs or DSPs is a JTAG connection with an emulator cable. With such a connection the programmer can directly spy into the DSP memory, write into it and interrupt the execution of a programme for debugging purposes. Although this is an ideal tool for testing and developing a code it is not usable for DSP programming as it does not integrate the TDAQ, IBLDAQ and IBL ROD environment. More about the usage of the JTAG emulator cable can be read in Section 8.1.1.

In Section 7.2.3 the basic memory alignment was presented. If the allocation of memory is not done in a proper manner a corrupted DSP software can be the result. This can be the case if new peripherals are implemented but no pragma statement is used to allocate the memory. Hence, a proper allocation of the memory is inevitable for a working DSP software. This has further to be considered after new structures or functions are implemented. In that case the compiler has to translate the complete DSP project from scratch because the memory has to be fully rearranged.

It can be seen that the DSP software is not only a c-programme which has to be understood and successfully compiled. Above all, the environment of the DSP has to be maintained and especially the limiting text buffers are challenging for development purposes.

7.4 Code adaptations and implementation for FE-I4

The DSP code for the IBL ROD uses the DSP code of the Pixel Detector ROD as starting point. This was done because of the limited time available until the IBL readout chain has to be fully implemented. The complexity of a code which was developed and debugged within the last years cannot be reproduced in that short time scale.

It was further decided to have different DSP versions for the ROD and the IBL ROD. The differences between the new FE-I3 and FE-I4 chips and especially the Histogrammer communication require so many changes that a new DSP code branch, the IBL DSP code, is needed. As the former Slave DSP tasks are shifted to the Spartan6 FPGAs and the off-ROD Fit Server and therefore the DSP is the only DSP on the IBL ROD the DSP code is named IBL DSP or DSP code in the following.

An IBL compiler flag was introduced in the complete IBLDAQ framework to differentiate between both code versions. This was necessary as the still identical declarations of structures and definitions lead to conflicts within the IBLDAQ package. As a result, the IBLDAQ framework included either the ROD or the IBL ROD DSP code.

A test module structure was implemented to get an understanding of the functionality of the code. It was a copy of the original *Module* structure and used to understand how a new peripheral is implemented into the *System* structure. Thus, the way bit streams are generated and subtleties in creating and using a peripheral were understood. Furthermore, a new Primitive was introduced to communicate with the test module to gain a better knowledge about the host-DSP communication.

Finally, after first implementations had been done all ROD DSP remnants had been removed from the IBL DSP code. This mainly includes structure declarations and value definitions for the FE-I3 and the MCC. Thus, IBLDAQ was able to treat the ROD and IBL ROD in parallel which was selected by the choice of the controller type, for instance the *IBLRODPixController*.

The first implementations towards the IBL DSP includes definitions for FE-I4 specific numbers like row and column and the number of FE chips per module. Furthermore, all peripherals have to be adapted to the IBL ROD components. At the moment the two Spartan6's contain the functionality of one FMT and two Histogrammer each. However, the number of the FMT is preliminary and might change in the future.

On the IBL DSP the Slow and Fast Commands have been completely rewritten for the FE-I4. To form a bit stream, a Slow Command header is added to a chip ID and further data. This is a flexible value and can be the Global Register address or configuration data and are passed by the invoking function. An example of a Slow Command bit stream can be seen in Figure 7.3.

The Fast Commands are completely hard-coded because they do not carry any chip specific data and are processed by all FEs receiving this command.

In the future, it is foreseen to only have the PPC and no DSP device on the IBL ROD. For development purposes both devices are used at the moment. This is done to develop the IBL DSP code for FE-I4 and simultaneously to port this code to the PPC. Both, the DSP and the PPC, have a different address conversion and hence all hard-coded register addresses within the DSP code have to be replaced by constant macros. Hence, two assignments of these macros to a register address are implemented for DSP and the PPC.

Most of the Primitives and Tasks of the ROD DSP code are reused for the IBL DSP. Some contain arrays with a length related to a FE-I3 specific number and hence this Primitive or Task is replaced by a FE-I4 specific one. Furthermore, additional Primitives are included to account for the new Histogrammer implementation. Thus, a Primitive to transmit the connection parameter to the Fit Server is implemented and sent to the Histogrammer.

The most important functionality for a module communication is the Global Register configuration and is used for simple tests with the full readout chain.

FE-I4 Global Register implementation

The implementation of the FE-I4 Global Register has to be renewed. This is due to the change of the configuration values of the FE-I3 and FE-I4. Moreover, it has to be considered that individual values are stored in memory with having their MSB or LSB first. In addition, each Global Register address is configured by writing 16-bit packages via a Slow Command. In the case of FE-I3 only the complete Global Register could be written with one Slow Command. As a consequence, many bits had to be transmitted to the modules although only one value needed to be changed. Furthermore, the 5 MHz clock used on the MCC required a modified bit stream generation on the DSP. The bit streams are sent with a 40 MHz clock to the modules. To read such a bit stream with a 5 MHz clock each single bit has to be sent eight times to account for the slower sampling rate. This modification is removed for FE-I4 because it reads the incoming bit stream with 40 MHz.

The FE-I4 Global Register implementation uses some concepts of the FE-I3 Global Register usage though. This includes the usage of a “typedef struct” directive to store all configuration values. Because the configuration values are transmitted from the host to the DSP using the compressed configuration format.

The configuration of a complete Global Register is done via a loop over all writable addresses. In each loop step one Slow Command with a 16-bit data package is filled by an extra function. This allows to write one Global Register address only. To account for the different FE-I4 types the FE flavour is passed to that function as well. Depending on the address and on the FE flavour the bit stream is filled with the corresponding 16-bit data package. The individual values of one such package are reversed if their LSB is stored first inside the register. The information if a value has to be reversed or not is hard-coded inside the function which creates the bit stream. This is done because there is no other usage of the bit reversion of single values as in the case of generating the bit stream. Moreover, the Global Register structure can be kept simple which is an important issue if many people are developing the same code.

An illustration on how the Global Register stream is implemented can be seen in Figure 7.8. To configure the FE-I4 it has to be set in configuration mode before the Global Register write commands are sent. Similarly, it is set back into run mode if the configuration stream has finished.

To test the readback of the Global Register, an input memory was provided on the Spartan6 firmware which contains the bit streams received at the IBL ROD input links. The current implementation is a read only FIFO. Hence, the DSP sends a Global Register command to the FE. The received data stream is simultaneously sent to the FMTs and to the input memory. After having issued a reset to the memory it is cleared and the data stream is read out.

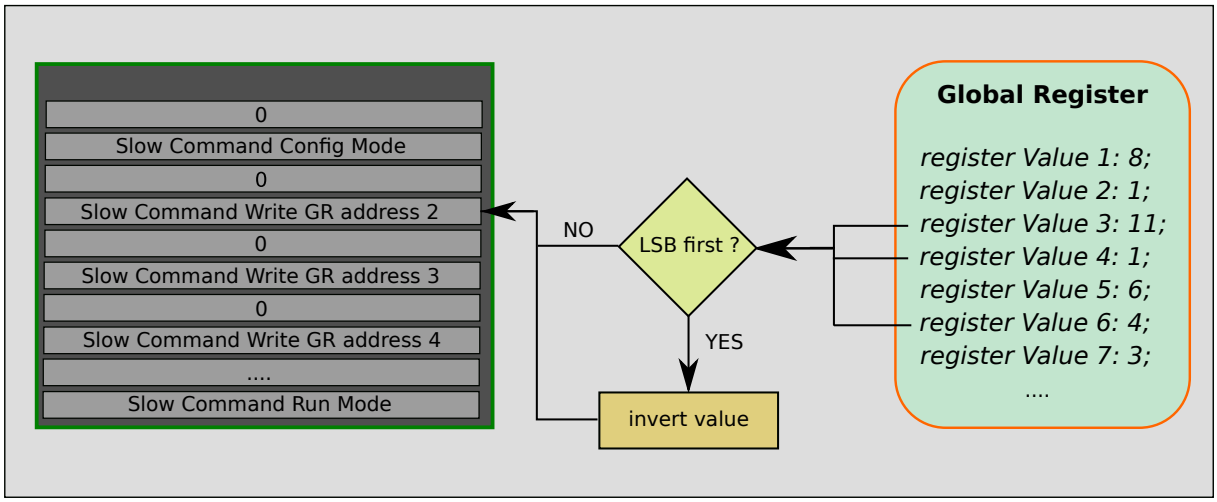

Figure 7.8: Bit stream creation of a Global Register configuration. The register values are filled into 16-bit packages depending on the FE-I4 type and if their MSB or LSB is stored first in memory. In the latter case the register value has to be reversed before it is added to the 16-bit package. In case of FE-I4A the first used Global Register address is two.

FE-I4 Pixel Register implementation

In the case of the Pixel Register realisation with 26,880 pixels, each containing 13 bits, the usage of a matrix is inevitable. The total amount of data transmitted from host to DSP via the VME interface is by far greater than in the case of the Global Register configuration.

The compressed configuration is decompressed and written into a 3D matrix with 336 rows and 80 columns. Each matrix element has a size of 16-bit and stores the 13 bits of the corresponding pixel. Hence, the single bits are not related to their actual values as in the case of the Global Register configuration but are written one after another into memory. This is not disadvantageous as the latches of each pixel are written bitwise. With an index every single pixel can be easily read out and written into an appropriate Pixel Register stream for configuration.

The write command for a Pixel Register is executed per DC. Hence, a loop over the two single columns and all rows is used to read the Pixel Register bit from the 16-bit matrix element. Because the pixel with the highest row is configured first by the Pixel Shift Register the loop over the rows starts with the 336 and decreases step by step. A mask selects which of the 13 bits is configured. The pixel bit is stored inside a 32-bit wide word. Therefore, 21 words are needed to keep the 672 pixel bits for one latch and one DC.

Each of the 21 32-bit words are added to the Slow Command which writes the configuration data into the Pixel Shift Register. This Slow Command is embedded in a sequence of several other commands. Before writing the Pixel Register the DC and the pixel latch has to be selected via the Global Register settings. After having sent the Slow Command to write a Pixel Shift Register the Global Register is configured in such a way that the Pixel Shift Register is able to copy its content into the appropriate pixel latches. The latter process is then triggered by a Global Pulse Slow Command. The Global Pulse is used for different purposes depending on the configuration inside the Global Register. In the case the Pixel Shift Register is used to store its content into the latches, an appropriate Global Register bit has to be enabled such that a global pulse is issued to the Pixel Shift Register. Similar to the Global Register configuration, the FE-I4 is set into configuration mode before the Pixel Register is written and set back into run

mode when the task has finished. Finally, the Global Register settings which had been changed during the process are restored and the next DC is configured.

Implementation of a normal scan

After the basic configurations were implemented the realisation of a first normal scan, for example a Threshold Scan, is done. The scan procedure is described in Section 7.2.2.

The basic structure of the scan procedure is similar to the FE-I3 case in the ROD. The main differences are the additional DC loop and the Histogrammer communication.

As a starting point, the initialisation procedure was adapted to the IBL case. Many settings had to be replaced. Formerly, variables like the number of consecutive triggers had been stored inside the MCC register. These moved to the Global Register configuration. The adaptation of the DAC value of the test charge injecting pulser circuitry and the enable bit for digital injection are two further examples. These Global Register values had been in the FE-I3 Global Register, too. In the former code the assignment was made using a special function. The IBL DSP code simply writes the new Global Register value directly into the structure.

The initialisation procedure also defines the trigger stream for the scan. This stream is a defined bit sequence. By receiving this stream the chip sends back the stored hit information on the FE memory. Because this command is the same on the FE-I3 and the FE-I4 it could directly be adopted for the IBL DSP code.

First steps have been undertaken to implement the DC loop. Due to elaborated problems caused by the missing communication with the Histogrammer and the IBL ROD these were commented out again to avoid possible and not tested failure sources. Hence, the idea of this implementation is described here.

First of all, the different mask stages are adapted to the FE-I4 which is done on the *IBLROD-PixController* side.

On the DSP side the DC loop is integrated in the existing loop implementation. During the scan control setup the DC loop parameters are set. This includes a DC mode and a DC address. The DC mode defines if only one double column or several double columns are selected for the scan. The address specifies one of the 40 double columns. An extra *setupDCloop* function is needed to set the appropriate DC parameters at the beginning of the scan and after every DC loop step incrementation. In this setup function the address of the DC to be scanned and the address mode have to be set accordingly inside the Global Register. Here, it has to be considered that the DC mode is different for the digital and analogue injection. The digital injection applies the test charge only to the digital circuit of the FE chip. In the analogue case the test charge is injected directly to the bump bond connection to the sensor. In the latter case not only double columns but also single columns are addressed. In addition, the Histogrammer has to be informed in case eight DC loop steps have been passed such that the partial histograms are transmitted to the Fit Server and the analysis can be started.

The current and maximal DC loop steps are added to the status parameters which are frequently read out such that the process can be followed on the host side. However, the execution of the DC loop is only executed on the DSP.

Because the Histogrammer communication has not been advanced enough at the last weeks of this thesis commands and request to this peripheral are disregarded yet inside. First efforts have been made to implement a memory location to which the DSP can write and read. This can be used to sent histogram parameters or to tell the Histogrammer that one eighth of the scan procedure has finished to initialise the fitting on the Fit Server.

8 First tests of the IBL readout chain

In this chapter the very first tests of the IBL ROD DSP code are described. This includes hardware tests with the first prototype of the new IBL ROD board in which the connections between the DSP and its external memories were tested. Furthermore, the implemented FE-I4 configuration was examined. This was first done with the Pixel Detector ROD because no IBL ROD had been available. As soon as the IBL ROD was produced it could be connected to a FE-I4 for the very first time. The FE-I4 configuration was tested and the initial communications with the external interfaces to the IBL ROD could be established.

8.1 First IBL ROD hardware tests

The studies described in this section were carried out during a research stay abroad at the INFN[1] in Bologna, Italy. The aim was to put the IBL ROD prototype A into operation for the first time. This included first hardware connection tests, especially the communication between the DSP and its external memory devices.

A FE-I4 SCC was prepared in Göttingen to be able to establish the first connection to the FE-I4 in Bologna. Within this preparation a FE-I4A chip without sensor was wire-bonded to a single chip carrier board. Furthermore, additional resistors needed to operate the carrier board were mounted. With a successful Digital Test carried out with the USBPix system a correct connection of the wire bonds was verified and the SCC card was delivered.

At Bologna a working environment was prepared which included a TDAQ installation to establish a connection to an IBL ROD via VME. While the main task was the operation of the DSP, first tests of other hardware components of the IBL ROD and the connection to the VME interface were done.

The tests were carried out with an externally powered IBL ROD prototype A by applying 5 V and 3.3 V to the power supply connector. This provided an easy access to all pins on the board instead of having it inside the VME crate. A rudimentary firmware was implemented on the PRM which was able to define from which memory location the DSP has booted. This can either be from the internal memory or the external flash memory of the DSP. This bootmode is set via several links to the DSP which can either be logical high or logical low. In addition, the Lattice clock manager contained an appropriate firmware to provide a clock on the IBL ROD which was also routed to the DSP.

In the two sections of this chapter the software environment used for debugging purposes of the DSP and the first DSP tests are explained.

8.1.1 Code Composer Studio

The Code Composer Studio (CCS) software is a debugging tool for the development of DSP software. The actual DSP code is embedded inside this software framework. It offers a compiler and DSP specific configuration files which define the memory usage or the EMIF setup needed

[1] Instituto Nazionale di Fisica Nucleare (Italian Institute for Nuclear Physics)

for external devices. Furthermore, it has a complex GUI which offers several tools and simplifies the debugging of the DSP code. This includes a memory window and the implementation of breakpoints. The memory window shows the memory range which is accessed by the DSP. Hence, the outcome of the implemented code writing into a certain memory address is directly seen. User defined breakpoints mark locations within the programme at which the execution is interrupted. With single steps it is then possible to go through the code line by line to be able to follow the process flow of the implementation. At the same time a dis-assembly window shows the current point of the programme execution. It displays the assembler code of the programme memory. Besides this machine language, the c-code is also displayed in this window [103]. Hence, it can be observed which memory address the DSP is writing to. This can then be compared to the content of the memory window at that address. Furthermore, a watch window to trace the current value of a variable and several control registers during processing can be used. The latter include the EMIF setup for example.

The CCS GUI and a JTAG connection to the DSP have to be available to make use of the full capabilities. The latter is done by a DSP emulator cable[2] which has a JTAG connection for DSPs and hence offers a connection while the DSP is processing.

For the DSP development two different setups of CCS are used. The IBL DSP code uses a more primitive implementation of that CCS software. Here, only the compiler, setup files and software libraries but no GUI are used. Thus, the compiled DSP code is loaded onto the processor using the VME interface and not via CCS. This was done because no JTAG connection to the DSP is available on the Pixel Detector ROD. On the IBL ROD it turned out that the JTAG connection was not very stable. For first tests of the DSP communication to its external memory devices the full CCS environment was used to be able to verify the memory and control register content.

8.1.2 DSP memory tests

In the first DSP memory test the access to the internal and the external memories were tested. To verify the communication to the external flash memory test words were written into the internal memory of the DSP. These words were then copied into the external flash memory. The read back test words were compared with the originally written stream.

The JTAG emulator cable connected the DSP JTAG pins on the IBL ROD to the PC running the CCS software, see Figure 8.1.

At first, the JTAG emulator connection was tested to verify a correctly powered supply and software installation. This was done by a simple tool which executed from a command shell and scans the path between the PC and the DSP [104]. Thereby, it was found out that two pins of the on-IBL ROD JTAG connector were not powered due to a faulty connection. This was temporarily solved by powering them with an extra external power supply. Later, additional resistors were implemented to establish the correct power supply.

After establishing the JTAG connection the EMIF was configured by several control registers to access the external devices. A global control register and four control registers which are specific for one external device. The global control register provides the parameter settings of ready or wait signals for instance. The ready signal is used to signalise if the external device is able to be addressed and hence to receive commands. The wait signal indicates that a process of connected devices is interrupted and further instructions are demanded. These adjustments are valid for all external devices using the EMIF interface [105]. Four control registers are used to interface with four external devices, respectively. They each adjust the timing of read and

[2] Texas Instruments XDS 510 Emulator cable

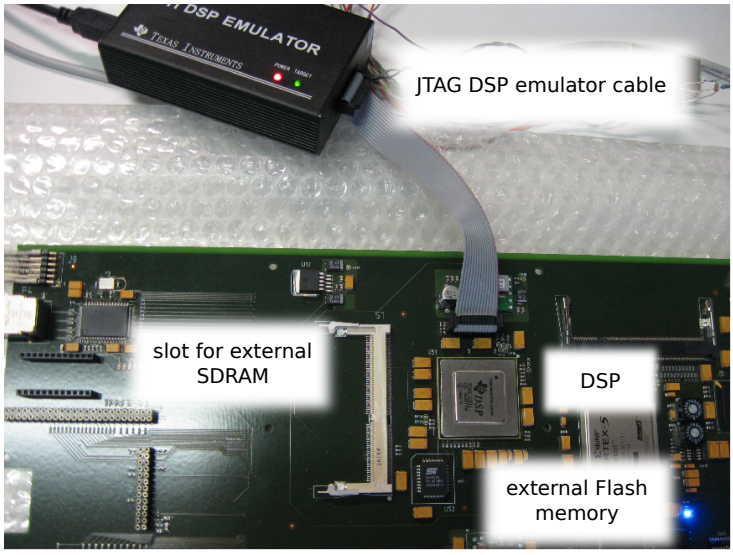

Figure 8.1: Setup to test the internal and external DSP memories. A connection with the JTAG emulator cable was established to access the DSP using CCS debugging software.

write signals to the DSP clock and the memory type of the external device. Furthermore, the PRM was modified such that the DSP booted from its internal memory.

Using the CCS window to check the correct writing of the control register settings the setup was verified. A software implementation provided by the manufacturer of the DSP was used to test the flash memory device and was further enhanced to also read the chip ID of the flash memory [106]. To start the programme the memory addresses of the flash and the internal memory were defined at the beginning of the software code. The flash memory test programme then processes write and read operations to verify the functionality of the flash device. The results of an incremented counter are subsequently written to a location inside the internal memory. Each value is stored in one 32-bit word according to the memory alignment of the DSP. To provide a clean memory the flash device is erased by a special bit sequence. Then the data which was written into internal memory is copied to the flash memory. Previous to that an appropriate bit sequence is executed which tells the flash memory device that the following data has to be written. For both commands to erase and write the flash the specified addresses inside the bit sequence were shifted by two bits to fit the EMIF address bus requirements. Finally, the content of the flash memory is read back.
In addition, a function to read the chip ID of the flash memory device was implemented. This procedure requires a different bit sequence to receive the acquired value [107]. During the whole process breakpoints were implemented to trace the programme procedure.

The incremented counter values could be observed inside the memory window of CCS. Furthermore, the flash device could be successfully written and erased and finally the correct chip ID was read out. Hence, the functionality of the device could be verified.

A programme to test the SDRAM similar to the flash memory was started in the final stage of the stay in Bologna but could not be finished there. Therefore, the SDRAM was directly tested using the IBL DSP code as soon as the VME interface to the DSP was working.

The whole testing procedure with the DSP emulator cable was very unstable and is therefore not recommended. The connection from the CCS GUI to the DSP as well as the loading of the firmware were not reliable although the initially described test to verify the JTAG connection

itself was always successful. If the programme could be loaded to the DSP it behaved in the same manner each time it was run and hence the final results are reliable.

8.2 Preliminary tests of the IBL DSP code

A major aim was a working communication between the SBC and the DSP device. It was tried to load the IBL DSP code onto the flash memory of the DSP from where it is booted. Therefore, an IBL ROD FPGA firmware for the Router and the PRM had been used. The PRM defines from which location the DSP boots. This can either be the DSP flash memory device or the Host Port Interface. The latter is the interface between the DSP and the host and only used if the flash memory is corrupted. Usually a programme on the SBC is executed which loads a compiled IBL DSP code to the flash device and boots it from there [108]. During this process the DSP always writes the hexadecimal code 0xC0FFEE into its start address. A proof that this procedure is successful can be received by directly reading the content of the DSP memory. A command executed from the SBC allows the dumping of a specified address range. After the DSP code was loaded onto the flash memory and booted the hexadecimal word was expected to be read in the DSP memory. This was used to figure out if the DSP access via VME was successful. During first tests the 0xC0FFEE identifier could not be read from the DSP start address.

Different procedures were undertaken to examine why the DSP flash memory device could not be loaded. This was done with test programmes executed on the SBC which read the IBL ROD registers. Furthermore, the programme to load the DSP firmware onto the chip was executed using a debugger. Finally, a more improved firmware of the IBL ROD FPGAs which also controls internal DSP signals was provided which solved the problem.

Finally being able to access the DSP, the IBL DSP code was loaded and booted on the IBL ROD for the very first time. To verify the functionality of the host-DSP communication and the processing of the DSP itself, the IBLDAQ environment was used. With sending a command via *CalibrationConsole* a detector module configuration stream was created by the DSP and read out via the DSP text buffer. The generated stream was identical to the one received by a Pixel Detector ROD MDSP. No influences which affect the general behaviour of the DSP were observed. Hence, it could be shown that the communication between the host and the DSP could be established successfully. As the DSP code uses internal and external memory the functionality of the SDRAM of the DSP was also shown. Furthermore, a working FE configuration procedure on the DSP could be proved.

So far, the implementation of the Global Register configuration could only be tested using DSP printout statements and reading the resulting bit stream via the DSP text buffer output. The next step was to send the bit stream off the ROD and measure it with an oscilloscope. Therefore, the IBL DSP used with an SSH connection to the IBL ROD was not sufficient for further tests. For this reason, the Pixel Detector ROD was used to send command streams off the ROD. This was possible for two reasons. The DSP device and its external memory devices are identical on the ROD and the IBL ROD. Hence, the DSP environment is the same and the IBL DSP code can also be processed on the ROD DSP. In addition, the DSP on the ROD and the IBL ROD both use the same communication path to send the bit streams off the board.

It was tested if the created configuration bit stream was correctly built and sent out via the serial port. This was done by sending the bit stream off the ROD and comparing it bit by bit with the bit stream observed in the DSP text buffer. To monitor the sent configuration bit

stream with an oscilloscope a test point of a command link of an electrical BOC[3] was used. The resulting bit stream to configure the Global Register addresses two and three is shown in Figure 8.2. At the beginning and at the end the FE is set in configuration and in run

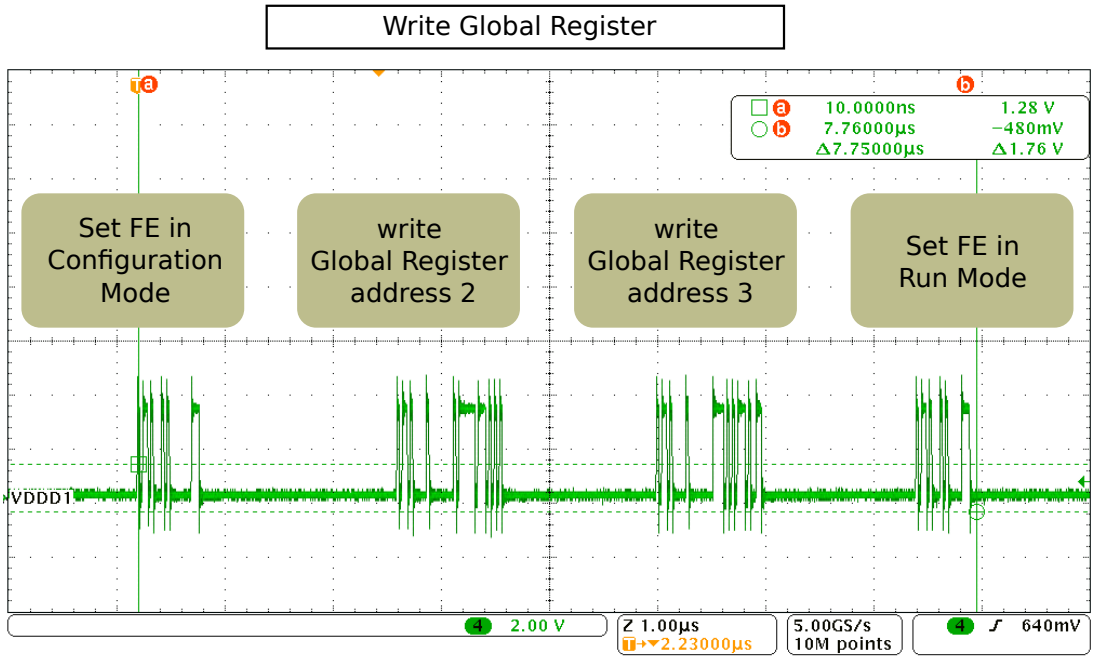

Figure 8.2: Screenshot which shows a bit stream which configures the addresses two and three of a FE-I4 Global Register.

mode, respectively. A detailed view of the first two Slow Commands is seen in Figure 8.3 and Figure 8.4. The first shows the Slow Command which sets the chip in configuration mode and contains one 32-bit word. The second figure shows the Slow Command which writes the Global Register address two and contains two 32-bit words. Both figures use the colour coding scheme which is used in Figure 7.3 for the different bit stream fields. The 16-bit data package of the Global Register stream contains a 4-bit value for the number of consecutive triggers "1111", a 1-bit value which enables the readback of the Global Register address and an 11-bit wide field which is used as spare register. The latter is filled with a bit pattern "10111010101" for test purposes. Because the FE-I4A and FE-I4B chip contain different Global Register values the 16-bit data packages of the configuration bit streams are not always the same. In the shown example of Global Register address two and three the bit streams are valid for the FE-I4A and FE-I4B.

However, the Slow Commands which set the chip into run or configuration mode are identical for both. The observed bit stream is as expected and the individual register values are identical to what was before written in the configuration. Hence, the IBL DSP is able to configure a FE-I4 chip. The chip itself could not be configured as it was not possible to include it in the existing ROD data path.

[3]The electrical BOC was plugged into the back plane of the VME crate. It was formerly used to test the Pixel Detector readout chain and was developed by the Berkeley National Laboratories.

8.3 Tests of the IBL DSP with the IBL ROD prototype B

Since May 2012 an IBL ROD prototype B has been available for tests in Göttingen. The firmware provided with the IBL ROD was preliminary and only some parts were included. However, it

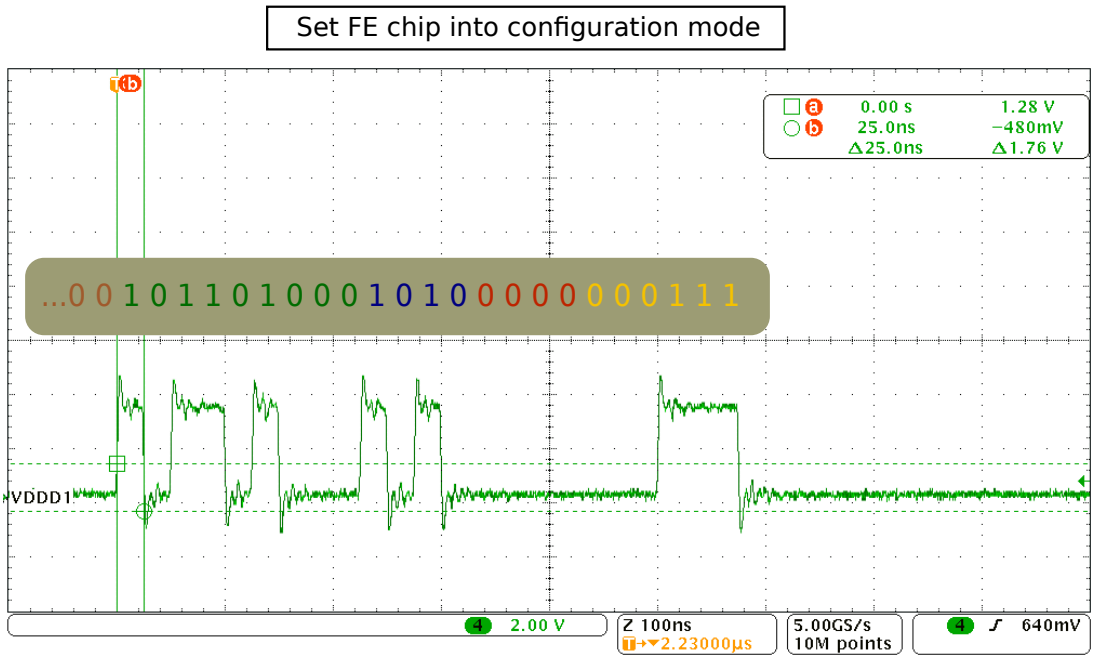

Figure 8.3: A detailed view of a Slow Command which sets the FE-I4 into configuration mode.

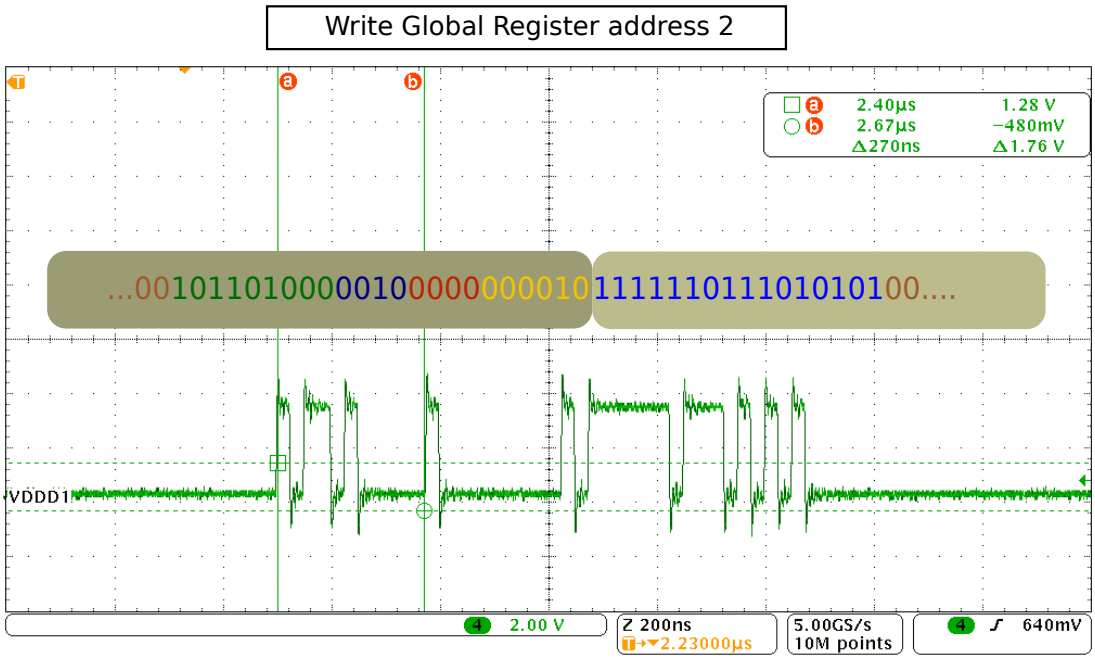

Figure 8.4: A detailed view of a Slow Command which configures the Global Register address two of the FE-I4.

gave the possibility to do first tests with the new board. In addition, it contained the IBL BOC firmware which was necessary to receive 8b10b decoded data streams. Especially the first configuration of a FE-I4A with an IBL ROD was undertaken. In this section the setup used to test the FE-I4A implementations on the DSP is described. Moreover, the tests themselves and the results are presented.

An overview of the setup with the IBL ROD prototype B is shown in Figure 8.5. The IBL ROD is plugged into the VME crate through which it is powered and accessed by the host via the VME interface. The connection between the host and the IBL ROD is managed by the PRM. Commands for the FE chip are received from the host and transmitted to the DSP where they are translated into serial bit streams. The Virtex5 and the Spartan6 FPGAs simply route the 40 Mb/s commands to the J6 connector of the IBL ROD. Currently one command link is provided and only the North Spartan6 FPGA was used for the test. The command signal is further transmitted to the Ethernet port of a FE-I4A SCC via a custom made connector. Besides the command signal, a 40 MHz clock is also transmitted from the FPGAs to the FE-I4A. The latter is externally powered with a voltage of 1.5 V and 1.2 V applied via the Molex power connector of the SCC card, see Figure 8.6. The returned data is sent to the J6 connector and further to the FPGAs. To be able to receive 8b10b decoded data with a bandwidth of 160 Mb/s

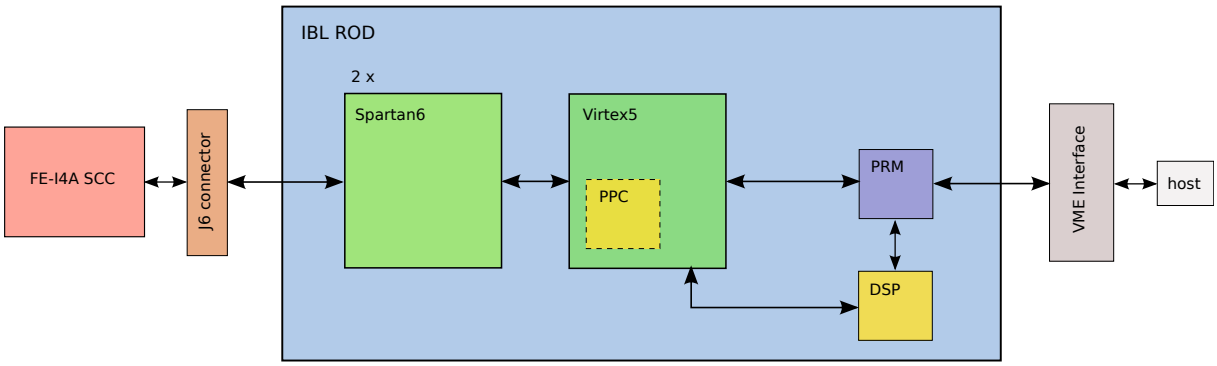

Figure 8.5: Schematic drawing of the setup used for first tests with the IBL ROD prototype B. For the sake of completeness the PPC included inside the Virtex5 is shown although it was not used within the tests explained in this section.

the current IBL ROD test firmware additionally contains the firmware of the IBL BOC as can be seen in Figure 8.7. Hence, one encoded 160 Mb/s stream can be decoded and deserialised into an 12-bit parallel stream as it is demanded by the FMTs. The same data stream which is sent to the FMTs is also linked to the Input FIFO which is used by the DSP as debugging tool. Following the path from the FMTs the data is further sent to the FMT FIFO where it is stored in frames of 256 32-bit words. A complete data frame is then transmitted to the EFB where it is sent to the Histogrammer. The Histogrammer uses an SRAM to receive Primitves from the host and the IBL DSP.

A detailed description of the IBL BOC module is given in the following, see Figure 8.8. The 160 Mb/s serial stream is translated into a 12-bit parallel stream and then 8b10b decoded. During this procedure each received 10 bit word is translated into its corresponding 8-bit word. This translation procedure is checked by several methods. First it is verified that the incoming data is correctly aligned with the IBL ROD clock. This is done as there is no direct clock signal from the FE-I4. The IBL ROD clock can be synchronised because the 8b10b encoded stream submits a continuous bit sequence. These bit sequences are either FE-I4 data words or

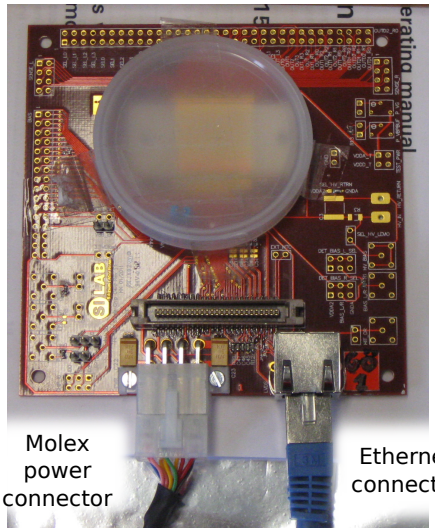

Figure 8.6: The FE-I4A SCC connected with a power supply via the Molex power connector. The Ethernet cable connects the SCC with the J6 connector of the IBL ROD.

Idle comma words. Thereby, the data which is sent with a 160 MHz clock is sampled with a 640 MHz clock. By sampling an incoming logical 1 or 0 several times the location of a stable clock cycle can be determined and used to adjust the phase of the clock at the receiver side [109]. If there is no corresponding 8-bit word for an incoming 10-bit word it cannot be translated and a decoder error occurs. Furthermore, a wrong running disparity results in an error, too. Finally, it is distinguished if the 8-bit word is a comma word, for example a data header or trailer or the Idle comma word. The FE-I4A data itself, which is embedded inside a header and trailer, is not a comma word. So far, data packages in which an error occurs are further sent to the FMTs and an advanced error handling method has still to be implemented.

After 160 Mb/s is decoded it is multiplexed such that it can be sent to the FMTs and to the Input FIFO simultaneously. This is done on a 12-bit bus using an 80 MHz clock. Each 12-bit bus is able to address four detector modules. Hence, to transmit the complete data of 32 FE-I4

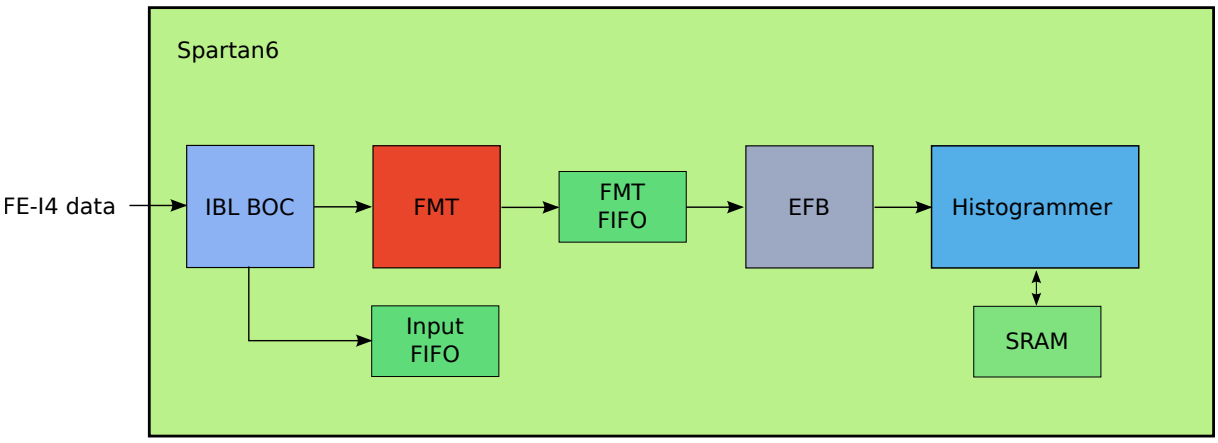

Figure 8.7: The firmware blocks of the Spartan6 FPGA which processes the received FE-I4A data. For test purposes it also contains the IBL BOC firmware modules.

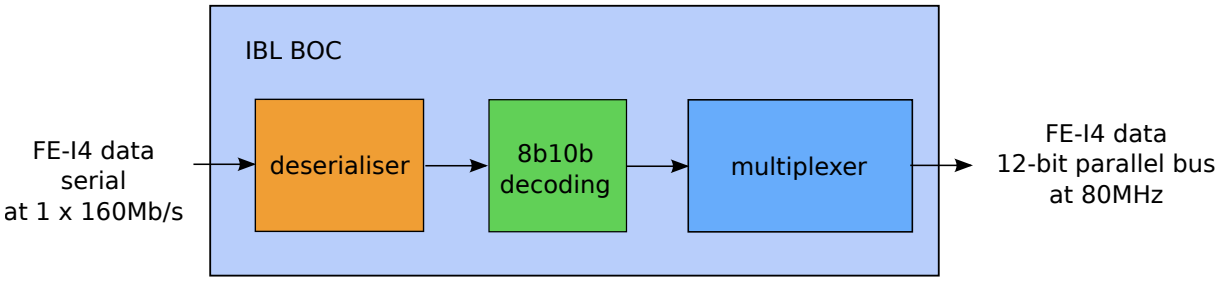

Figure 8.8: The IBL BOC data path handles the 8b10b encoded FE-I4 data such that it can be further processed by the IBL ROD firmware modules.

chips connected to one IBL ROD-BOC pair 4 x 12-bit links are used.

The clock on the IBL ROD is distributed by the Lattice clock manager. It receives a 40 MHz clock from either an on-board oscillator or from an attached IBL BOC and sends it together with a 100 MHz clock generated by the FPGA to the other IBL ROD components. The Spartan6 FPGA uses the 40 MHz clock to generate an 80 MHz clock which is fed into the FMT and the EFB. The faster 100 MHz clock is transmitted to the Histogrammer. Here, the FMT FIFO is also used to avoid a wrong phase relation between the EFB which uses an 80 MHz clock and the Histogrammer which uses a 100 MHz clock [111].

To load the FPGA firmware a JTAG USB Platform cable II, plugged to the J9 connector, and the FPGA development framework ISE[4] were used. The connector provides access to the two Spartan6 and the Virtex5 FPGAs. The ISE software is a GUI to develop and debug FPGA firmware. The FPGA code is programmed with an hardware description language VHDL[5] and synthesised into a bit file which can be programmed onto the FPGAs. Besides programming the devices, the JTAG connection permits access to the FPGAs while being in operation. This is done with a software part of ISE called “ChipScope”. Similar to a real oscilloscope it taps signals inside the FPGA. Several signals at the same time can be displayed and a trigger can be used to stop the signal at the appropriate trigger signal. This can be a single rising edge or a bit sequence. Hence, it permits to trigger on a data header within an 8b10b encoded stream which is not possible using a normal oscilloscope.

8.3.1 Pixel Register configuration

Similar to the already done Global Register test in the previous section the Pixel Register was tested. This was especially important as the limited DSP text buffer was not able to display the complete Pixel Register configuration. Parts of the stream generation were commented out or the number of rows and columns had to be reduced to see reasonable results during implementation and debugging. Because the buffer provided by ChipScope and used to store the bit stream data is not large enough, the Pixel Register configuration stream could only be tested with a conventional oscilloscope. The signal was tapped at the command pin of the J6 connector and hence no FE-I4A was attached during this test.

One command which transmits 672 1’s to each pixel latch of one DC is shown in the zoomed part of Figure 8.9. The large flat top is the 672-bit sequence. Before and after that several commands can be seen which configure individual Global Register entries or send other Slow Commands. These are used to select the correct DC to be written or enable a Global Pulse

[4]Xilinx Integrated Software Environment (ISE) 13.4 [110]
[5]Very High Speed Integrated Circuit Hardware Description Language

command which causes the Pixel Shift Register to write the bits into the pixel latches. The picture above the zoomed part shows the first ten write commands of the sequence. It can still be seen that the first ten write commands transmit the sequence "0010111001" to the individual pixel latches, respectively. It could be verified that the complete sequence is identical to the one seen in the DSP text buffer in which each single Pixel Register contains the complete sequence of "0010111001011". A Pixel Register write command which transmits only 0's to the pixel latches of one DC can be seen in Figure 8.10.

The FE-I4 Pixel Register implementation shows the expected bit stream to configure the module. During the tests which only comprise the DSP text buffer only parts of the bit stream could be verified. This was caused by the limited size of the DSP text buffer. With this test the complete Pixel Register bit stream could be observed for the first time. It was verified that the correct sequence of individual Global Register and Pixel Register write commands was sent as demanded by the FE-I4 specifications. Furthermore, the commands were compared bitwise with the partial bit sequences observed in the DSP text buffer. The correct agreement between both was verified and hence the DSP is able to configure a FE-I4 Pixel Register.

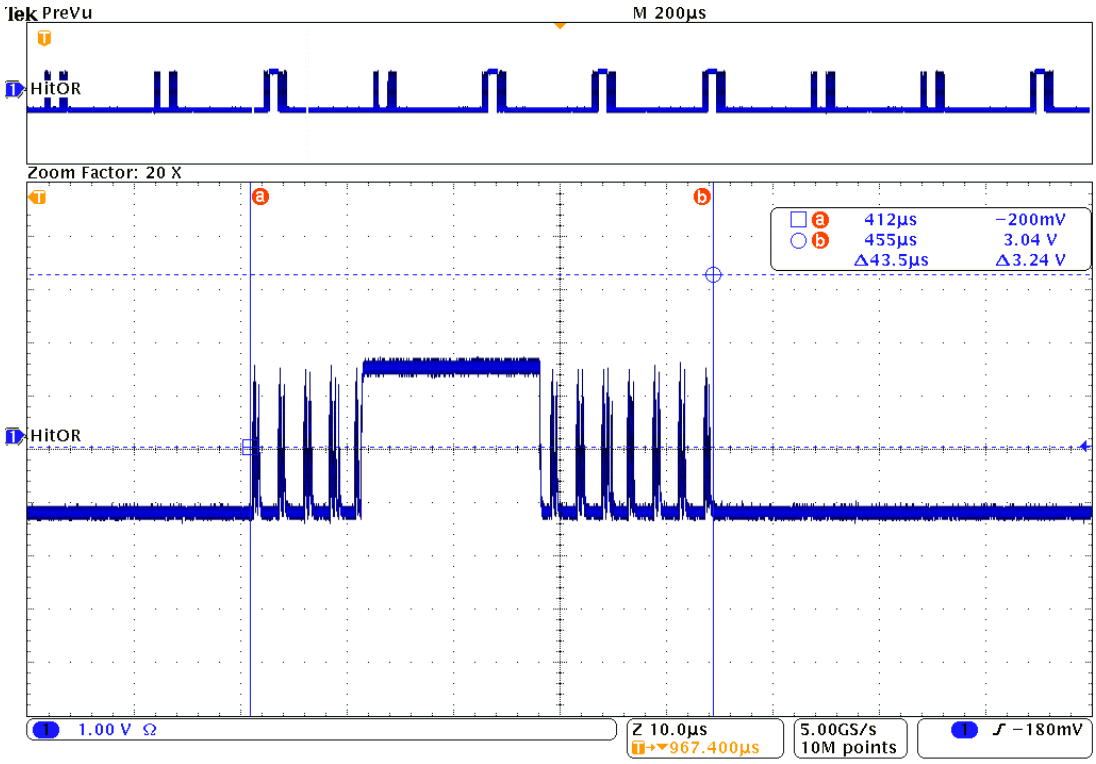

Figure 8.9: Zoomed part: A single Pixel Register write command which sends 1's to all 672 pixel latches of one DC. Before and after the flat top Slow Commands are sent to prepare the Global Register for DC writing or send a Global Pulse command such that the Pixel Shift Register transmits the bits into the pixel latches. Above the zoomed part: First ten write commands to configure a Pixel Register.

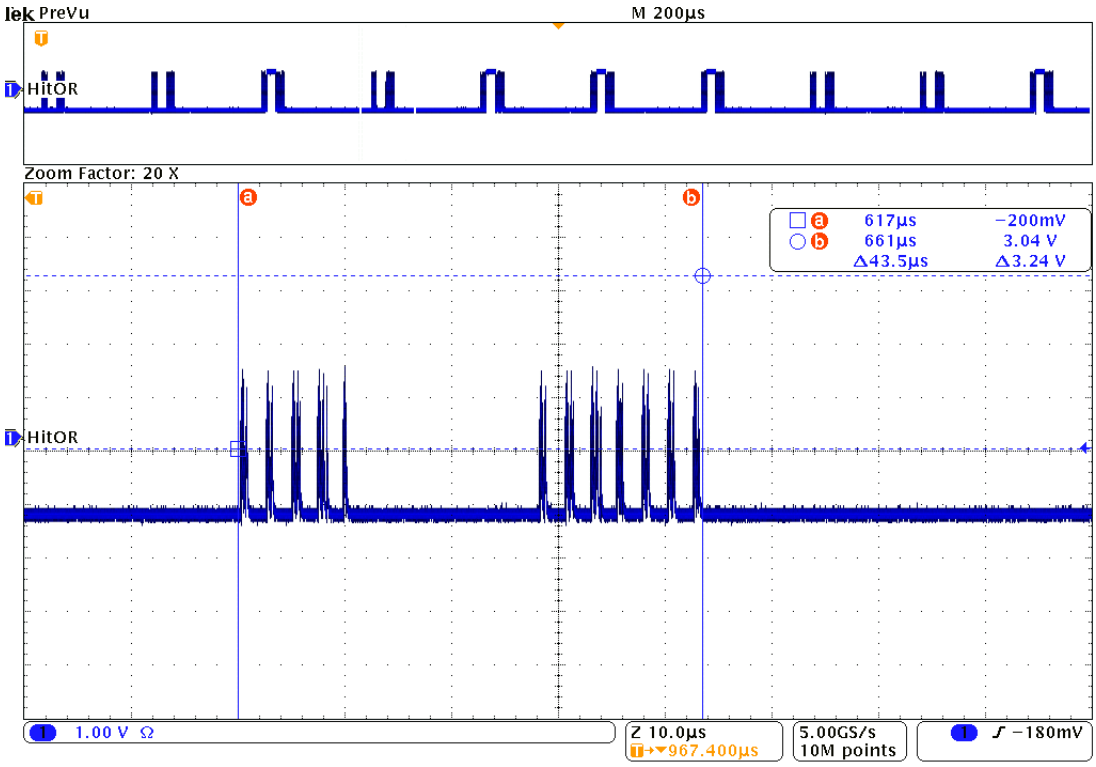

Figure 8.10: Zoomed part: A single Pixel Register write command which sends 0's to all 672 pixel latches of one DC. Before and after the gap Slow Commands are sent which are identical to the command described in Figure 8.9.

8.3.2 First FE-I4A configuration with an IBL ROD

After having tested the individual streams to configure the Global Register and the Pixel Register the complete stream was sent to the FE-I4A. As a chip has a higher current consumption when it is configured this is the first indication that configuration was correctly transmitted. The same FE-I4A SCC was attached to a USBPix readout system. Here, the FE-I4A was configured with *CalibrationConsole* using exactly the same configuration file. The currents of the unconfigured and configured FE-I4A of both readout systems were compared. As can be seen in Table 8.1 the FE-I4A showed similar values for the respective currents for both systems. The small difference of the currents in the unconfigured and configured state can be explained by an extra adaptor card which is used by the USBPix system. This adaptor card uses a slightly different power management to supply the FE-I4A SCC.

Due to the increased current it is proved that the IBL DSP code implementation is able to configure a FE-I4A chip. Furthermore, the current value of a configured FE-I4A is in good agreement with the current of a FE-I4A which is configured by a USBPix system.

8.3.3 Global Register readback

To verify the correctness of the Global Register configuration each single address can be read back. Normally a test function controlled by *CalibrationConsole* inside the DSP code was supposed to be used for that. In that case the received FE-I4 bit stream is directly written inside the Input FIFO which is then read out by the DSP. Due to the fact that the Input FIFO

Current (power supply display)	IBL ROD [mA]	USBPix [mA]	$\lvert\Delta I\rvert$ [mA]
$I_{D\_unconfigured}$	100	101	1
$I_{A\_unconfigured}$	47	79	32
$I_{D\_configured}$	117	121	4
$I_{A\_configured}$	316	333	17

Table 8.1: The measured currents of the FE-I4A SCC in an unconfigured and configured state attached to the IBL ROD or the USBPix system. With the IBL ROD system a digital voltage $U_D = 1.2$ V and an analogue voltage $U_A = 1.5$ V are directly applied to the SCC card. The USBPix System applies $U_D = U_A = 2$ V to an additional multi I/O card which generates $U_D = 1.2$ V and $U_A = 1.5$ V for the attached SCC card.

was not implemented into the IBL ROD firmware in time it was decided to test the readback with ChipScope. Unfortunately, also this was not possible due to timing errors inside the FPGA firmware which could not be solved at that time. An example of the received output with that error can be seen in Figure 8.11. A Global Register readback command was sent to the FE-I4 to receive the content of one address which is embedded in two 8-bit comma words: a Start-of-Frame (SOF) "0xFC" and an End-of-Frame (EOF) "0xBC". To get the signals the trigger was adjusted to detect a FE-I4 SOF word. The "rx_rod_data" line shows the decoded 8b10b stream. The "0x3C" at the beginning of that stream corresponds to the Idle comma word "00111100". An "rx_decoder_valid" signals a logical 1 each time a valid 8-bit encoded word is detected. The "rx_decoder_k_char" is high as long as a comma word is transmitted. To check if the incoming data is aligned with the IBL ROD clock the "rx_decoder_aligned" signal is shown. Furthermore, an "rx_decoder_dispErr" and "rx_decoder_decErr" signal indicate a disparity error and a decoder error during the 8b10b decoding process. Finally, a "data_from_fei4" and a "data_from_v5" signal are used to see the 10b decoded data from the FE-I4 and the commands transmitted by the Virtex5, respectively. It can be seen that with the beginning of the "0x1C" rx_rod_data signal a disparity and a decoder error occur. As the reason for the faulty signal was not clear another method to test the Global Register readback was used. Thereby, a possible error which results from a wrong configuration should be excluded or revealed.

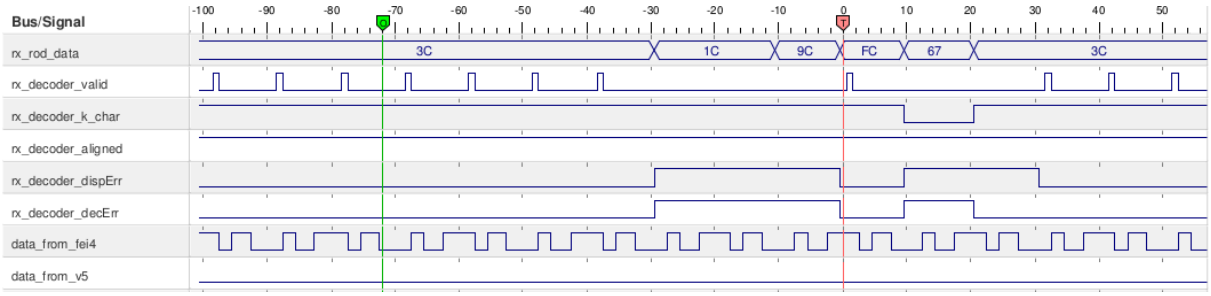

Figure 8.11: A faulty Global Register readback signal was detected in the first stages of the IBL ROD firmware development.

The FE-I4 data line was tapped with a conventional oscilloscope before it was linked to the J6 connector of the IBL ROD to check if the received stream is as expected. Idle comma words are transmitted on the data link in case of a configured FE-I4. The result is shown in Figure 8.12. A zoomed in picture can be seen in Figure 8.13. Although the quality of the signal is not very

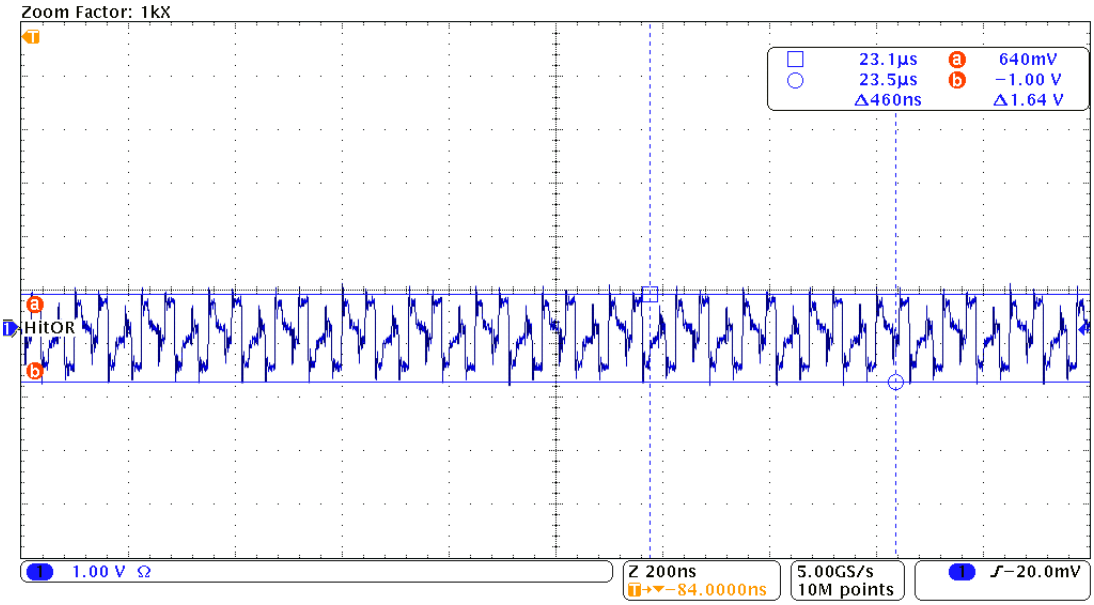

Figure 8.12: The 10b encoded data stream of the FE-I4. The signal was measured with an oscilloscope at the output of the Ethernet cable.

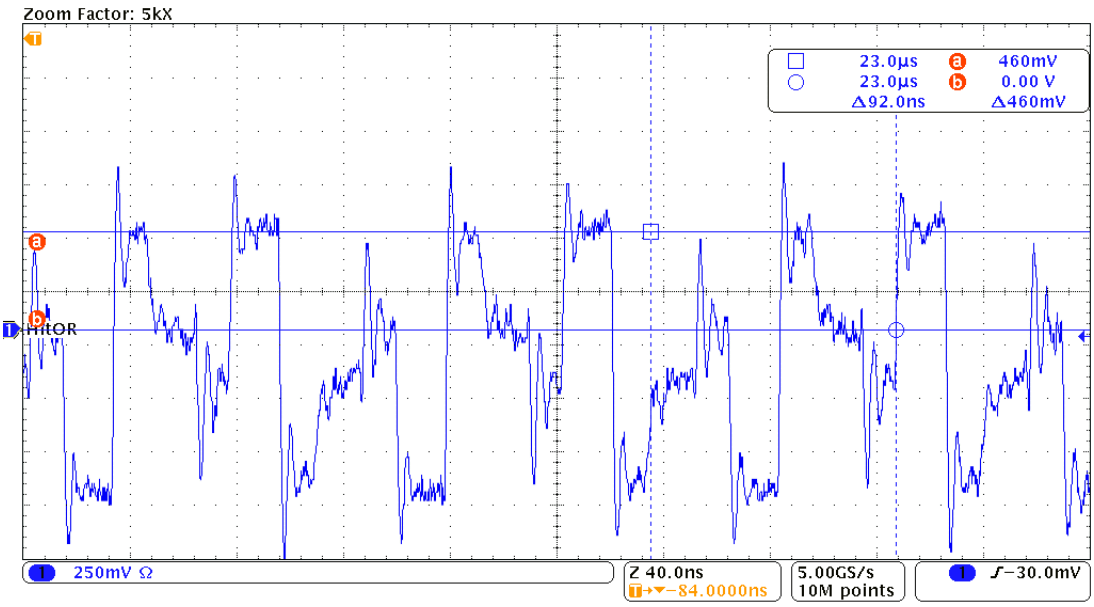

Figure 8.13: A zoomed in picture of the encoded data stream. It shows the alternating 10b encoded words of the Idle comma word: "1100000110"and its inverse "0011111001".

good this further indicates a successful configuration of the FE-I4. If the chip is not configured no 8b10b Idle comma words are submitted.

In the next step it was checked if the transmitted command stream is aligned with the clock sent to the FE-I4, see Figure 8.14. The green coloured signal shows the command which sets the FE into configuration mode. It can be seen that the quality is not very good although it is well aligned to the 40 MHz clock which is the blue coloured signal.

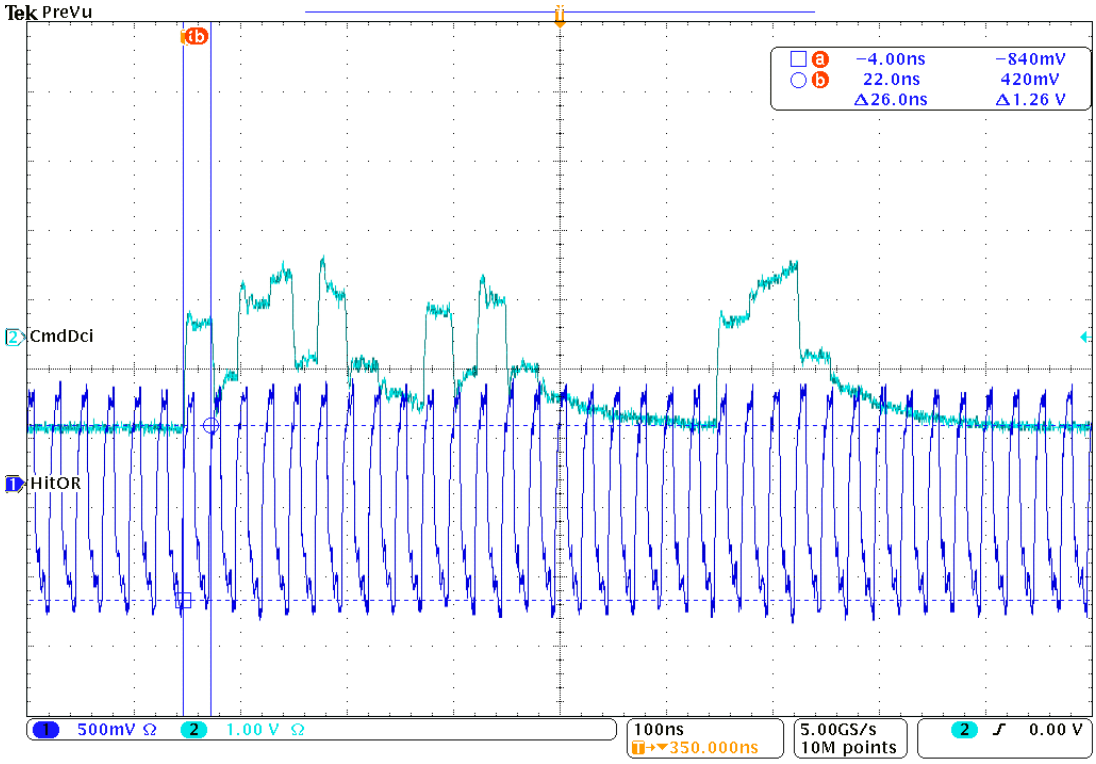

Figure 8.14: A Slow Command which sets the FE-I4 in configuration mode (green coloured signal) and the 40 MHz clock transmitted from the IBL ROD to the FE-I4A (blue coloured signal).

The successful configuration of some Global Register values can directly be proved as they change the behaviour of the out-going data stream. Hence, the 8b10b coding was disabled by reconfiguring the appropriate register address and no Idle comma words were seen on the oscilloscope. Furthermore, the data output block which sends the data off the FE-I4 can be reconfigured. It was setup such that it sends out the clock which is used to transmit the pixel data instead of the pixel data itself. Adjusting the Global Register accordingly a 160 MHz clock could be measured at the data out link of the FE-I4. Furthermore, the data can be sent with a 40 MHz clock which was also measured after sending the appropriate Global Register configuration. In addition, the "Empty Record" register was used. The bit sequence of that register entry is sent in case 8b10b encoding is disabled and no data is transmitted. The default value of only zeros was replaced by an arbitrary bit sequence which was also measured with the oscilloscope. These examples show that the general Global Register configuration and the readback of certain values are reliable.

After the provided FPGA firmware was improved no errors occurred in the sampling of the ChipScope signal and the readback test was also verified by this method. At first, Global Register address two was configured with a test value 0xAAAA and then read back. The result can be seen in Figure 8.15. At the beginning of the rx_rod_data line the last Idle comma word is shown. The trigger is marked with a red line and applies as soon as an SOF is received. After the SOF a so called "address record" with the bit sequence 0xEA and the 16-bit Global Register address 0x0002 are shown. The following "value record" with the bit sequence 0xEC indicates the beginning of the 16-bit data package which is filled with the Global Register bits of address

two. It can further be seen that each start of an 8-bit word is detected by the rx_decoder_valid signal. The rx_decoder_k_char is logically high for all comma words and logically low for the different records and data values. Furthermore, no disparity and decoder errors are seen.

The next example in Figure 8.16 shows the configuration of the Global Register address ten. After the address record the bit sequence 0x000A indicates the correct address. The 16-bit register contains two register values which are called "FdacVbn" with a default value of 50 = 0x110010 and "Amp2Vbpff" with a default value of 13 = 0x00001101. Both values have to be reversed according to the specifications for this register and hence the resulting 16-bit stream is 01001100 10110000 = 0x4CB0. The read back stream finishes with an EOF with 0xBC.

It can be seen, that the IBL ROD is able to not only transmit command streams but also handle data sent from the FE-I4 and that the bit streams can be correctly tapped with ChipScope. Hence, a firmware is provided which enables the testing of the Global Register readback by tapping the received streams in the IBL ROD.

Finally, a trigger stream was sent to the FE-I4. 0xBC and 0xFC indicate the end and the start of a data frame. The data header with the bit sequence 0xE9 signalises the start of incoming pixel hit data. As no physical data has been taken with the FE-I4 chip the content of the different values is not meaningful. However, the specific FE-I4 SOF and EOF words as well as the data header were detected. It could be shown that the IBL DSP is able to sent trigger streams to the FE-I4 to receive pixel data.

With a further improved IBL ROD firmware the Input FIFO could be used and the data from the FE-I4 was also received and read out with the DSP. This is the first step towards a Register Test. Here, the Input FIFO is used by the IBL DSP to receive the read back values of all Global and Pixel Registers. The received data is compared with the configuration stored in the IBL DSP memory and the writing for each individual register can be checked.

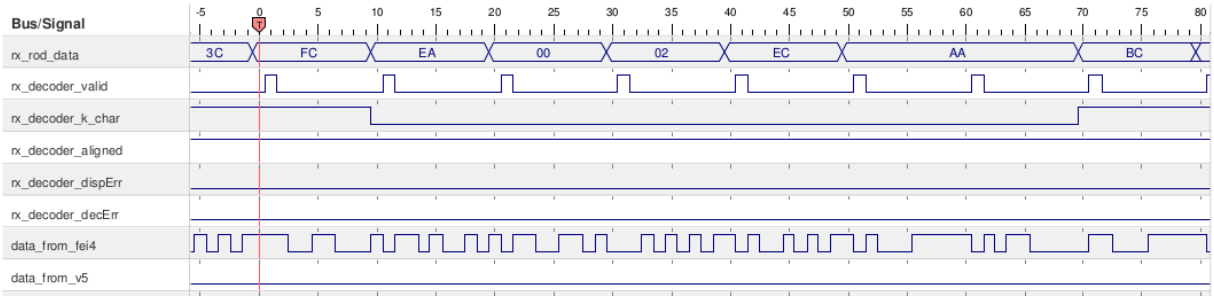

Figure 8.15: A readback test of the Global Register address two which was configured with a test word 0xAAAA.

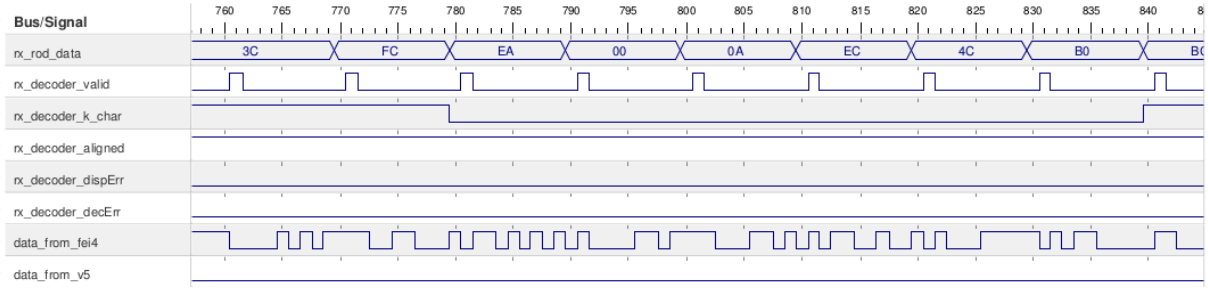

Figure 8.16: A successful readback of Global Register address ten. The trigger line is not displayed here.

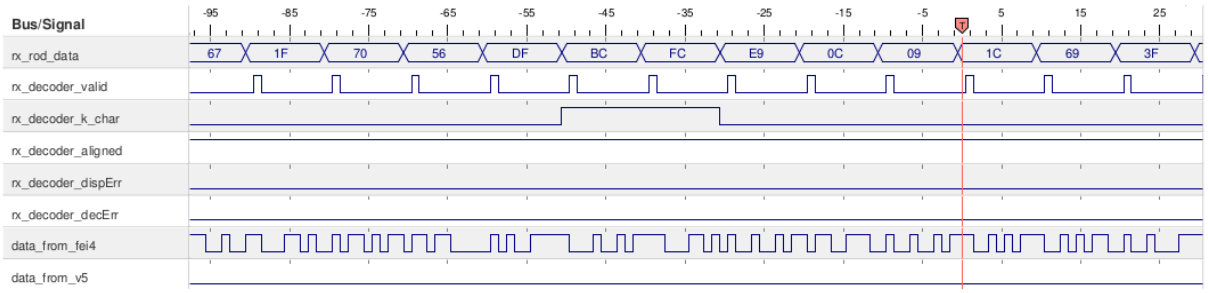

Figure 8.17: The end and start of a FE-I4 pixel hit data frame after a L1 trigger was sent.

8.3.4 Scan implementation issues

A successful scan procedure completes a first working IBL ROD test chain in which a FE-I4 can be configured and scanned. The first scan to be implemented is a Threshold Scan as it uses all processing loops described in Chapter 7.2.2.

Because a full functioning IBL ROD environment was not given the scan could not be implemented. However, it was started to provide a possible implementation for a scan procedure for the IBL ROD. Furthermore, necessary communication requests for a full scan procedure between the IBL DSP and its external devices were identified.

Although the communication to the Histogrammer was very rudimentary a first communication to its SRAM was established. The complete SRAM contains 512 32-bit words. All words were successfully written and read with a test bit stream. Also first changes to the intended scan implementation were done but were not finished because no full implemented IBL ROD firmware was provided.

9 Conclusion and outlook

Until 2022 the luminosity of the LHC is upgraded in three phases. The increased particle rate requires new detector modules and an improved data acquisition chain to cope with the higher data throughput. Hence, an enhancement of the ATLAS Pixel Detector is necessary which is realised by the IBL Upgrade Project. An advanced IBL ROD is developed to be able to read out the data of the new FE-I4 readout chip. One part of the IBL ROD is the DSP which is used to communicate with the FE-I4 when being in calibration mode. The configuration of the chip and the control of scan processes are the main functionalities of the DSP.

In this thesis the integration of the IBL ROD into the existing data acquisition software TDAQ/IBLDAQ is described. In addition, hardware tests on the first IBL ROD prototype proved a successful communication of the DSP with its external memory devices. Implementations have been done to provide an IBL DSP code to carry out first tests with an IBL ROD chain connected to a FE-I4 chip. It could be shown that a FE-I4 chip was integrated into the new readout chain for IBL. Moreover, a successful FE-I4 configuration was demonstrated. In addition, a communication was established to be able to read out the IBL ROD Input FIFO for debugging purposes and to read and write the Histogrammer SRAM to send and receive command Primitives.

Although a first version of the IBL DSP code is provided the development is not completed. One main issue for a first fully functioning IBL DSP code is the implementation of a scan procedure. Until the next LHC shutdown in 2013 the development of the IBL readout components has to be finished and a working IBL readout chain has to be provided to improve the physics performance for the next LHC run period.

Until then an IBL System test is necessary to verify the communication between all components of the IBL readout chain. This includes an IBL ROD-BOC pair with an optical connection to 32 FE-I4 chips as well as the cooling of the modules. Basic tests like a scan procedure which includes all FE chips or the verification of the electrical connections can then be carried out.

Finally, an IBL testbeam is foreseen to test the on- and off-detector parts in data taking mode and demonstrate that the IBL is ready to be installed into the Pixel Detector.

Anhang

A Acronyms

ATCA	Advanced Telecommunications Computing Architecture
ATLAS	A Toroidal LHC Apparatus
BCID	Bunch Crossing Identification
BCR	Bunch Counter Reset
BOC	Back Of Crate Card
CCS	Code Composer Studio
CMS	Compact Muon Spectrometer
CSC	Cathode Strip Chamber
DAC	Digital to analog converter
DC	Double Column
DCS	Detector Control System
DDR	Double Data Rate (RAM)
DRX	Data Reveicer IC
DORIC	Digital Opto-Receiver IC
DSP	Digital Signal Processor
EMIF	External Memory Interface
FCAL	Forward Calorimeter
FE	Front End
FPGA	Field Programmable Gate Array
FTK	Fast Track Trigger
GbE	Gigabit Ethernet
GDAC	Global DAC
HOLA	High Speed Optical Link for ATLAS
HPI	Host Port Interface
IBL	Insertable B-Layer
IC	Integrated Circuit
ID	Inner Detector
IP	Internet Protocol
ISE	Integrated Software Environment

ITk	Inner Tracker
JTAG	Joint Test Action Group
L1ID	Level-1 Identification
LAr	Liquid Argon calorimeter
LED	Light Emitting Diode
LDC	Local Decoupling Capacitor
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LSB	Last Significant Bit
LVDS	Low Voltage Differential Signal
Mb	Megabit
MB	Megabyte
McBSP	Multichannel Buffered Serial Port
MCC	Module Control Chip
MDSP	Master Dgital Signal Processor
MDT	Monitored Drift Tube
MSB	Most Significant Bit
PCB	Printed Circuit Board
PiN	Positive intrinsic Negative (diode)
PPC	PowerPC
PRM	Program Reset Manager
RCF	ROD Controller FPGA
ROB	Read Out Buffer
ROBIN	Read Out Buffer Input Stage
ROD	Read Out Driver
ROS	Read Out Subsystem
RPC	Resistive Plate Chamber
RRIF	ROD Register Interface
SBC	Single Board Computer
SCC	Single Chip Card
SCT	Silicon Strip Detector
SDRAM	Synchronous Dynamic Random Access Memory
SDSP	Slave Digital Signal Processor
SEU	Single Event Upset

SM	Standard Model
SSRAM	Synchronous Static Random Access Memory
TDAC	Trimming DAC
TDAQ	Trigger and Data Aquisition
TGC	Thin Gap Chamber
TIM	TTC Interface Module
TOT	Time over Threshold
TRT	Transition Radiation Tracker
TTC	Timing, Trigger and Control
VCSEL	Vertical Cavity Surface Emitting Laser
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VME	Versa Module Eurocard

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List of Figures

List of Tables

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