Assembly and Electrical Tests of the First Full-size Forward Module for the ATLAS ITk Strip Detector

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Abstract

The ATLAS experiment will replace the existing Inner Detector by an all-silicon detector named the Inner Tracker (ITk) for the High Luminosity LHC upgrades. In the outer region of the ITk is the strip detector, which consists of a four layer barrel and six discs to each side of the barrel, with silicon-strip modules as basic units. Each module is composed of a sensor and one or more flex circuits that hold the read-out electronics. In the experiment, the modules are mounted on support structures with integrated power and cooling. The modules are designed with geometries that accommodate the central (barrel) and forward (end-cap) regions, with rectangular sensors in the barrels and wedge shaped sensors in the end-caps. The strips lengths and pitch sizes vary according to the occupancy of the region.

In this contribution, we present the construction and results of the electrical tests of the first full-size module of the innermost forward region, named *Ring 0* in the ATLAS ITk strip detector nomenclature. This module uses a sensor with stereo annulus geometry, having four segments of strips of different lengths and pitch. The two innermost strips segments are read out through eight chips, for a total of 2048 strips, while the two outermost segments are read out through nine chips, for a total of 2304 strips. We introduce the assembly procedure that lead to the construction of the module as well as the testing during the intermediate

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steps.

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1. Introduction

In the context of the High Luminosity LHC upgrade, the ATLAS tracker [1] will have to cope with much higher radiation and particle density, which forces changes in the whole tracker. The future Inner Tracker (ITk) will be an all-silicon detector, with a modular design that integrates cooling and electronics, and provides mechanical support [2].

Modules are the smallest unit of the detector, made from an n-in-p silicon strip sensor onto which read-out hybrids are glued and wire-bonded. The modules are then glued onto the structures that integrate cooling, electronics and support. These are named *staves* in the barrel and *petals* in the end-caps. This contribution is centred on the latter, shown in Figure 1 [2].

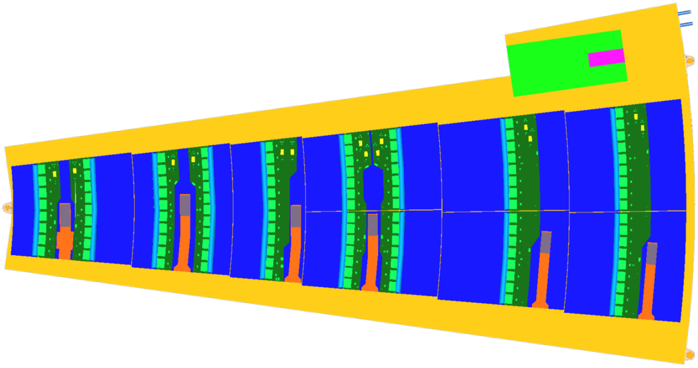

Fig. 1: Sketch of a *petal*, showing all six rings from left to right.

Petals are made of modules laid out in *Rings*, with the innermost ring named *Ring 0* (R0), increasing in number with radius for a total of six rings. The first module, using a full size sensor fabricated in a six-inch wafer, has been produced and tested. The sensors have a *stereo annulus* shape [3] and the read-out circuits, called hybrids, hold the read-out chips that are connected to the strips. The *Ring 0* sensor has four strips segments, with the two innermost comprising of 1024 read-out strips and the two outermost segments having 1152 strips. The strip pitch varies along the length of the strips, between 73.5 and 84 micrometres. The sensor is about 105 millimetres long and between 77 and 100 millimetres wide. The sensor has an active thickness of about 300 micrometres.

The following sections describe the process used to build and test this first *Ring 0* module.

2. Hybrid Building

The read-out hybrids are flex circuit boards made in polyimide with multiple copper layers for the electrical connections. They hold dedicated read-out ASIC (Application Specific Integrated Circuit) chips, named ABC130 [4]. A Hybrid

Controller Chip, named HCC130 [2], is used to transmit the data from the ABC130 chips to outside the hybrid. Both chips are designed in a 130 nm CMOS process.

In the hybrid assembly process, the ASICs were glued onto the flex board using ultra-violet cured glue for fast attachment, dispensed with a programmable robot. Special tooling is used for precise positioning of the chips on the boards, as well as for control of the glue thickness. The chips were held by vacuum on the pick-up tools and the hybrid flex circuits were held by vacuum on a custom built and precisely machined jig. The curing of the glue was done by illuminating with an ultra-violet LED for 120 seconds.

After the chips were attached onto the board, the electrical connections of the chips to the hybrid PCB were performed by automated wire-bonding.

Once assembled and wire-bonded, the hybrids were electrically tested, to verify the functionality of all the read-out chips by reading out their registers and measuring the voltages on the hybrids and at the chips linear regulators. Their analogue performance was also assessed in further electrical tests. Noise measurements and calibrations were run to assess the performance of the chips, and the values were compared before and after assembly of the full module. Details about the tests performed on the constructed hybrids and module presented in this paper are given in Section 4.2.

3. Module Building

The tested hybrids were glued on the sensor using an epoxy glue that is cured for at least ten hours at room temperature. The sensor was held by vacuum on another custom built precision jig. The same tools used to glue the ASICs were used to pick-up the hybrids and hold them during the glue curing process.

After the glue was fully cured, the sensor electrical characteristics were measured on the probe station again, prior to wire-bonding of all the strips to the front-end channels of the chips. The measurements performed on the sensor are presented in Section 4.1.

Figure 2 shows a picture of the assembled module. The front-end channels were bonded using four rows of bonds with different lengths and loop heights. The use of four rows poses extra difficulty when assessing the correctness of the bonding process. No bonds failed in this four row bonding and there were no short circuits between bonds.

In a final step, a power-board was glued onto the sensor and connected to the hybrids. This power-board includes a DC-DC converter [5] which steps down an input voltage between 6 and 12 V to 1.5 V. By using DC-DC conversion, the power losses on the cables are reduced, resulting in a reduction of the material inside the tracker and a more stable operation.

4. Electrical Tests

4.1. Sensor Testing

The sensors used for module building are measured during the whole assembly process. Current and capacitance as a function of the bias voltage (I/V and C/V) of the bare sensor are measured on a probe station. The depletion voltage is extracted from the C/V curve and is found to be at around 300 V [6].

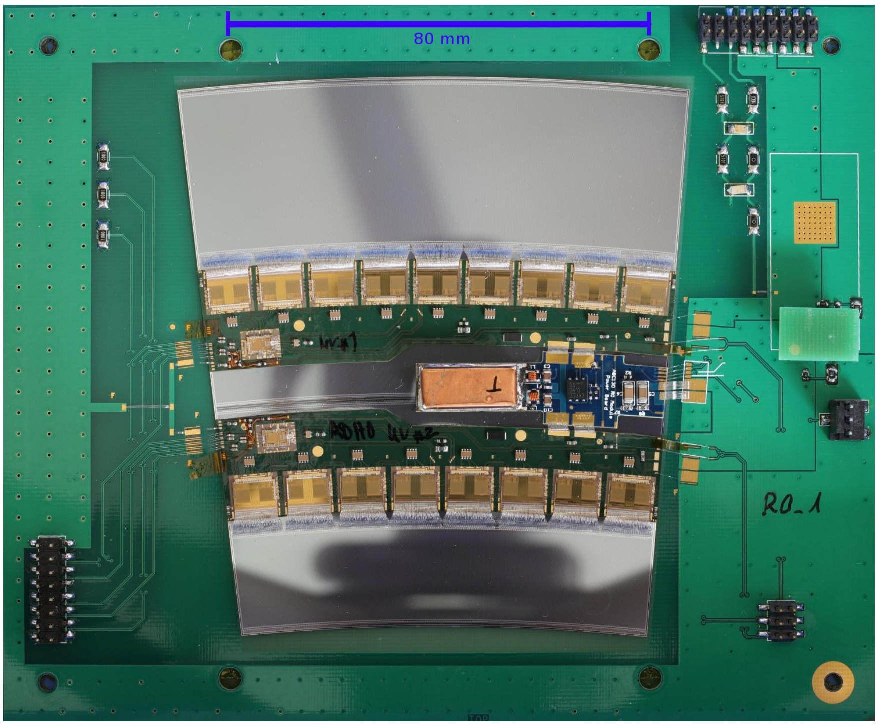

Fig. 2: The first completely assembled R0 module on a test-frame, showing the sensor, both hybrids and the power-board. The bottom hybrid is called R0H0 and the top hybrid is called R0H1.

After the hybrid has been glued onto the sensor, another I/V curve is taken in order to check for sensor degradation due to the gluing process.

Last, a final I/V is taken after all the strips are wire-bonded to the read-out front-end channels on the ASICs. Figure 3 shows the results of the I/V curves taken. It exhibits a slight worsening of the behaviour after gluing and wire-bonding, which points at possible signs of mechanical stress on the sensor.

4.2. Module Testing

Digital and analogue tests were performed on the fully assembled module. The digital tests involve communicating with the read-out chips and configuring them.

For all tests, the module is powered in two ways: with a direct connection to the power supply which has to provide 1.5 V to the hybrids, or with a power-board, fed with 11 V from the power supply.

The analogue tests performed on the fully assembled module include the following:

- *Strobe Delay*, consisting of varying the phase of the charge injection relative to the trigger signal to the chips. This test is used to find the timing at which all injected pulses are detected at low thresholds, and is essential for the following two tests to work properly.

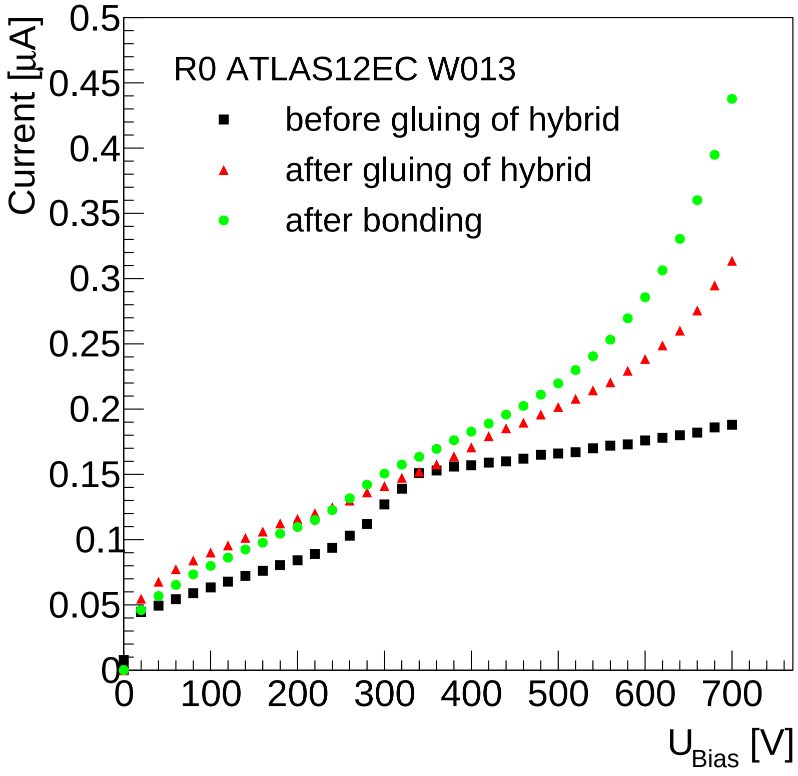

Fig. 3: I/V curves of the sensor used for the first R0 module during the whole building process: before and after gluing, and after wire-bonding. All measurements were performed on the same probe station.

- *Trim Range*, in which the trims in the chips are optimised in order to minimise the variations in the response among channels. It consists of a series of threshold scans with a fixed injected charge, varying the trim settings of the chips, in order to find the ones that result in a homogeneous response. The result of this test is either a failure due to untrimmable channels or chips, or the trim settings for each channel.

- *Response Curve*, which consists of ten threshold scans with varying injected charges. The output noise of the front-end is extracted from the variance of the occupancy for each value of injected charge, and the median point, or V_{t50}, is extracted and used to determine the gain in mV/fC from an exponential fit with all ten points. Using the gain and the output noise, the input noise is calculated in electrons Equivalent Noise Charge (e^{-}ENC).

- *Noise Occupancy*, a high statistics threshold scan is performed without injected charge, in order to determine the noise occupancy of each channel as a function of the threshold.

The *Response Curve* test was performed at different sensor bias voltages, scanning from under-depletion up to over-depletion of the bulk. Figure 4 shows the results for this bias voltage scan, exhibiting the expected behaviour of noise reduction until the sensor is fully depleted.

It also shows the noise values of each strip segment, which are different due to the varying lengths of the segments: 19, 24, 29 and 32 millimetres. Noise is dependent on other parameters, such as temperature, front-end tuning and total capacitance. The capacitance is dependent on the strip length as well as other added capacitance such as a metallic plane over the sensor. The areas where a hybrid is glued onto the sensor have an extra capacitance, which drives the noise up, and this is observed for the second and third segments. These results correspond to the module prior to the attachment of the power-board.

The comparison between the bare hybrids and the fully assembled module without power board shows a noise increase of around 180 electrons for the first (shortest) strip segment, 272 for the second segment, 350 for the third segment, and 354 for the fourth (longest) segment. As mentioned above, the segments for which there is a hybrid glued onto the sensor, exhibit a larger noise increase due to the extra capacitance. This results in the third segment having a noise increase close to the fourth segment, despite the difference in strip length.

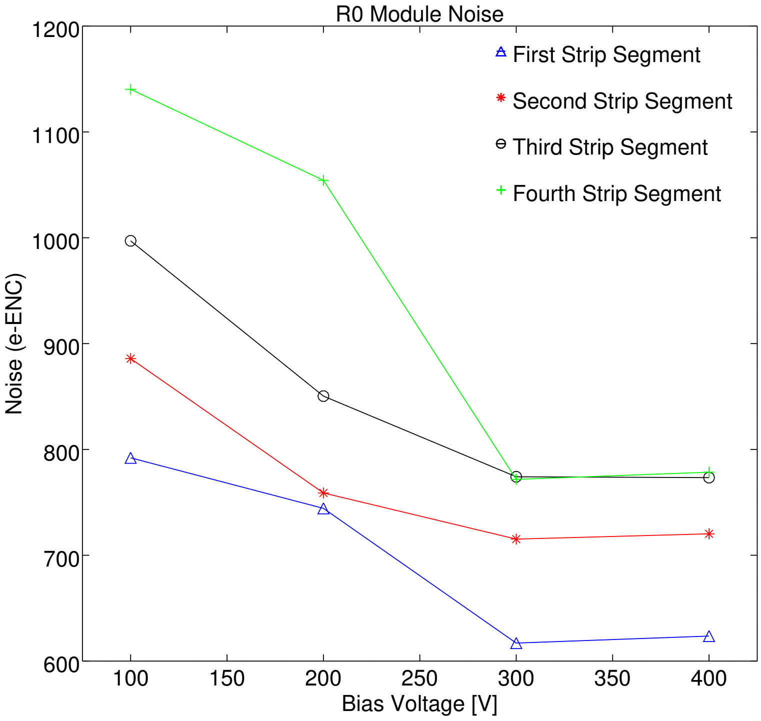

Fig. 4: Input noise for different bias voltages.

The noise was measured before and after attaching and connecting the power-board. Figure 5 shows the comparison of the noise before and after attaching the power-board on the module. As shown in Figure 6, only the four chips on the right of R0H0 and the strips running underneath the power-board, corresponding to the second strip segment, are shown in this plot. *Chip 16* is the first chip from the right and *Chip 19* is the fourth. Chip to chip variations in the noise without the power-board are due to gain differences amongst chips, which are caused by the front-end tuning.

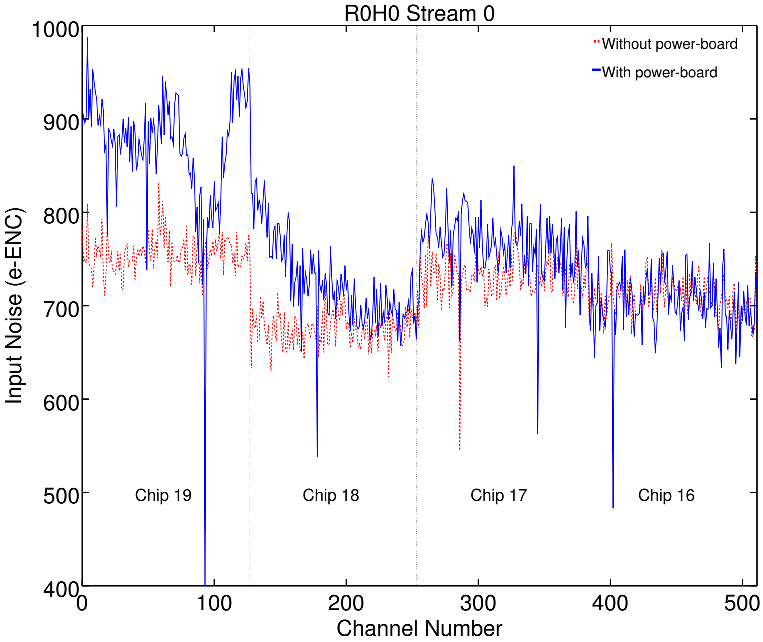

Fig. 5: Input noise measurements with (solid red line) and without (dashed blue line) the power-board, for the four rightmost chips of the R0H0 hybrid, strips underneath the power-board.

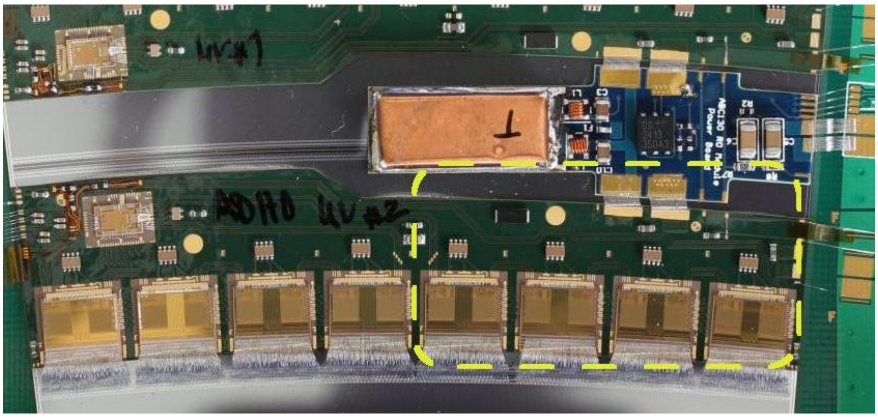

Fig. 6: Area of the module exhibiting the noise increase due to the power-board.

This extra noise is associated with a leakage of the magnetic field in the inductance used to store the energy for the DC-DC conversion. This noise excess can be addressed by improving the shielding of the coil.

Even with this additional noise, the module fulfils the requirement of less than 1000 electrons which would result in a signal to noise ratio larger than 10 after irradiation at the full HL-LHC fluence [2].

For the noise occupancy tests, results show values well below the requirement of less than 10^{-3} channel noise occupancy at a threshold that results in detection efficiency greater than 99%.

5. Conclusions

The first full-size module using a *stereo annulus* shape sensor, fabricated in a six-inch wafer for the ATLAS ITk Strips Upgrade has been successfully built and tested. This module is one of the components of the forward region, covering the innermost ring.

This contribution shows that the building process is under control, with precision attachment of the read-out chips, gluing of the hybrids onto the sensor and the wire-bonding step.

All performance parameters extracted from the electrical tests are consistent with the sensor characteristics and comply with the specified values for the upgrade of the ATLAS tracker.

The addition of the power-board is still under study, with a slight noise increase due to leakage of the magnetic field generated by the coil that is part of the DC-DC converter.

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References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 (2008) S08003.

[2] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, CERN-LHCC-2017-005. April 2017.

[3] C. Lacasta et al., *Design of the first full size ATLAS ITk Strip sensor for the endcap region*, HSTD11&SOIPIX. December 2017.

[4] J. Kaplon and M. Noy, *Front end electronics for SLHC semiconductor trackers in CMOS 90 nm and 130-nm processes*, IEEE Trans.Nucl.Sci. 59 (2012) 1611–1620.

[5] F. Faccio et al., *FEAST2: A Radiation and Magnetic Field Tolerant Point-of-Load Buck DC/DC Converter*, 2014 IEEE Radiation Effects Data Workshop (REDW).

[6] R. Hunter et al., *First bulk and surface results for the ATLAS ITk Strip stereo annulus sensors*, HSTD11&SOIPIX. December 2017.