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ATLAS ITk Short-Strip Stave Prototype Module with Integrated DCDC Powering and Control

Ashley Greenall[1], on behalf of the ATLAS Collaboration
University of Liverpool (UK)
E-mail: ashley@liv.ac.uk

During the Phase II upgrade, the ATLAS detector at the LHC will be upgraded with a new Inner Tracker (ITk) detector. The ITk prototype barrel module design has adopted an integrated low mass assembly featuring single-sided flexible circuits, with readout ASICs, glued to the silicon strip sensor. Further integration has been achieved by the attachment of module DCDC powering, a HV sensor biasing switch and autonomous monitoring and control to the sensor. This low mass integrated module approach benefits further in a reduced width stave structure to which the modules are attached. The results of preliminary electrical tests of such an integrated module are presented.

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[1]Speaker

1. Introduction

A new all silicon tracking detector is being designed to replace the current Semiconductor Tracker (SCT) within the ATLAS detector at CERN [1], for operation at the High Luminosity LHC (HL-LHC) in 2026. The HL-LHC will expose the replacement detector to a harsher radiation environment and increased detector occupancy, requiring increased radiation hardness of the semiconductor devices and data readout at up to 1 MHz trigger rate.

The Inner Tracker (ITk) is composed of an inner pixel and outer strip detector; the pixel system comprised of 5 barrel and 4 endcap ring layers whilst the strip system is made up of 4 barrel layers and 6 disks in the endcap, shown schematically in Figure 1. The strip barrel layers being segmented into two layers of short-strip and two layers of long-strip modules, resulting in ~3800 short-strip and ~7200 long-strip modules.

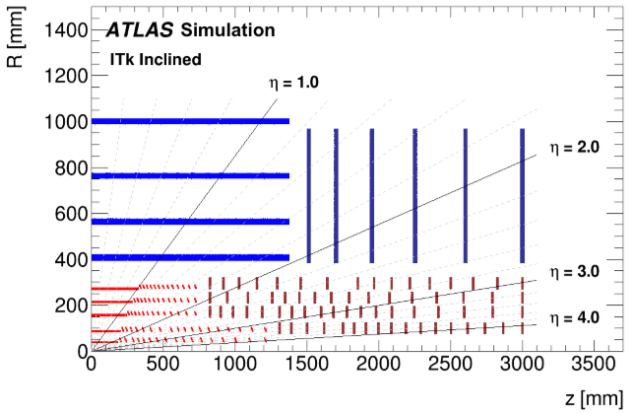

Figure 1. Schematic layout of the ATLAS ITk showing the strip detector in blue and pixel detector in red.

2. Prototype Barrel Strip Detector Module and its Components

Barrel modules come in 2 flavours, referred to as short-strip and long-strip types. The difference arising due to their sensor geometries having either 4 rows of short strips of 24.10 mm length in the z-direction or 2 rows of long strips of 48.20 mm; with long-strip modules being assigned to the lower occupancy larger radii region (layers L2 and L3) and short-strips to the lower radii (layers L0 and L1). Each module having a total active sensor area of ~96.6 × 96.6 mm^2. Attached to the sensor are low mass flexible polyimide circuits (referred to as hybrids) which retain both the readout and control ASICs (Application Specific Integrated Circuit), ten ABC130 and one HCC respectively; one hybrid for long-strip and two for short-strip modules. Furthermore, there is also attached a single auxiliary power board, this comes with a custom Point of Load DC-DC buck converter [2], a sensor bias High Voltage switch [3] and a custom control and monitoring ASIC (AMAC, Autonomous Monitoring and Control).

All circuits are attached directly to the silicon sensor using electronics grade epoxy, this eliminates the requirement for a substrate between the respective circuits and the sensor and thus saving on material. This topology takes advantage of the heat path through the large cross-

sectional area of the sensor to the embedded cooling within the carbon fibre stave support structure to which the modules are further glued to. An exploded view of a short-strip module is shown in Figure 2 alongside a photograph of a fully assembled prototype module with sensor, two hybrids with ABC130 readout ASICs and a power board between the hybrids.

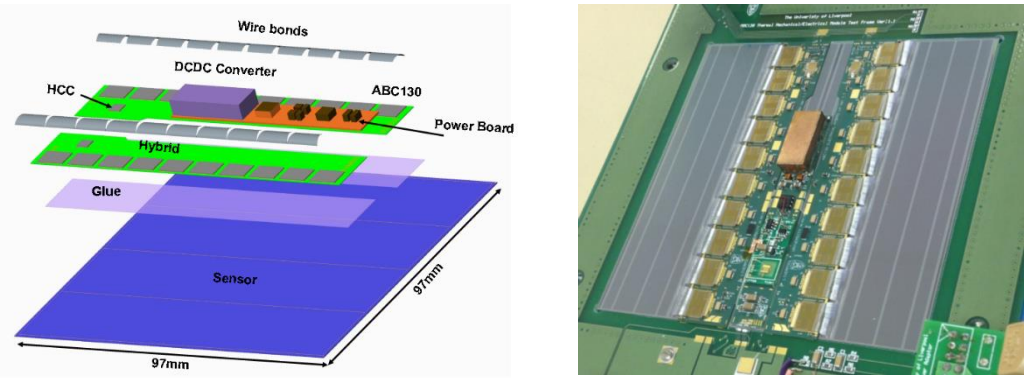

Figure 2. Exploded view of a short-strip module, shown left. Shown right is a photograph of a fully assembled prototype module.

2.1 The Readout Hybrid

The hybrid provides not only mechanical support for the attachment of the ten ABC130 readout ASICs and single HCC control ASIC but also the routing of the electrical services and their physical connection to the ASICs via 25 µm diameter Al wire-bonds. The hybrid is manufactured as a polyimide flexible circuit with three copper layers using 50 µm thickness dielectrics, resulting in a total build thickness of ~275 µm. The circuit stack-up has the bottom ground layer acting as a pseudo shield to prevent digital signalling coupling into the sensitive silicon sensor; to maintain the integrity of this shield layer blind vias are used throughout to ensure its non-perforation. All fast differential signalling is impedance controlled, utilising differential strip-line topology for signalling adjacent to the sensitive analogue front-end and differential micro-strip for the digital signalling that is away from the front-end. Finally, a single power and ground domain has been adopted to service all ASICs on the hybrid, the ASICs having Low Drop Out (LDO) voltage regulators integrated within them to regulate the higher 1.5 V hybrid voltage down to the 1.2 V core voltage required by their analogue and digital circuitry. Figure 3 shows the hybrid stack-up and geometry.

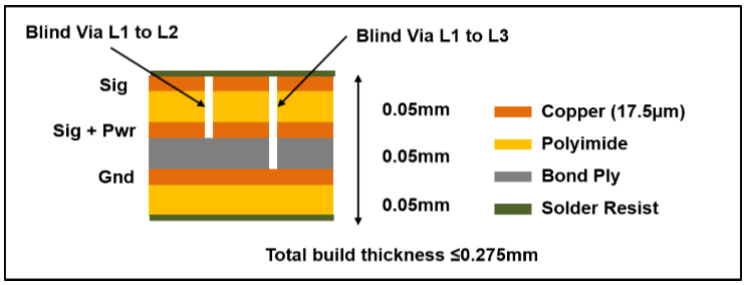

Figure 3. Hybrid Flex circuit stack up.

2. The Power Board

The constrained geometry of barrel modules necessities module powering, HV sensor switching and control to be attached to the silicon sensor, as per the readout hybrids. This has been realised as an auxiliary power board which comes with a custom Point of Load DC-DC buck converter, switchable sensor biasing utilising a GaNFET and localised autonomous monitoring and control via the AMAC custom ASIC. The integration of the power board and readout hybrids onto the silicon sensor results in a compact, self-contained module topology. An overview of the power board is shown in Figure 4 with its physical realisation shown in the adjacent photograph.

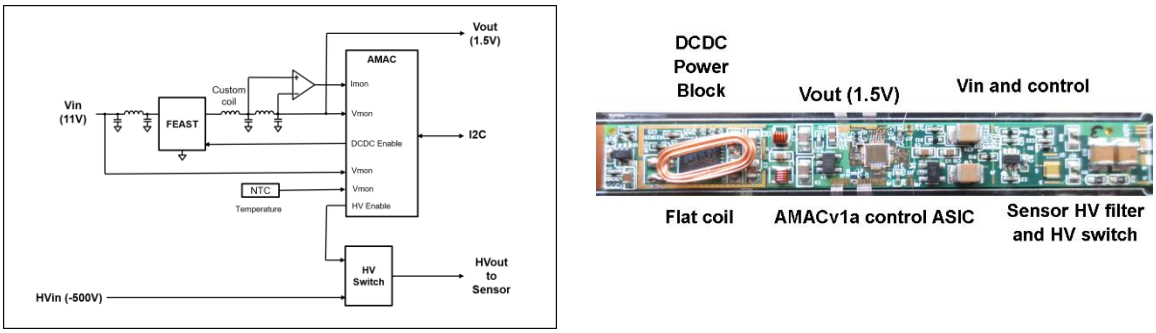

Figure 4. Schematic overview of the power board, shown left, with its physical realisation shown in the photograph on the right.

The use of a buck converter, with its inherent large EMI emissions, can result in induced noise into both the silicon strip sensor and sensitive front-end readout ASICs. Limitations in both height and width make it non-trivial to fit a toroidal coil of the nominal inductance, instead a flat solenoid type was chosen. Attenuation of EMI has been achieved using a low mass, mixed material (Al/Cu) shielding solution whilst still maintaining a target efficiency of >70% at the nominal load of 2 A. Figure 5 shows both the converter efficiency under differing loads and supply voltages and a prototype shield box with flat coil (the shield box measures 18 x 8 x 4.5 mm^3 made up of 75 µm Al wall thickness and <10 µm Cu plating).

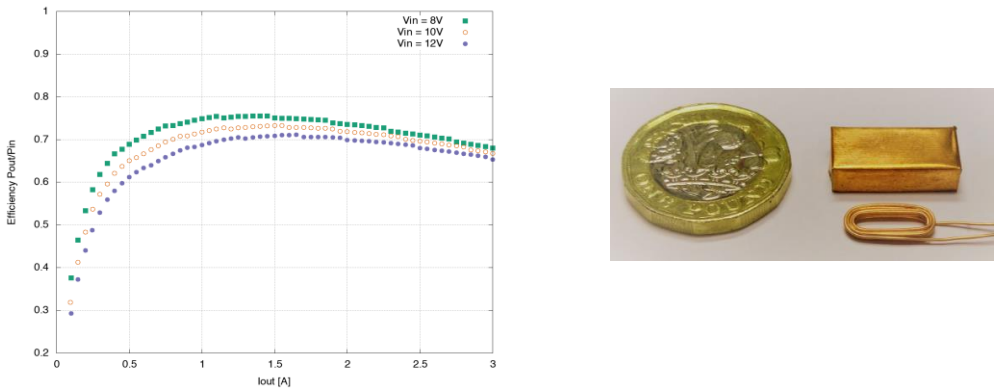

Figure 5. DC-DC converter efficiency under different load conditions and prototype shield box with flat solenoid coil.

3. Module Test Results

A prototype short-strip module was constructed and first tested without the power board attached and then retested with the board attached; if the shielding of the EMI from the power board works, one should expect to see a negligible change in the module input noise. However, a change is seen due to the construction of the power board and the inclusion of an embedded shield layer, this will lead to an increase in load capacitance presented to the front-end ASICs. Consequently, resulting in an increase of the input noise of the strips covered by the power board.

Figure 6 shows the test results for the module before and after the power board has been attached. Sensor strips that are not covered (channels 1 to 384) show marginal change in their input noise, whereas strips covered by the power board (channels 385 onwards) show an increase of ~20 electrons, this being attributed to the embedded shield layer only and not EMI.

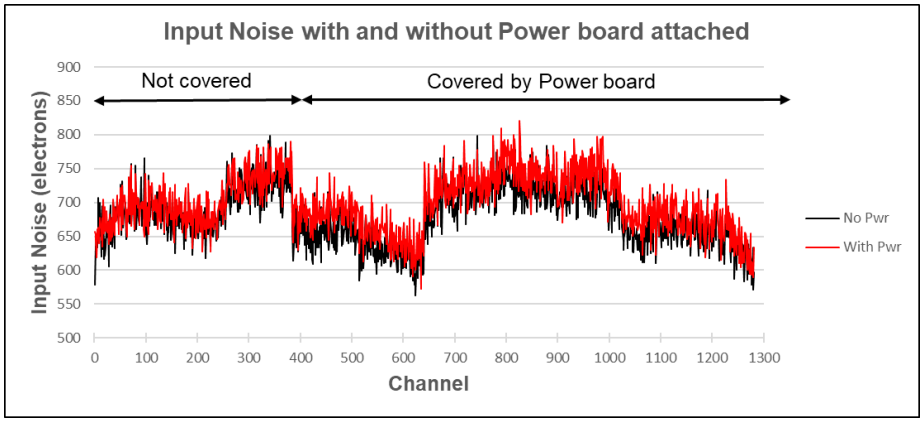

Figure 6. Module test results showing input noise vs channel before the power board has been added (shown black) and after its attachment to the sensor (shown red).

4. Conclusion

An integrated module assembly with both hybrids and a DC-DC buck converter glued to the top surface of a silicon strip sensor has been successfully tested and shown to have negligible effect on module performance and noise. The successful demonstration of this module topology has resulted in this being adopted as the baseline for the ATLAS ITk strip detector, as defined in the Technical Design Report, April 2017 [4].

References

[1] ATLAS Collaboration, 2008 JINST 3 S08003.

[2] http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEAST2.1%20datasheet.pdf

[3] D. Lynn et al, Radiation Hard GaNFET High Voltage Multiplexing (HV-MUX) for the ATLAS Upgrade Silicon Tracker, Proceedings of this conference

[4] The ATLAS Collaboration, CERN-LHCC-2017-005, ATLAS-TDR-025.