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A First Level Calorimeter Trigger Processor for the Large Hadron Collider

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Abstract

As part of an R&D project to study first-level calorimeter triggers for the LHC, a preliminary design of a bit-parallel digital trigger processor system is presented in this note.

The trigger processor will process 4096 electromagnetic and 4096 hadronic trigger cells, selecting events on the basis of high-transverse-momentum electrons, jets and missing transverse energy.

The results of the first-level trigger processor will be sent on to the central trigger processor and to the region-of-interest builder for use in the second-level trigger; the information will also be available for monitoring and off-line evaluation.

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1. Introduction

Triggering at the LHC will be an extremely challenging task since the machine will have a very high luminosity and a bunch-crossing period of 25 ns. Each bunch crossing will contain a large number of interactions, most of which will not involve interesting physics. The function of the trigger is to select the small fraction of events which have interesting physics signatures.

The rate at which data will have to be processed by the level-1 trigger system will be extremely high and the trigger system will have to analyse new data every 25 ns. The first-level trigger will have to achieve a rejection factor of about 10^4–10^5 compared to the interaction rate without introducing any dead time – this requires a hard-wired processor operating in a pipelined mode.

Figure 1 shows a trigger architecture based on three levels, and indicates the order of magnitude rates which might be achieved after each level of triggering. Relatively crude decisions made quickly (at most 2 μs) at the first-level can be refined at the second and third levels using more detailed information from the detectors [1].

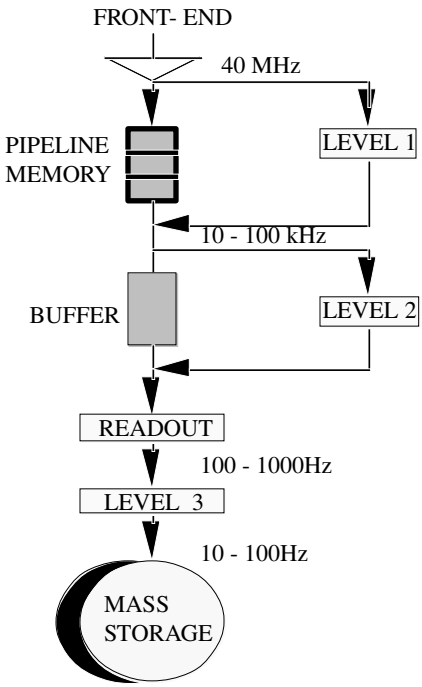


Fig. 1 Multi-level trigger architecture

The bit-parallel first-level digital trigger processor design described here is based on the latest technology available now or in the near future. The trigger processor will consist of electromagnetic-cluster (electron/photon) trigger logic, jet trigger logic and missing-E_T trigger logic. The electromagnetic-cluster trigger logic is the most demanding in the system and will consist of four crates of electronics, each processing 1/4 of the electromagnetic (EM) and hadronic (HAD) calorimeter trigger cells. The remaining electronics will be housed in two other crates, making a total of six. The trigger processor will require four different Application Specific Integrated Circuit (ASIC) designs, and seven different circuit board designs. The trigger crates are 18 SU (1 SU = 25 mm) in size. Figure 2 shows a block diagram of the trigger processor system.

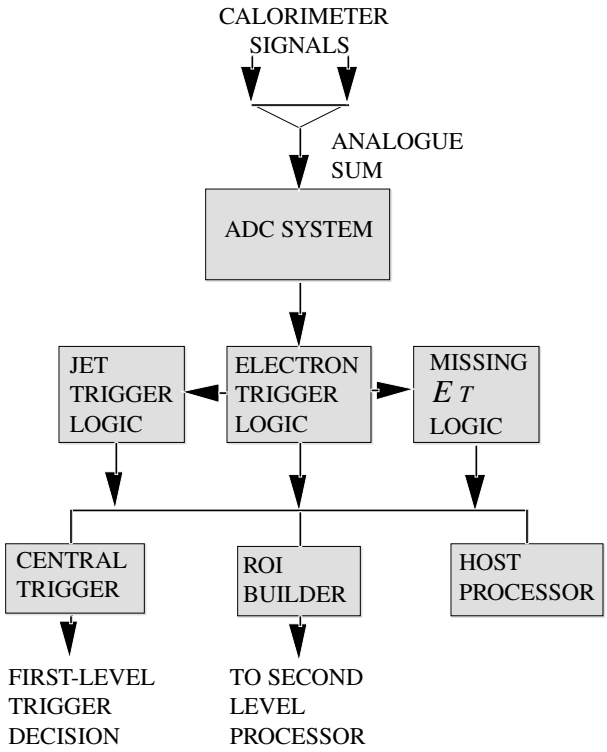


Fig. 2 Trigger system

2. EM CLUSTER TRIGGER ALGORITHM

The trigger algorithm [2] will use digitised signals from an ADC system providing a calorimeter granularity appropriate for the first-level trigger. The ADC system could be FERMI [3] or it could be a custom-built trigger ADC system independent of the calorimeter readout. For more details on the requirements for the ADC system refer to Appendix 1. In the case of the independent ADC system, the analogue signals are summed before digitising to give a granularity of about 0.1 × 0.1 in pseudorapidity–azimuth $(\eta - \varphi)$ space giving approximately 4000 each of EM and HAD trigger cells for a pseudorapidity coverage of $|\eta|$<3.

Figure 3 shows a 4 × 4 area of the EM calorimeter and the HAD calorimeter which will be used in the algorithm. The algorithm will search for EM energy clusters with an (optional) isolation requirement. The algorithm considers a reference cell (2.2) within the 4 ×4 area and it requires that the vertical sum (2.2 + 3.2) or the horizontal sum (2.2 + 2.3) exceeds a programmable cluster threshold; it also requires that the "outer" EM sum and the transverse energy (E_T) in the 4 × 4 area of the HAD calorimeter is less than a programmable threshold. The process is replicated using each EM trigger cell in the calorimeter as the reference cell so as to cover all the trigger cells in the calorimeter. The algorithm will also provide the sum of the 4 × 4 area of the EM calorimeter which will be used to calculate the missing transverse energy and jets.

A "demonstrator" ASIC [4] using a 0.8 micron CMOS gate array has been designed and manufactured to perform the above algorithm, excluding the hadronic information to simplify and reduce the cost. The demonstrator has been tested with clock speeds up to 70 MHz.

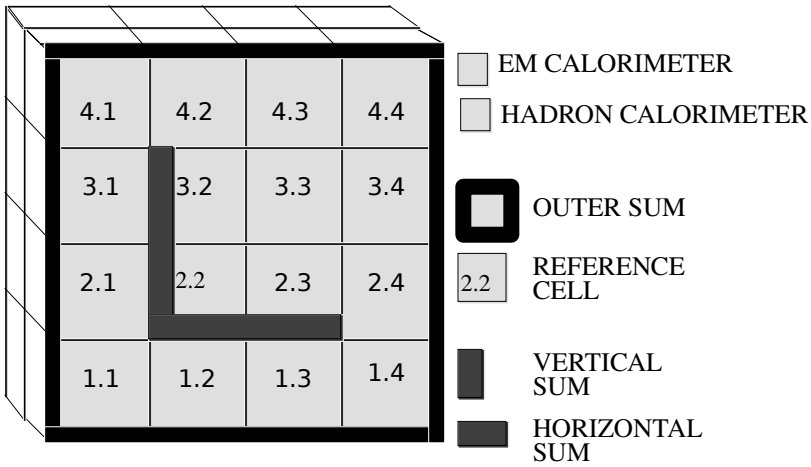


Fig. 3 View of the 4 × 4 area of the calorimeter

3. Demonstrator Trigger System – Phase 1

A demonstrator trigger system [5] as shown in Figure 4 has been built and is under test. The trigger module contains nine of the above mentioned ASICs, and will fully process a 3 ×3 area of the EM calorimeter. The number of I/O connections to the trigger module is in excess of 300 (36 × 8 + 2 × 9 + 12) signals, excluding any control and set-up signals. If a full trigger system were to be built with the present modularity, approximately 450 such modules would be required to process ≈4000 EM calorimeter cells envisaged in the final system. This would be a very large system.

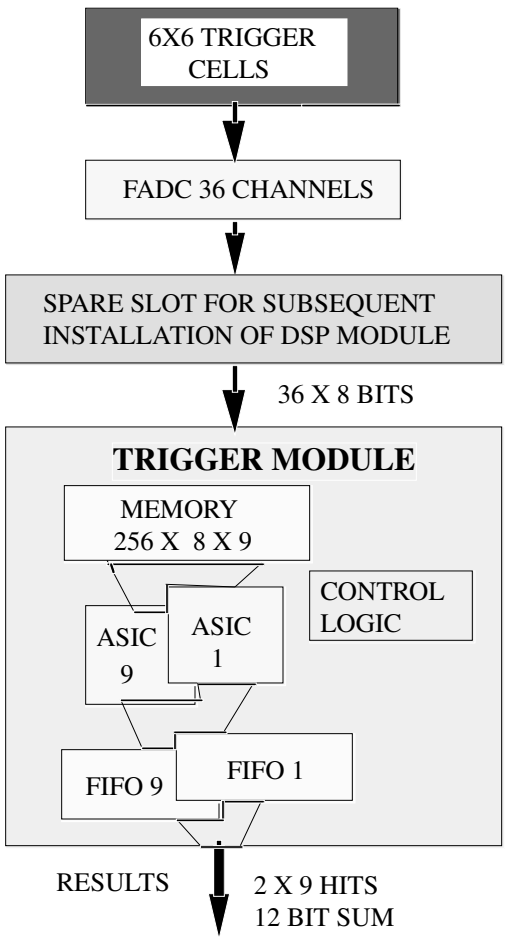


Fig. 4 Demonstrator trigger system

4. System Design for Full LHC Trigger

The system design presented here uses various methods to reduce the system size, and includes:

- More processing elements on a single cluster-finding ASIC than the one cell processing capability of the phase-1 demonstrator ASIC – RAL 114.
- Use of zero-suppression techniques to reduce the bandwidth into the processor.
- Fewer I/O pins onto the EM cluster-finding ASIC by using serial links operating at 160 Mbits/sec.

Appendix 1 gives a brief description of the ADC system which will digitise the analogue signals from the trigger cells, apply zero suppression and tagging and transmit these data to the trigger processor logic using serial links operating at 160 Mbits/sec.

4.1 EM Cluster Finding ASIC

The most complex part of the logic required for the trigger processor will be implemented on the cluster-finding ASIC which has the following requirements:

- Receive digitised information from the EM and HAD trigger cells using one serial link per trigger cell operating at 160 Mbits/sec.
- Synchronise and perform serial-to-parallel conversion of input data.
- Provide buffer (16 bits × 4) and tag-matching logic for each input channel.
- Provide 16 processing elements per ASIC (requires data from 7 × 7 area of the EM and HAD calorimeters).
- Provide eight sets of threshold values {cluster threshold, isolation threshold} for the isolated EM cluster trigger.
- Number of trigger cell input signals to the ASIC:
  - [(4+3)(4+3) × 2 × 1] {(EM + HAD) × bits/cell} = 98 input signals @ 160 Mbits/sec.
- Results:
  - 16-bit region-of-interest (ROI) "ROI pixel array" (4 × 4) for one threshold value.
  - 8-bit hit result – one bit per threshold giving OR over 4 × 4 area.
  - 13-bit transverse energy sum over 4 × 4 area (EM + HAD) – this is serialised onto four lines operating at 160 Mbits/sec.
- Memory to capture results (37 bits × 80 deep) and input data (8 bits × 80 deep ×32 EM and HAD reference cells) – for 40 MHz bunch-crossing frequency this give a 2 μs pipeline length.
- Following a positive first-level trigger decision ("T1-Yes" signal received), the data corresponding to the appropriate bunch-crossing number should be transferred out from the RAMs
- Include logic to test the ASIC.
- The ASIC will use a 160 MHz clock. While the serial links will run at 160 Mbits/sec the core logic will run at 40 MHz rate, but can do more processing between pipeline steps than in the phase-1 demonstrator ASIC (RAL 114), thus reducing the latency.

The cluster-finding ASIC can be implemented on a 0.5 micron CMOS gate array which is available from Fujitsu with gate counts up to 820k gates. A total of 256 such ASICs would be required to process the entire EM plus HAD calorimeter (4096 each of EM and HAD calorimeter trigger cells). Figure 5 shows a block diagram of the cluster-finding ASIC.

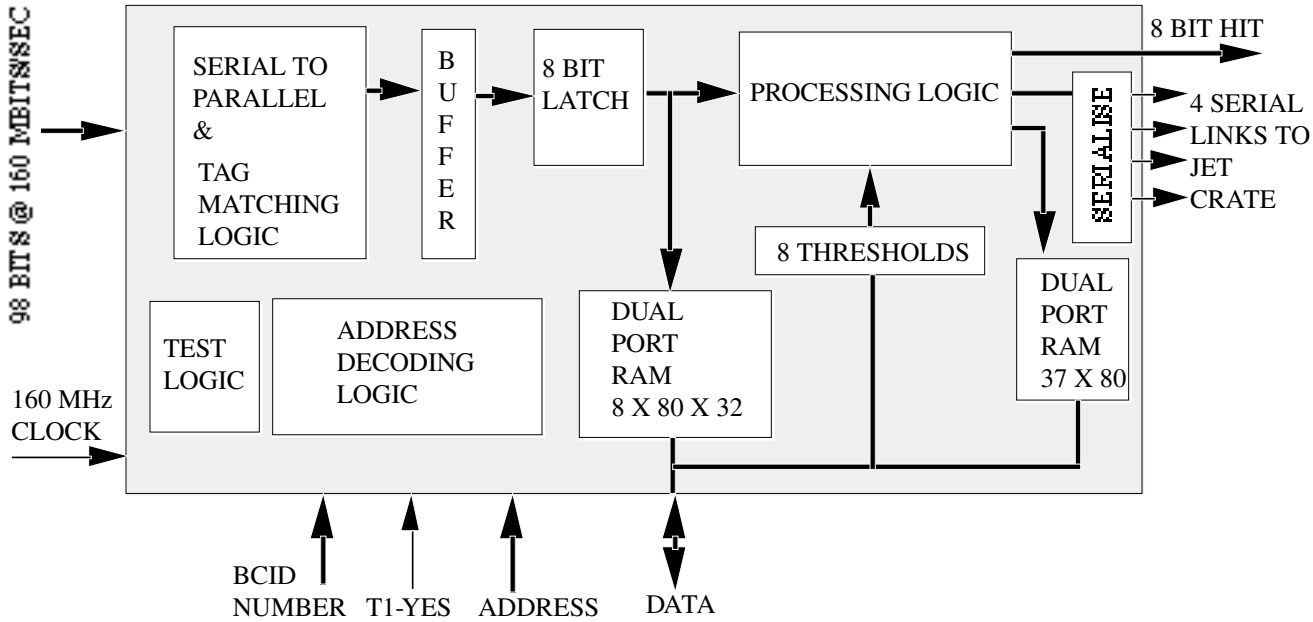


Fig. 5 Cluster-finding ASIC block diagram

4.2 Cluster Processor Board

The cluster processor board (Figure 6) will contain four of the cluster-finding ASICs, one adder ASIC for adding four 13-bit E_T sums (see Appendix 2 and 3), look-up tables (LUT) to convert the energy to its E_x and E_y components, and other control and interface functions. With four cluster-finding ASICs on a processor board, each board can process fully an 8 × 8 area of the EM and HAD calorimeter. The functionality and the requirements of the cluster processor board are listed below:

- Number of input signals:
  - [8+3)(8+3)] × 2 × 1 =242 signals @ 160 Mbits/sec. Of these, 128 signals would be from the ADC system via a receiver board (see section 4.3) and the remaining 114 signals from the neighbours via the backplane. The receiver and the cluster processor board will be plugged back-to-back in the crate. Provision will be made for inter-crate connections where required.
- Results:
  - The 8 × 4-bit hit patterns will be transmitted to the EM decluster crate via cables and to the readout controller (ROC = crate controller) via the FIFO buffer.
  - The 4 × 13-bit E_T sum which is serialised on to 4 × 4 links will be transmitted to the jet processing crate and also to the ROC as above.
  - The 16-bit signed (2's complement) E_x and E_y missing energy values will be transmitted to the results board (see Section 4.4).
  - On receipt of T1-Yes, the data corresponding to the BCID number and the ROI will be transferred to the ROC. More details on the data-transfer procedure are given in Section 4.9.
- The physical size of the board would allow a backplane connector 16 SU (400 mm) high allowing over 600 connections on to the backplane with the current connector technology (Molex Omnigrid 2.5 connectors).
- A total of 64 cluster processing boards would be required for the complete trigger system (16 boards/crate × 4 crates)

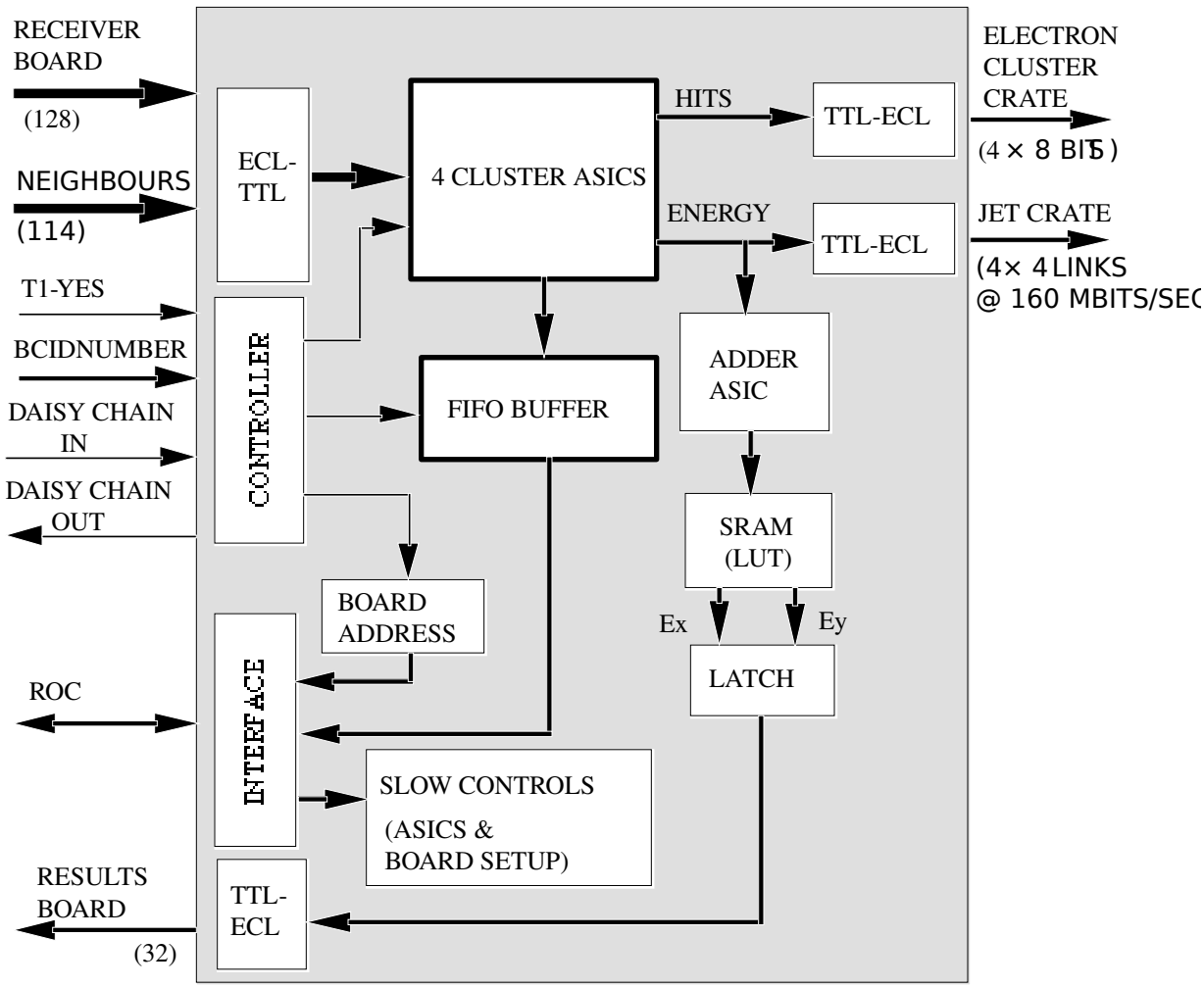


Fig. 6 Cluster Processor Board Block Diagram

4.3 Receiver Board

The receiver board will receive digitised, serialised data at 160 Mbits/sec from the ADC system. Ideally these signals should be optical since the volume of ≈8000 (EM and HAD) copper cables will be difficult to manage. If the connections are optical, the receiver board should receive 128 (EM + HAD) optical signals from the ADC system and convert them to electrical signals. Since each cluster processor board processes an 8 × 8 area of the calorimeter which requires signals from 242 trigger cells, the remaining 114 signals must come from the neighbouring receiver boards via the backplane. The other function of the receiver board will be to fan out signals (44 maximum) and drive them onto the backplane; these will be required by the neighbouring cluster processor boards. Figure 7 shows a block diagram of the receiver board.

The Receiver board also would include facilities for inter-crate connections where required.(not shown in figure 7) The crate to crate connections are required only between crates 2 and 3 (see appendix 7). The Receiver board should therefore be capable of receiving additional 16 ECL signals other than the 128 optical signals.

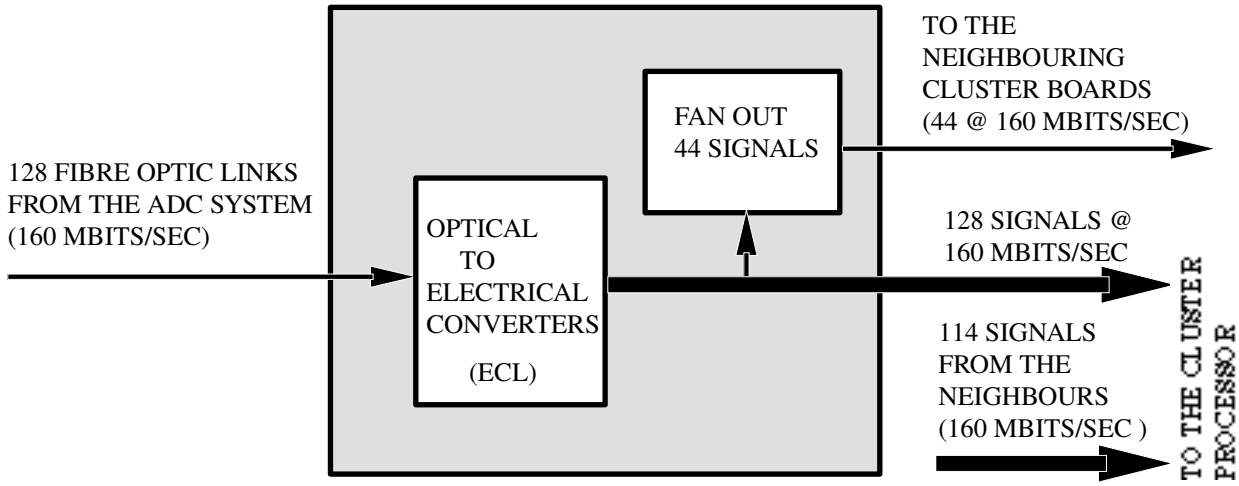


Fig. 7 Receiver board

4.4 Results Board

The Results board will receive E_x or E_y values from 16 cluster processing boards and carry out addition using the adder ASICs. The 16-bit, 2's complement results of this adding process will be sent to the Missing-E_T board. For further details see Appendix 3. Figure 8 shows a block diagram of the receiver board. The intermediate results are available on the FIFOs if required for off-line evaluation. Each cluster processor crate will require two results boards, for the E_x and E_y values respectively.

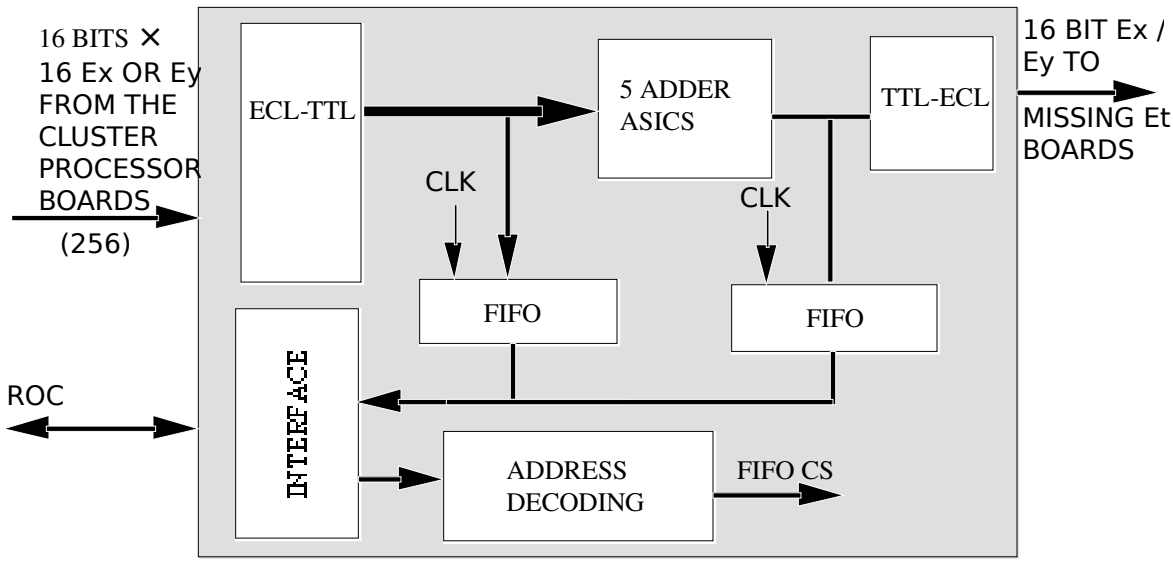


Fig. 8 Results board

4.5 Missing-E_T Board

The function of the missing-E_T board is to receive the partial E_x and E_y sums from the 8 results boards (2 results boards/crate × 4 processor crates) and carry out further addition using the adder ASICs and then test $E_T = \sqrt{(E_x^2 + E_y^2)}$ against thresholds using look-up tables.

It provides four threshold values and the 4-bit E_T hit flag will be transmitted to the central trigger logic (CTL). Only one missing-E_T board is required in the system. The board will receive four 16-bit E_x and four 16-bit E_y values from the eight results boards in the cluster processor crates. Figure 9 shows a block diagram of the missing-E_T board. Appendix 3 gives more details of the missing-E_T calculation.

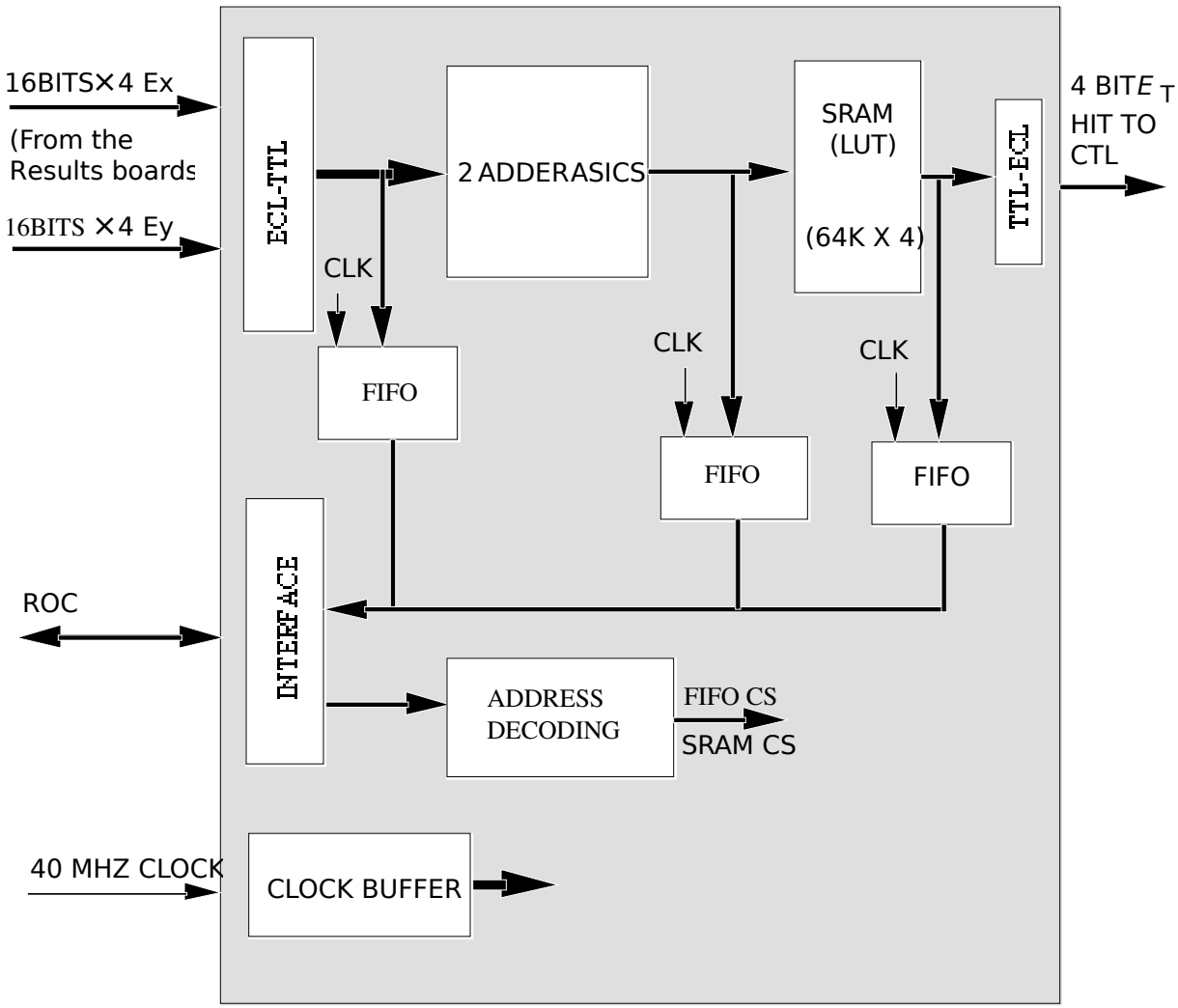


Fig. 9 Missing-E_T board block diagram

4.6 Jet Processing

The jet algorithm is performed using the 13-bit E_T sums calculated over the 4 × 4 areas of the calorimeter; these are available from the cluster processing boards. The algorithm will use a 2 × 2 window, and the sums of four jet cells will be compared with eight threshold values (see Appendix 4 for further details of the jet algorithm) . An ASIC ("jet ASIC") will be designed to perform the algorithm over a 4 × 4 area, thereby fully processing nine jet windows. Since there are 256 13-bit sums, approximately 30 jet ASICs would be required to process the jets. With four jet ASICs per jet processing board, 13-bit sums from 49 jet trigger cells would be needed. Since the 13-bit sums are serialised on to 4 lines operating at 160 Mbits/sec on the cluster-finding ASIC, the input to the jet processor board would be 49 × 4-bit serial links. Transmitting these data using balanced ECL would require 392 twisted pairs onto the jet processing board. With this modularity, i.e. four jet ASICs per processing board, eight Jet processing boards would be required for the system.

Figure 10 shows a block diagram of the jet ASIC which will receive 16 × 4 bits at 160 Mbits/sec from the cluster processor board and will convert these serial data to parallel data before the signals go on to the jet algorithm. Some test logic, e.g. boundary scan, would be included in the ASIC in order to test it. The ASIC will be implemented on a 0.5 micron CMOS gate array.

Figure 11 shows a block diagram of the jet processing board. By using the Molex 2.5 Omnigrid connectors, the signals can be brought directly onto the backplane connector. The hits will be transmitted using twisted-pair cables to the declustering boards.

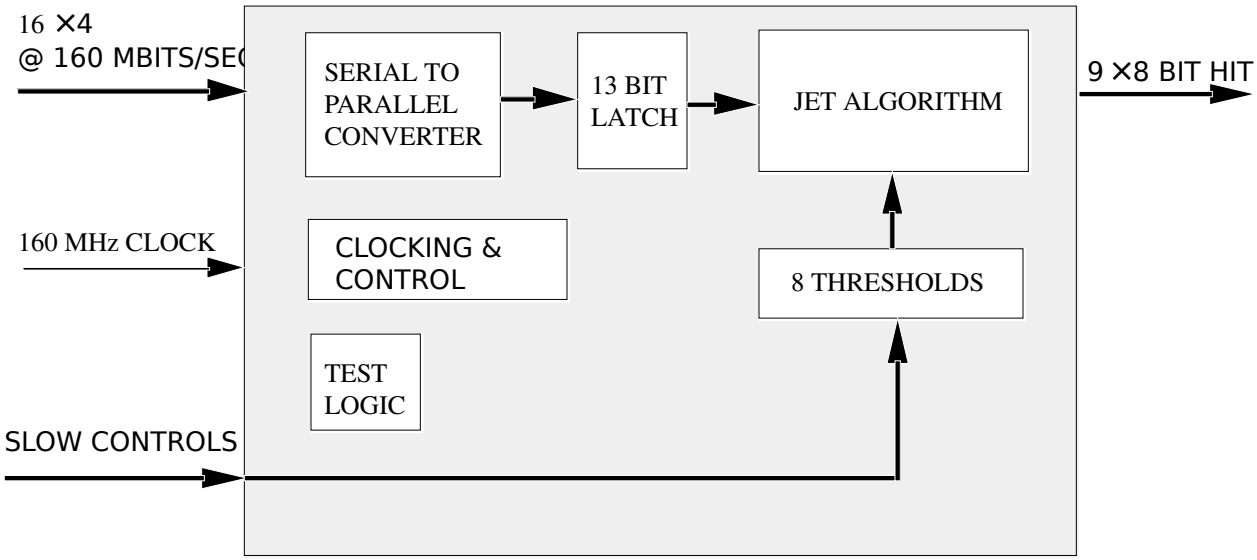


Fig. 10 Jet ASIC block diagram

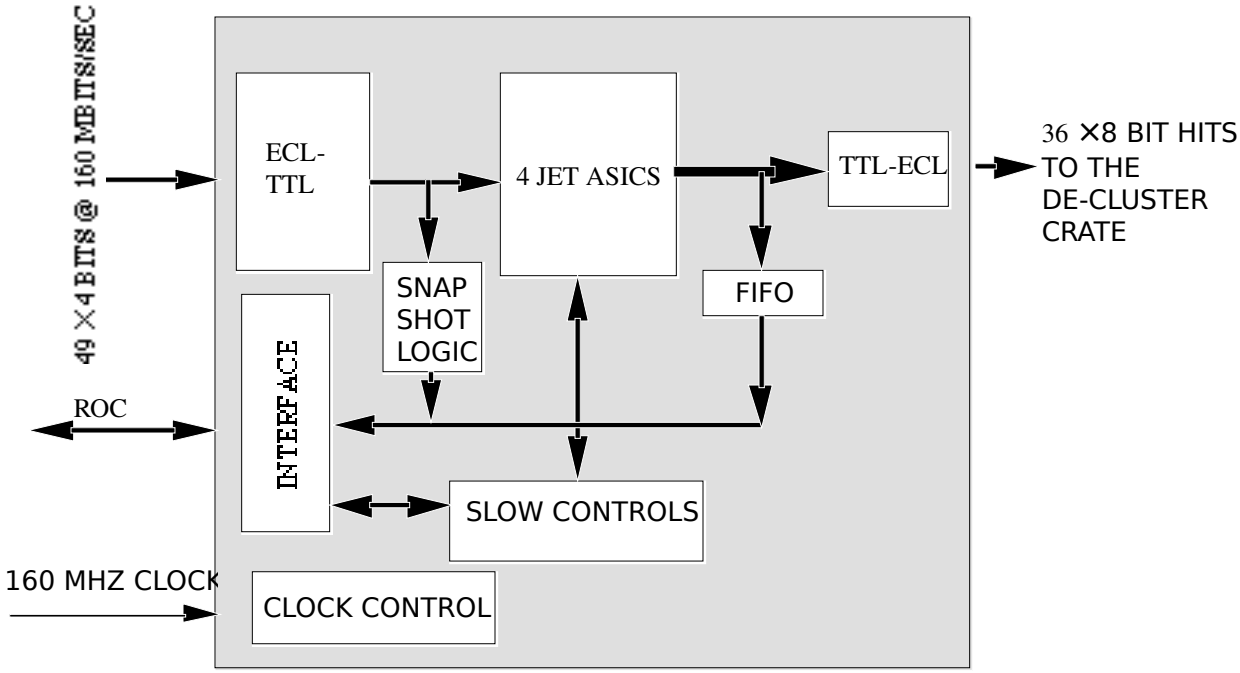


Fig. 11 Jet processing board

4.7 Declustering

The declustering (cluster counting) electronics for jets and EM clusters will be identical, providing the following functions:

- Receive the 256 pixel array (hits) from either the cluster processor boards or the jet processor boards.
- Apply veto and count non-vetoed pixels – this attempts to avoid double counting of contiguous hits (see Appendix 5).
- Compare multiplicity with eight threshold values [more than required].

Part of the vetoing and counting logic will be implemented on an ASIC (veto ASIC), and to complete the adder tree the adder ASIC will be used. The declustering board will process 256 pixels corresponding to one EM cluster or jet threshold. Each veto ASIC will process 16 pixels, requiring 16 veto ASICs per board. The system will include eight declustering boards each for processing EM clusters and jets.

Figure 12 shows a block diagram of the declustering board. It has ECL-to-TTL converters to receive the 256 balanced ECL signals and convert to TTL before feeding the signals to the veto ASICs. There are 16 veto ASICs and five adder ASICs to carry out the declustering. The results are transmitted to the central trigger logic via twisted-pair cables. There are FIFOs to capture the incoming data as well as the results, which can be read out for off-line evaluation.

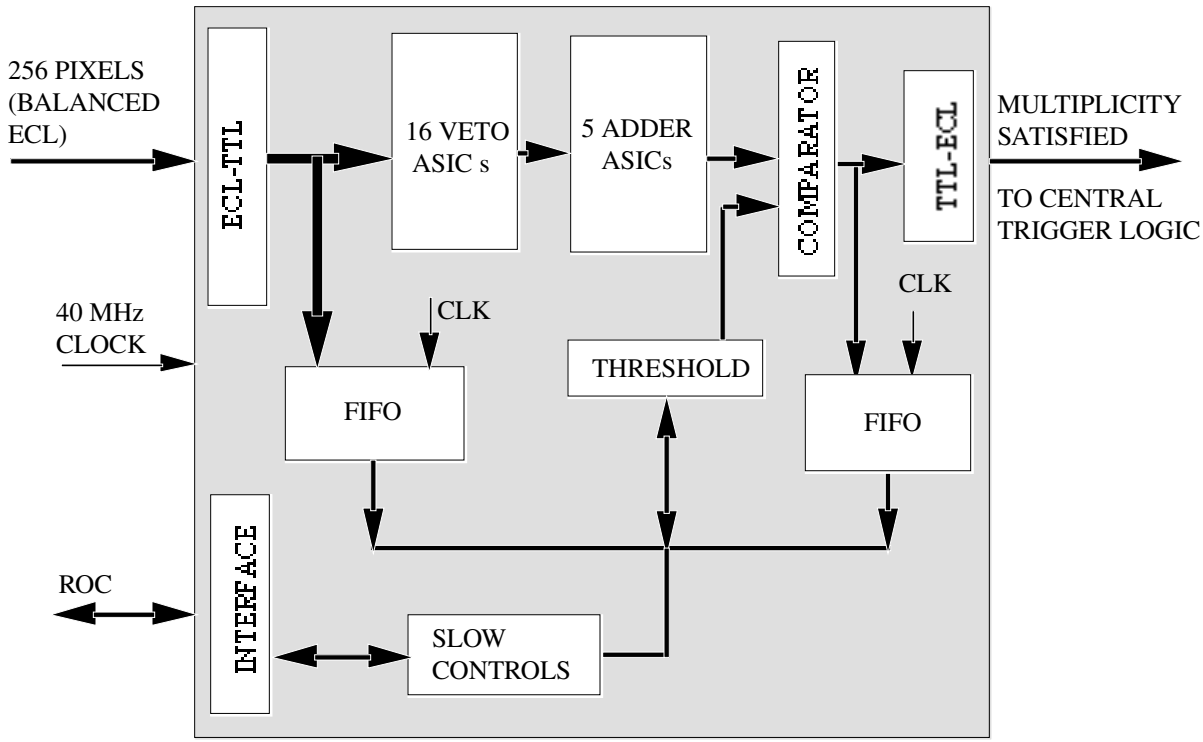


Fig. 12 Declustering board block diagram

4.8 Readout Controller/Crate Controller

A readout controller/crate controller (ROC) is required in each crate so that the host computer can communicate with the boards on the crates, and also to provide an interface to the second-level trigger. The ROC might have a CPU to control and format the data and to provide the following functions.

- Interface to the host computer
  - receive set-up data
  - transfer data from the boards for off-line evaluations
- Interface to level-2 and central trigger
  - Receive T1-Yes, the BCID number and transfer the ROIs and other relevant information
- Interface to the boards on the crates
  - Initialise and set-up ASICs and the boards
  - Receive data from the boards
- Provide test facilities:
  - When the CPU is idle it could perform a test routine (e.g. a software cluster algorithm) on the data received from the boards. The test results can be recorded on a status register to be read out by the host computer.

Figure 13 shows the block diagram of the ROC. For further details on the data transfer procedures see Section 4.9.

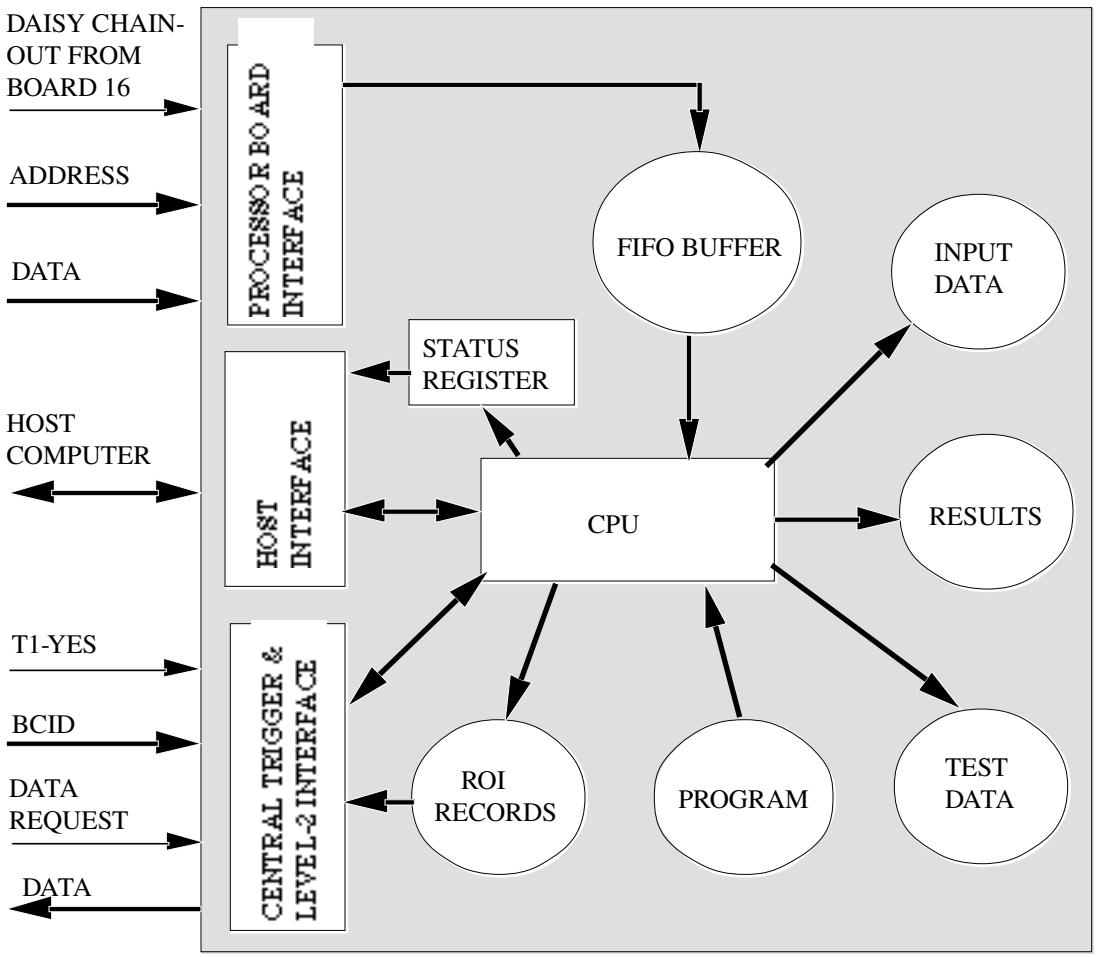


Fig. 13 ROC block diagram

4.9 Data Transfer Procedure

The following is a description of the procedure by which the data distributed over the first-level calorimeter trigger system, from the cluster-finding ASICs onwards, can be collected and transferred to level-2 and also read out for off-line evaluation.

- On each clock cycle (25 ns) the input data corresponding to the reference cells, and the results are captured in the dual-port RAM.
- When the level-one trigger signal "T1-Yes" is received by the ASICs the data corresponding to the BCID number are copied from the ASICs into the on-board FIFO buffer.
- The 16 cluster processor boards will be daisy-chained for the purpose of data transfer, and each board will take its turn to transfer data from the on-board FIFO to the FIFO buffer in the ROC. The address of the board is also recorded.
- The above transfer can be made on the backplane.
- When the last processor board on the chain has completed its transfer, it can signal the ROC by the daisy-chain out signal.
- When the ROC receives the daisy-chain out signal, the CPU (or equivalent logic) can read the FIFOs and make copies of the input data and results. These data are used to provide ROI information to the level-2 trigger and for the readout.
- The CPU could make up a record from the data available as follows:
  - BCID-Number
  - Crate Number
  - Card Number
  - ROI location
  - Energy, etc. as required
- The ROCs in the system can transfer the records to the second-level when requested. Zero-suppression could be implemented if required.
- The data are available in the ROCs if required by the readout for off-line evaluation.

5. TESTING AND MONITORING FACILITY

The system will provide some form of test and monitoring facility by incorporating FIFO buffers, which will act as "spy memory". The FIFOs will be placed at the input and the output of a board (see board block diagrams), and the data can be read out for analysis or, as mentioned in section 4.9 on the Data Transfer Procedure, the CPU on the ROC can perform data analysis on all the boards in the crate and set a flag so that the host computer can pin- point a faulty board in the crate. Since all the crates would have a ROC, the complete system can be monitored in this manner.

6. SYSTEM CRATES

6.1 Cluster Processor Crates

Each cluster processor crate will process 1024 each of EM and HAD trigger cells and will include:

- 16 cluster processor boards
- 16 receiver boards to receive the digitised, serialised data from the trigger cells. One receiver board will be required per cluster processor board. The receiver boards and the cluster boards will be plugged back-to-back via the backplane connectors (Figure 14). Only the signals required for the neighbouring boards will be driven on the back plane.
- Two results boards

- One readout controller.

Four crates would be required for the cluster processor logic.

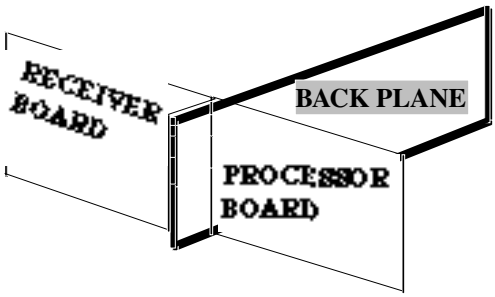


Fig. 14 Receiver to cluster processor connection

6.2 Jet Processor Crate

The jet processor crate will include eight jet processor boards and one readout controller board. Since there is space in the crate, the eight declustering boards required for the jet declustering could be housed in the same jet crate.

6.3 EM Decluster Crate

The EM declustering crate would include eight declustering boards for declustering electrons and one readout controller board. Since there are spare slots in this crate the missing-E_T board can be housed in the decluster crate.

6.4 Overall System

The system will make use of 18 SU size crates (1 SU=25mm) with 20 slots per crate. Figure 15 shows the building blocks of the calorimeter trigger system.

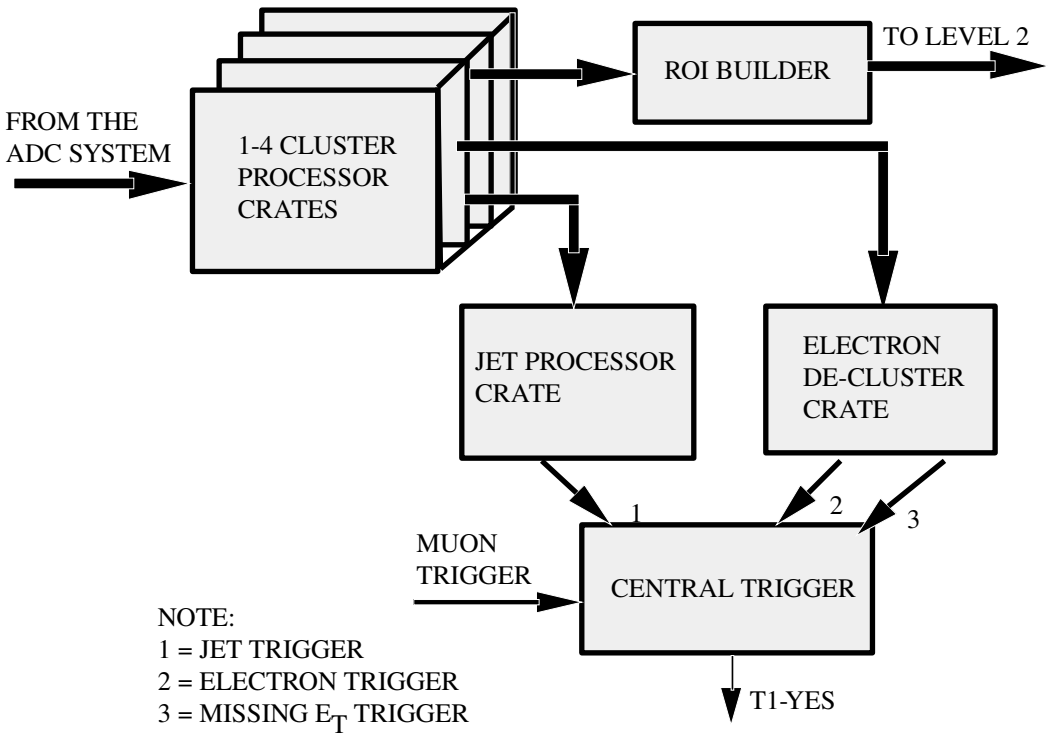


Fig. 15 First-level calorimeter trigger system

7. DEMONSTRATOR TRIGGER SYSTEM – PHASE 2

7.1 ASIC

We envisage designing an ASIC that will test critical functions of the final system (see Figure 16). The critical functions that we would like to test are:

- "Transmit" block: Receiving and buffering 8-bit wide data, performing zero suppression, tagging and parallel-to-serial conversion, and transmitting serial data at 160 Mbits/sec. This section would be part of the ADC system in an LHC experiment.
- "Receive" block: Receive data at 160 Mbits/sec, perform serial-to-parallel conversion, buffering and tag matching.
- "Algorithm" block: Receive data as above for 16 EM trigger channels and perform cluster processing for a 4 × 4 area as in the phase-1 demonstrator.
- If the gate counts permit, we could include the BCID logic, at least for one channel.

The transmit block will receive 4 × 8-bit data every 25 ns, process these data and output 4 × 1-bit at 160 Mbits/sec. The receive block will receive 4 × 1-bit data at 160 Mbits/sec, process these data and output 4 × 8-bit data every 25 ns. Four channels are included in each of the transmit and receive blocks to test for cross talk. This modularity will also be useful for the demonstrator system. The cluster algorithm will use data from four receive blocks as shown in the Figure 16. The cluster processing will be carried out at 40 MHz rate, but with more processing between pipeline steps than the phase-1 demonstrator ASIC. Figures 17 and 18 show block diagrams of single channels of the transmit block and the receive block respectively.

The I/O pin requirement for the ASIC would be about 63 inputs and 51 outputs. If required the I/O pin count could be reduced by 36 by using bi-directional pins for the transmit block and sharing these pins with the first receive block, since the transmit block and the receive block will not be used at the same time on the same ASIC – a mode register could be provided to select between the two blocks. The ASIC will be implemented on a 34k, 0.5 micron CMOS gate array.

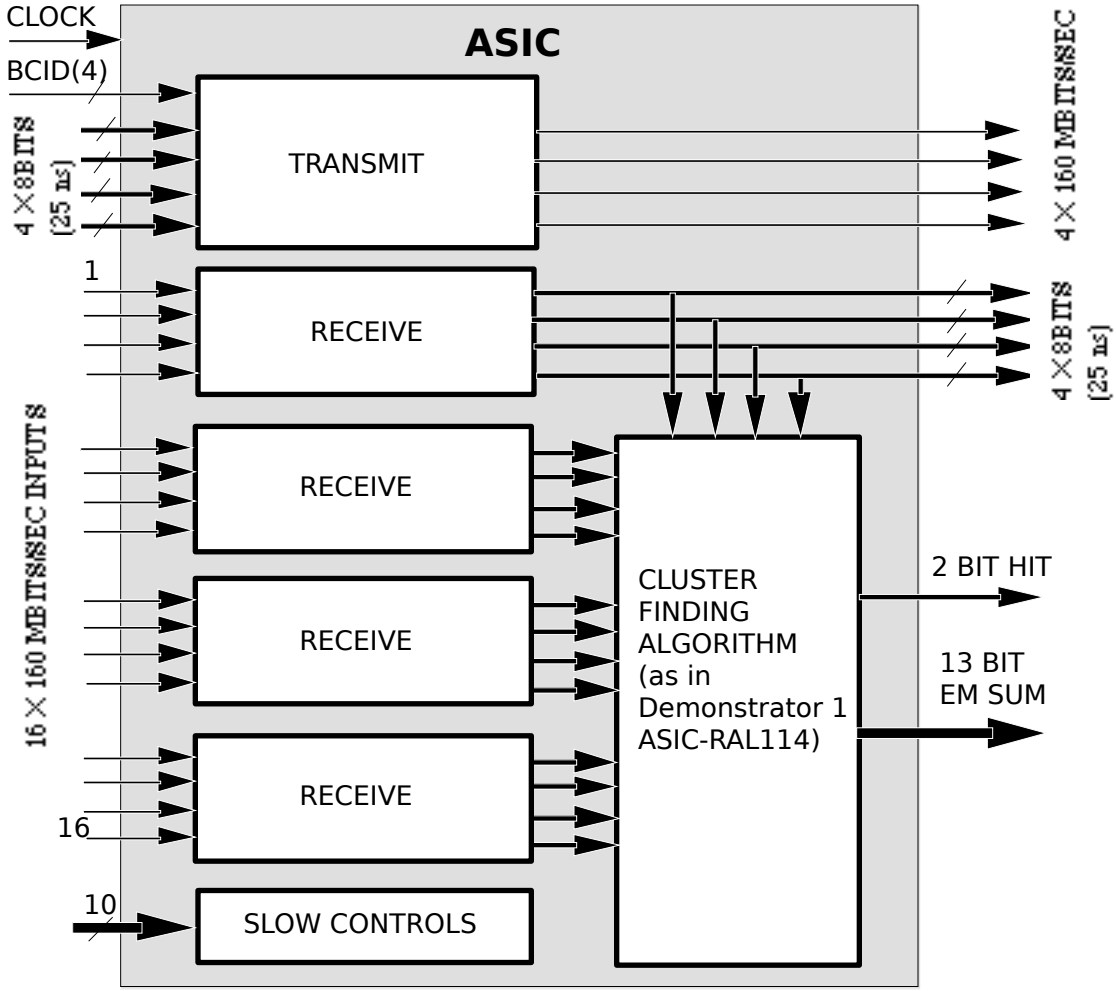


Fig. 16 Demonstrator ASIC 2

7.1.1 Transmit

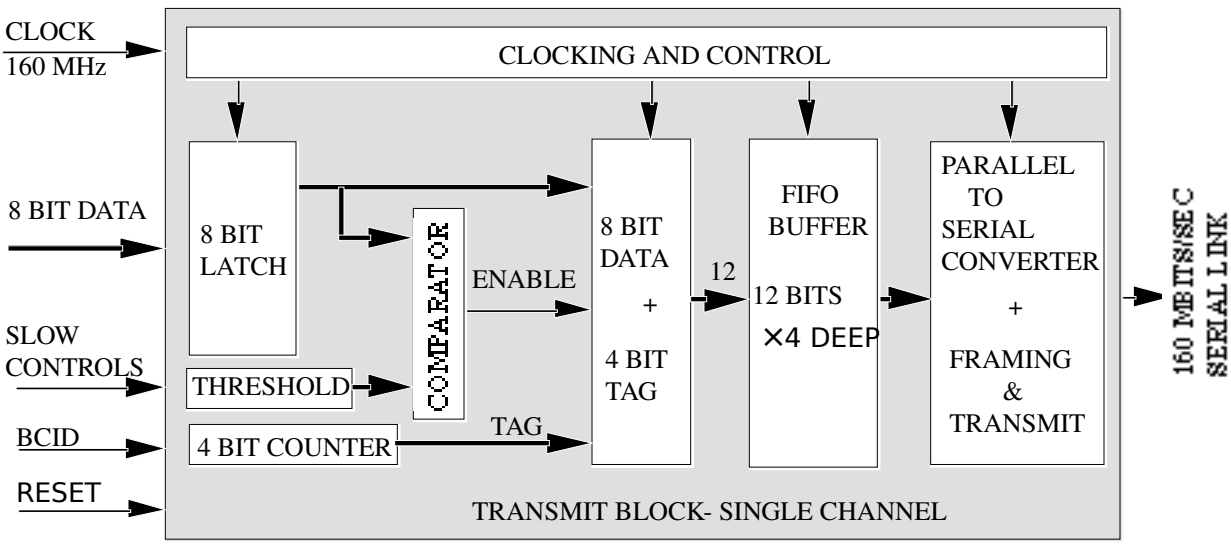


Fig. 17 Transmit Block-Single Channel

Eight-bit (or nine-bit) data which arrive every 25 ns will be compared with a threshold (zero suppression). If the data value is above the threshold then:

- A 4-bit (or 5-bit) tag will be attached to the data making it 12 bits.
- The resulting 12-bit data will be transferred to a FIFO buffer since more than one bunch crossing (25 ns) is required to transfer the data.
- The data from the FIFO buffer will be serialised and transmitted at 160 Mbits/sec after adding framing bits.

7.1.2 Receive

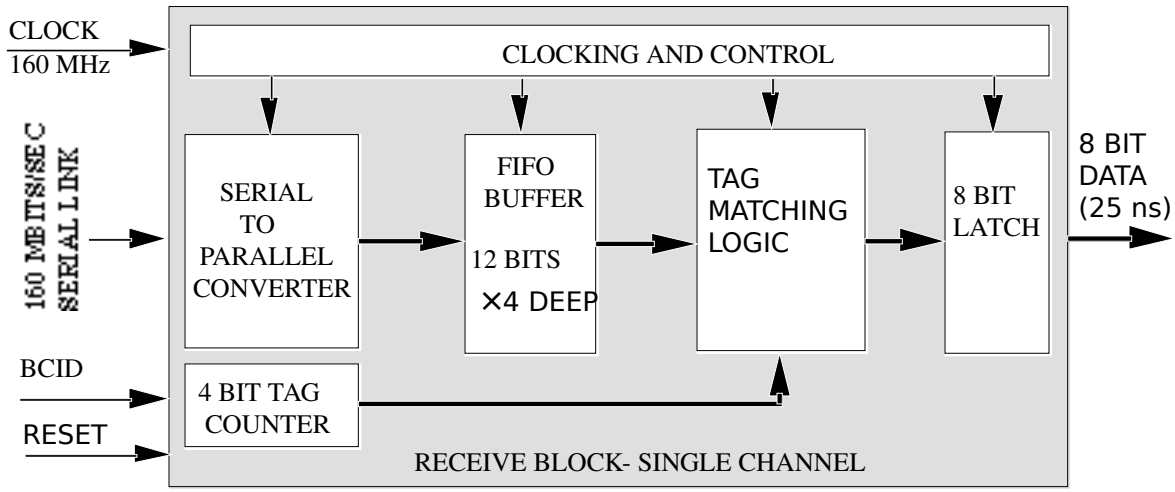


Fig. 18 Receive block for single channel

The Receiver receives serialised data at 160 Mbits/sec and will:

- Synchronise and convert the serialised data to parallel data.
- Buffer the data until the tag is matched.
- Transfer the tag-matched 8-bit (9-bit) data every 25 ns.
- If the tag is not matched then the data will be zero.

7.2 Demonstrator System

The demonstrator system could be similar to the existing demonstrator system, which fully process a 3 × 3 area of the calorimeter using 9 ASICs. Data from 36 trigger cells are required to process the 3 × 3 area. Figure 19 shows a block diagram of the proposed system using the demonstrator ASIC 2. The receiver/transmitter (RT) board will have 9 of the ASICs in mode T which will use only the transmit block of the demonstrator ASIC. The RT board will receive 8-bit parallel data from 36 ADC channels and will transmit the processed data via a transmit interface board on 36 serial links at 160 Mbits/sec/link; these links could be optical or electrical. The cluster processing board will receive the serial data at 160 Mbits/sec via a receive interface board, and will have 9 ASICs in mode R which will use the receive blocks and the cluster algorithm block to carry out the cluster finding algorithm. The design of the interface boards will depend on whether the links are optical or electrical. An additional board with LUTs can be included between the ADC system and the RT board to subtract the pedestals before the zero suppression.

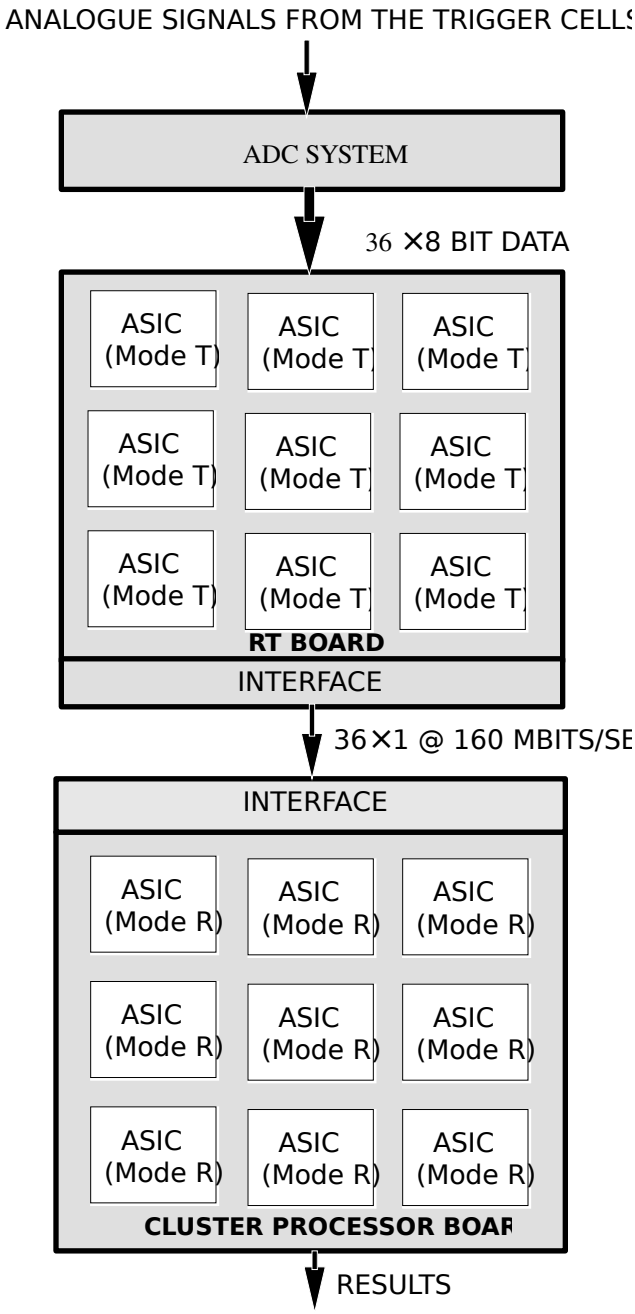


Fig. 19 Demonstrator trigger system

8. Summary and Conclusions

The first level calorimeter trigger system will process 4096 electromagnetic and 4096 hadronic trigger cells of granularity $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$ for $|\eta| < 3$ and will provide the following subtriggers to the central trigger logic:

- EM cluster (electron/photon) trigger with eight sets of programmable cluster and isolation threshold values, each with several programmable multiplicity thresholds.
- Jet trigger with eight programmable threshold values, each with several programmable multiplicity thresholds.
- Missing transverse energy trigger with four threshold values.

Apart from providing the above subtriggers to the central trigger logic, the system will provide region-of-interest information to the second-level trigger, and allow intermediate results to be read out for off-line evaluations and monitoring.

The following is a list of electronics required to achieve the above:

- Four crates of EM cluster processing electronics with 16 cluster processing boards per crate.
- One receiver board per cluster processor board (interface to ADC system).
- Two results cards per cluster processor crate (for partial missing-E_T calculation).
- One jet processing crate containing 8 jet processing boards plus 8 declustering boards.
- One electron declustering crate containing 8 declustering boards.
- One missing-E_T board which will occupy a spare slot in the electron decluster crate.
- Each crate will have a readout Controller (ROC) module.

The total number of crates require is six 18 SU (1 SU = 25mm), 20 slot crates. The system requires seven deferent circuit board designs and four different ASIC designs.

The above system can be implemented using technology which is either already available or which will be available in the very near future. The digital processor has manageable complexity and a trigger latency (see Appendix-6) of under 500 ns. The phase-2 demonstrator ASIC and the demonstrator system will allow us to study the most critical and demanding aspects of the final system.

9. REFERENCES

[1] N. Ellis, S. Cittolin and L. Mapelli, "Signal processing, triggering and data acquisition", CERN 90-10 (Vol. 1), pp. 504–538.
See also: N. Ellis, "Level-1 and level-2 triggering at LHC", RD-27 note 4.

[2] N. Ellis and J. Garvey, "A digital solution to first level triggering using calorimetry at LHC", CERN 90-10 (Vol. 3), pp. 80–83.
See also: N. Ellis, "Level-1 and level-2 triggering at LHC", RD-27 note 4.

[3] FERMI Collaboration, "A digital front-end and readout microsystem for calorimetry at LHC", IEEE Nuclear Science Symposium, Orlando USA, October 1992.

[4] V. Perera et al., "First level calorimeter trigger system for the Large Hadron Collider", IEEE Nuclear Science Symposium, Orlando, USA, October 1992; RD-27 note 5.

[5] R. Staley et al., "Demonstrator calorimeter trigger system", transparencies shown at RD27 meetings.

[6] I. Brawn, "BCID studies" transparencies shown at RD27 meetings.

Appendix-1
ADC System

The first-level calorimeter trigger system requires digitised information from the trigger cells to process and generate the triggers. The ADC system could be FERMI [3] or custom built. Whether it is FERMI or custom built, the ADC system could be on the detector and the digitised information could be transmitted using fibre optic cables to avoid handling large volumes of copper cables. The following are the requirements of the ADC system.

(1) 8-bit (or 9-bit) analogue-to-digital conversion at 40 (or 80) million samples per second.

(2) Bunch-crossing identification [6].

(3) Look-up table for pedestal subtraction and calibration.

(4) Zero suppression and tagging.

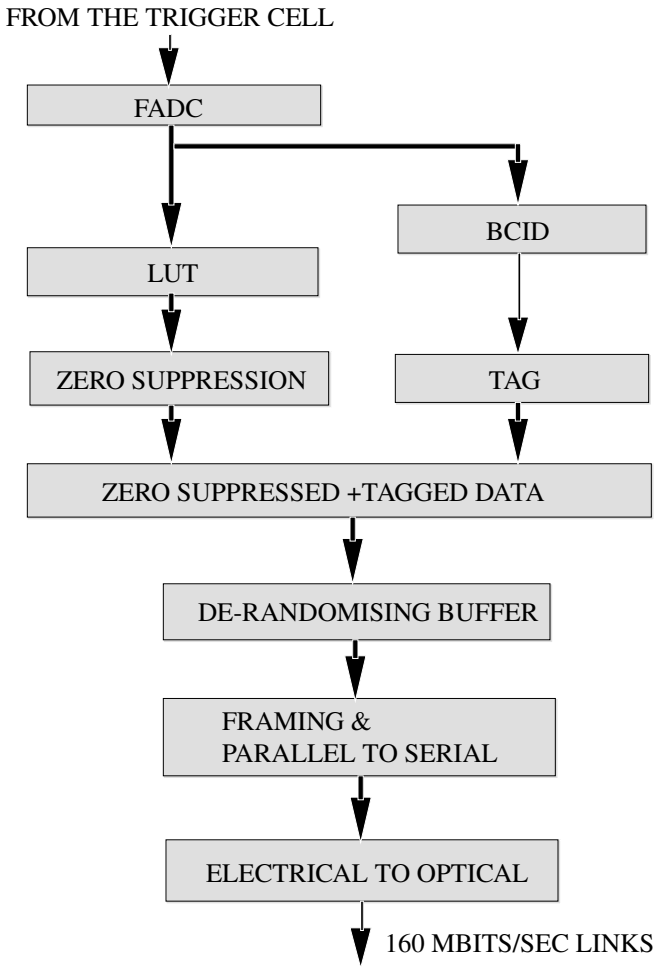
(5) 32-bit derandomising buffer.

(6) Serialise and transmit data at 160 Mbits/sec.

Transmitting data at 160 Mbits/sec requires two bunch-crossings (25 ns) to transmit an 8-bit word. Physics simulation studies show that the occupancy of both the electromagnetic and the hadronic calorimeters will be under 10% for an E_T = 1 GeV threshold using a granularity of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$. It is therefore profitable to reduce the bandwidth using zero suppression. However, given that the analogue signals from the calorimeter are slow compared to the bunch-crossing period, bunch-crossing identification must be applied in addition.

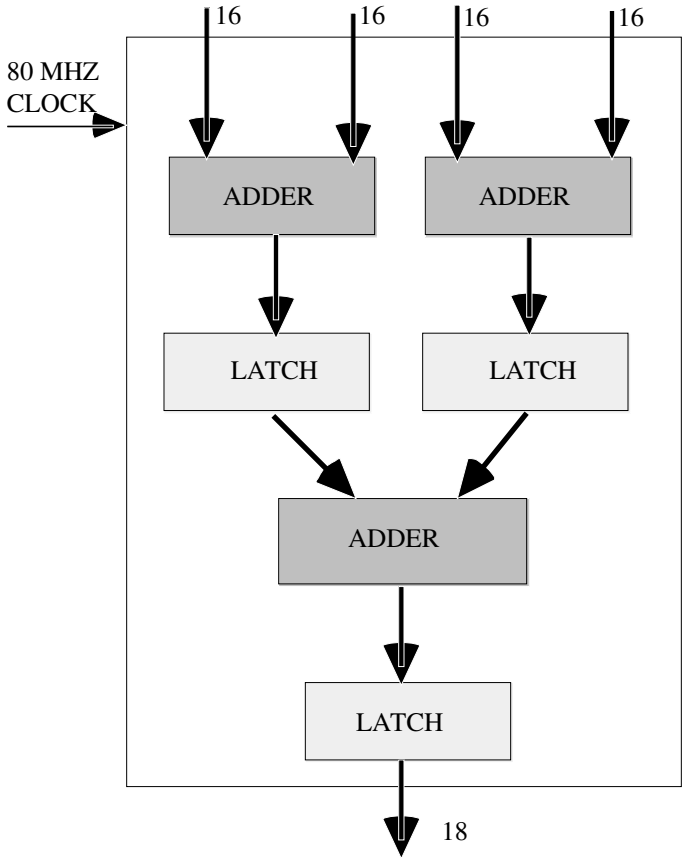
With zero-suppression, a tag (the bunch crossing number modulo 16 or 32) has to be attached to the data since the transmission will be asynchronous. A de-randomising buffer has to be included to average out fluctuations in the rate of arrival of the data. Assuming 16-bits per word, which includes 2 framing bits, 9-bit data and 5-bit tag, the 16-bit word can be transferred in four bunch crossings.

The system becomes synchronous again when the tags are matched on the cluster-finding ASIC. The scheme of tagging has the added advantage of synchronising the data coming from various parts of the calorimeter. Following is a block diagram of the ADC system.


FROM THE TRIGGER CELL
FADC
BCID
LUT
ZERO SUPPRESSION
TAG
ZERO SUPPRESSED +TAGGED DATA
DE-RANDOMISING BUFFER
FRAMING &
PARALLEL TO SERIAL
ELECTRICAL TO OPTICAL
160 MBITS/SEC LINKS

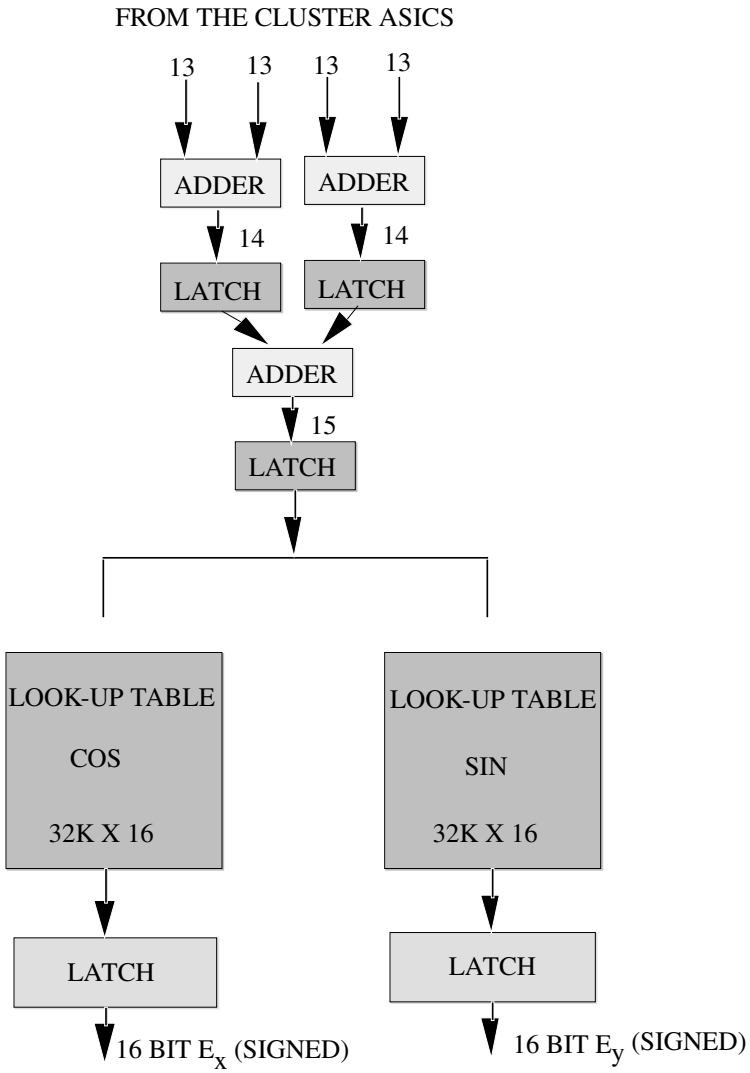
Appendix-2
Adder ASIC

The following type of adder structure, allowing input widths from 5 bits to 16 bits, is required for completing the adder tree in the missing-E_T and declustering logic. An ASIC designed to handle 16-bit adding could be used for the adder tree where necessary. This can be clocked at 80 MHz, so that in effect the adding will take only one 25 ns clock period which will reduce the overall latency of the trigger. The ASIC could be implemented on a 0.8 micron CMOS gate array.



Appendix-3
Missing E_T Calculations

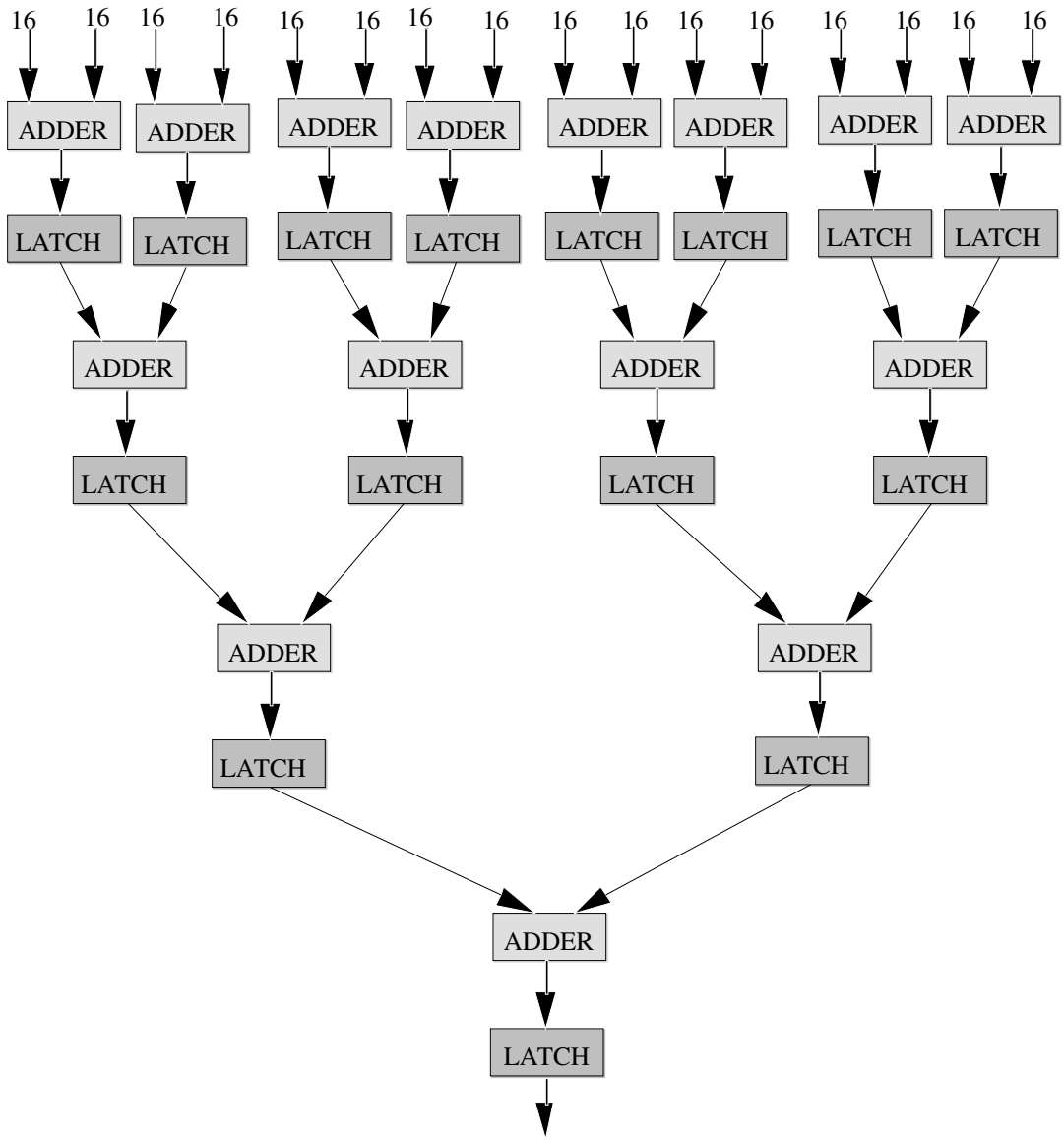
A3.1 On The Processor Board



16 BIT SIGNED SUMS TO THE RESULTS BOARD.

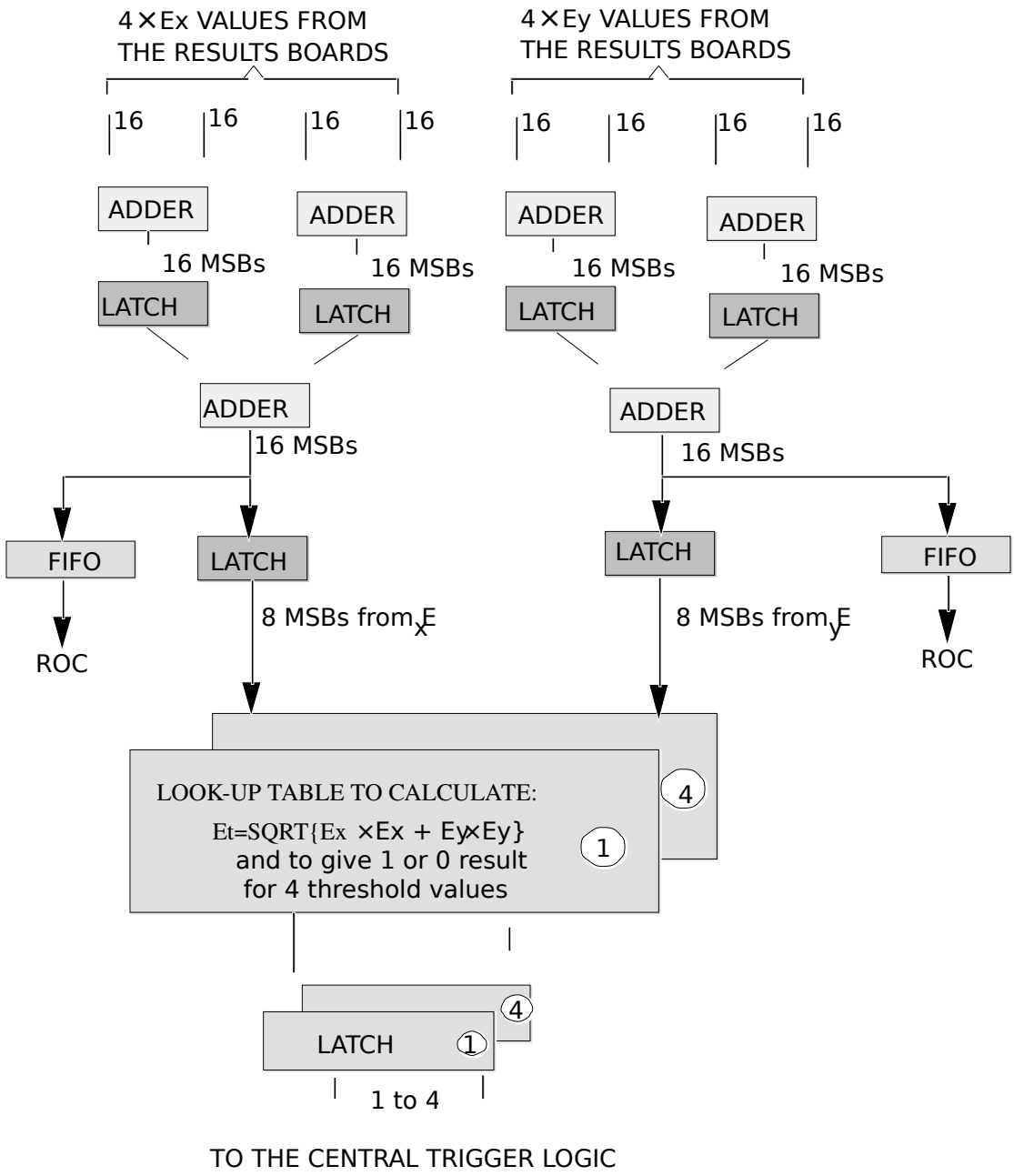
The above shows how the 4 ×13-bit energy sums from the cluster-finding ASICs are summed on the processor board and the resulting 15-bit sum is converted to its E_x and E_y components using a 32k ×16 look-up table. The 16-bit (2's complement) signed result of this is sent on to a results boards on the same crate. There will be a total of sixteen, 16-bit E_x and E_y each from the sixteen processor boards. There will be two results boards on each crate, one will deal with the E_x values and the other with the E_y values.

A3.2 On The Results Board



Each results board will receive the E_x and the E_y values respectively via the backplane. The results board will continue the summing tree and transfer the result (16-bit 2's complement) to the missing-E_T board via twisted-pair cables.

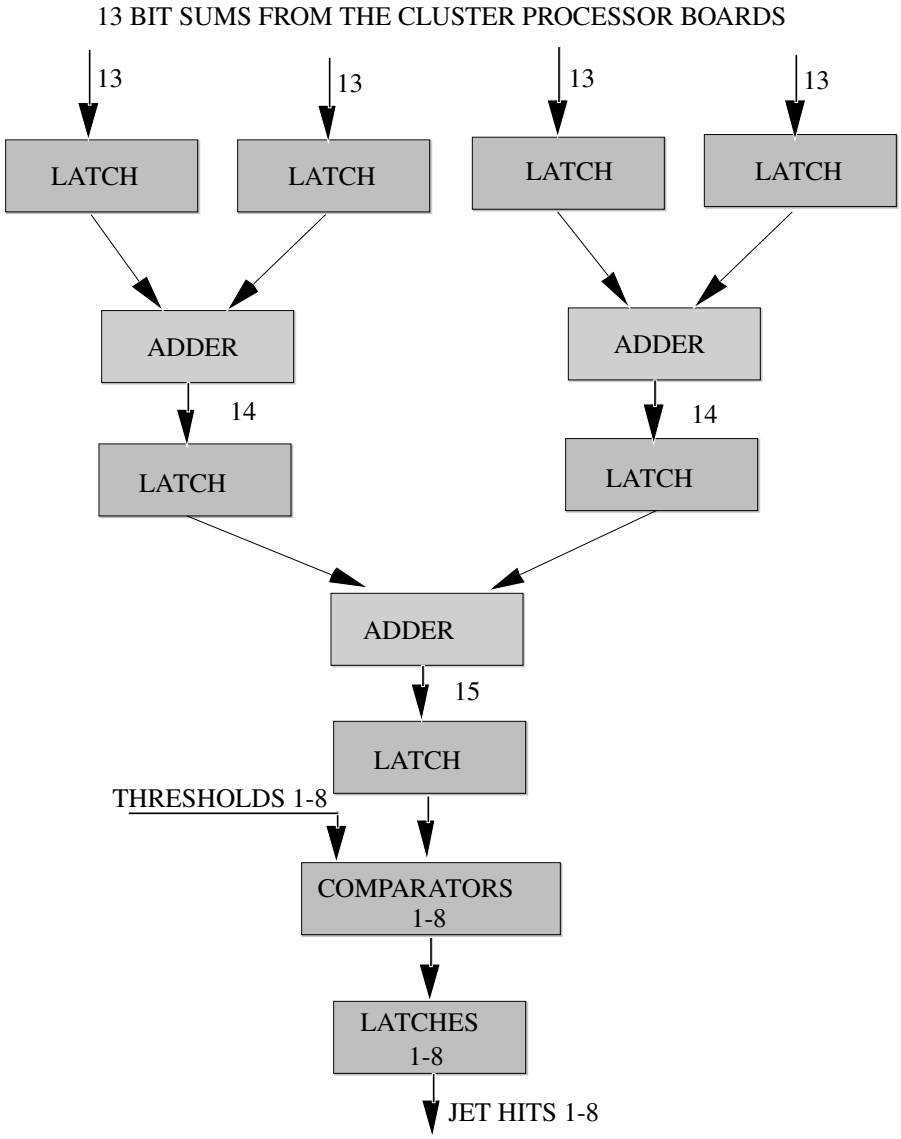
A3.3 On The Missing E_T Board



The missing-E_T board in the system will receive the E_x and the E_y values from the eight results boards. It will complete the adder tree as shown above. The E_T hit is generated by applying the eight most significant bits of the E_x and E_y values to a look-up table to calculate E_T which is: $E_T=\sqrt{(E_X^2+E_Y^2)}$. Four threshold values will be used and the final 4-bit result will be transmitted to the central trigger logic.

Appendix-4
Jet Algorithm

The following diagram shows how the jet algorithm is implemented. The algorithm uses a 2 × 2 sliding widow over the 256 jet cells (13-bit sums from the cluster ASICs). The four cells are summed and then compared with eight threshold values. The jet ASIC will process nine windows in an area of 4 × 4 jet cells using the 2 × 2 sliding window.



Appendix-5
Declustering Algorithm

The declustering of the electrons and the jets is carried out using veto ASICs and adder ASICs as described below:

The veto ASIC vetoes and counts the electrons/jets from a 4 × 4 pixel array. The ASIC counts the cells marked R, provided that the cells marked 1 to 4 are not set. See Figures A5 and A5.1 for details. This process of vetoing and counting is carried out for the entire 256 pixels using 16 veto ASICs and 5 adder ASICs.

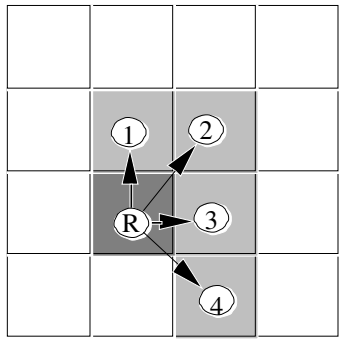


Fig. A5 Vetoing 4 × 4 pixel array

A5.1 Veto and Counting Logic on the Veto ASIC

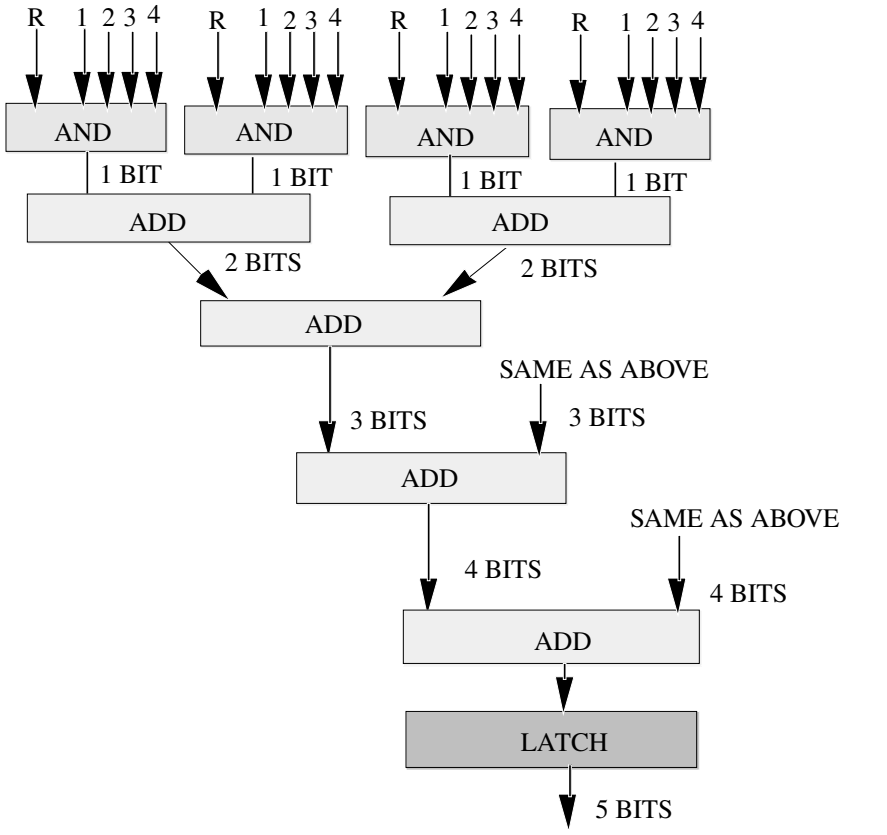


Fig. A5.1 Veto ASIC Logic

A5.2 Completing the Counting.

The 5-bit sums from the 16 veto ASICs will be added together using five of the adder ASICs and then compared with a programmable threshold as shown in Figure A5.2. The result will be transmitted to the central trigger logic via twisted-pair cables.

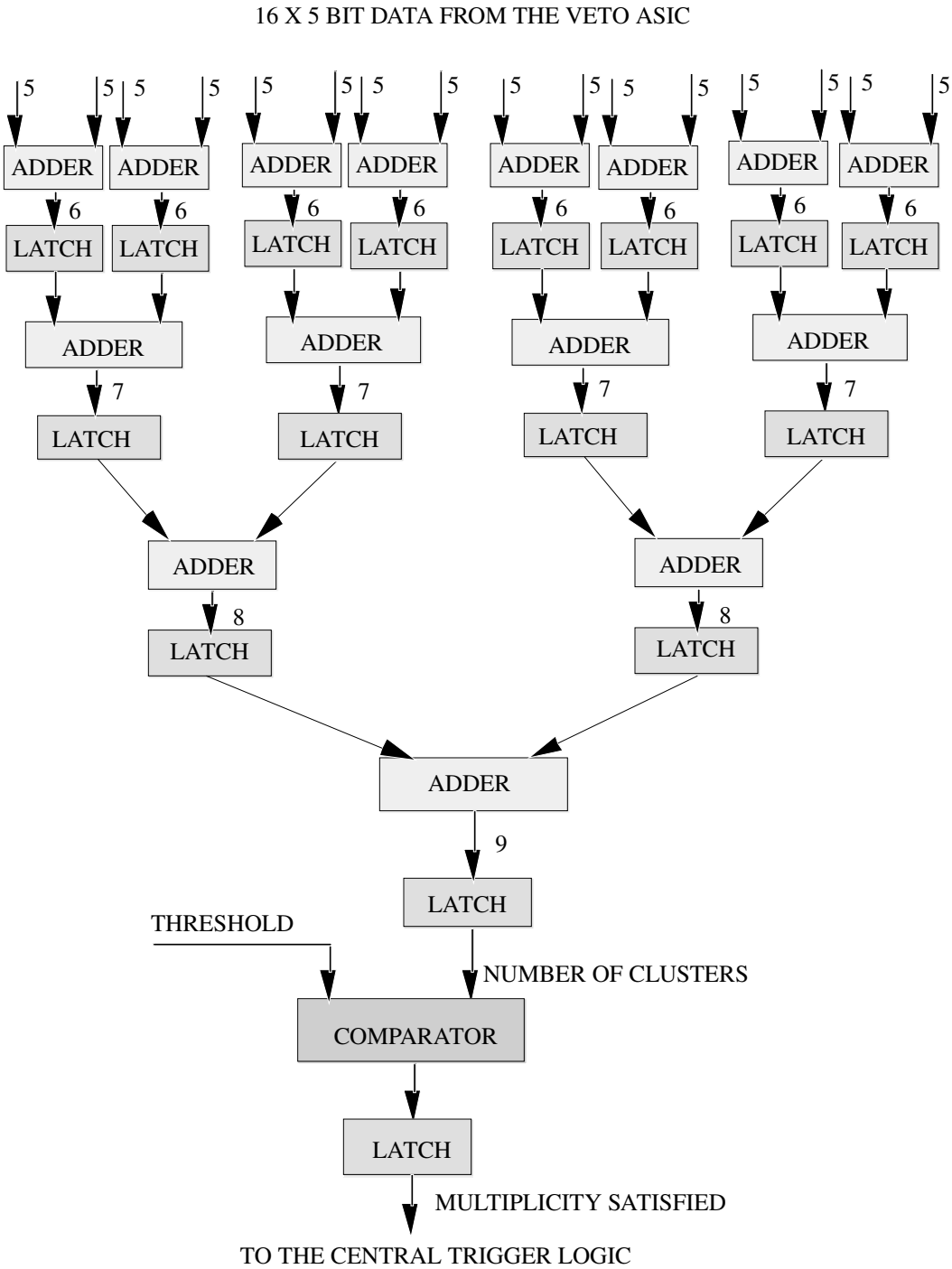
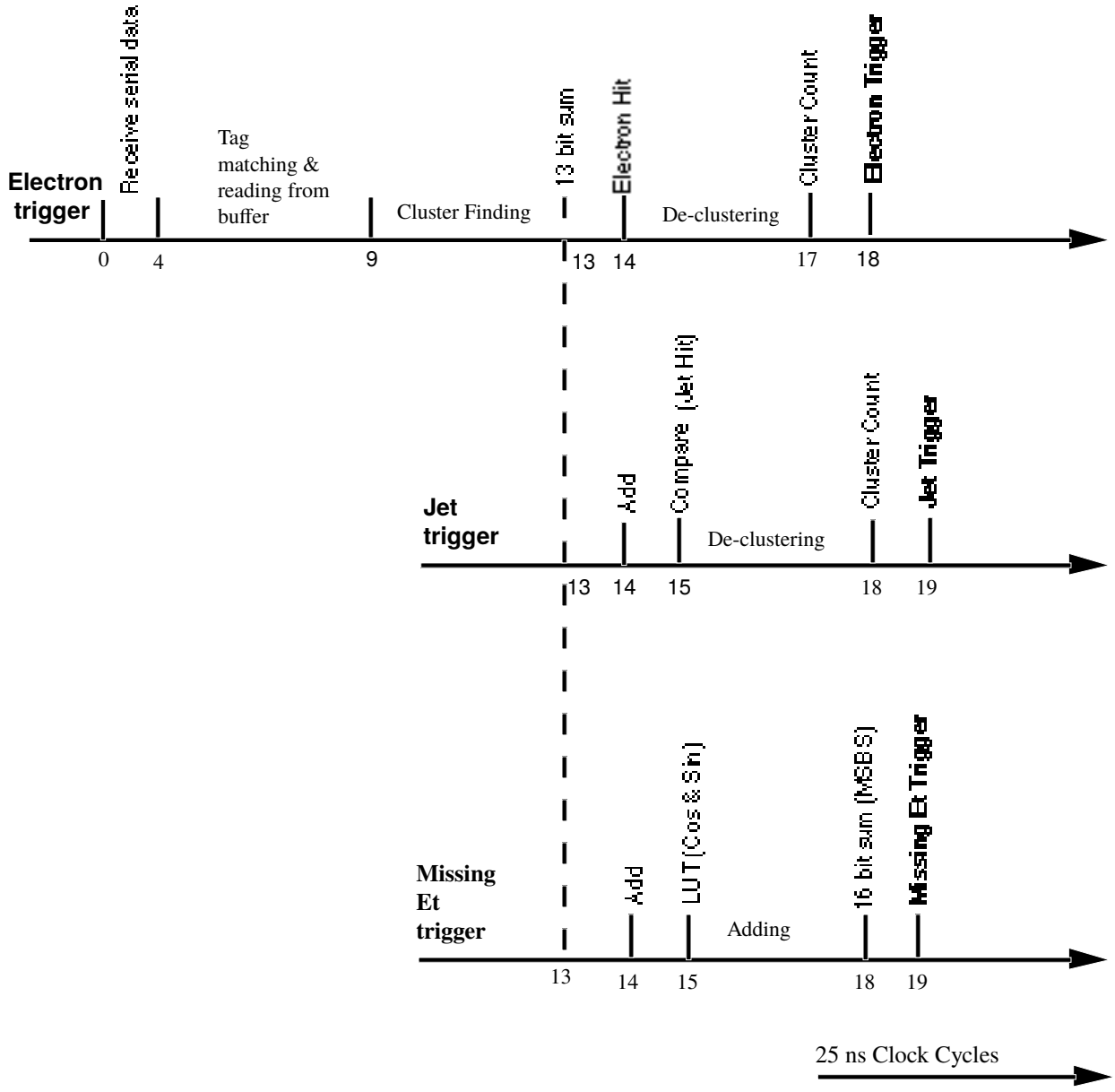


Fig. A5.2 De-Clustering Logic

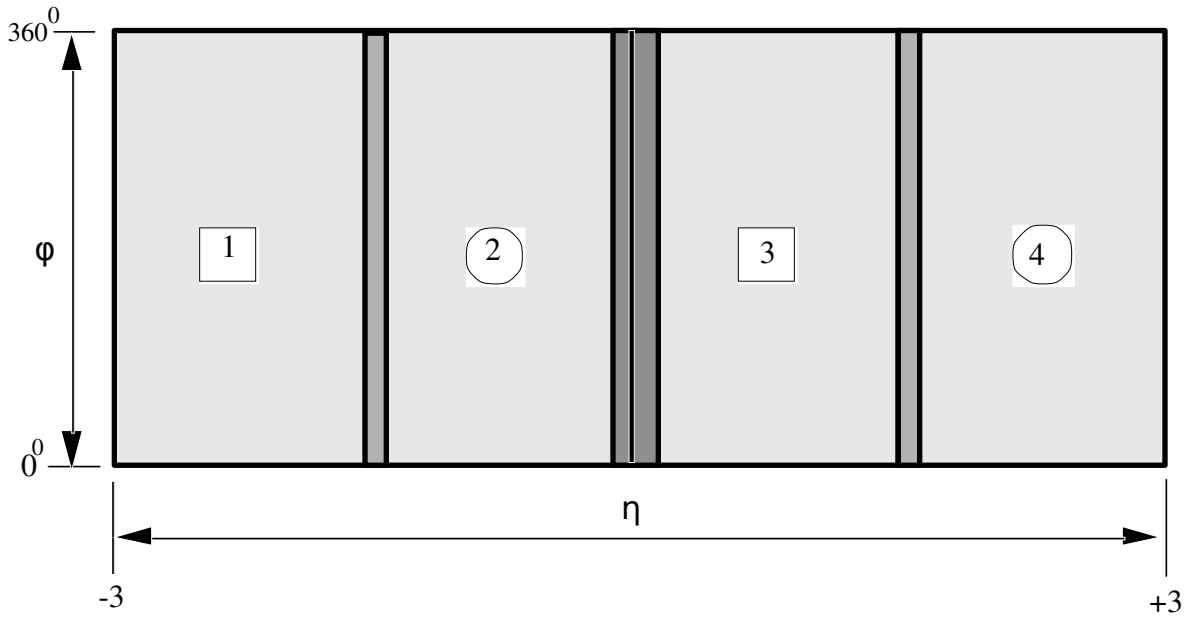
Appendix-6
Trigger Latency

The latency of the trigger system shown below is calculated from the time the data arrive at the cluster processor to the time the trigger decisions are made.

The trigger system is fully pipelined, in steps of 25 ns. The EM cluster trigger takes 18 clock cycles, while the jet trigger and the missing-E_T triggers take 19 clock cycles. If we take the worst case, i.e. 19 clock cycles, then the trigger will have a latency of 475 ns.



Appendix-7
Calorimeter to Cluster Processor Map



The above figure shows how the calorimeter could be mapped onto the four cluster processor crates. Provided that the physical separation of the calorimeter at the endcaps matches 16×64 in η and φ space, each cluster processor crate will fully process 16×64 area of the calorimeter.

The crate-to-crate inter connections are given bellow:

- From/To Crate 1 — No inter-connections are required.
- From Crate 2 to Crate 3 — 2 columns from left = 128 cells
- From Crate 3 to Crate 2 — 1 column from right = 64 cells
- From/To Crate 4 — No inter-connections are required.