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Development and Commissioning of the GigaTracker Data Acquisition and Control Systems for the NA62 Experiment at CERN

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Contents

Introduction

This thesis presents the results of years of work dedicated to the development, commissioning and testing of the NA62 GigaTracker data acquisition and control systems as well as analysis of the data for alignment and quality checking. The GigaTracker beam detector is part of the NA62 experiment at CERN-SPS. The experiment is proposed to provide an accurate measurement of the $K^+ \to \pi^+\nu\bar{\nu}$ rare decay branching ratio.

Flavour changing transitions, the understanding of which is one of the most important objective in particle physics, are described by the Standard Model by means of the Cabibbo-Kobayashi-Maskawa (CKM) unitary matrix. Present experimental data on hadron weak decays are in agreement with Standard Model predictions within theoretical and experimental uncertainties. Nevertheless new physics contributions cannot be ruled out since in most cases theoretical errors on decay amplitudes are large due to long-distance non perturbative contributions. The $K^+ \to \pi^+\nu\bar{\nu}$ however belongs to a limited class of decays in which the matrix elements can be extracted from experimentally well measured decay branching ratios. As a consequence the $K^+ \to \pi^+\nu\bar{\nu}$ branching ratio can be determined with an extremely high accuracy, allowing to determine the possible presence of contributions beyond the Standard Model.

The NA62 experiment aims to collect about 100 $K^+ \to \pi^+\nu\bar{\nu}$ events with a signal to background ratio of S/B $\approx 10/1$ in 2 years of data taking using the decay in-flight of a 75 GeV/c kaon beam. The latest Standard Model prediction for the $K^+ \to \pi^+\nu\bar{\nu}$ branching ratio is $BR(K^+ \to \pi^+\nu\bar{\nu}) = (7.81^{+0.80}_{-0.71} \pm 0.29) \times 10^{-11}$ whilst the only experimental result, based on 7 events, comes from the BNL E787/E949 collaborations and gives $BR(K^+ \to \pi^+\nu\bar{\nu}) = (1.73^{+1.15}_{-1.05}) \times 10^{-10}$.
The presence, in the final state, of two undetectable neutrinos imposes an experimental strategy based on precise timing, kinematic rejection, hermetic vetoes and particle identification to suppress the overwhelming background.

A crucial role in timing and kinematic rejection is performed by the beam spectrometer named GigaTracker. It consists of three stations of hybrid silicon pixels sensors with an overall resolution of 150 ps (RMS) on time, $\sigma(p_K)/p_K \sim 0.2\%$ on momentum and ~ 16 μrad on direction of the track. In addition the system will operate under a high rate of particles i.e. 0.75 GHz in total, with a peak of intensity around the centre of 1.3 MHz/mm^2.
Each GigaTracker station is read out continuously by 10 on-detector chips con-

nected to the same number of off-detector boards where the event data are stored waiting the trigger decision. The trigger-matched output from an entire station is estimated to reach ~ 900 MB/s. A small farm of sub-detector PCs hosts the data acquisition software and the control software, both developed and maintained by the author; the first organizes data and performs higher level trigger matching, while the second controls and configure the front-end and off-detector electronics as well as the data acquisition software itself.

The layout of the thesis is the following: in Chapter 1 an overview of the physics motivations behind the $BR(K^+ \to \pi^+ \nu\bar{\nu})$ measurement, present experimental status and a description of the NA62 experimental strategy to perform such measurement is given; Chapter 2 contains a description of the NA62 detector; in Chapter 3 a detailed overview of the crucial components of the GigaTracker such as the sensor, read-out electronics and cooling system is carried out; Chapter 4 contains a description of the data acquisition and control software characteristics and follows the commissioning of the GigaTracker's data acquisition system during the first three years of NA62 data taking; finally in Chapter 5 the work on the analysis of the GigaTracker's data is reported, with studies on alignment and quality checking.

Chapter 1

Theoretical and Experimental Framework

The main aim of the NA62 experiment is the study of the ultra rare decay $K^+ \to \pi^+\nu\bar{\nu}$. The final goal is to measure the Branching Ratio of this process with a 10% accuracy, in order to provide a stringent test of the Standard Model (SM) predictions or lead to a discovery of deviations from the SM which turns into evidence of new physics

The theoretical framework of the $K^+ \to \pi^+\nu\bar{\nu}$ decay is described in Section 1.1. Among the many rare flavour changing neutral current (FCNC) K and B decays, the ultra rare decays $K \to \pi\nu\bar{\nu}$ play a key role in the search for new physics through underlying mechanisms of flavour mixing. The Branching Ratio can be computed in the framework of the Standard Model to an exceptionally high degree of precision: the prediction for the $K^+ \to \pi^+\nu\bar{\nu}$ channel is $(7.81 \pm 0.75 \pm 0.29) \times 10^{-11}$ [12]. The first error comes from the uncertainty on the CKM matrix elements, the second one is the intrinsic theoretical uncertainty. This decay is one of the best probes for new physics effects complementary to direct searches, especially within non Minimal Flavour Violation models [26]. Since theoretical cleanliness of these decays holds also in these scenarios, even deviations from the SM value at the level of 20% can be considered signals of new physics.

Within the SM, the Branching Ratio value provides a measurement of $|V_{td}|$ free from hadronic uncertainties and independent from that obtained from B meson decays.

The present experimental status is reported in Section 1.2. The decay $K^+ \to \pi^+\nu\bar{\nu}$ has been observed by dedicated experiments E787 and E949 at the Brookhaven National Laboratory and the measured Branching Ratio is $(1.73^{+1.15}_{-1.05}) \times 10^{-10}$ [7]. However only a measurement of the Branching Ratio with at least 10% accuracy can be a significant test of new physics.

Section 1.3 gives details of the NA62 experimental strategy. The goal is collecting about 100 events of the $K^+ \to \pi^+\nu\bar{\nu}$ decay, with a Signal over Background ratio (S/B) of 10/1, in two to three years of data taking. 10^{13} K^+ decays are required, assuming a 10% signal acceptance and a $K^+ \to \pi^+\nu\bar{\nu}$ Branching Ratio of 10^{-10}. The need of reducing the systematic uncertainty, requires a rejection factor for

generic kaon decays of the order of 10^{12} and the possibility to measure efficiencies and background suppression factors directly from data.

1.1 $K^+ \to \pi^+ \nu\bar{\nu}$ theoretical framework

1.1.1 CKM matrix and the Unitarity triangle

The Cabibbo-Kobayashi-Maskawa (CKM) matrix describes the quark flavour-mixing in weak decays within the Standard Model [30]. It is a unitary 3×3 matrix and connects the weak eigenstates (d', s', b') to the corresponding mass eigenstates (d, s, b):

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \equiv \hat{V}_{CKM} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{1.1}$$

One notes that the CKM matrix unitarity ensures the absence of transitions governed by charged currents with flavour change at tree level; this means that elementary vertices involving neutral gauge bosons (gluons, Z^0, γ and Higgs boson H^0) conserves flavour. This property is known as GIM mechanism (S. Glashow, J. Iliopoulos, L. Maiani).

Various parametrization of the CKM matrix exists. The so-called Wolfenstein parametrization [43] foregrounds the hierarchical configuration of the CKM matrix elements absolute values: elements on the diagonal are close to unity, elements $|V_{us}|$ and $|V_{cd}|$ of order 0.2, elements $|V_{cb}|$ and $|V_{ts}|$ of order $4 \cdot 10^{-2}$ and elements $|V_{ub}|$ and $|V_{td}|$ of order $5 \cdot 10^{-3}$.
It is an approximate parametrization of the CKM matrix in which every element is expanded in series of powers with respect to the parameter $\lambda = |V_{us}| \sim 0.22$:

$$\hat{V} = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4) \tag{1.2}$$

The CKM matrix is therefore described by 4 independent parameters, in this case:

$$\lambda\,, \quad A = \frac{|V_{cb}|}{\lambda^2}\,, \quad \rho\,, \quad \eta \tag{1.3}$$

Including order $\mathcal{O}(\lambda^4)$ and $\mathcal{O}(\lambda^5)$ terms, one obtains the generalized Wolfenstein parametrization:

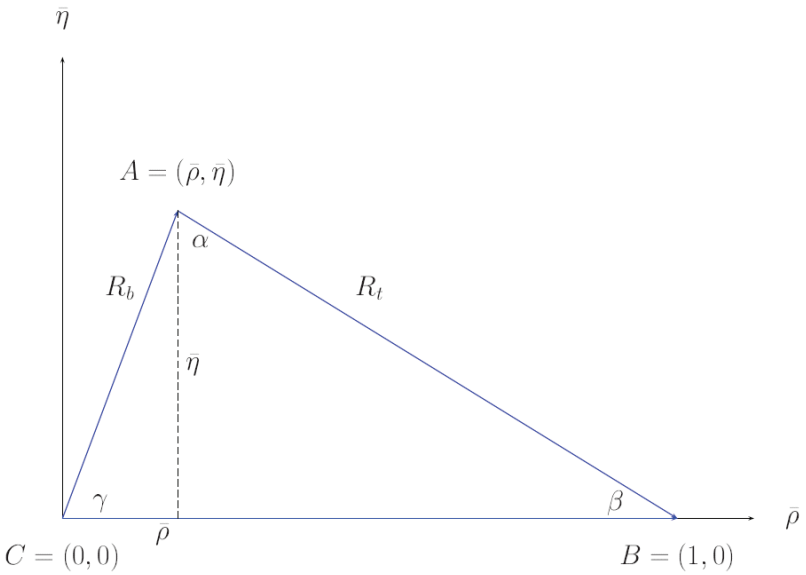


Figure 1.1: Unitarity triangle in complex plane $(\bar{\rho}, \bar{\eta})$.

$$\begin{aligned} V_{ud} &= 1 - \tfrac{\lambda^2}{2} - \tfrac{\lambda^4}{8}\,, & V_{us} &= \lambda \\ V_{ub} &= A\lambda^3(\bar{\rho} - i\bar{\eta})\,, & V_{cd} &= -\lambda + \tfrac{1}{2}A^2\lambda^5[1 - 2(\bar{\rho} + i\bar{\eta})] \\ V_{cs} &= 1 - \tfrac{1}{2}\lambda^2 - \tfrac{1}{8}\lambda^4(1 + 4A^2)\,, & V_{cb} &= A\lambda^2 \\ V_{td} &= A\lambda^3(1 - \bar{\rho} - i\bar{\eta})\,, & V_{ts} &= -A\lambda^2 + \tfrac{1}{2}A\lambda^4[1 - 2(\bar{\rho} + i\bar{\eta})] \end{aligned} \tag{1.4}$$

where $\mathcal{O}(\lambda^6)$ terms are neglected and:

$$\bar{\rho} = \rho\left(1 - \frac{\lambda^2}{2}\right)\,, \quad \bar{\eta} = \eta\left(1 - \frac{\lambda^2}{2}\right) \tag{1.5}$$

After this choice the 4 independent parameters becomes:

$$\lambda\,, \quad A = \frac{|V_{cb}|}{\lambda^2}\,, \quad \bar{\rho}\,, \quad \bar{\eta} \tag{1.6}$$

The CKM matrix unitarity implies the existence of 6 independent orthogonality relations between its parameters, e.g.:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0 \tag{1.7}$$

Relation 1.7 can be represented by an unitarity triangle in $(\bar{\rho}, \bar{\eta})$ plane. See Figure 1.1.

Length of sides R_b and R_t are expressed by relations:

$$\begin{aligned} R_b &= \frac{|V_{ud}V_{ub}^*|}{|V_{cd}V_{cb}^*|} = \sqrt{\bar{\rho}^2+\bar{\eta}^2} = \left(1-\frac{\lambda^2}{2}\right)\frac{1}{\lambda}\left|\frac{V_{ud}}{V_{cb}}\right| \\ R_t &= \frac{|V_{td}V_{tb}^*|}{|V_{cd}V_{cb}^*|} = \sqrt{(1-\bar{\rho})^2+\bar{\eta}^2} = \frac{1}{\lambda}\left|\frac{V_{td}}{V_{cb}}\right| \end{aligned} \tag{1.8}$$

From relations 1.8 trivially derives that angles β and γ are directly bounded to the complex phases of CKM matrix elements:

$$\begin{aligned} V_{td} &= |V_{td}|e^{-i\beta} \\ V_{ub} &= |V_{ub}|e^{-i\gamma} \end{aligned} \tag{1.9}$$

The 1.7 invariance with respect to any phase transformation implies that, under this transformation, the corresponding triangle is rotated in $(\bar{\rho},\bar{\eta})$ plane; since angles and sides in such triangle (given by CKM matrix elements moduli) remain unchanged, they are independent with respect to phase transformations and therefore are physical observables. Angles and sides of the Unitarity triangle can then be directly measured in dedicated experiments.

Let us also note that the areas A_Δ of the 6 unitarity triangles that can be constructed from the 6 orthogonality relations are equal and related to the CP violation measure: $|J_{CP}| = 2A_\Delta$. The current knowledge of the CKM matrix, based on tree decays, such as semi-leptonic K and B decay, can be summarized as [31, 36]:

$$\begin{aligned} |V_{us}| = \lambda = 0.2252 \pm 0.0009\,, \quad |V_{cb}| &= (40.9 \pm 1.1)\times 10^{-3} \\ \frac{|V_{ub}|}{|V_{cb}|} = 0.089 \pm 0.012\,, \qquad |V_{ub}| &= (4.15 \pm 0.49)\times 10^{-3} \end{aligned} \tag{1.10}$$

from which:

$$A = \frac{|V_{cb}|}{\lambda^2} = 0.817 \pm 0.015\,, \quad R_b = 0.40 \pm 0.06 \tag{1.11}$$

The informations enclosed in previous 1.10 and 1.11 indicates that the vertex A of the unitarity triangle lays on the dark-green band in Figure 1.2, which shows the so-called unitarity circle. Tree decays, from which are determined the values of $|V_{us}|, |V_{cb}|, |V_{ub}|$ and consequently R_b, are essentially independent from new physics contribution: these values are then universal constant and valid in every extension of the Standard Model.
The study of other decays is required to determine the exact point where the vertex A lays inside the unitarity circle, most promising of which are the so-called "loop induced" decays and CP violating B decays, sensitive to β and γ angles and to R_t.

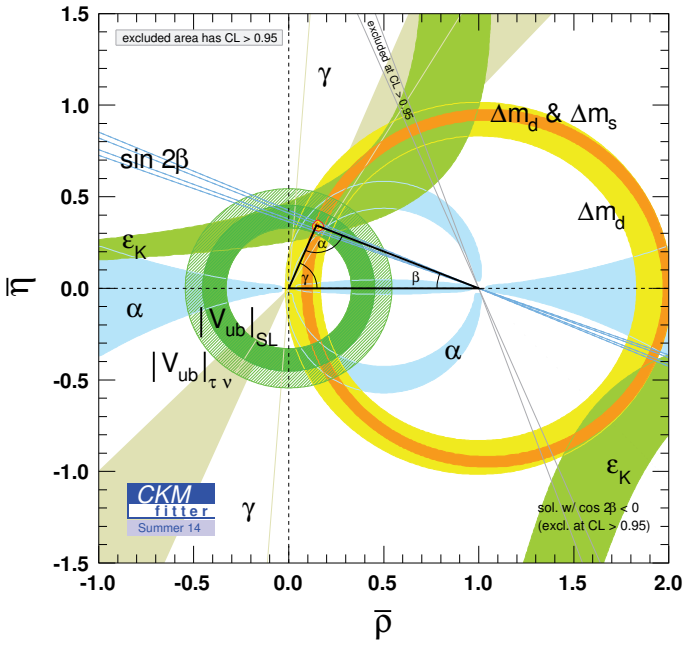


Figure 1.2: Constraints on the Unitarity triangle in the complex plane $(\bar{\rho}, \bar{\eta})$ [19].

The determination of one of the parameters (R_t, β, γ) combined to the knowledge of the universal parameter R_b, or the determination of any parameter couple between (R_t, β, γ) is sufficient to build the unitarity triangle. This should allow to comprehend whether the Cabibbo-Kobayashi-Maskawa representation of the CP violation is correct and more generally if the Standard Model offers a proper description of hadron weak decays.
In the Unitarity triangle language this translates to understanding whether the curves in $(\bar{\rho}, \bar{\eta})$ plane, extracted from various decays and transitions using SM formulas, intersect in the same point, and whether angles (α, β, γ) in the corresponding triangle are in agreement with those extracted from CP violations in B decays and from B decays that conserves CP. Figure 1.2 shows an illustrative situation.

Every inconsistency in the $(\bar{\rho}, \bar{\eta})$ plane can provide a hint of physics beyond the Standard Model.
In this context R_b plays a key role because of its universality, while the other parameters (R_t, β, γ) are in general sensitive to new physics contribution. This means that, assuming the CKM matrix built from 3 quark generations to be unitary and the Standard Model to be part of a wider theory, the Unitarity triangle vertex must lay inside the unitarity circle with radius R_b, determined by decays at tree level.
Thus, even in the case in which SM expression would put $(\bar{\rho}, \bar{\eta})$ outside the uni-

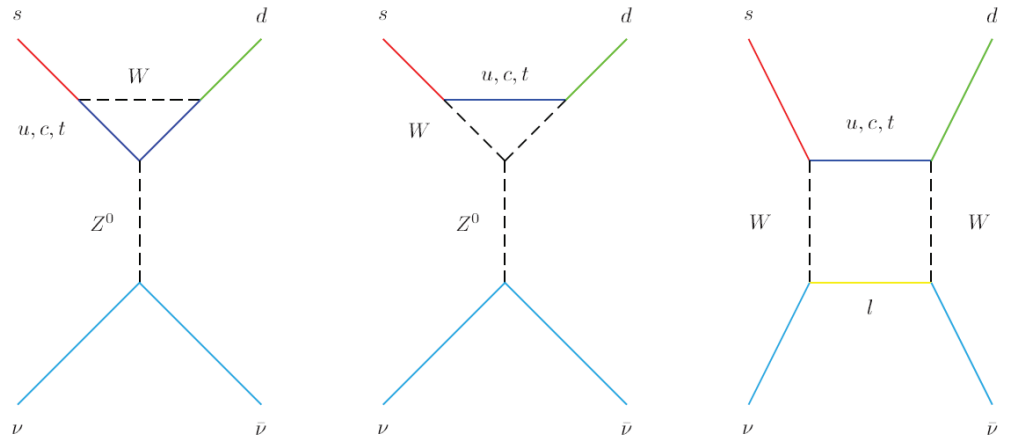


Figure 1.3: Graphs for $s \to d\nu\bar{\nu}$ in the Standard Model.

tarity circle, the corresponding expressions of the wider theory would include properly new contributions capable to put $(\bar{\rho}, \bar{\eta})$ back inside the dark-green band of the unitarity circle in Figure 1.2.
The better is the knowledge of R_b, the thinner becomes the unitarity circle band in Figure 1.2, making possible to select the correct theory. On the other hand a precise knowledge of $|V_{cb}|$ is important since the branching ratios of CP violating rare decays depends significantly from the parameter A.

1.1.2 Branching Ratio of the $K^+ \to \pi^+\nu\bar{\nu}$ decay

In the study of decay amplitudes, long-distance contributions contain low energy strong interaction contributes, not treatable in perturbative way and featuring the main theoretical uncertainty source.
However, rare meson decays exist, whose matrix elements can be extracted, thanks to isospin symmetry, from experimentally measured decay branching ratios. For this reason, the process $K^+ \to \pi^+\nu\bar{\nu}$ represents one of the theoretically clearer meson decays for the study of flavours dynamics.
Since the GIM mechanism is active, tree level processes that can activate this decay do not exist; therefore this process is described by box and penguin diagrams, which are sensitive to short range dynamics. This decay is then extremely useful for deepening the knowledge of flavour dynamics and CKM parameters, and it is a powerful SM test.
At quark level the process that describes this decay is $s \to d\nu\bar{\nu}$, which in the SM originates from electroweak penguins (the first two graphs in Figure 1.3) and box diagrams, the third graph. Since two neutrinos occur in the final state, electromagnetic penguin graphs do not contribute. As a consequence, this decay shows an hard GIM suppression, with a quadratic dependence on up-type quark masses. For this reason the decay amplitude is:

$$A_q \sim \frac{m_q^2}{M_W^2} V_{qs}^* V_{qd}, \quad q = u, c, t \tag{1.12}$$

It follows that up-quark contributions are negligible, as well as the long-distance contributions from the charm; the top-quark contribution dominates, so that $s \to d\nu\bar{\nu}$ is essentially a short-distance process, well described by a low-energy effective Hamiltonian. Let us also note that, in the box diagram case, the exchanged lepton l mass is negligible with respect to quark masses if $l = e, \mu$. Instead, in the τ case, its effects must be considered if the exchanged quark is $q = c$ as τ and c masses are comparable.

Generally, the $s \to d\nu\bar{\nu}$ effective Hamiltonian can be written as [33]:

$$\mathcal{H}_{eff} = \frac{G_l}{\sqrt{2}} \sum_{l=e,\mu,\tau} (\bar{s}_L \gamma_\mu d_L)(\bar{\nu}_{lL} \gamma_\mu \nu_{lL}) + h.c. \tag{1.13}$$

where G_l is the effective coupling constant. Given G_l, the branching ratio is directly related by isospin to the well experimentally measured K^+_{e3} decay [13, 14]:

$$BR(K^+ \to \pi^+\nu\bar{\nu}) = 6 r_{K^+} BR(K^+ \to \pi^0 e^+ \nu) \frac{|G_l|^2}{G_F^2 |V_{us}|^2}; \tag{1.14}$$

here, $r_{K^+} = 0.901$ is an isospin-breaking correction that includes phase-space and QED effects. The effective coupling constant G_l can be expressed as the sum of two contributions, the first arising from an internal top-quark line, the second from a charm-quark [14]:

$$G_l = \frac{\alpha G_F}{2\pi \sin^2 \theta_W} [\lambda_t X_t + \lambda_c X^l] \tag{1.15}$$

where the X_i are the Inami-Lim functions, which parametrize short-distance contributions and $\lambda_i = V^*_{is} V_{id}$.
In terms of the leading-order (LO) contribution:

$$X = \frac{x}{8} \left[\frac{x+2}{x-1} + \frac{3x-6}{(x-1)^2} \ln x \right] \tag{1.16}$$

with $x = m^2/M_W^2$ and m is the mass of the exchanged fermion.

The X coefficients have been computed including several corrections [12]. The theoretical uncertainty on X^l is 2.5% after next-to-next-to-leading order (NNLO) QCD and next-to-leading order (NLO) electroweak corrections are taken into account, leading to a small resulting error on the branching ratio.
For the function X_t, unknown higher-order QCD corrections result in a 1% uncertainty while sub-leading electroweak contribution uncertainties have been calculated to be 0.134% including two-loop electroweak corrections.

The SM prediction for the decay branching ratio is therefore:

$$BR(K^+ \to \pi^+\nu\bar{\nu}) = (7.81^{+0.80}_{-0.71} \pm 0.29) \times 10^{-11} \tag{1.17}$$

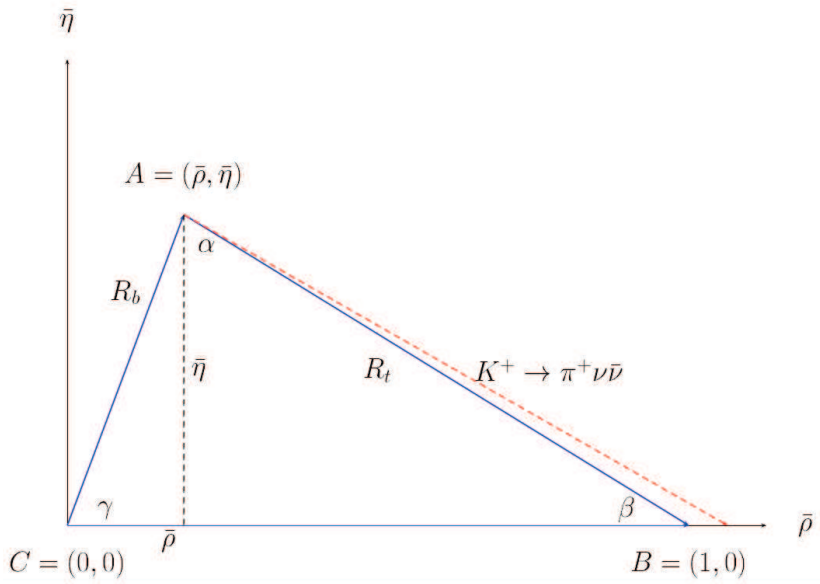


Figure 1.4: Unitarity triangle. The dashed line is proportional to $BR(K^+ \to \pi^+ \nu\bar{\nu})$.

where the uncertainties were separated in order to highlight the first contribution, which is due to the CKM input parameters [12].

The knowledge of $BR(K^+ \to \pi^+ \nu\bar{\nu})$ is extremely important in the determination of the unitarity triangle. In fact this process offers a complementary study of the unitarity triangle with respect to the B physics. Since this decay is sensitive to the V_{td} coupling, its measure can provide a determination of the length R_t in the unitarity triangle, independent from B physics.
Particularly, identifying charm-quark exchange contributions and knowing the well-measured quantities V_{cd}, V_{cs}, V_{ts} in 1.15 from B decays, V_{td} can be experimentally determined (see 1.14) from the measurement of the $K^+ \to \pi^+ \nu\bar{\nu}$ branching ratio. At this point, knowing V_{td} and the well known V_{cb}, is then possible to link the measurement of the branching ratio to R_t as in Figure 1.4.
A deviation from the expected measure would be a strong evidence of the presence of physics beyond the Standard Model.

Particularly, new physics contributions can be introduced through box or penguin diagrams which involve loops of new particle such as charged Higgs, charginos or other supersymmetric particles (Figure 1.5) that replace the W boson and the up-type quark in SM (Figure 1.3).

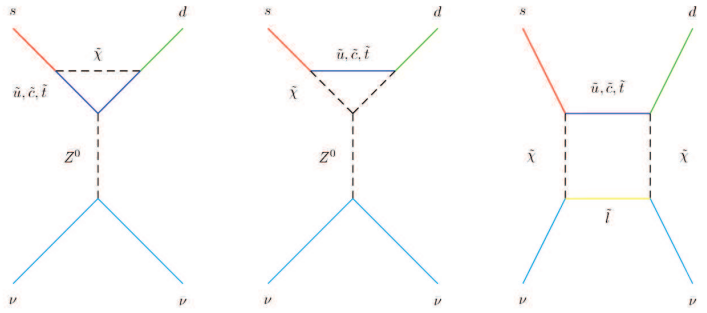


Figure 1.5: Graphs for $s \to d\nu\bar{\nu}$ in supersymmetry.

1.2 Experimental Status

The study of the $K^+ \to \pi^+\nu\bar{\nu}$ decay is not new. The first experimental search for the decay took place in 1969 when experimentalists were looking for neutral currents. Camerini et al. looked at decays of kaons stopped in a bubble chamber filled with Freon and placed in a magnetic field [17]. The collaboration established the basic experimental techniques used in subsequent stopped kaon experiments. Three main criteria were used to disentangle the signal from the other backgrounds. First, a pion decaying at rest had to correspond to each stopped kaon. The pions were identified thanks to the $\pi^+ \to \mu^+ \to e^+$ chain reaction. Second, no detector activity compatible with photons could be seen. Third, the π^+ momentum, calculated by looking at its range, had to be away from the peaks corresponding to the $K^+ \to \mu^+\nu_\mu$ and $K^+ \to \pi^+\pi^0$ decays. The group reported $BR(K^+ \to \pi^+\nu\bar{\nu}) < 5 \times 10^{-5}$ with a 63% confidence level.

Two subsequent stopped kaon experiments were carried on at the Berkeley's Bevatron [28, 16], the advances of the electronics allowed them to record more kaon decays. The incoming particles were stopped in scintillation counters surrounded on one side by spark chambers and on the other side by lead glass Čerenkov counters. A stack of scintillation counters placed on top of the spark chambers was used to determine the range of the produced pion. A Čerenkov detector identified the pions and the kaons in the beam. The groups used the same criteria as the experiment of Camerini et al. to select the signal. They lowered the upper limit to 5.6×10^{-7} with a 90% confidence level.

A similar geometry was used by Asano et al. at KEK [8]. The spark chambers were replaced by multi-wire proportional chambers otherwise the analysis technique was similar as the three previous experiments. The group set the upper limit for the branching ratio at 1.4×10^{-7} with a 90% confidence level.

The E787 experiment and its successor, E949, moved to a "4π" solid angle coverage [9] by equipping both detector hemispheres with drift chambers and stacks of scintillators. The whole apparatus was placed inside a uniform 1 T magnetic field directed along the beam axis. The experiment benefited from a 710-790 MeV/c

beam composed of 75% of kaons. Kaons were stopped in an active segmented target built with scintillating fibers. The photon rejection was assured by electromagnetic calorimeters placed between the target and the drift chambers. The particle momentum was extracted from the bending radius and from the number of triggered scintillator layers. A Čerenkov detector identified and tagged the beam particles. Combining their datasets, E787 and E949 reported the observation of 7 $K^+ \to \pi^+\nu\bar{\nu}$ candidates and established the current best branching ration measurement [6]:

$$BR(K^+ \to \pi^+\nu\bar{\nu}) = (1.73^{+1.15}_{-1.05}) \times 10^{-10}\,. \tag{1.18}$$

1.3 NA62 experimental strategy

The NA62 experiment main goal is to collect about 100 $K^+ \to \pi^+\nu\bar{\nu}$ in two years of data taking, with a background contamination around 10% and a signal acceptance of at least 10%. These requirements can be achieved only using high energy kaons and tracking their decays in-flight. Assuming a 10% signal acceptance and a $K^+ \to \pi^+\nu\bar{\nu}$ branching ratio of 10^{-10}, at least 10^{13} K^+ decays are required to achieve the experiment objectives.
The presence of the two undetectable neutrinos in the final state motivates the necessity of a very accurate kinematic reconstruction to discriminate the various decay channels in order to achieve a signal to background ratio $S/B \simeq 10/1$. The experiment is then required to have the following features:

1. A precise timing to associate the downstream π^+ to the parent K^+.
2. Kinematic rejection of two- and three-body decays.
3. An hermetic veto system to reject events with γ and μ.
4. A system for the identification of K^+s in the charged beam and to distinguish π^+ from μ^+ and e^+ in the final state.

The suppression of $K^+ \to \pi^+\pi^0$ and $K^+ \to \mu^+\nu$ decays is extremely important since they have branching ratios up to 10^{10} times larger than the expected signal. The two-body kinematics reconstruction can be affected from background tails due to the missing detection of photons coming from $K^+ \to \pi^+\pi^0$ or if the muons of the $K^+ \to \mu^+\nu$ decay are wrongly detected as pions. To limit the background caused by two-body decays, kinematic rejection must be employed together with the particle identification (PID). Also three- and four-body decay background can be potentially harmful.
Table 1.1 shows the most frequent K^+ decays modes together with their rejection techniques.

1.3.1 Kinematic rejection

The signal reconstruction is based on one reconstructed track in the downstream spectrometer and one in the beam spectrometer. The kinematics of the decay

Decay mode	BR	Background rejection
$K^+ \to \mu^+\nu$ ($K_{\mu 2}$)	63.55%	μ PID, two-body kinematics
$K^+ \to \pi^+\pi^0$	20.66%	Photon veto, two-body kinematics
$K^+ \to \pi^+\pi^+\pi^-$	5.59%	Charged particle veto, kinematics
$K^+ \to \pi^+\pi^0\pi^0$	1.761%	Photon veto, kinematics
$K^+ \to \pi^0\mu^+\nu$ ($K^+_{\mu 3}$)	3.353%	Photon veto, μ PID
$K^+ \to \pi^0 e^+\nu$ (K^+_{e3})	5.07%	Photon veto, E/p

Table 1.1: The most frequent decay modes of the K^+ meson.

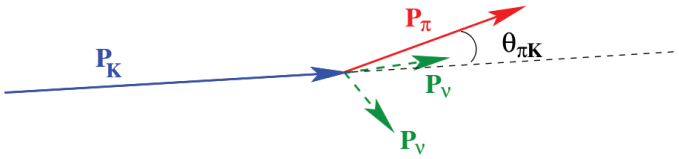


Figure 1.6: Kinematics of the decay under study.

under study is sketched in Figure 1.6, where the incoming kaon momentum P_K, the momentum of the outgoing pion P_π and finally the angle between the parent and the downstream particle $\theta_{\pi K}$, are the only measurable quantities. The kinematics of the most frequent K^+ decays are compared to that of the $K^+ \to \pi^+\nu\bar{\nu}$ in Figure 1.7.
The squared missing mass is considered as the main kinematic variable, defined as $m^2_{miss} \equiv (P_K - P_{track})^2$, where P are the 4-momenta of the particles and the track is assumed to be a π^+.
This quantity can be rewritten using the relation of the invariant mass $m^2_{miss} = E^2_{miss} - \vec{P}^2_{miss}$ and then approximated as:

$$m^2_{miss} \simeq m^2_K \left(1 - \frac{|P_\pi|}{|P_K|}\right) + m^2_\pi \left(1 - \frac{|P_K|}{|P_\pi|}\right) - |P_K||P_\pi|\theta^2_{\pi K} \tag{1.19}$$

The squared missing mass can discern two categories of background: one is kinematically constrained (Figure 1.8) and the other is kinematically not-constrained (Figure 1.9). More than 90% of the total K^+ branching fraction is composed by kinematically constrained decays. Among them, the signal $K^+ \to \pi^+\pi^0$ is the most insidious, being a line at $m^2_{miss} = m^2_{\pi^0}$ (ignoring mass resolution effects), lying within the signal region. The m^2_{miss} of three-body decays has a lower limit. The m^2_{miss} of $K_{\mu 2}$ is not constrained to a line at $m^2_{miss} = 0$ since the muon is considered mis-identified as a pion and then depends on the final particle momentum and has $m^2_{miss} = 0$ as upper bound.
Since the $K^+ \to \pi^+\pi^0$ decay line is placed inside the signal region, it is necessary to split the signal acceptance into two regions:

- Region I: $0 < m^2_{miss} < m^2_{\pi^0} - (\Delta m)^2$
- Region II: $m^2_{\pi^0} + (\Delta m)^2 < m^2_{miss} <$ min $m^2_{miss}(\pi^+\pi^+\pi^-) - (\Delta m)^2$

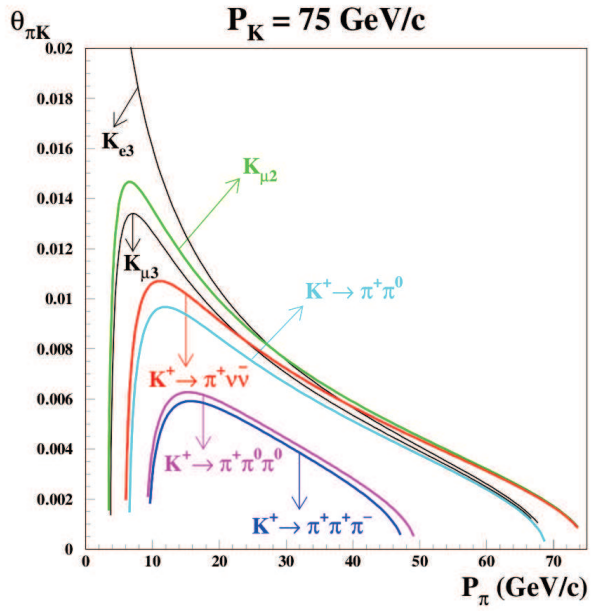


Figure 1.7: A comparison of the charged track angle-momentum relation for the most frequent K^+ decays and $K^+ \to \pi^+\nu\bar{\nu}$. For the three-body decays, the curves indicate the kinematical limit.

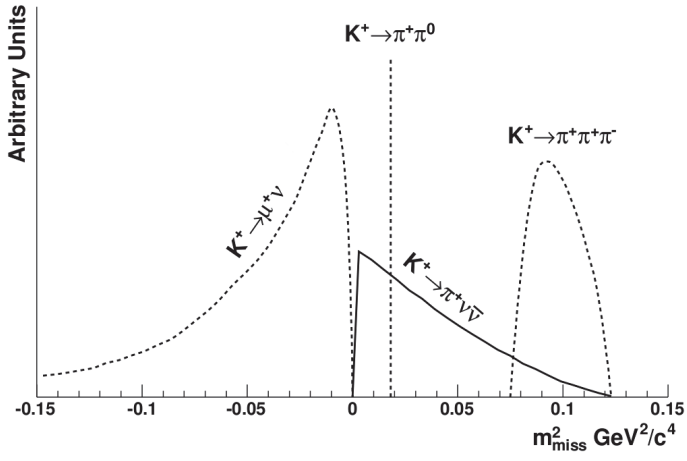


Figure 1.8: Shape of the m^2_{miss} for signal (thick solid line) and background events under the hypothesis that the charged track is a pion. These background sources refer to decays which are kinematically constrained.

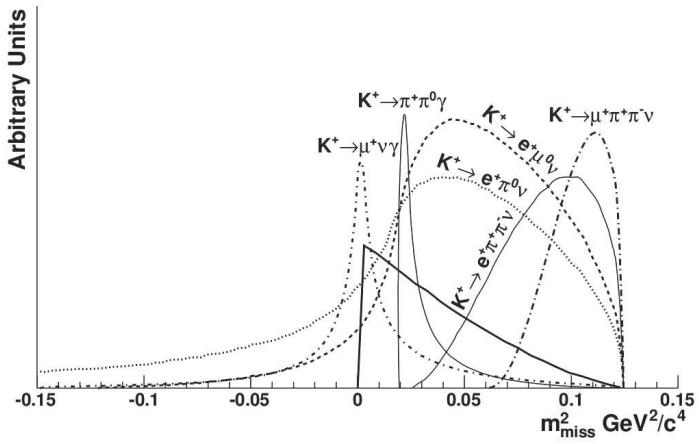


Figure 1.9: Shape of the m^2_{miss} for signal (thick solid line) and background events under the hypothesis that the charged track is a pion. These background sources refer to decays which are kinematically not-constrained.

where the Δm term depends on the m^2_{miss} resolution.
Background can then enter the signal region because of the finite resolution on m^2_{miss}. In order to minimize m^2_{miss} indetermination and consequently lower background contributions, low mass and high precision detectors placed in vacuum are required for the tracking.
The high particle rate on the beam detector (750 MHz) demands a close time correspondence and a good spatial resolution in order to associate the incoming kaon to the downstream pion track. Any missed correspondence between the two tracks causes a loss of kinematic rejection power. A Čerenkov Differential Counter (KTAG) placed on the beam line, the Gigatracker beam tracker (silicon pixel detector) and a RICH (Ring Imaging Čerenkov counter), provide the timing of the experiment. Notably the beam tracker must reconstruct the beam tracks with at least 150 ps time resolution.
The correspondence between the two tracks is reconstructed mainly (apart from timing) using a cut on the closest distance of approach (CDA) between the Gigatracker and the downstream spectrometer. The latter, called Straw Tracker, is positioned in vacuum and provides the track momentum measurement.

Geant4 simulations [23, 24] show a resolution on kaon momentum of about 0.2%, on kaon direction of about 16 μrad, on pion momentum of about $(0.330 \pm 0.007)\% \times P_{track}$ and on pion direction between 45 and 15 μrad. The expected kinematic rejection power against $K^+ \to \pi^+\pi^0$ and $K^+ \to \mu^+\nu$ decays is then about 2×10^4 and 2×10^5, respectively. The limitation comes from the non-Gaussian tails from multiple scattering in the detector materials and from a possible K^+ - π^+ mismatching.

1.3.2 Vetoes

The requested level of background suppression needs an additional factor coming from γ and μ detection, since the kinematic rejection alone cannot respect the requirements. Particularly the rejection of the $K^+ \to \pi^+\pi^0$ decay, with the requirement of a 10^{-8} inefficiency for π^0 detection, is the main point in the design of the photon veto system. A photon detector system that can hermetically cover an angular region up to ≈ 50 mrad around the beam axis is then required. The detectors designed for this purpose are, in order of increasing angular coverage: SAC (Small Angle Calorimeter) and IRC (Intermediate Ring Calorimeter) covering respectively forward and small angles ($\lesssim 1$ mrad), the Liquid Krypton electro-magnetic calorimeter (LKr) covering the region between 1 and 8.5 mrad and finally 12 Large Angle photon Veto (LAV) detectors covering the region between 8.5 and 50 mrad.

The key points to fulfil the experimental goals are:

- A cut at 35 GeV/c in the maximum π^+ momentum at analysis level to deal with π^0 of at least 40 GeV/c as a consequence of the 75 GeV/c kaon momentum.
- A detection inefficiency below 10^{-5} for γs in the $1 - 10$ mrad region above 10 GeV and, anyhow, within 10^{-3} for γ down to 1 GeV.

Since the largest fraction of K^+ decays contains muons in the final state, a muon veto system is mandatory. The Muon Veto system (MUV), placed at the end of the experimental apparatus, consists of two iron-scintillator hadronic calorimeter (MUV1 and MUV2) and, behind an iron wall, a plane of fast scintillators (MUV3). The MUV system is placed at the end of the apparatus. Monte Carlo simulations predict an overall inefficiency for muon detection of about 10^{-5}, achievable by exploiting the electromagnetic and hadronic shower separation capability of the hadronic and LKr calorimeters together. Further muon rejection is provided by the Ring Imaging Čerenkov counter (RICH).

Finally a veto for charged and neutral particles placed just downstream of the last GTK station, provides additional rejection of the accidental background coming from hadronic interactions of the beam particles in the last GTK station. This detector, called CHANTI, consists of scintillators surrounding the beam.

1.3.3 Particle Identification

Kinematically not-constrained backgrounds (Figure 1.9) are the 8% of the total branching and are shown partially in Table 1.2. These backgrounds cannot be suppressed by the kinematic rejection and vetoes alone. The needed additional 10^2 factor in the background rejection will come from a particle identification system complementary to the calorimeters. A RICH has been designed to fulfil such a goal: it should separate π^+ from μ^+ with inefficiency below 1% in the relevant momentum range. It must also provide the timing of the event with a

Decay mode	Branching ratio
$K^+ \to \pi^0 e^+ \nu$ (K^+_{e3})	$(5.07 \pm 0.04)\%$
$K^+ \to \pi^0 \mu^+ \nu$ ($K^+_{\mu 3}$)	$(3.353 \pm 0.034)\%$
$K^+ \to \mu^+ \nu\gamma$ ($K_{\mu 2\gamma}$)	$(6.2 \pm 0.8) \times 10^3$
$K^+ \to \pi^+\pi^- e^+ \nu$ (K_{e4})	$(4.09 \pm 0.10) \times 10^5$
$K^+ \to \pi^+\pi^- \mu^+ \nu$ ($K_{\mu 4}$)	$(1.4 \pm 0.9) \times 10^5$

Table 1.2: Some K^+ not-kinematically constrained decay modes.

resolution below 100 ps.

The LKr is a powerful particle identifier, not only for muons, as stated before, but also for positrons and electrons. It is, therefore, a viable option to complement the RICH in the suppression of final states with $e^\pm$. The π - e separation is possible, thanks to the LKr excellent energy resolution, by means of the E/p measurement.

Since about 93% of the beam particles are π^+ or protons, the positive identification of the K^+ is also important in the experiment. In fact these particles can produce a signature that can be associated to the signal by means of interaction with the residual gas contained in the vacuum tank. The K^+ identification is achieved by the KTAG, operated to be blind to all particles but kaons of appropriate momentum.
The KTAG will also improve the rejection of candidates originating from pion and proton interactions on the last GTK station.

1.3.4 Sensitivity

A sensitivity analysis has been performed using Geant4 based simulations [24]. Results shows Region I acceptance to be $\approx$ 3.5% while Region II acceptance $\approx$ 10.9%. The overall acceptance is then about 14.4%, showing that the target of 10% of signal acceptance is safely achievable even taking into account efficiency losses caused by dead times and additional inefficiencies occurring in a real data taking.
The use of the RICH constrains the accepted pion tracks within the $(15 - 35)$ GeV/c momentum range. The higher cut is an important loss of signal acceptance, but assures that events like $K^+ \to \pi^+\pi^0$ deposit at least 40 GeV of electromagnetic energy, making their rejection easier.

Many sources of background have been considered and just a simple counting of signal and background events in the signal regions indicates that the 10% background appears to be within reach.

Chapter 2

The NA62 experiment

In this Chapter, a brief description of the beam and main detectors of the NA62 experiment will be given. Main references used in this chapter are [23, 22].

2.1 Beam for the experiment

The charged kaon beam for the experiment is derived from the primary proton beam at 400 GeV/c of the SPS impinging a beryllium target. With the use of an empirical formula has been calculated that the maximum K^+ production, per primary proton at fixed momentum p_0, occurs for $p_K \approx 0.35 \times p_0$. In addition K^+ production increases as p_K^2 (and also as p_0^2).
It can be calculated that the maximum number of K^+ decays, in the defined fiducial length constrained by detector geometry, is maximum when $p_K \approx 0.23 \times p_0$ and it increases as p_K (and therefore as p_0). Moreover, at higher energy, detectors like calorimeters, photon- and muon-veto counters, have better performances in terms of acceptance, resolution and efficiency. The choice of a positive kaon beam is motivated by the ratio of the production rates: $K^+/K^- \approx 2.1$ (for a 400 GeV/c proton beam).
A kaon momentum of 75 GeV/c has been chosen as central value. This is a compromise of the parameters listed in Table 2.1.
The number of produced K^+ and the percentage in the beam increases with the momentum, but there are other aspects to take into consideration: the distance of the decay region (102 m from target), the length of decay region itself (65 m) and the detector acceptance (particles near the beam pipe can not be detected).

The hadron beam is derived from the existing target station T10. The elements are installed along the K12 beam line in Hall ECN3 at SPS North Area.
The 102 m long beam line selects a 75 GeV/c, narrow momentum-band (1.2% RMS), beam with an average rate of 750 MHz distributed on a 14 cm^2 area. The secondary beam is positron-free and composed by $\sim 6\%$ of K^+. The described beam line should produce 5×10^{12} K^+ decays assuming a 65 m decay region and 100 run day at 60% efficiency.

Beam characteristics		60 GeV/c	75 GeV/c	120 GeV/c
Fluxes at production for 10^{12} incident protons per s	$p \times 10^6$	89	171	550
	$K^+ \times 10^6$	40	53	71
	$\pi^+ \times 10^6$	353	532	825
	Total $\times 10^6$	482	756	1446
Survival factor over 102 m	K^+	0.797	0.834	0.893
	π^+	0.970	0.976	0.985
Fluxes at 102 m from target for 10^{12} incident protons per s	$p \times 10^6$	89	173	550
	$K^+ \times 10^6$	32	45	63
	$\pi^+ \times 10^6$	343	525	813
	Total $\times 10^6$	464	743	1426
Decays in 60 m fiducial length for 10^{12} incident protons per s	$K^+ \times 10^6$	3.9	4.5	4.1
	$\pi^+ \times 10^6$	6.1	7.4	7.2
K^+ decays / π^+ decays in 60 m		0.64	0.61	0.57
K^+ decays in 60 m / total hadron flux	$\times 10^{-3}$	8.4	6.1	2.9
$K^+ \to \pi^+ \nu\bar{\nu}$ acceptance (Region I, no p_π cut)		0.08	0.11	0.11
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ / 10^{12} protons per s	$\times 10^6 \times BR$	0.31	0.50	0.45
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ / π^+ decays in 60 m	$\times BR$	0.052	0.067	0.062
Accepted $K^+ \to \pi^+ \nu\bar{\nu}$ / total hadron flux	$\times 10^{-3} \times BR$	0.67	0.67	0.31

Table 2.1: Criteria for the choice of the beam momentum.

The beam line design employs a triplet of radiation-resistant acceptance quadrupoles to focus the beam to the mid-point of a front-end achromat, which is composed of four dipole magnets to provide momentum selection and recombination. In the middle of the achromat the wanted beam is displaced vertically downwards by 100 mm, allowing its momentum band to be defined and primary protons and unwanted secondary hadrons to be dumped in the two motorized dump/collimator units (TAX), among which the e^+ radiator is located. A subsequent quadrupole triplet refocuses the beam through a collimation and muon-sweeping stage.

A quadrupole doublet then renders the beam parallel, matching it to the KTAG differential Čerenkov counter. A final quadrupole doublet is used to match the beam to the spectrometer and tracking system, whilst limiting the beam size in the apertures of the downstream detectors.
The beam tracking system consists of three GigaTracker (GTK) stations installed in vacuum. These are rearranged so that the space between GTK 1 and 3 is occupied by a toroidally magnetized muon scraper and a second achromat of four C-shaped dipole magnets, with their yokes arranged so as to enhance the defocusing action of the scraper for μ^+. In the middle of the second achromat, where GTK 2 is located, the magnets cause a parallel displacement of the 75 GeV/c beam by +60 mm in the horizontal plane to provide the momentum measurement. GTK 3 is placed after the final (variable) cleaning collimator and is followed by a guard-ring of scintillation counters (CHANTI) mounted in vacuum.

The opposite deflections of the last two magnets of the second achromat are actually so tuned that the beam is centred at GTK 3, but is directed away from the axis by -1.2 mrad in the horizontal plane. This angle is chosen so that the subsequent Single Spectrometer magnet will deflect the beam back into the central aperture of the LKr calorimeter.
The magnet provides a p_T-kick of +270 MeV/c, giving a +3.6 mrad deflection to the +75 GeV/c beam. In conjunction with the upstream deflection of -1.2 mrad, the beam thereby converges to the undeflected beam axis at a point near the exit of the LKr calorimeter.

The beam is finally deflected to the side by a 3 m long dipole magnet which provides a +1620 MeV/c p_T-kick (+21.6 mrad deflection) and dumped in a concrete plug inside an hole at the end of Hall ECN3.

2.2 Detectors

In this section will be given a description of each sub-detectors. The following detectors and features are incorporated in the NA62 layout (see Figure 2.1).

To better understand Figure 2.1 refer to the acronyms list below:

- KTAG
  A differential Čerenkov counter placed on the incoming beam to tag the

minority particles of interest (kaons).

- GigaTracker (GTK)
  Thin silicon micro-pixel detectors for direction and momentum measurement of the incoming beam particles with sub-nanosecond time resolution to provide a tight time coincidence between the incoming kaon and the outgoing pion before entering the decay region.

- CHANTI (Charged ANTI counter)
  A set of six ring scintillation anti-counters positioned after the last GTK station to form a guard-ring at the beginning of the decay region to provide a veto to charged particles outgoing from the collimator and produced from strong interactions in GTK 3.

- LAV (Large Angle Veto)
  A set of 12 ring-shaped scintillation anti-counters surrounding the vacuum tank and providing full coverage for photons originating from the decay region with angles between 8.5 and 50 mrad.

- Straw Tracker
  A magnetic spectrometer measuring the direction and momentum of the outgoing charged decay products. Four chambers of straw tubes are used as the tracking detector for their capability to operate in vacuum along with a dipole magnet.

- RICH
  A gas Ring Imaging Čerenkov counter providing muon/pion separation.

- CHOD (Charged Hodoscope)
  A charged-particle hodoscope, positioned between the RICH and the LKr calorimeter, covering the acceptance and providing a veto for interactions in the RICH material.

- LKr (Liquid Krypton Calorimeter)
  An high-resolution electromagnetic calorimeter acting as photon veto in 1 to 8.5 mrad region.

- MUV (Muon Veto)
  Two-part hadron calorimeter followed by an additional iron and a fast scintillator muon veto. This system supplement and provides redundancy with respect to the RICH in the detection and rejection of muons and to measure pion energy.

- IRC (Intermediate Ring Calorimeter) and SAC (Small Angle Calorimeter)
  Intermediate ring and small angle photon veto calorimeters covering the angular regions around and in the beam.

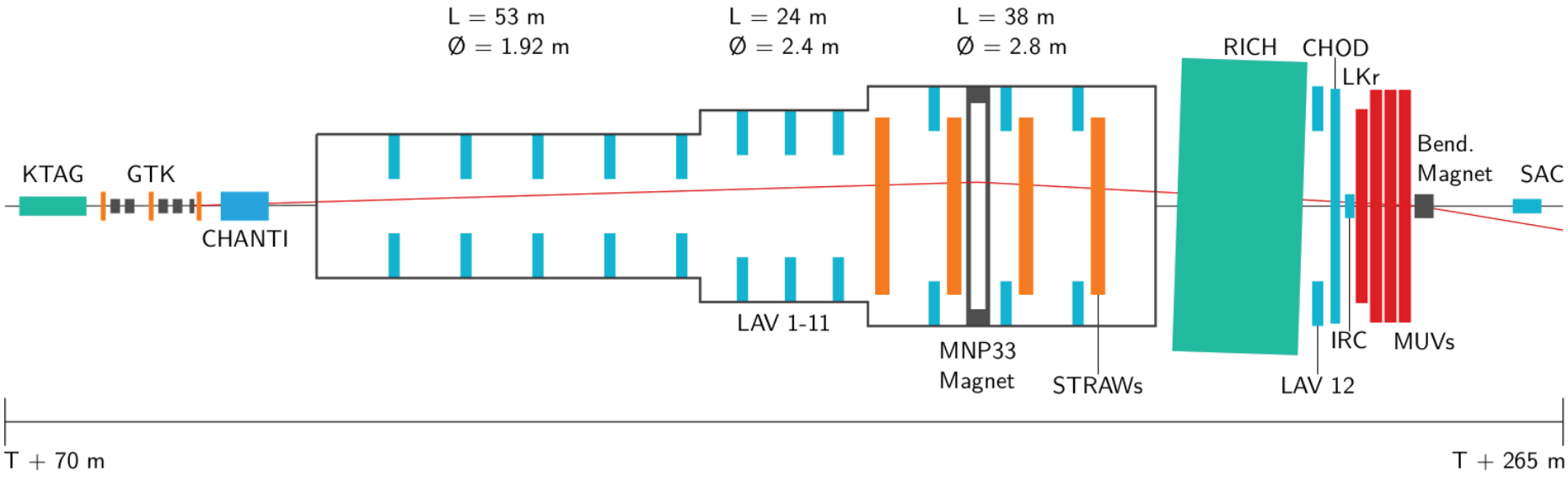


Figure 2.1: Longitudinal view of the NA62 experimental setup.

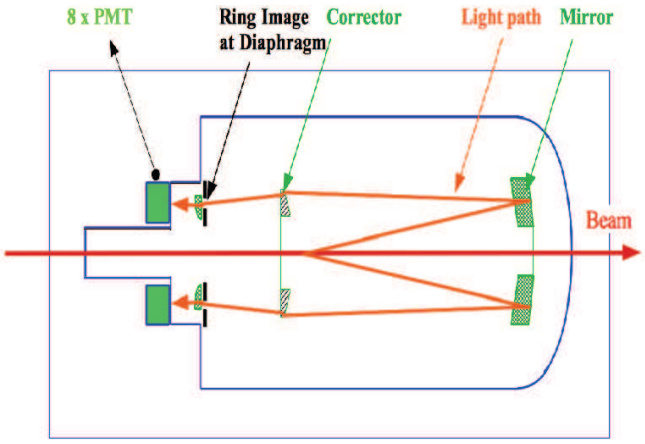


Figure 2.2: Schematic layout of KTAG detector.

2.2.1 KTAG

The KTAG consists of a pressure vessel of 558 mm diameter and $\sim$ 5 m long, filled with gas maintained at a precisely controlled pressure. A spherical Mangin mirror placed at the downstream end of the vessel reflects the Čerenkov light onto a ring-shaped diaphragm of 100 mm radius with adjustable aperture width, located at the beginning of the vessel as in Figure 2.2. Eight sectors equipped with 48 photo-multipliers are placed behind the slit; the coincidence of at least 6 of them will indicate the passage of a particle of the wanted mass since Čerenkov angle of the light produced by the particles traversing the vessel is function of their masses. Trimming the pressure of the gas it is possible to transmit through the diaphragm only the light produced by a K^+ particle at a given angle, whilst light associated to protons and pions will be stopped. The rate in the detector is limited to 50 MHz, which corresponds to the kaon rate in the beam.
Finally, to increase the efficiency of the light collection, a system of corrector lenses redirect the light rays to the diaphragm with the same radius independently on the wavelength and point of emissions.

NA62 uses an updated version of the West CEDAR built for the SPS secondary beams. The main characteristics are listed in Table 2.2. The KTAG detector is required to achieve a kaon efficiency of at least 95%, with a time resolution of 100 ps. Multiple photo-detectors were developed to achieve a singles rate on each pixel not higher than 3 MHz mm^{-2}. The KTAG includes upgraded optics, photo-detectors, associated mechanics and electronics.

2.2.2 GigaTracker

The beam spectrometer is one of the key elements for the NA62 experiment. It has to provide a precise time, angle and momentum measurement of all the incoming particles in the 75 GeV/c beam. In particular the GTK has to measure

Gas type	H_2
$n-1$	$\sim 142 \times 10^{-6}$
Nominal pressure for kaons	3.85 bar
θ_K	30.9 mrad
Kaon rate	50 MHz
Time resolution	< 100 ps
$\Delta\theta/\theta$	4.8×10^{-3}
$\Delta\beta/\beta$	5×10^{-6}
Number of photons per kaon	100
Rate per photomultiplier	3 MHz

Table 2.2: Characteristics and resolutions of the KTAG.

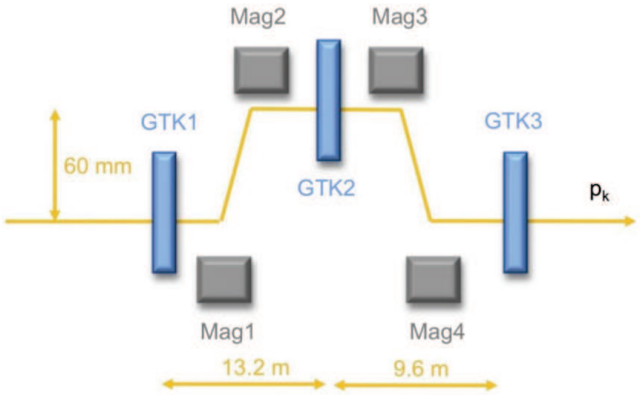


Figure 2.3: Layout of the GigaTracker stations.

the momentum with relative resolution of $\sigma(p_K)/p_K \sim 0.2\%$ and the direction with a resolution of $\sim$ 16 µrad. The detector is exposed to a very high and non-uniform beam rate of 0.75 GHz in total, with a peak of intensity around the centre of 1.3 MHz/mm^2. The GigaTracker is composed of three stations of hybrid silicon pixels sensors mounted on the beam around four dipole magnets and inside the vacuum tank as in Figure 2.3. The distance between GTK1 and GTK2 is 13.2 m, between GTK2 and GTK3 is 9.6 m. To compensate the vertical bending of the beam at the achromat the GTK2 is displaced vertically by 60 mm. Each station covers an area of $60.8(x)$ mm $\times$ $27.0(y)$ mm, matching the expected beam dimension, and is subdivided in (300×300) µm^2 hybrid p-in-n (or n-in-p) pixels with 200 µm thickness. Pixels are arranged in 10 $12.0(x)$ mm $\times$ $13.5(y)$ mm matrix, each with 1800 pixels as in Figure 2.4. The pixel thickness is a compromise between the request of a small material budget to avoid multiple scattering and the need of a sufficient charge yield ($\approx$ 15000 e^-). Table 2.3 summarizes the material budget of the active components in the beam. The required time resolution of the GTK on every single track is $\approx$ 150 ps (RMS) to resolve the high intensity beam. The stringent time resolution requires a design where the

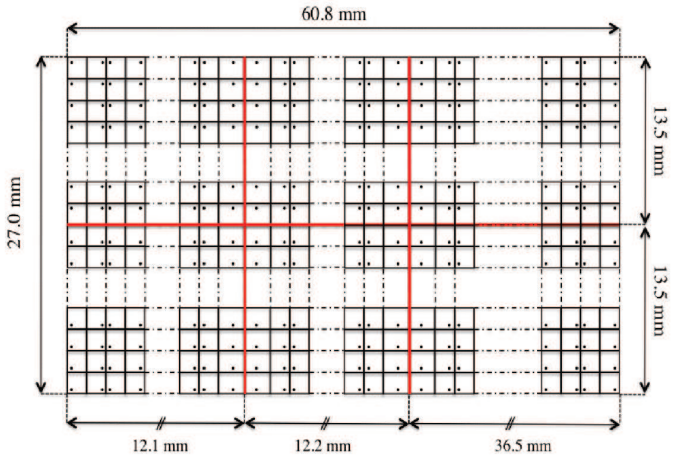


Figure 2.4: Layout of the GigaTracker sensors.

Component	Material	Thickness [μm]	X_0[%]
Sensor	Si	200	0.22
Bump bonds	Pb-Sn	~ 25	0.001
Readout chip	Si	100	0.11
Cooling	Si	~ 200	~ 0.2

Table 2.3: Material budget of sensor, read-out chip and bump bonds per station.

on-pixel front-end is optimized to enhance the time performances and obtain a time resolution of 200 ps for each pixel hit (RMS).

Each component of the hybrid silicon pixel is optimized in terms of material budget and performance. For the on-detector read-out system integration the following parameters are optimized:

- Material budget in active beam area.
- Read-out chip size and active matrix size
- Accessibility to power and I/O connections on the chip
- Particle rate per pixel
- Heat dissipation and cooling

The main topics regarding the GigaTracker will be studied in detail in Chapter 3.

2.2.3 CHANTI

The general veto design foresees a six ring anti-counter after the last GigaTracker station (GTK3) in order to detect the charged particles produced by inelastic interactions of the beam with the collimator and the GTK stations. The necessity of such a system arises from the fact that pions, or other charged particles, produced at small angles, can reach the Straw Tracker and mimic a kaon decay in the fiducial region.
The detector consists of 6 stations made up of two rectangular layers (x and y) composed by two sub-layers of scintillator bars. Each bar is triangularly shaped and staggered bars are arranged in order to face oppositely in order to fill inter gaps. Light is collected by means of one WLS (Wave Length Shifter) fiber placed inside each bar and read at one side by a silicon photomultiplier.

The CHANTI, by itself , is able to veto about 95% of all inelastic interactions of K^+ in GTK3 regardless of the final state. This vetoing efficiency reach almost 99% if one restricts to potentially signal-like events.

2.2.4 LAV

The Large Angle Veto is made of 12 stations placed along z axis between 120 and 240 m (see Figure 2.1) inside the vacuum decay tube except the last one.
These detectors are composed of lead glass crystals with attached photo-multipliers (PM) from the OPAL electromagnetic calorimeter. Each lead glass block is a 370 mm long truncated prism of SF57 lead glass. The light is collected by an Hamamatsu R2238 PMT glued to the crystal through a lead glass light guide. The guide and the PM are enclosed by an external mu-metal shield.
Crystal detectors (lead glass crystals + PMs) are assembled radially inside the vacuum tube to form a complete ring of lead glass blocks. Each LAV station

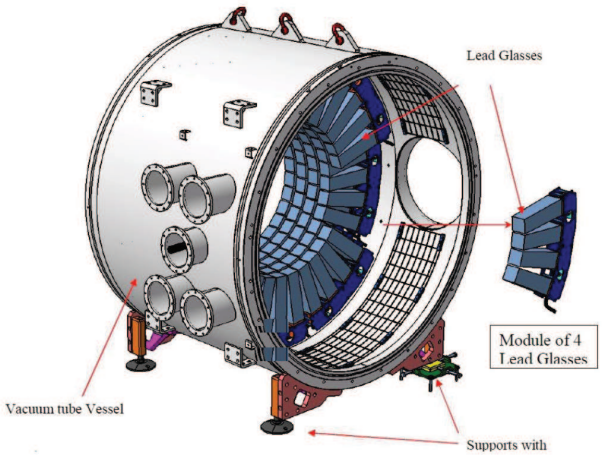


Figure 2.5: LAV: Complete station layout.

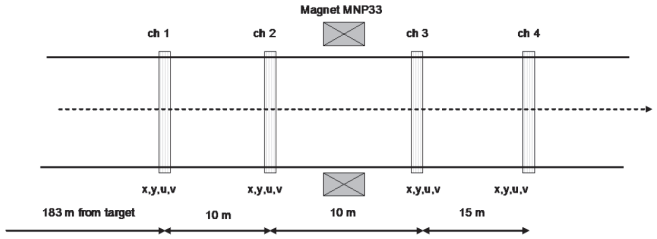


Figure 2.6: The Straw Tracker layout.

is made up of 4 or 5 rings, which are staggered in azimuth providing complete hermeticity of at least three blocks (20 X_0) in the longitudinal direction. The layout of a complete station is shown in Figure 2.5.
The LAV has been optimized to detect photons with inefficiency lower than 10^{-4} well suited by the measured inefficiency of the lead glass blocks (studied at Daphne BTF in Frascati) and a timing resolution lower than 1 ns.

2.2.5 Straw Tracker

The downstream magnetic spectrometer is essential to measure the momentum and angle of secondary particle tracks and it consists of four chambers intercepted in the middle by an high aperture dipole magnet providing a vertical B-field of 0.36 T (Figure 2.6).
Two principal performance requirement follow from $\Delta P/P \leq 1\%$ and $\Delta\theta_{K\pi} \leq 60$ μrad. This implies the minimization of the amount of material crossed by the particles. It means that every straw chamber has a limit of $\leq 0.5\%$ X_0. In addition, to reduce the multiple Coulomb scattering, the tracker must operate in vacuum and so it will be installed in the decay region.

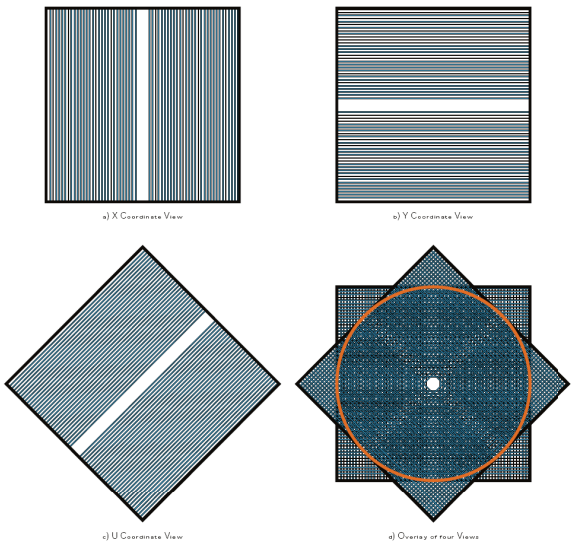


Figure 2.7: Schematic layout of the four views of a chamber.

Each straw chamber is made of four views (x, y, u, v) rotated with respect to the following by 45° providing measurement of four coordinates and enhancing the spatial resolution per space point ≤ 80 µm (Figure 2.7). Finally each view consists of four staggered layers of 112 straw tubes of 2.1 m length (in Figure 2.8), increasing the coordinate resolution beside solving left-right ambiguity and maintaining a material budget of $\sim 0.1\%$ X_0 per view. A region free of tubes, 12 cm large, in the middle of each view-plane form an octagonal hole in each chamber where the intense charged beam of undecayed particles pass through. The dipole magnet, placed after the second chamber, gives a 256 MeV/c momentum kick in the horizontal plane to allow momentum measurement. The chambers are displaced in the bending plane according to the 75 GeV/c positive beam path.
Straw tubes are composed by a cylindrical Mylar 9.75 mm diameter tube, internally metallised with gold-plated copper; Mylar wall thickness is 36 µm. Inside the tube is placed a 30 µm diameter gold-plated Tungsten wire. Each straw tube is filled with a gas mixture of CO_2 (80%), Isobutan C_4H_{10} (10%), CF^4 (10%).

2.2.6 RICH

The Ring Imaging Čerenkov counter is needed to:

- Provide separation of π^+ from μ^+ between 15 and 35 GeV/c momentum providing a muon suppression factor of at least 10^{-2};
- Measure the pion crossing time with a resolution of about 100 ps or better;
- Produce the L0 trigger for a charged track.

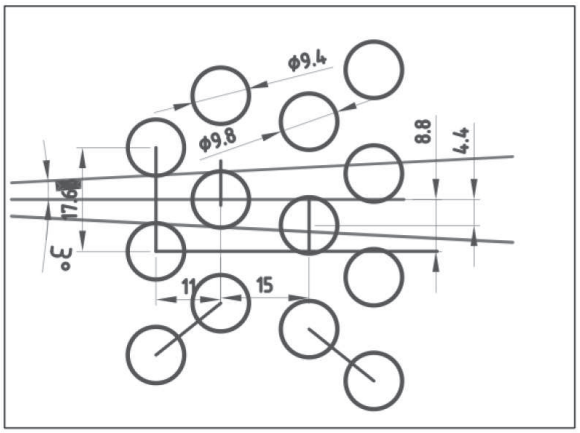


Figure 2.8: Straw staggered layers.

The detector is placed between the last Straw chamber and the LKr (Figure 2.1). It consists of a steel cylindrical vessel 17 m long and 3 m large around the beam pipe. The vessel is filled with neon gas at a slight overpressure w.r.t. the external atmosphere.
A charged particle of velocity β crossing the gas volume, with index of refraction n, emits a cone of radiation with angle θ_c with respect to the particle trajectory:

$$\cos\theta_c = \frac{1}{n\beta} \tag{2.1}$$

The momentum threshold for a charged particle of mass m to emit Čerenkov radiation is related to the index n by the equation:

$$p_t = \frac{m}{\sqrt{n^2 - 1}} \tag{2.2}$$

The neon gas has the right index of refraction to guarantee the maximum efficiency for a 15 GeV/c pion.
Inside the vessel is placed a 17 cm diameter beam tube used to let the undecayed particles to pass through in vacuum.
At the downstream end of the vessel a mosaic of mirrors is placed; in order to avoid the beam pipe shadow, Čerenkov photons are reflected by two groups of mirrors pointing to two different regions. The focal length of the mirrors is 17 m. Each focal region is equipped with about 1000 PMs Hamamatsu R7400-U03 with a pixel size of 18 mm, ensuring a quantum efficiency and time performances which fit the requirements, in a compact hexagonal packing. The active area of each PM is about 8 mm large and a Winston cone is used to direct the Čerenkov light from the 18 mm pixel size. The centre of each PMs region is about 1 m far from the beam pipe axis. The schematic layout of the RICH detector is shown in Figure

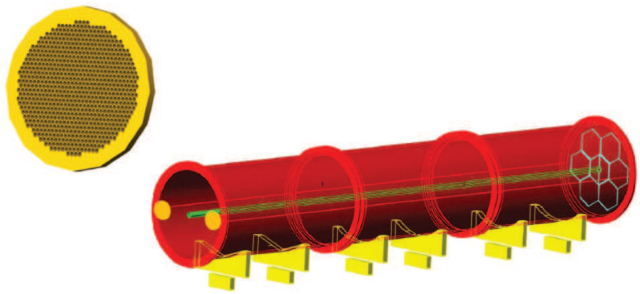


Figure 2.9: Schematic view of the RICH detector; the downstream section shows the mirror mosaic. The upstream section shows the 2 PM arrays with a magnification of one array.

2.9.

2.2.7 CHOD

The NA48 charged hodoscope is composed by a system of scintillation counters with high granularity and excellent time resolution (200 ps). It is supposed to detect possible photo-nuclear reaction in the RICH mirror plane and back-up the RICH in the L0 trigger for the charged tracks.
The detector consists of 128 detection channels which are arranged in two plane (x-y) of 64 horizontal and vertical BC408 plastic scintillators covering a radius of 121 cm. The scintillation light is collected via a short Plexiglas fishtail light guide, followed by a Photonis XP2262B PM.

2.2.8 New CHOD

A new charged hodoscope was designed and used for the first time in the 2016 run together with the old CHOD. The main reason to build the New CHOD is the high hit rate at which the long slabs (1 m) of the CHOD are exposed. The intrinsic dead time and the light transit time inside the scintillator are not compatible with the expected overall rate on the detector above 10 MHz.
The New CHOD is a two-dimensional array of 152 scintillator tiles installed after the LAV12. In each quadrant, a 30 mm thick plastic scintillator is divided into 38 tiles. The scintillation light is collected and transmitted by 1 mm diameter wavelength shifting fibres to be detected by arrays of 3×3 mm^2 silicon photo-multipliers (SiPMs) on boards located on the periphery of the detector. A maximum rate of the order of 500 kHz is expected on the tiles close to the beam pipe. The signals are shaped using constant fraction discriminators to improve the time resolution.

2.2.9 LKr

The electromagnetic calorimeter at liquid Kripton of NA48 will be used to cover intermediate region from 1 to 8.5 mrad for vetoing photons from K^+ decays. In this region the photon detection inefficiency has to be 10^{-5} for photons with energy above 35 GeV. The calorimeter is also supposed to provide trigger signals evaluating the energy deposition, in order to contribute reducing the L0 trigger rate.
The performances of the calorimeter as used in NA48 has been checked to be good for NA62 but, since the L0 rate is expected to be two order of magnitude larger, the old read-out system will no longer be usable. A CREAM (Calorimeter REAdout Module) has been designed for this end.
The TALK (Trigger Adapter for Liquid Krypton) board has been developed as an interface between the old and the new trigger system. In addition, other subsystem (e.g. the calibration system logic and software) will need updating.

Its efficiency for single γ detection above 2.5 GeV has been measured on data collected by NA48/2 in 2004 and during a test beam in 2006 and found in perfect agreement with the requirements (see Section 1.3).

2.2.10 MUV

The target of the MUV system is to provide muon suppression with an overall inefficiency of about 10^{-5}. The system consists of three distinct parts, called MUV1, MUV2 and MUV3 according to their longitudinal position along the beam axis. The first two, placed after the LKr, are classic iron-scintillator sandwich hadronic calorimeters for measurements of deposited energies and shower shapes of incident particles to distinguish hadronic from electromagnetic showers. MUV1 is composed by 24 layers of scintillator strips while MUV2 by 22.
After MUV1 and MUV2 and an 80 cm thick iron wall, the fast muon veto MUV3 module, has the aim of detecting non-showering muons and acts as muon veto detector at trigger level. To achieve the required time resolution of < 1 ns at each transversal position, a design is chosen, which employs scintillator tiles arranged to minimize differences in the light path trajectories.

2.2.11 IRC and SAC

There are two types of small angle vetoes: Intermediate Ring Calorimeter (IRC) covering the beam tube between the LKr and the RICH, and the Small Angle Calorimeter (SAC) placed after the MUV and covering the region near zero degrees. Both detectors will be built using the shashlyk technique, which consists of lead-scintillator sandwiches and WLS fibers passing through them via holes, to collect the light.
Both the SAC and the IRC are exposed to photons with energies higher than 5 GeV. In order to achieve the necessary background suppression, both the SAC and the IRC have to provide detection inefficiency better than 10^{-4}, achievable by a depth of at least 16 X_0.

Parameter	Value	Description
f(L0) max	1 MHz	Maximum average L0 trigger rate
Δt(L0) min	75 ns	Minimum L0 trigger time separation
T(L0P) max	100 µs	Maximum latency for generation of the L0 Trigger primitives
T(L0) max	1 ms	Maximum total L0 trigger latency
f(L1) max	100 kHz	Maximum average L1 trigger rate
T(L1) max	1 s	Maximum total latency for L1 trigger
f(L2) max	$\mathcal{O}$(15 kHz)	Maximum average L2 trigger rate
T(L2) max	Spill period	Maximum total latency for L2 trigger

Table 2.4: Main TDAQ parameters.

2.3 Trigger and Data acquisition

The high hit rate and the consequent need of a good time resolution in order to have an efficient selection of the events, led the collaboration to use a TDC-based system for many detectors. Consequently most of the detectors of the experiment (KTAG, CHANTI, the LAVs, RICH, CHOD, NewCHOD and MUV3) are read out by a unified system built around TEL62 FPGA-based motherboards [5]. Depending on the requirements, up to four daughter boards can plugged in. Each TDCB daughter board interfaces four HPTDC chips [20]. The TEL62 memory buffers store the hits while waiting for a L0 trigger accept signal. The IRC, SAC, LKr, MUV1 and MUV2 are read out by CREAM boards [18]. Each module provide 32 channels connected to ADCs. The boards buffer the data while waiting for a L1 trigger decision. In parallel, it provides energy sums for triggering purposes.
The Straw Tracker electronics is based on the CARIOCA chips [11] integrated in custom FPGA-based cover front-end boards.
The GigaTracker employs as well its own readout chain that will be detailed in Sections 3 and 4.

The interesting events are selected by a three-level fully digital trigger. The first level (Level-0 or L0) is implemented on FPGAs. The LAVs, RICH, CHOD, NewCHOD, LKr and MUV3 TEL62s are programmed to generate and send simple primitives to the Level-0 trigger processor (L0TP) [42]. A primitive is a 32-bit word built when a given set of conditions is met and immediately transmitted. The primitive generators apply subdetector-dependent time offsets to the generated primitives to ensure that they are aligned.

The L0TP stores the primitives from each subdetector in a RAM at the address defined by the primitive time. Next, it combines them and it looks for programmable matching conditions. For each match (or event), the L0TP sends a L0 trigger accept signal to all the subdetectors after a fixed latency of 1 ms. A 32-bit timestamp is assigned to the event using the time attached to the primitive

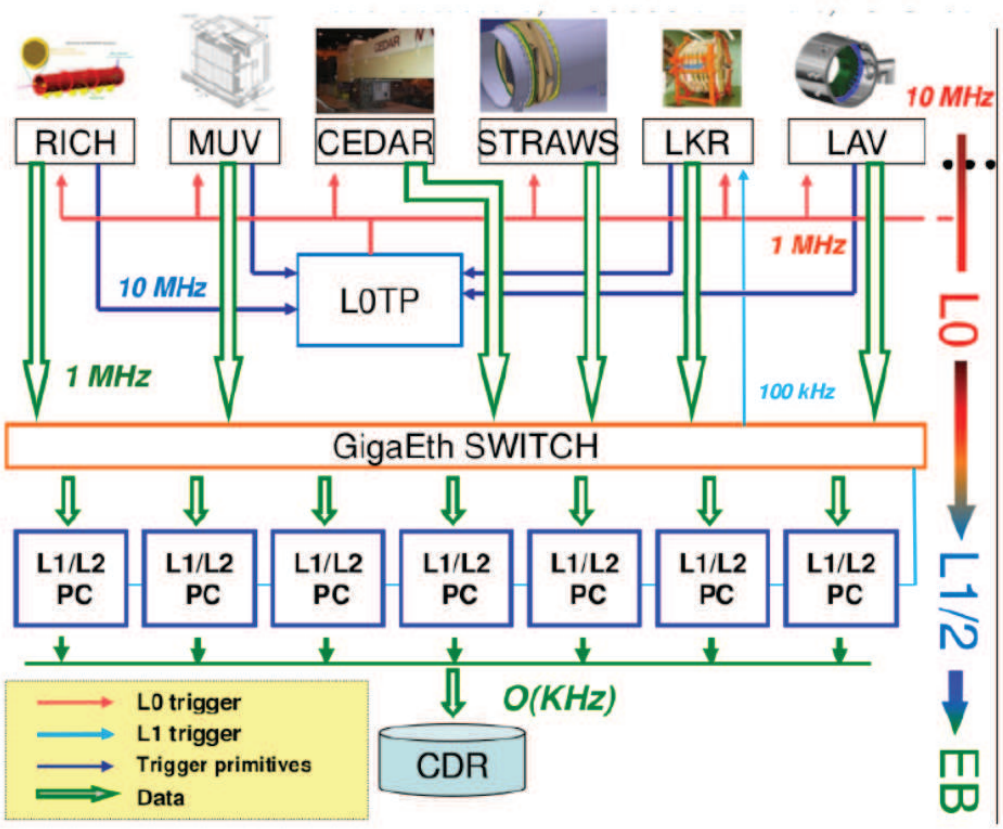


Figure 2.10: Logical scheme of the data-flow, trigger distribution and online farm.

coming from the reference detector. In response to the trigger accept signals, all the subdetectors, except CREAM-based ones and GTK, must send the corresponding hits to a PC farm for further evaluation. The CREAM readout and the GTK-PC store the data waiting for a L1 trigger decision.

The Level-1 (L1) and Level-2 (L2) trigger algorithms run on a off-the-shelf PC farm. The L1 routines have access to the complete data stream of individual subdetectors and can reconstruct higher level objects like tracks or clusters. Finally the L2 algorithms combines the information from all the subdetectors to make the final decision on whether to store the event or discard it. A summary of rates and the latencies is provided in Table 2.4.
The overall logical scheme of trigger and data acquisition is sketched in Figure 2.10.

Chapter 3

GigaTracker

The GigaTracker (GTK) measures the momentum, the direction and the time of passage of all the NA62 secondary beam particles. Three constraints are immediately apparent: the detector has to cope with the high intensity hadron beam, the amount of matter in the beam path must be minimal to reduce the elastic and inelastic scatterings and the detector should be radiation hard.

The GigaTracker is composed of three independent stations. The first and second stations are separated by 13.2 m while the second and the third are 9.6 m apart. A long lever arm helps to measure accurately the direction of the particles. The middle station is placed between two achromatic magnet pairs and displaced by $\sim$ 60 mm along the horizontal axis. The vertical offset matches the 75 GeV/c beam momentum and the field strength of the magnets.
Each GigaTracker station houses a detector. They are completely interchangeable, a detector can be installed in any of the three stations as the mechanical interface is identical. All the detectors are operated inside the secondary beam vacuum (10^{-6} mbar). The detector itself is made of assemblies mounted successively together. A 3D model is presented in Figure 3.1. The different pieces are (a) the *sensor assembly* which is a sensor bump-bonded to ten readout chips. (b) The *cooling assembly* which consists of a sensor assembly glued on a cooling plate. (c) The *carrier card* assembly, which is a cooling assembly clamped to a carrier card. (d) Finally, a complete detector is a carrier card mounted on a *mechanical frame*. A sketch of the detector is presented in Figure 3.2.

GigaTracker is a new milestone in the hybrid silicon pixel detector landscape. The custom readout ASIC (TDCpix) has an unprecedented timing capabilities: below 150 ps with a sensor attached for a bias voltage of 300 V. It can process up to 210 MHits/s spread over the 1800 channels. GigaTracker is the first detector which is equipped with a micro-channel cooling plate; the total thickness in the beam acceptance is equivalent to less than 0.5 mm of silicon. The full detector was installed and tested in beam for the first time in autumn 2014.

In this chapter, the topics regarding the crucial components of the GigaTracker will be explained. Every system component is optimized to reach the required

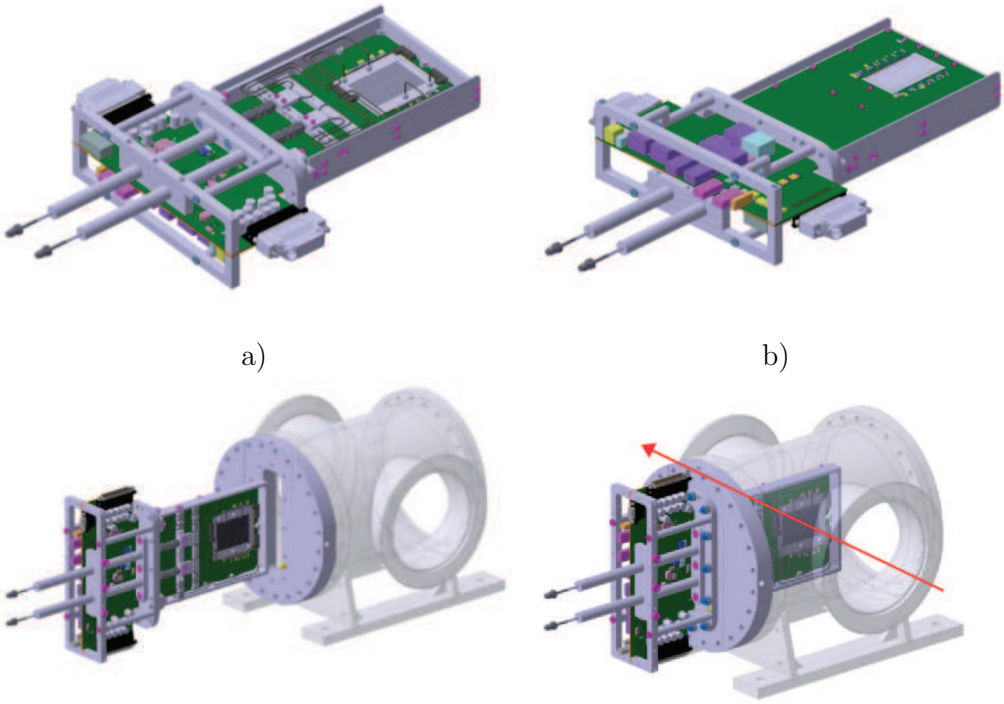


Figure 3.1: 3D views of a GigaTracker station: a) cooling plate side, b) sensor side, c) detector insertion, d) operation position (the red arrow symbolises the particle beam).

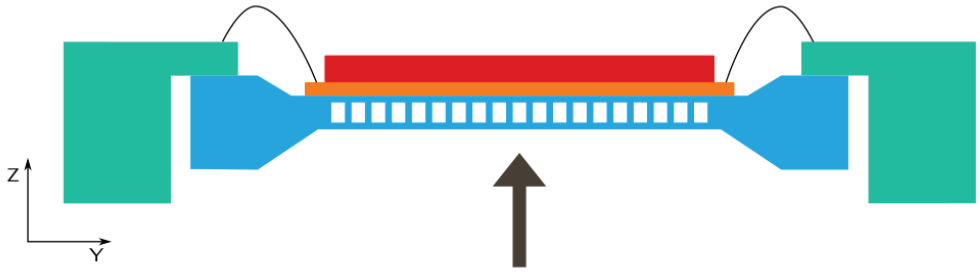


Figure 3.2: Cross-section (Z-X) of the central region of a GigaTracker station. The sensor is in red, the readout chips in orange, the cooling plate in blue and the carrier card in green. The bump-bonds, the glue and the thermal interfaces are not represented. The beam is going from bottom to top. This schema is not on scale.

precision on beam measurements and to operate in a severe environment.
The main reference used in this chapter is [23].

3.1 Silicon sensor and bump-bonding

Every GTK station is composed of one large sensor (60.8 mm × 27.0 mm) connected to 2×5 readout chips. The interconnections between the sensor and the readout chips are made with Sn-Pb bump bonds.

3.1.1 Silicon sensor

Two main requirements for the detector led to the choice of thickness of the sensor:

- Minimum material budget.
- Sufficient signal to provide the necessary time resolution.

Since these requirements are mutually exclusive, a compromise had to be found. Simulations on timing resolution and signal to noise ratio over sensor thickness showed that a thickness of 200 μm per station (corresponding to 0.22% X_0) is a good compromise and that a timing resolution of ≈ 200 ps can be achieved [1].
The GigaTracker silicon sensor measures 60.8 mm by 27.0 mm and is 200 μm thick. The most probable charge released by a 75 GeV/c charged hadron in such sensor is about 2.4 fC. The sensor is segmented into 300 μm by 300 μm pixels except in the inter-chip regions where they are enlarged to 400 μm by 300 μm.

The operating environment is also an important parameter in the choice of the sensor since the radiation environment presents a severe challenge to its lifetime. The expected fluence in 100 days of data taking is $\approx 2 \times 10^{14}$ 1 MeV n_{eq} cm^{-2} (1 MeV neutron equivalent per cm^2). In addition the beam distribution will be non-uniform across one sensor with a larger beam intensity in the central region (Figure 3.3). The GTK sensor assemblies are expected to be replaced at the end of a defined operation period.
An hybrid silicon detector was chosen to cope with the requirements for the electronic readout chip, i.e. the required time resolution of 200 ps, and the relative harsh radiation environment for the sensor. This allows to separately optimise the individual components, the chip and the sensor respectively.
The baseline choice for the sensor material was initially p-in-n due to simpler processing procedures, availability and experimental arrangement in 2008. However, the front-end design was designed to allow the connection of other sensor types, such as n-in-p (which has been successively produced and currently employed).
The required time resolution can be obtained operating the sensor at high overdepletion. This allows to operate close to the charge carrier saturation velocity, minimizing the charge collection time to $2 - 4$ ns. Collection times of this order are reached in 200 μm sensors applying bias voltages of 400 V and more. A target operating voltage of approximately 500 V was defined and a multi-guard

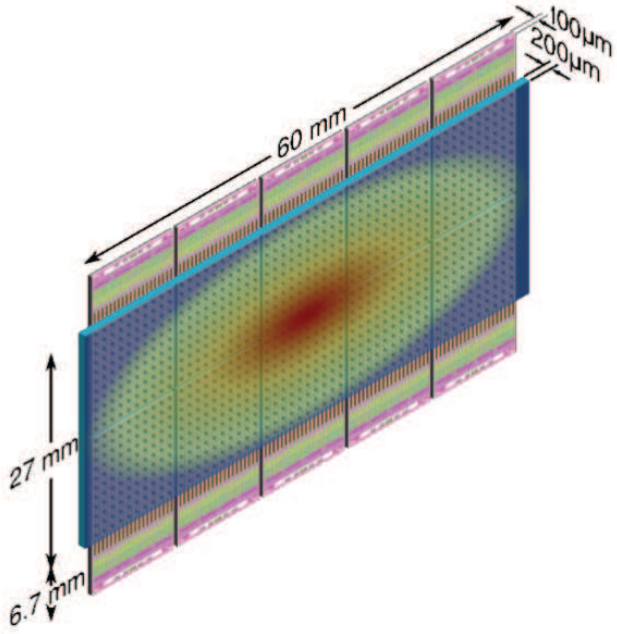


Figure 3.3: Beam intensity distribution over a GigaTracker sensor (foreground). On the back part the 2×5 read-out chips are visible.

ring structure is implemented in every sensor in order to ensure stable operation at relatively high voltage.

The radiation would degrade the sensor material leading to macroscopic changes:

- Increase of the leakage current.
- Change of the depletion voltage.
- Charge trapping and signal degradation.

Radiation damage effects were studied using test-diodes produced by the manufacturer that delivered also the final GTK sensor wafers (FBK-Trento, Italy). Irradiations were carried out up to a fluence of 2×10^{14} 1 MeV n_{eq} cm^{-2} and detailed annealing studies investigated the effects on leakage current and full depletion voltage. The results were summarized in an Internal notes [4, 2]. The maximum acceptable operating temperature for the GTK stations was set to 5 °C which allows an operation time of approximately 50 days using standard p-in-n sensors. In fact measurements on irradiated diodes indicated that the leakage current of a full size sensor, at an operating temperature of 5 °C and 50 days of operation, reach a maximum acceptable value of approximately 270 µA. However, efforts are being made to design the cooling system to operate at −20 °C, which allows an operation of 100 days.
Charge collection efficiency, speed and sensor capacitance influence the overall timing performance of the GTK station. As a consequence, under irradiation of

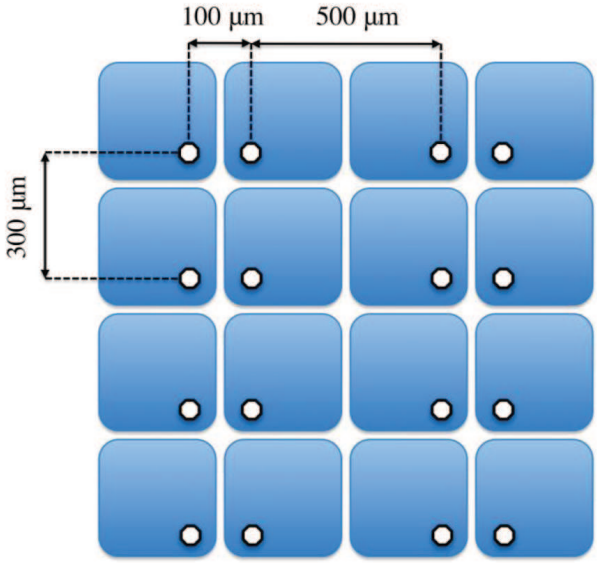


Figure 3.4: Bump pads arrangement scheme.

the sensor, the collected charge degrades. This degradation is non-uniform from chip to chip and pixel to pixel and may introduce non-uniform pixel response.

3.1.2 Bump bonding

The hybrid pixel system requires high quality interconnections between the on-detector readout electronics and the sensor. Each pixel cell contains one bump pad to connect it with the corresponding channel in the front-end chip. The bump-bonding pads have octagonal shape (26 µm with 20 µm opening in the passivation) and the bump pad centre is located at about 50 µm from the pixel edge. The bump-bonding pads are arranged in a mirrored scheme on the neighbouring columns (Figure 3.4) with enlarged pixel cells (300 µm × 400 µm) in the inter-chip region. This allows a fully sensitive area over the full sensor size to be maintained.
The thinning of the final GTK readout chips is relevant in order to meet the material budget requirement of 0.33% (corresponding to ≈ 300 µm of silicon) for the sensor-chip assembly. A final thickness of 100 µm or less is compliant with the requirements, but also demands the development of specific process steps during production.

3.2 Readout ASIC

The specifications on the GTK on-detector electronics are challenging and requires performance close to the limits of the employed 130 nm CMOS technology. The design of the circuit is the product of trade-offs between acceptable power

General	Maximum material budget per station	0.5% X_0
	Overall efficiency per station	$> 99\%$
	Pixel size	300 µm × 300 µm
Architecture / Geometry	Chip active area	13.5 mm × 12 mm
	Chip size	19.5 mm × 12 mm
	Number of pixel per chip	40 columns× 45 rows = 1800
	Size of pixels	300 µm × 300 µm
	Thickness of readout chip	100 µm
Pixel analogue front end	Input dynamic range	$0.8 - 9.6$ fC; $5000 - 60000$ e^-
	Time resolution of the discriminator	100 ps RMS
	Discriminator time walk after correction	80 ps RMS
	Power dissipation per pixel	1 mW max
	TDC time binning	100 ps
Data rate	Beam rate	750 MHz
	Average centre chip hit rate	105 MHz
	Average particle rate per pixel in station	42 kHz
	Average particle rate per pixel in centre chip	58 kHz
	Peak rate per pixel on beam centre	114 kHz
	Center chip data rate (48 bit per hit word)	5.0 Gb/s
	Center chip data rate (incl. 8b10b encoding, 30% contingency)	7.5 Gb/s
	Serialiser data rate (4 used per chip)	1.9 Gb/s
	Readout efficiency	99% (98% in beam centre)
	Operating temperature in vacuum	-20 °C to $+5$ °C
Radiation	Centre pixel total dose in 1 year	2×10^{14} MeV n_{eq} cm^{-2}, 6×10^4 Gy
Trigger	Number of levels	1 (L0)
	Latency	$\lesssim 1$ ms
Off chip trigger	Trigger window	75 ns

Table 3.1: GTK ASIC specification.

dissipation of 2 W/cm^2, better than 200 ps timing precision, maximum particle rate of a centre pixel of 114 kHz and an output data rate per readout chip of up to 7.5 Gb/s including data transmission overhead. Table 3.1 presents a summary of the specifications.
Assuming a 48 bit word per hit, and considering the average chip hit rate, a data rate of about 5 Gb/s (not considering overheads) needs to be processed and sent off each readout chip. The data are shipped off the chip in a triggerless, data driven architecture to off-detector FPGA-based readout cards. In order to reduce digital noise and connectivity, a low number (4) of Gbit serial links are used for each chip.

A significant part of the ASIC is crossed by the secondary beam, therefore key digital logic elements have to be protected against single event upset (SEU). Finally, for practical reasons, the ASIC had to be manufactured with IBM 130 nm CMOS technology.

3.2.1 Design options

The integration of the analogue front-end together with time-to-digital converters must be done so that the digital noise does not disturb the analogue performance. In this respect two solutions were considered.
One was to integrate the time-to digital converter (TDC) together with the analogue front-end directly in the pixel cell. The TDC is active only during a hit in that particular cell. A reference clock needs to be distributed over the entire pixel matrix; this can represent a possible noise source to the analogue front-end electronics. Figure 3.5 shows the basic architecture of the TDC per pixel option.

The other approach was to keep the pixel cell as simple as possible, containing only the analogue front-end, and send the discriminator signal to the end-of-column area of the pixel matrix inside the ASIC where the TDC evaluates the arrival time. In this configuration the pixel cell stays simple, no clock needs to be distributed, but the discriminator signal needs to traverse the pixel matrix to be evaluated in the end-of-column. Figure 3.6 shows the basic architecture of the end-of-column (EoC) option.

Given the expected input dynamic range, the specified time resolution requires efficient time walk compensation. Two time walk compensation architectures were investigated:

a. Constant Fraction Discriminator (CFD), which directly gives a compensated discriminator signal, but uses sensitive analogue circuitry.

b. Time-over-Threshold (ToT) discriminator, which delivers two trigger events to be time tagged but uses simpler and less sensitive circuitry.

As simulations could not fully characterize performances and drawbacks of different architectures and time-walk compensation schemes, test structures for both

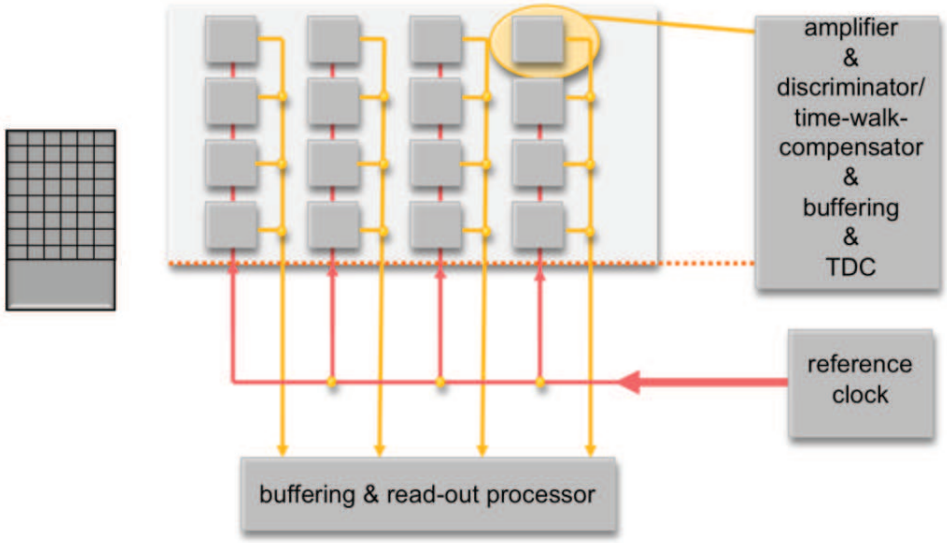


Figure 3.5: Block diagram of the TDC per pixel option.

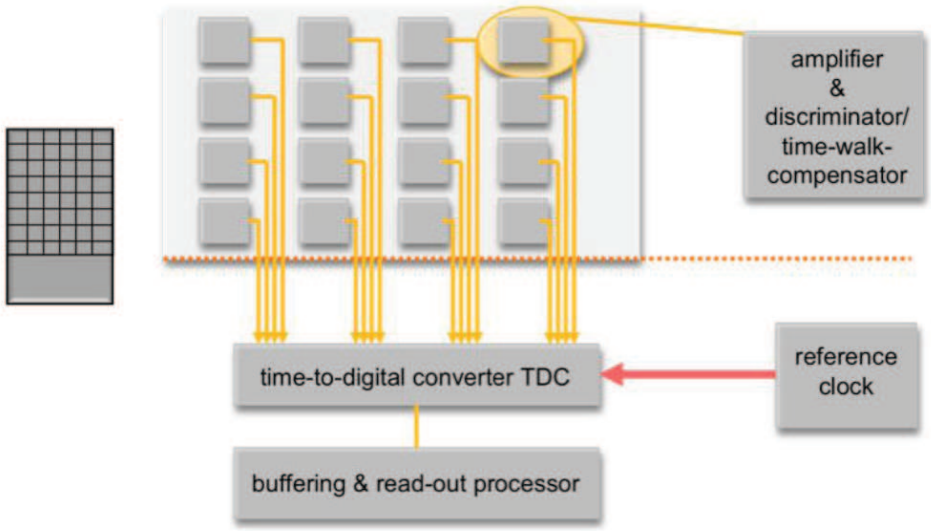


Figure 3.6: Block diagram of the end-of-column option.

versions of the chip were produced.
In a technical review held in September 2010, the end-of-column (EoC) architecture with ToT discriminator has been chosen as baseline solution for the GigaTracker readout chip, given the time constraints of the experiment and the functionality of this option, combined with the good results of laser and beam tests carried out with a demonstrator bump bonded assembly.

3.2.2 ASIC architecture

High speed serial differential signals are used to communicate to and from the pixel read-out chip. Serial lines allow to reduce the number of connections and thus to increase module reliability. The number of I/O pads is limited, as the connections to the module are done on one side of the chip only. A high number of single ended data lines would increase the digital system noise. The clock signal and the serial control signals are connected on two high speed serial input lines. Configuration data and settings are transmitted on one slower serial input port and one parallel input port. The pixel hit data output ports consist of four multi Gigabit serial ports for the data and one slower serial port for status information. For test purposes a number of single ended outputs are foreseen.

As stressed before, the design and layout of the digital processing units must be done so that the digital noise has minimum effect in the analogue front end. The implementation of the GTK pixel readout chip is done in 0.13 μm CMOS technology and studies indicated that this technology might be sufficiently radiation hard by itself for the expected average total dose of 10^5 Gy/year [23]. However, a large variation of dose is expected between chips of a GTK station and between chip edge and centre. This dose gradient might introduce variation of signal response between pixels. To circumvent this effect, the trimming in each pixel can also partially compensate for the dose gradient.

3.2.3 End-of-Column (EoC) architecture overview

The EoC architecture was selected to equip the full scale GigaTracker detector; the resulting ASIC was named the TDCpix [29].

The ASIC is composed of four identical quarter chips organized in the columns of the 45 pixels.
The EoC option employs a time walk compensation based on time over threshold correction (ToT) measurements. The correction is based on the time tags of rising and falling edges of the discriminator signal. The leading edge time provides information of the hit arrival time and the trailing edge provides input charge amplitude information used to correct time walk. At the time of the leading edge, a synchronous coarse clock counter value is latched to increase the dynamic range of the TDC to 12.8 μs. The double time stamp with coarse counter and address information are stored in buffer, before they are serialized and sent off the chip.

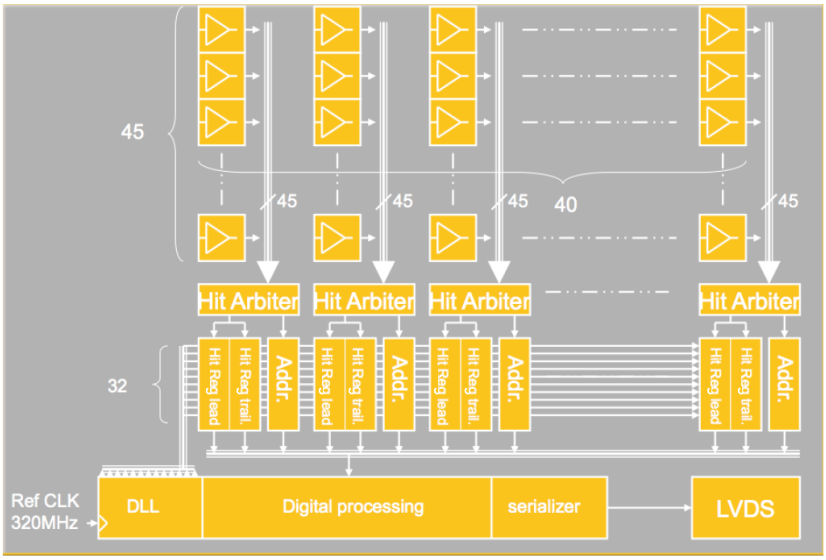


Figure 3.7: EoC architecture block diagram.

A block diagram of the final EoC chip architecture is showed in Figure 3.7. The EoC chip employs simple pixel channels containing the amplifier, ToT discriminator and a transmission line driver per pixel cell, which sends the discriminated signal to the end-of-column region of the chip. A delay locked loop (DLL) based TDC time tags the rising and falling edge of the discriminator signal with a time bin of ~ 98 ps. In the chip, 5 not-neighbouring pixels in a column are multiplexed together and connected to one TDC using a combinatorial hitArbiter circuit. Simulation showed that the hit efficiency for the worst-case centre column stays above 99.5%. Pixel hit addresses and rising and falling time tag words are sent to a buffer FIFO before the data are serialized and sent out of the chip. The time walk compensation using the two time tags is performed off-line allowing the evaluation of the input signal charge for each hit. In this architecture no clock signals are distributed over the matrix, reducing possible interference with the analogue electronics and data are only transmitted to the EoC circuits once a hit has been registered. The digital processing and transmission units are geographically separated from the analogue front-end electronics.

A series of configuration blocks allow to set the chip up. Parameters of special importance are the trim DAC values, the threshold levels and the serialiser operating mode. Key register are triplicated for SEU protection.

3.3 Electrical integration

The eletrical integration of the cooling assemblies with the outside world is done through a carrier card (GTK Carrier) which also provides mechanical support

for the cooling assembly. It is a complex multi-layers T-shaped PCB carrying the signal lines and the power lines from the readout chips through the vacuum-atmosphere interface. A gap to host the cooling assembly is machined in the vacuum end of the card. A stair structure supports the assembly on the top and bottom edges.

More specifically, the accessible signals are:

- 1× general digital clock,
- 1× clock for the delay-locked-loops,
- 1× test pulse signal,
- 1× coarse frame counter reset signal,
- 10× 320 Mb/s serial configuration links,
- 10× 320 Mb/s serial configuration status links,
- 40× 3.2 Gb/s serial links.

The electrical connection between the readout chips and the carrier is provided by wire bonds. The signal lines are connected to optical transceivers installed on the carrier and eventually transmitted to the GigaTracker readout boards.

The detector is powered by 10× 1.2 V analogue lines and 10× 1.2 V digital lines; two lines for each of the ten chips. Furthermore, 2.5 V, 3.3 V and 5 V lines are needed for the carrier card. All these channels are interlocked with the readout chip temperature sensors. A 5.3 V non-interlocked line supplies the temperature interlock logic.

The low voltages power supplies are installed in the cavern, next to the detector. High voltage power supplies are sitting in surface for easy access.

3.4 Cooling

The cooling design was driven by the following GTK requirements:

- Material budget
  - total radiation length in active beam area $\leq 0.5\%$ of X_0 ($\simeq 500$ μm of silicon) per station (~ 200 μm for the cooling system),
  - minimum amount of material in the sensor area (60×27) mm^2 plus a 10 mm safety zone,
  - outside those zones no material budget constraints.
- Detector operating temperature of 5 °C or lower.

- Best possible uniformity of the temperature across the sensor area (< 2 °C difference over the sensor).
- Power dissipated by one GTK station > 32 W.
- System operating in vacuum.

The main goal of the cooling system for the GTK is to avoid thermal run-away and destruction due to the low mass of the detector module. Furthermore it reduces the radiation damage of the sensor and consequently increases the module life time. The upper limit of the operation temperature were set to 5 °C by the radiation damage study, but a lower operation temperature is highly desirable, as the module life time would increase from 50 days to 100 days when cooled at -20 °C. The material budget and the operation in vacuum are the main integration challenges of the project. Mechanics and cooling integration can profit from the fact that no material budget restrictions exist for the area 10 mm outside the beam. From a cooling performance point of view the anticipated 2 W/cm^2 power dissipation by the active electronics is not difficult to meet. However, the cooling and mechanics support architecture must introduce only a minimum of material into the beam area and at the same time assure mechanical stability of the module and allow access to high speed electrical connections. Two independent solution were pursued:

1) a micro-channel structure based on a thin silicon micro-channel cooling plate circulating liquid C_6F_{14};
2) a gas cooling vessel with Mylar walls, where low temperature nitrogen gas is flushed through the detector.

In December 2011 the micro-channel technique has been chosen as the baseline solution for the front-end cooling [21].

The development of the micro-channel cooling aimed for an operating temperature of -20 °C to -30 °C. Figure 3.8 shows the section of the baseline layout for the micro channel cooling. The coolant enters and exits the straight channels via manifolds positioned on both sides. The channels, distribution manifold and openings for the inlet and outlet connectors are etched into a silicon wafer, which is then coupled to a second wafer closing the hydraulic circuit. The final goal is to have both wafers in silicon bonded together by fusion bonding to produce a monolithic cooling element to be glued to the chip-sensor assembly. The maximum temperature difference of the coolant between the inlet and outlet has been set to $\Delta T = 5$ K to guarantee a relatively uniform temperature distribution and minimize all thermal stress and related deformations. Also, to limit the mechanical stress in the micro-channel cooling plate, the maximum acceptable pressure drop inside the cooling plate has been set to $\Delta p = 4$ bar. Based on the above criteria the micro-channel dimensions were set as follows:

- 70 µm deep channels etched into a silicon wafer of 200 µm thickness.

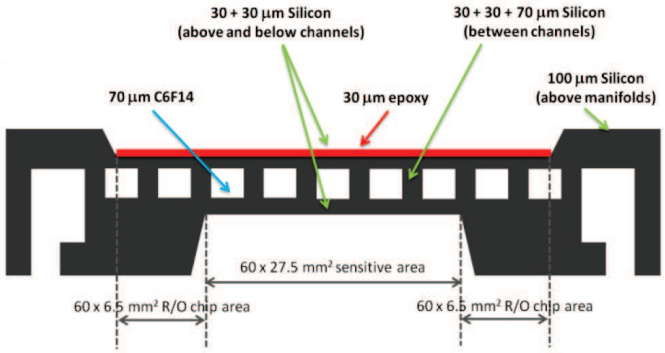


Figure 3.8: Schematic of the side section of the micro-channel cooling device.

- Covered by a fusion-bonded silicon wafer with 100 µm thickness over the active area.
- Bonded assemblies are then thinned down in order to obtain a $\sim$ 200 µm thickness.
- Outside this area, the thickness of both silicon wafers is 520 µm, allowing for 400 µm deep outlet and inlet manifolds as well as good structural stabilization of the whole device.

This design leads to an additional material budget $\sim 0.2\%$ of X_0 on the sensitive area and it is characterized by a difficult construction as well as a difficult integration procedure with the sensor assembly due to issues related to chip-sensor planarity.
A 300 W cooling plant installed next to the detectors cools C_6F_{14} in liquid phase which is circulated in the channels to dissipate the heat. A very detailed description of the micro-channel cooling system can be found in [35].

3.5 Off-detector readout electronics

As shown in the diagram in Figure 3.10, each GTK sensor is read out by 10 GigaTracker ASICs (TDCpix) whose output data flows continuously toward the GTK off-detector readout (GTK-RO) cards. These cards provide temporary data storage until the Level 0 trigger decision, upon which the GTK-RO cards extract trigger matched data from the on-board memory buffers and transmit the data to the sub-detector PCs through Gigabit Ethernet links. The GTK-RO design is actually made of two decked units: the mother board (Figure 3.9), hosting the main functional blocks, and a daughter card featuring TTC interface block and various timing functions necessary to the operation of the connected ASIC. The most relevant GTK sensor/ASIC parameters for the GTK off-detector read-out are summarized below:

- maximum hit rate in centre pixel $\approx$ 1.3 MHz/mm^2, 114 kHz/pixel;

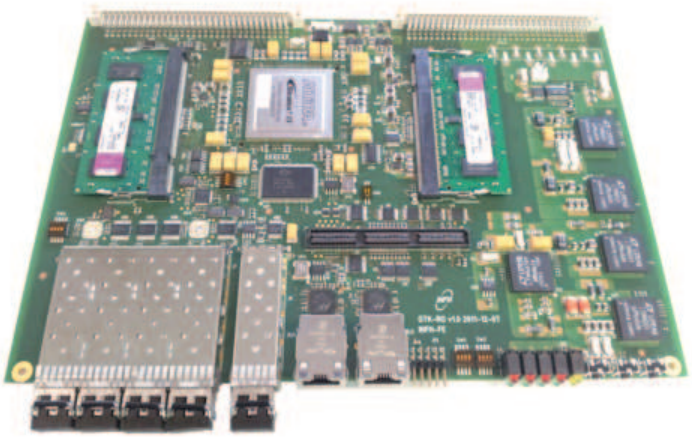


Figure 3.9: The GTK-RO motherboard.

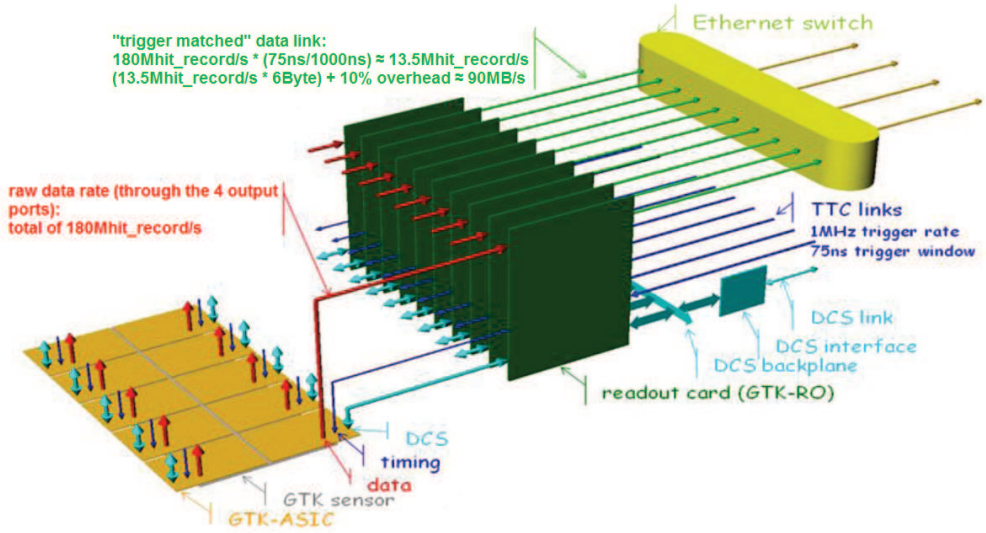


Figure 3.10: GTK read-out block diagram.

- average hit rate per sensor plane $\approx$ 750 MHz;
- data word width: 48 bit;
- average centre chip hit rate: 105 MHz;
- average centre chip data rate: 5 Gb/s;
- design data rate (chip rate + contingency): 7.5 Gb/s;
- serial links per chip: 4;
- readout window: 75 ns.

The TDCpixs continuously send periodic frames (defined as a 6.4 µs packet of hits) to the GTK-RO board. Synchronization words are sent carrying a rolling frame number, which is zeroed at the beginning of the data spill. The hit record provides the local hit address within the pixel matrix and the time measurement which consists of two fine measurement (one for the leading and one for the trailing for the Time-over-Threshold measurement) derived from the TDC in the TDCpix and a coarse measurement from the synchronous clock counter in the TDCpix. Each hit record is encoded in 6 Byte to provide relative leading- and trailing-edge timing information.

Each TDCpix features 4 output ports. Depending on the TDCpix internal distribution of the data flow and assuming an average hit rate of 58 kHz (42 kHz + 35% contingency) per pixel (see Table 3.1), each output port transmits up to: $[58 \times 10^3 \text{ Hz} \times 6 \text{ B} \times 8 \text{ b/B} \times (10/8) \times 1800]/4 = 1.56$ Gb/s including the 8b/10b encoding overhead.
The read-out parameters for all three detector stations where 1 GTK-RO board serves one TDCpix and trigger matched data is transmitted using 2 GbE links per GTK-RO board are summarized:

- 900 MB/s of trigger matched data per GTK station
- 2.7 GB/s of trigger matched data for the entire GigaTracker detector (3 stations).

A 90 MB/s data rate at the output of a GTK-RO card is achievable with a single GbE link but two links were foreseen, providing some headroom in case the actual data rates would exceed the expected ones.
Considering that 1 trigger-matched event contains, on average, 180 Mhit/s $\times$ 1 µs $\times$ 0.075 = 13.5 hit per TDCpix, and thus 135 hit records per GTK station, one has 405 hits per event for the all GTK (3 stations) and thus, assuming 6 Byte per hit record and a 10% overhead one finds that the average size of a GTK event $\approx$ 2700 B.

The implementation of the GTK-RO board is outlined in the block diagram in Figure 3.11.

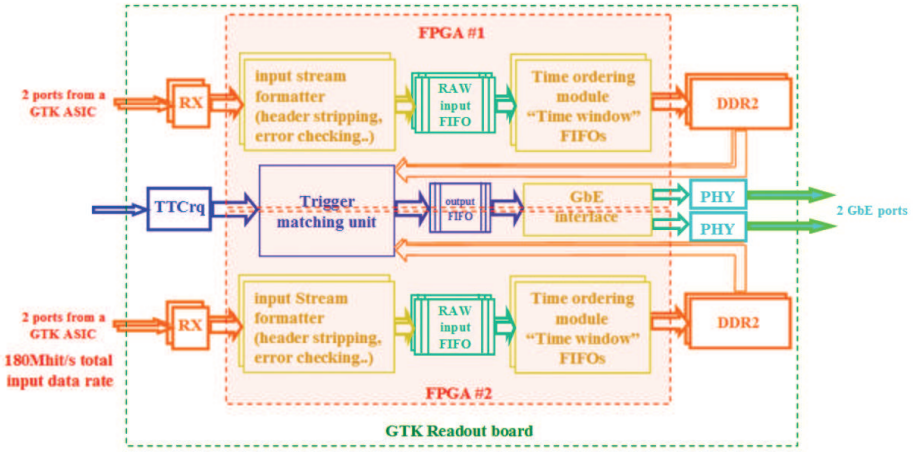


Figure 3.11: GTK read-out board block diagram.

3.5.1 Memory device

The key elements of the GTK-RO card architecture are the memory devices used for the temporary storage of the GTK data during the trigger latency time interval. GTK-RO board use a DDR2 SDRAM as main buffer memory device. Memory interface is of Double Data Rate type (DDR) allowing two memory accesses per single memory clock. Memory has 64 bit data bus (allowing to write/read all the expected 48 bit of one hit with a single access). The GTK-RO board FPGA controls two DDR2 sections working in parallel, allowing to sustain the TDCpix overall data (180 Mhit/s) and trigger (1 MHz) load.
The first prototype of GTK-RO boards used Stratix IV GX70 FPGA with speed grade C3. First tests showed both DDR2 buses working at 240MHz which allowed transfer rate per bank of $2 \times 240 = 480$ Mtransfer/s. For the final production the FPGA has been upgraded to a bigger Stratix IV GX110 device with a faster speed grade C2 (higher DDR2 transfer rates were possible).

3.5.2 Input stream formatter

The input stream formatter controls the packets coming from the TDCpix and checks the frame number against the one calculated on the GTK-RO card. It also strips off the header from the TDCpix and transfers the hit data words into the Raw-Input FIFO appending an End-of-Frame (EOF) marker to the data packet for 1 frame. Any error detected in the incoming packets would be coded into a specific field of the EOF marker to forward the error information.

3.5.3 Time ordering module

The time ordering module (see Figure 3.12) is necessary for the trigger-matching operation since the hit records coming from the TDCpixs are not necessarily time-ordered. It seems then advisable to pre-order the input data in bins and store

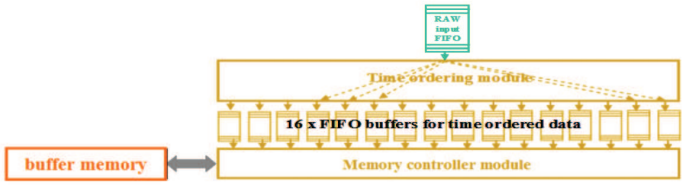


Figure 3.12: Block diagram of time ordering.

the content of each bin in a specific memory page of the buffer memory (DDR2). A bin is actually a small FIFO (time-Window FIFO) memory inside the FPGA which is filled as the input data is extracted from the Raw-Input FIFO. Part of the coarse time measurement field of a particular hit record determines the bin it will be assigned to.
The content of each Time-Window FIFO are then transferred to a specific memory page in the buffer memory. The frame number and the ID of the Time-Window FIFO (i.e. part of the coarse timing information in the hit record) determine the base address of the target memory page. When the content of the Time-Window FIFO is completely transferred to a memory page an End-of-Page terminator is also stored.
When processing an L0 trigger request, the trigger matching module must evaluate, from the known trigger latency, the memory page containing requested data.

The outcome of the trigger matching should be the extraction of an average of 13.5 hits from each GTK-RO. Assuming that the hits are recorded in 6 Bytes, and taking into account an overhead of 10% for the event header, the average size of an event packet should be about 90 Bytes. The overhead due to transmission protocol must be considered too; for example an UDP/IP packet transported by ethernet frames has a minimum header length of $14 + 28 = 42$ Byte. Multi-event packets could be assembled to optimize the bandwidth of the Gigabit Ethernet connection.

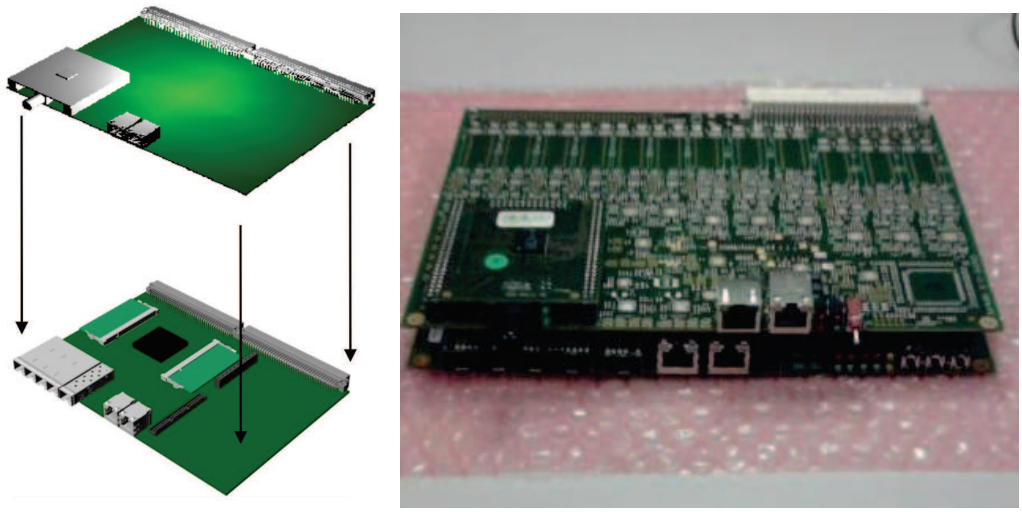
The architecture outlined here is capable of meeting the 1 MHz L0 trigger rate. More details on the commissioning of the GTK-RO boards are provided in Section 4.3.

3.6 GigaTracker TTC interface

The interface between the GigaTracker data acquisition system and the Timing, Trigger and Control (TTC) system [10] is provided by a set of GigaTracker TTC interface boards. The latter is a daughter module for the GTK-RO main board, featuring one TTCrq [34] module and that can be configured in two different modes:

GTK-INT mode The GTK-INT board is a base version providing the signals from NA62 TTC system to the GTK-RO motherboard, including 40 MHz clock

and L0 triggers. It also features Choke/Error port interface and Gigabit ethernet port for additional board management.



a) b)

Figure 3.13: a) Sketch of GTK-RO mother board (bottom) with GTK-INT daughter board (top) assembly. b) Final mother+daughter boards assembly.

GTK-TTC mode The GTK-TTC board is a fully populated version of the GTK-INT board, that acts as main source of timing signals to the 3 GTK Carriers. These signals are DLL clock and Digital clock at 320 MHz, Coarse frame counter reset and Test pulses by means of optical transmitters.
In preparation for the 2016 NA62 run, three optical drivers were added in order to be able to control also the 3 reset lines of the GigaTracker Carrier boards.
The Test pulses can trigger the generation of test hits in the TDCpix. The pulses can be adjusted in frequency, width and phase. This allows to create a variety of different test setups.

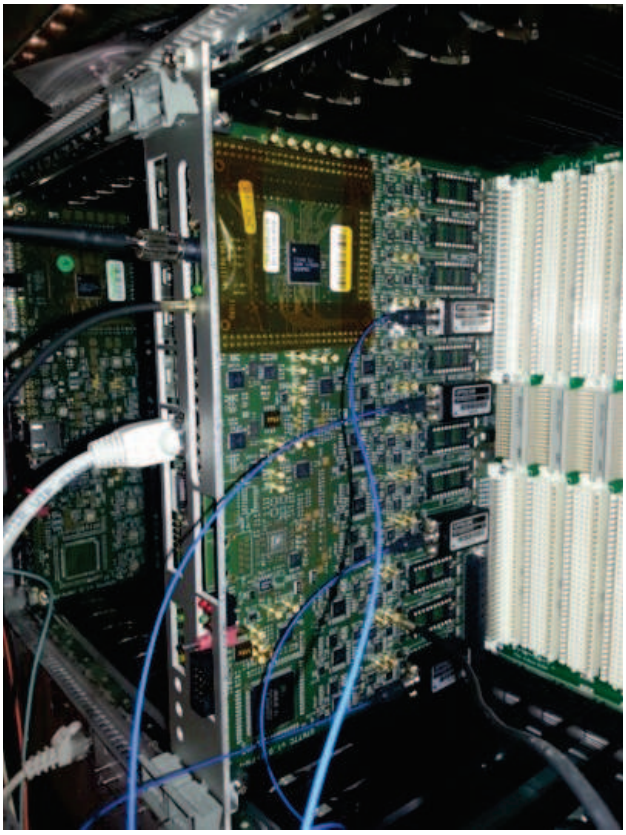


Figure 3.14: A GTK-TTC board installed in the VME crate.

Chapter 4

GigaTracker Data Acquisition and Control Systems

In the present chapter, description of the components of the data acquisition and control systems for the GigaTracker are presented, as well as an overview of the work for the integration of all components carried out starting in 2014.

4.1 GigaTracker Data Acquisition System

The system for data acquisition of the GigaTracker is composed by three main components:

- TDCpix front-end electronics
- off-detector read-out boards
- sub-detector PC Farm (GTK-PCs)

The TDCpix is described in Section 3.2 while the off-detector read-out (GTK-RO) boards in Section 3.5. The GigaTracker PC Farm is composed of 6 PCs, each one associated to a group of 5 GTK-RO boards (and their coupled TDCpixs). Each station in particular is read out by a set of 10 GTK-RO boards sending data to and controlled by 2 PCs as shown in Figure 4.1. The characteristics and implementation details of the sub-detector PC Farm data acquisition software will be described.

4.1.1 Sub-detector PC DAQ software

As already pointed out, each GTK-RO board sends trigger matched events to a sub-detector PC by means of two 1 Gb/s Ethernet interfaces. The purpose of the six identical sub-detector PCs is to collect and organize the data extracted from the GTK-RO boards upon L0 triggers requests and to send them (or a subset of them) to the NA62 PC Farm. The sub-detector PCs are dual-CPU servers with 32 GB of RAM and two 10 Gb/s Ethernet ports, running Linux as operating system. In the present configuration one PC receives data from 5 GTK-RO boards

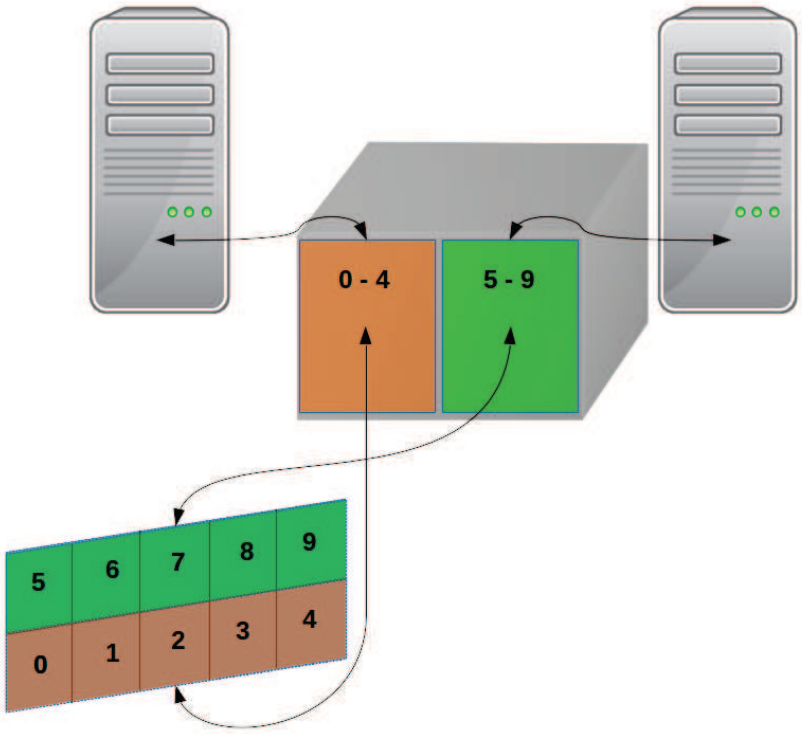


Figure 4.1: Schematic view of the data acquisition and control chain of a GigaTracker station.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	Chip ID				L1A event counter																							
Timestamp of the L1Accept signal																															
1	1	1	1	Chip ID				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Trigger type							
Number of hits								Number of processed L1A																							

Figure 4.2: The two trailer words of the GTK data format [25].

corresponding to a row of chips, for a total of 10 different data streams.
Data is transmitted using UDP datagrams composed by 8 trigger matched event fragments with the exception of the last one containing the End of Burst (EoB) event.
Assuming 105 MHz as average centre chip hit rate [23], the expected event fragment dimension can be computed as:

$$105 \text{ MHz} \times 75 \text{ ns (trigger window)} \times 8 \text{ B (hit size)} = 63 \text{ B}\,. \tag{4.1}$$

The event fragment dimension from a half chip is then: 63 B/2 = 31.5 B.
Every event fragment trigger-matched by the GTK-RO is then identified by means of two trailers of 8 B each (Figure 4.2, so that the overhead for each event is 16 B. This gives 31.5 + 16 = 47.5 B as total event fragment size. As mentioned a frame is composed by 8 trigger matched event fragments so we can obtain the

total payload dimension:

$$47.5 \text{ B} \times 8 + 10 \text{ B (GTK-RO custom header)} = 390 \text{ B} \tag{4.2}$$

from which we can compute the total data flux, taking the nominal 1 MHz L0 trigger rate:

$$390 \text{ B} \times 1 \text{ MHz}/8 = 49 \text{ MB/s}\,. \tag{4.3}$$

This value leaves a safety factor of $119/49 \simeq 2.4$, where 119 MB/s is the maximum data rate of a 1 Gb/s Ethernet interface.
In general, taking the nominal 750 MHz particle rate hitting a GigaTracker detector, one can compute the expected trigger matched data rate from an entire station resulting in ~ 900 MB/s.

The 20 data streams of a GigaTracker station are aggregated and routed through an Ethernet switch with 24 1 Gb/s ports and 2 10 Gb/s port used as multiplexer. The 2 10 Gb/s port are then connected to the 2 PCs for data transmission. This allows each PC to receive the 10 streams of data from 5 GTK-RO boards (via 10 1 Gb/s links) with a substantial safety margin.

The sub-detector PC software is based on a multi-threaded architecture[1] implemented in C++ with specialised classes. The 4 *Receiver* threads receive UDP frames from the network socket and store them in buffers shared with "reader" classes: the *Consumer* and *SDEAssembler* classes that can in fact concurrently access these shared buffers in order to carry out their operation. In particular the 4 *Consumer* threads read the frames stored in the shared buffers, identifying the position in memory, event number, GTK-RO link IP and size of every event fragment inside the frame. A table of indexes (*IndexTable*) is then filled with these informations ordered by sender IP and event number. Moreover different consistency checks are performed on the counter and key fields. Finally the single *SDEAssembler* thread reads L1 trigger requests (sent from the NA62 PC Farm through network), extracts event fragments corresponding to each request, builds the complete events and finally sends them to the NA62 PC Farm.
In Figure 4.3 a simplified block diagram of the outlined software is presented.

In order to balance the input load between the 4 different *Receiver* threads, we implemented a strategy exploiting the transmission of frames by the GTK-RO link interfaces with modulated UDP destination port on a frame-number-based round-robin schedule. On the PC side, each *Receiver* thread is connected to a network socket exploiting the Hardware Packet Filtering (also referred as in-NIC filtering) featured in modern networking interfaces in order to accept only frames with a specific UDP destination port. In this way frames (and contained event fragments) are received by the same *Receiver* thread and complete events can be later assembled. The networking part of the software relies on the *zero copy*

[1]Programming and execution model that allows multiple threads to exist within the context of a single process. These threads share the process resources, but are able to execute independently.

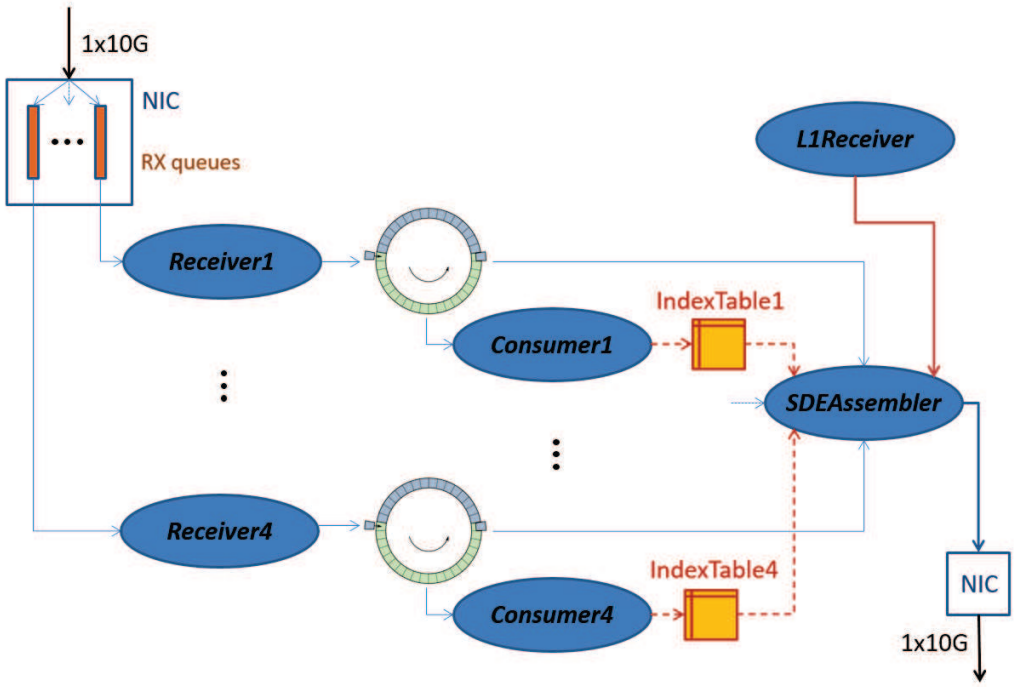


Figure 4.3: Simplified block diagram of the DAQ PC software.

module of the PF_RING library [37] and hardware filters are set using its tools.

The L1 trigger requests are received by the *L1Receiver* via network *multicast* from the NA62 PC Farm and pushed in a memory queue[2].
The *SDEAssembler*, as already mentioned, pulls this queue and fetches the event fragments to be assembled. The data are assembled in *SDE*s ("sub-detector event data to PC farm after request" as referred in [25]). The SDE header is shown in Figure 4.4. The subdetector-specific data is composed by a sequence of event fragments ordered according to GTK-RO board ID and board's Ethernet link ID as sketched in Figure 4.5. When assembled, the SDE is transmitted to the requesting PC Farm node using standard UDP datagrams, exploiting the network programming tools provided by the C++ Boost_Asio library.

The software features also specific classes for interfacing with NA62 Run Control and DIM [3] services. The *RCInterface* class reads the configuration file created by the GigaTracker Run Control software (Subsection 4.2.3) during initialisation and saves the corresponding fields, like station and sub-station identifiers and active GTK-RO boards.
The *DimInterface* class is used to maintain synchronisation with the experiment,

[2]Abstract data type or collection in which the entities in the collection are kept in order and the principal (or only) operations on the collection are the addition of entities to the rear terminal position, known as enqueue, and removal of entities from the front terminal position, known as dequeue. This makes the queue a First-In-First-Out (FIFO) data structure.

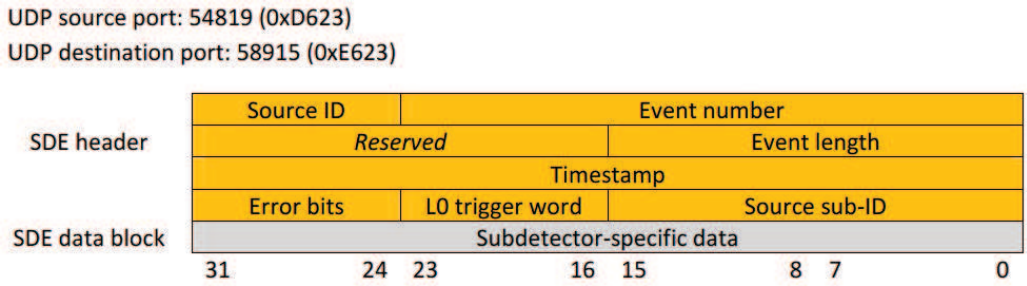


Figure 4.4: SDE format.

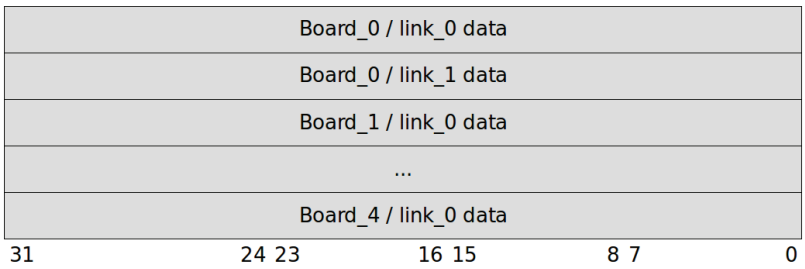


Figure 4.5: Subdetector-specific data (SDE payload).

since informations like Start and End of Burst are published on DIM. It is also used to publish monitoring informations on number of processed events.

The software is also designed with routines logging debug and monitoring informations on file. This allows to offline check the performances of the data acquisition system.

4.2 GigaTracker Run Control System

The developed system for the control of the GigaTracker data acquisition system comprises different elements, including executables for stand-alone testing, software for control from the NA62 Run Control and libraries for the different sub-systems (TDCpix, GTK-RO, GTK-TTC).
Hereafter these elements will be briefly described.

4.2.1 TDCpix configuration

In order to configure the TDCpix, the optical 320 MHz serial configuration links of the GTK-RO are exploited. The control software running on the GTK-PC exchanges UDP packets with the slow control socket of the GTK-RO board, and the board itself forwards the control packets to the front-end configuration system via the configuration link. Replies from the TDCpix follow the same path back to the control software. The library developed for the TDCpix testing has been imported and modified in order to be used with the UDP protocol and the GTK-

RO boards, instead of the FPGA-PCIe test bench developed for testing purposes by CERN EP−ESE−FE developers.
The library includes operations for the complete configuration of the TDCpix i.e. pixel matrix (thresholds and trims), TDC, PLL and global configuration.

4.2.2 GTK-RO board configuration

The configuration of the GTK-RO boards is also performed via UDP frames exchange via a dedicated port in one of the two Ethernet interfaces. In order to discriminate these packets from the TDCpix configuration ones, the communication protocol foresees the use of packet markers in both a) requests to GTK-RO and b) replies from GTK-RO with possible requested informations. The main operations are:

- Send board control packet:
  - Load destination addresses for data packets.
- Send TDCpix DAQ control packet:
  - Soft reset of GTK-RO board.
  - Enable/Disable data acquisition.
  - Set TDCpix configuration link phase.
  - Set various simulated test signals and modes.
- Request data registers:
  - Various status information including “data link frequency locked”.

4.2.3 GigaTracker Run Control Software

The control software for the GigaTracker is a specific implementation of a standard NA62 Run Control server [32], taking care of initialization and maintaining the read-out operational during data taking.
The NA62 central Run Control stores XML configuration files for all detectors and provides the sub-detector's Run Control servers with the corresponding configuration file during Initialisation and/or Start run. The GigaTracker XML configuration file comprises informations like station and sub-station ID, network interfaces IP, active boards, pixel matrix confguration file and finally L0 time offset.
The implemented commands relies on the developed TDCpix and GTK-RO board libraries and comprise:

Initialisation The initialization procedure is taking care of the configuration of the GTK-RO boards and TDCpix. Automatised operations include GTK-RO soft reset, synchronization of the configuration links, PLL setup, data acquisition link synchronisation and finally complete configuration of the TDCpix.

The synchronization of the configuration link exploits the possibility to select 4 possible phases in the configuration module of the GTK-RO's FPGA. The 4 phases split the 320 MHz clock of the configuration link and can be selected in order to send data to the TDCpix chip far from clock edges and therefore assuring stable operation. A phase searching mechanism with possibility to set a starting phase (correct phases are stable over weeks) has been implemented. The correctness of a phase is repeatedly checked evaluating the stability of link's configuration.
The PLL setup is performed by specific calls to the TDCpix library.
Data acquisition (DAQ) link synchronisation is performed setting a TDCpix's mode sending periodic synchronisation character on the DAQ link. After this it is possible to synchronise the optical receivers of the GTK-RO on these periodic characters. Synchronisation is then confirmed reading 4 "data link frequency locked" registers (one for each data link).
The complete configuration of the TDCpix relies on the TDCpix library tools. This procedure also creates the configuration file for the sub-detector PC DAQ software (Subsection 4.1.1) read by the *RCInterface* class.

Start/End run This procedures Enable/Disable data acquisition via packets to the GTK-RO and executes/kills the data acquisition software on the sub-detector PC.

Reset The Reset performs the same actions of a End run command, resetting the TDCpix's PLL in addition.

End of burst procedure After the End of Burst, this procedure is executed in order to check the status of the read-out elements and the data acquisition itself. In particular, configuration link, data links and PLL statuses are checked. In case of problem in any of the elements a soft reset on the interested GTK-RO board is performed. A complete configuration of the TDCpix registers is performed every time, in order to guarantee stable operation conditions (preventing possible SEU generated mis-configurations).

Main loop This method is called continuously and is implemented to act as a watchdog for the data acquisition software during the run (in case of software crash it executes again the software).

4.2.4 GTK-TTC board Run Control

The GTK-TTC board (Section 3.6) is a single board providing clock and timing signals to the TDCpixs of the 3 GigaTracker stations by means of optical splitters. This board also features 3 optical drivers connected to the reset lines on the GigaTracker Carrier boards (Section 3.3) installed on the beam line.
The control of these 3 optical reset lines is managed by 3 Run Control servers interfacing to the GTK-TTC board via a custom library and scripts.

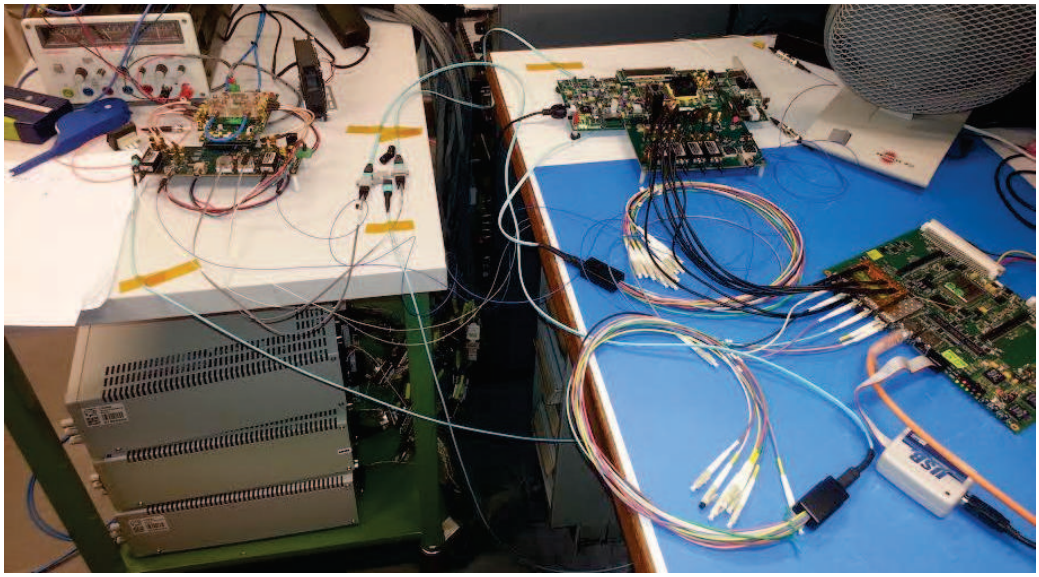


Figure 4.6: Single TDCpix chip setup in CERN laboratory. The TDCpix single chip assembly board is on the left, whilst the modified GTK-RO board is on the right.

4.2.5 I^{2}C controller for Carrier board

The GTK Carrier (Section 3.3) in its second version (Carrier.v2) features some registers to be set after any power cycle in order to be operational as well as temperature sensors. These registers can be controlled through an I^{2}C bus [15]. In order to set these registers we chose to employ 3 Raspberry Pi single-board computers [39] (one per station). Thanks to the featured I/O pins and ready-to-use I^{2}C Python [41] libraries it has been possible to develop custom scripts to set the needed registers and monitor temperature on the sensor.

4.3 System Integration

In September 2014, the integration and testing of communication between the readout boards and TDCpix started. This needed a joint effort in order to incrementally test new features and develop the GTK-RO firmware on one side and software controls on the other, as well as debug tools.

4.3.1 Single TDCpix chip integration

The first step was to test the communication between a GTK-RO board and a single TDCpix chip in laboratory at CERN (Figure 4.6). On the firmware side, the configuration tools already developed for the TDCpix workbench were adapted to the GTK-RO board firmware. In the same way the C++ TDCpix test library were imported and developed in order to communicate to the TDCpix through UDP packets sent to the GTK-RO board and forwarded through the 320

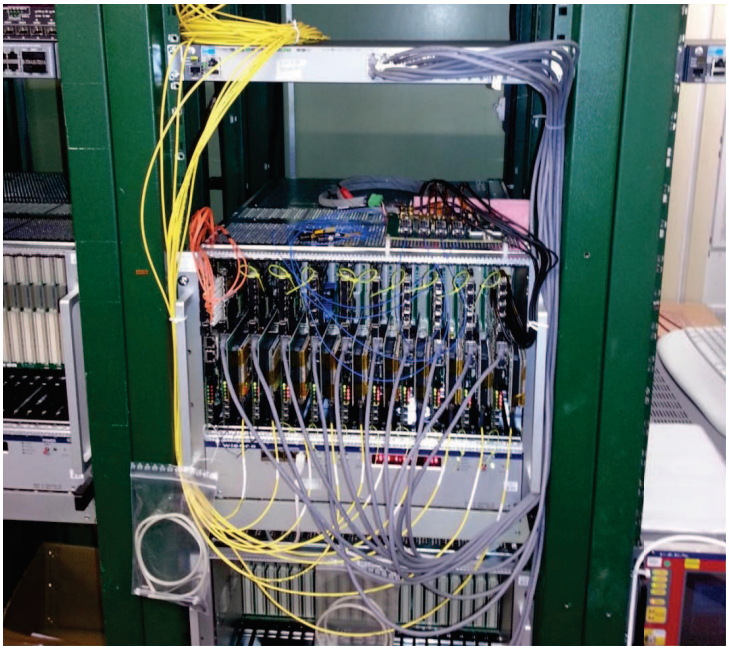
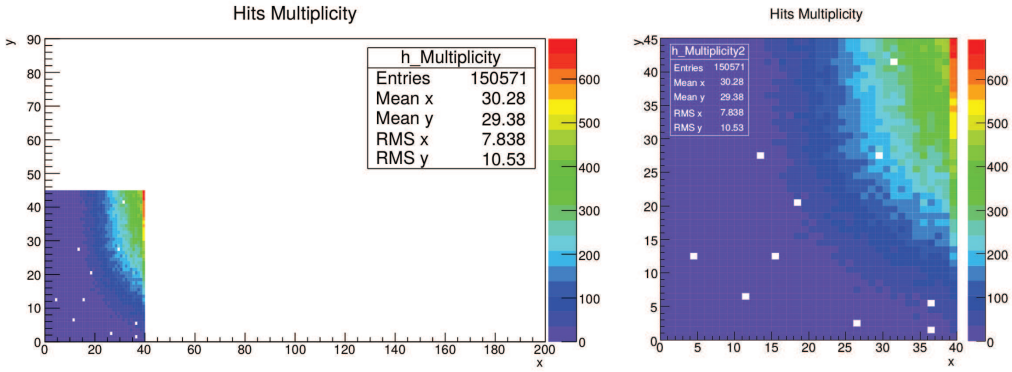


Figure 4.7: VME crate with first 10 GTK-RO boards installed in Bldg. 918's PC Farm room at the end of October 2014.

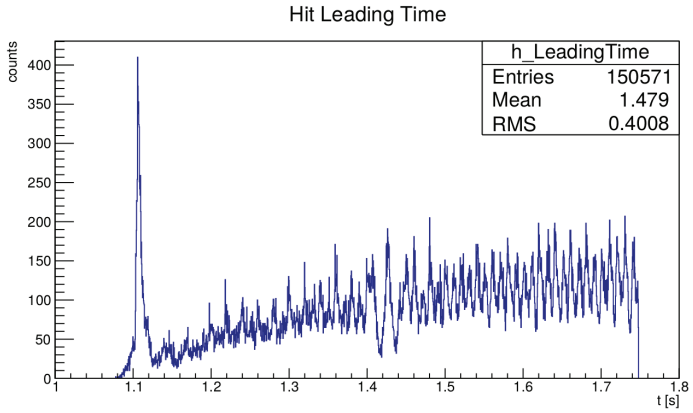
MHz configuration optical serial link. Also the core library used to communicate with the GTK-RO board was developed in C++ in this first phase.
After successful communication and configuration tests, we debugged and tested the data acquisition. Initially the test firmware used for calibration has been imported in order to work on the GTK-RO board. This allowed us to develop the software needed for the acquisition in "trigger-less" mode. In this operation mode, all hits digitised by the TDCpix are sent through the 3.2 Gb/s optical links and the GTK-RO board reorganise them and ships data through UDP packets to the sub-detector PC. In the laboratory we could then be able to send test pulses (sent by the GTK-RO controlled by the PC) to the TDCpix front-end and to read back the hit (or hits) corresponding to the test pulse.
After this first confirmation the first VME crate with 10 GTK-RO boards were installed in the NA62's PC Farm room (Figure 4.7) at the end end of October 2014 for further testing and awaiting for the first GigaTracker assembly.
Finally in the second half of November 2014 the first GigaTracker assembly was installed and we could be able to debug the system in real conditions leading to the first data to be acquired (Figure 4.8). Only one chip was readable in this GigaTracker station due to defects on the Carrier board.

4.3.2 NA62 Commissioning

2015 Run During the first year of NA62 physics run in 2015 (started in June), the work was dedicated to the commissioning of the trigger-matched GigaTracker data acquisition system, in particular on the development of the GTK-RO board firmware, final implementation of the DAQ software and design of the run con-



a) b)



c)

Figure 4.8: First few tenth of second of GigaTracker recorded data in triggerless mode: a) Hit map of recorded hits in the complete 10 TDCpix chips assembly (chip 0 is read-out). b) Zoom of the hit map on chip 0. c) Beam profile. November 2014, triggerless data.

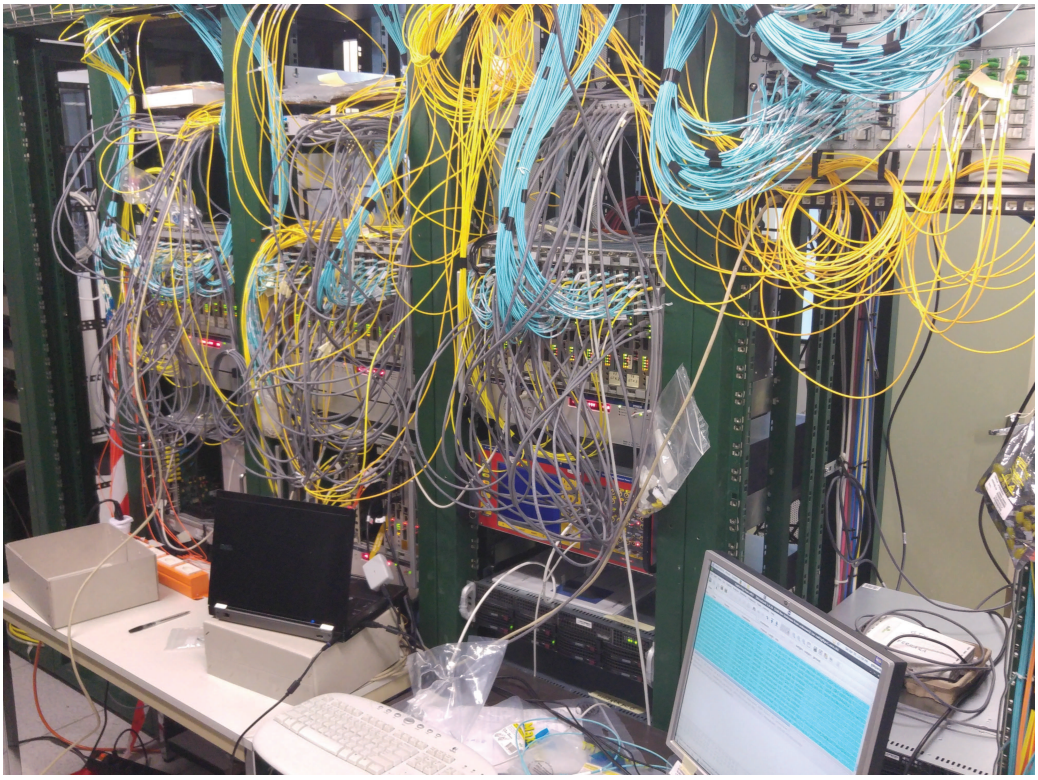


Figure 4.9: The complete GigaTracker data acquisition hardware installed in the PC Farm room at NA62 (August 2016).

trol software. These activities were carried out mostly in parallel as parts of a team work. Debugging interactions and changes in specifications were made on a weekly basis.
The complete DAQ hardware was ready and installed at the beginning of the run (Figure 4.9).

Initially an upgraded version of the triggerless firmware was employed to commission the available GigaTracker detectors and verify timing correlation with respect to the timing reference detectors (KTAG, CHOD). New features were added to the firmware including a) the possibility to select between 4 phases for the serial configuration link with the TDCpix and b) a limiter on the input multiplicity, needed to limit the amount of data read out regardless of beam intensity.

As for end of August, first trigger-matched data could be acquired from the 3 (not fully working) GigaTracker stations (Figure 4.10) with work-in-progress firmware versions. These versions presented different issues that might be present only in some GTK-RO boards. For example, some boards were sending less events with respect to the others, resulting in the complete loss of part of the burst for the entire NA62 data stream. This complete loss, caused by the event merging failure, was due to missing events both at the GTK-PC level and consequently at the NA62 PC Farm level.

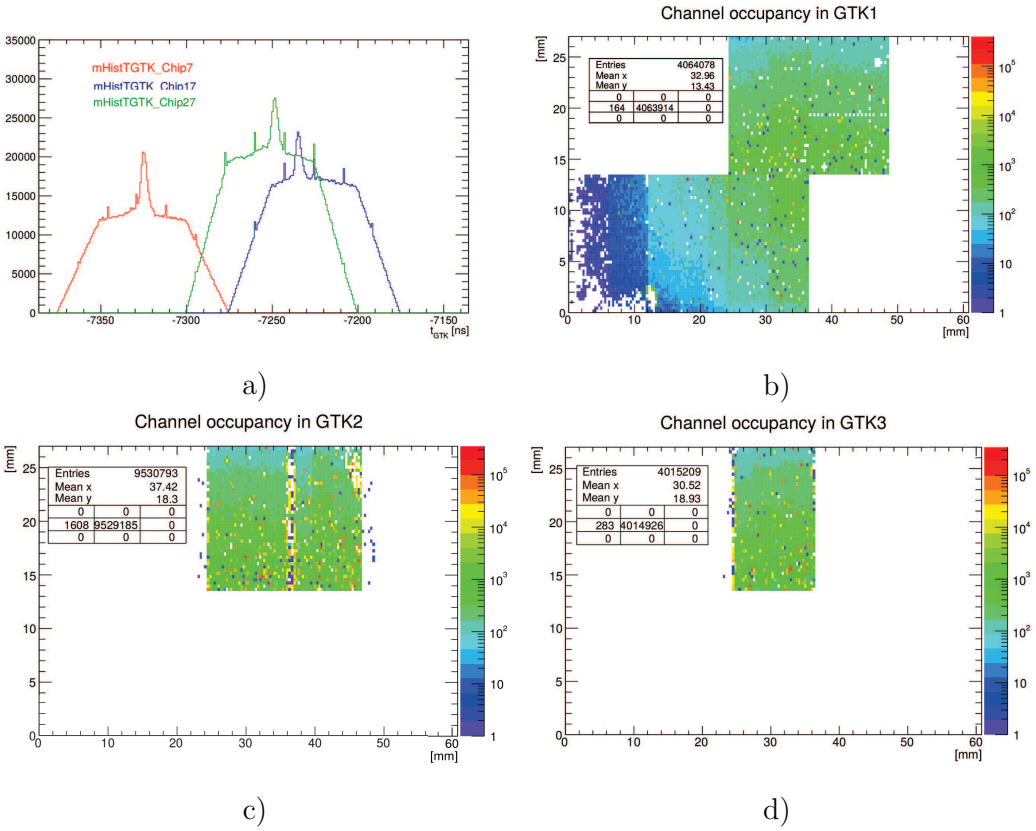
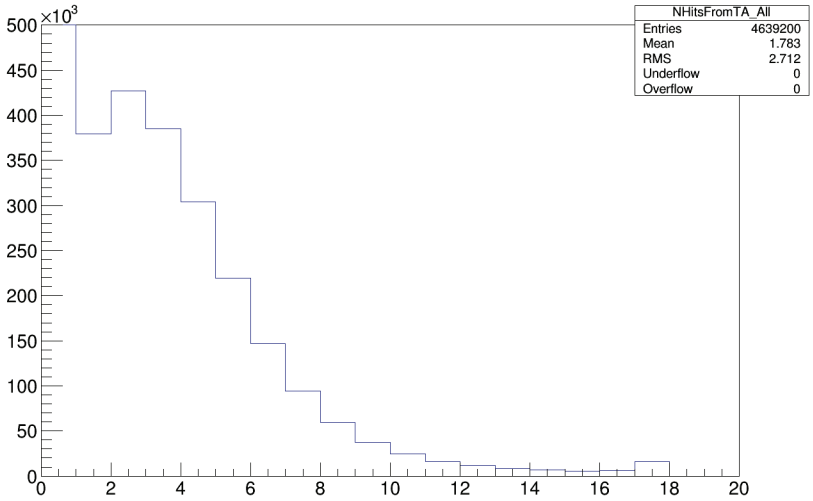


Figure 4.10: ~ 50 bursts of trigger-matched data: a) Time correlation between GTK hits and trigger timestamps. b,c,d) Hit maps of readable chips. August 2015, trigger-matched data.

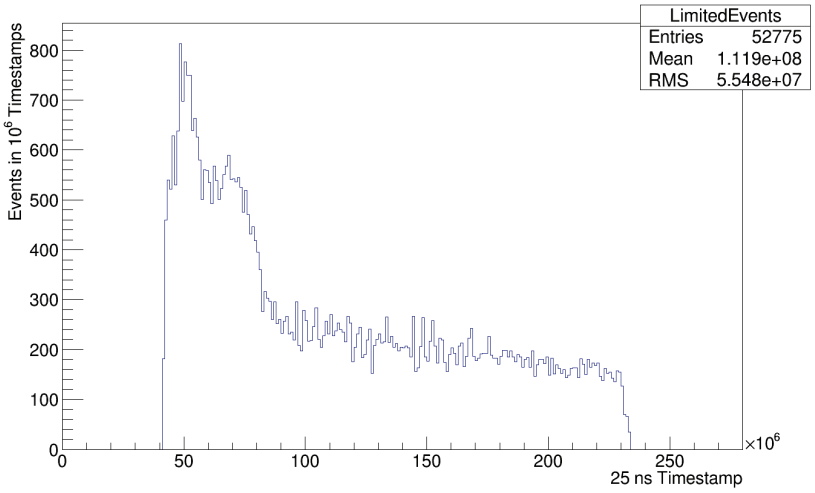
The initial design for the sub-detector PC provided one PC per station (3 GTK-PCs in total).
The GTK-PC DAQ software was in a finalized state, merging event fragments (triggered at L0) and sending all of them to the NA62 PC Farm. This version differs from the one depicted in Subsection 4.1.1, assembling all received event fragments from 10 GTK-RO boards with a *EventAssembler* that puts complete events in a queue. Events are then assembled in Multi Event Packets (MEPs) [25] by a single *MEPAssembler* that pulls events in round robin from the 4 event queues and that finally also sends MEPs to the NA62 PC Farm. Moreover this version had several checks on received data and screen printouts to help with firmware debugging.
The first implementation of the GigaTracker Run Control software was also employed in this period, with complete procedures for configuration and start/end of a run. As already mentioned each instance of the control software, running on a GTK-PC, controlled 10 GTK-RO boards.

During the rest of the run, various problems were spotted and solutions adopted. For example, a limiter on the number of hits from a half GTK-RO board (reading two TDCpix's quarter chips) was introduced in the firmware. This prevented problems connected to modules of the half board getting stuck because of unmanageable number of hits. Some other problems concerned hardware that was promptly replaced.
Eventually, 7-8 TDCpix chips could be read out in each GigaTracker station, even if afflicted by the noise problem (see Appendix B).
After the end of the run, problematic items were identified like the undetected unlocking of PLL in some chips, erratic behaviour of some TDCpix/GTK-RO during initialisation procedure (in general limits in control of the DAQ chain) and limits in the manageable rate by GTK-PC. Regarding this last point, tests were performed at 50% of nominal intensity and different L0 trigger rates, in order to identify possible limitations. These were actually found above $\sim 9 \times 10^5$ triggers/burst or, taking 3.5 s as effective burst duration, equivalent to ~ 250 kHz.
The limitation was then tracked back to a bottleneck in the single *MEPAssembler* entitled to assemble MEPs pulling all L0 events from 4 queue (filled in parallel) and to send over network these packets. Some ideas were proposed to solve this problem, like the already planned doubling of PC, the clean-up of code (debugging checks and printouts) and the possibility to read out the GTK-PC at L1 trigger.

After the end of the run, some analysis were performed on the data in order to understand the behaviour of the GigaTracker DAQ system.
The analysis of the half-board limiter was meant to show the probability of limiter activation as a function of the beam intensity, measured during runs at different intensities up to the nominal. Some examples of plots obtained are shown in Figure 4.11. The occurrence probability of the half-board limiter in a event at nominal intensity was estimated to be $\sim 4\%$.
Finally analysis revealed an unexpected half-chip structure (Figure 4.12), point-



a)



b)

Figure 4.11: Example of half-board limiter related plots: a) Number of hits from a half board module (two quarter chips) in an event. The count excess in bin 17 is due to the cut: all events with 17 or more hits from a half board are counted in bin 17. b) Limited event rate during a burst period at nominal intensity (40 bursts statistics). A crowding of limited events at the beginning of the burst can be traced back to extraction intensity peaks saturating the limiter.

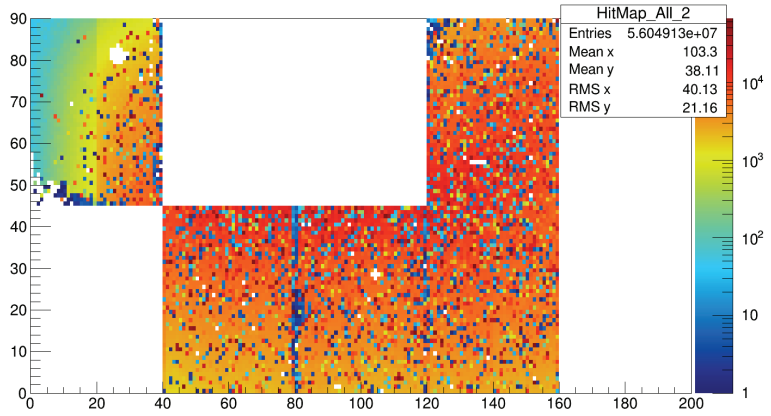


Figure 4.12: A hit map of the GigaTracker with the half-chip inefficiency structure clearly visible on the top left chip.

ing to some kind of inefficiency. From the hardware point of view, the TDCpix chip has only quarter chip structures, so differences in calibration couldn't be accounted for this problem. The GTK-RO board on the other hand features two identical modules that handle half TDCpix (or two quarter chips) making the limiter or some other bug in the firmware be the most probable cause.

2016 Run During the preparation for the 2016 run, various activities were carried out in order to deal with problems pointed out at the end of the previous run and from the analysis of acquired data.
Two main actions groups were identified:

1. finalisation and refinement of the controls for the different DAQ items.
2. optimisation of the GTK-PC's output.

For what concerns the first point:

(a) Carrier board reset via optical fibre from the GTK-TTC.

(b) Individual GTK-RO board soft reset.

(c) Software controls for (a) and (b) to be included in the GigaTracker Run control software.

(d) Automatic (inter-burst) confirmation of correct configuration of the TDCpix.

Regarding the GTK-PC's output optimisation, we finally opted to read out events upon L1 requests, since there was no request for GigaTracker's data in L1 trigger algorithms.
All these items were successfully accounted for and tested before the beginning of the 2016 run together with the planned extension from 3 to 6 GTK-PCs. In particular, for this last item, the control software as well as data acquisition software

were upgraded to be consistent with the new setup. The GigaTracker run control software was updated with new optimized procedure for GTK-RO+TDCpix initialisation. For what concerns the GTK-PC data acquisition software, logging was added in order to help identify new problems.
The Raspberry Pis for I^2C control of the Carrier board (Subsection 4.2.5) were also installed and scripts developed.
Finally, in order to help the debugging of the trigger-matched firmware of the GTK-RO, a parallel acquisition system was set up. This is composed by 3 GTK-RO boards prepared for triggerless operation and 12 optical splitters for the data serial output links (4 per TDCPix/GTK-RO). In this way it was possible to duplicate the 3.2 Gb/s data signals coming from a TDCpix and send them to the standard trigger-matching GTK-RO board and to the triggerless board together. The trigger-matching board maintains the control of the TDCpix for what concerns the configuration, while on the other hand the triggerless one acts as a slave board. In order to control and acquire these triggerless slave boards, the software used for classical triggerless operation was modified and upgraded.
In this way it was possible to acquire pools of data in which both trigger-matched and triggerless data were available, allowing for offline analysis and comparison on a hit by hit fashion in order to spot inefficiencies in the trigger-matched firmware.

All the effort spent in preparation of the 2016 run, allowed for stable data taking conditions since the start of the run.
Nonetheless, the half chip structures identified during 2015 data analysis, revealed a heavy inefficiency in hit extraction by the GTK-RO board firmware. The inefficiency was estimated to be $> 50\%$ and with a sensible variability between boards. At the end of June we spent time in the setup of a test bench with the aim to spot the source of inefficiency. Exploiting the possibility to send periodic pulses to the TDCpix (using the GTK-TTC board), we synchronised these pulses with the L0TP periodic triggers. The goal was to inject pulses at the same time of a trigger in order to have a one-to-one correspondence. This test allowed to spot missing hits and hits extracted out of time, allowing to identify and cure the inefficiency problem in the firmware.
The new firmware version however introduced a new issue, clearly visible in Figure 4.13. Some insight on this new problem was provided with a quick analysis of data. Some reconstructed hits were out of time of several tens of ns, and plotting the projection of the hit map of a chip on the column's axis for hits in-time and out-of-time revealed that the quarter-chip structures were made up by out-of-time hits (Figure 4.14).
A following version of the firmware solved also this problem and starting from the end of July the GigaTracker could be read out with an efficiency of $> 96.5\%$ on the single hit [38], with the inefficiency dominated by edge effects on the 75 ns extraction window (not affecting triggered physics hits). This efficiency was measured taking advantage of the parallel acquisition system, set up at the beginning of the run.

A milestone was successively set in mid-September, with 3 completely read out

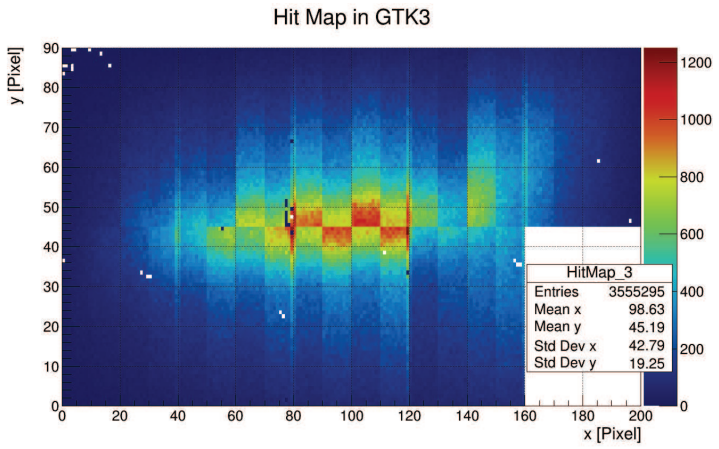
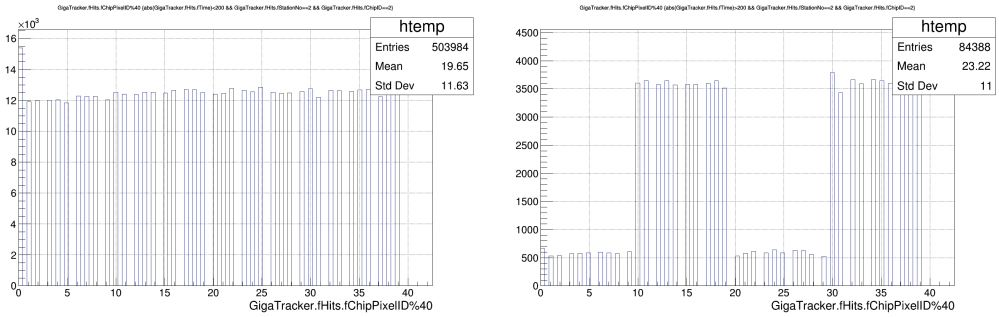


Figure 4.13: A hit map of the GigaTracker with the quarter-chip inefficiency structure clearly visible in all chips.



a) b)

Figure 4.14: Projection of a chip's hit maps on the pixel column's axis for a) in-time hits and b) out-of-time hits.

Run	$I_{T10}[10^{11}]$	Hit limited event fraction
6846	~ 20	2.5%
6847	~ 25	3.1%
6848	~ 31	4.2%

Table 4.1: Limited event fraction for runs with increasing beam intensity.

GigaTracker stations.
In this final phase of the run, the GigaTracker data acquisition worked reliably with few minor issues affecting bursts with bad beam quality (spikes in beam intensity). On the control side, some updates of the code allowed for stable initialisation and run conditions.
Regarding the DAQ problems, the most notable was the "event number jump" problem, found to occur in case of L0 trigger rates $\gtrsim$ 650 kHz. In this cases, some of the GTK-RO board's half modules were losing the "true" event number synchronisation (actually counting more L0 triggers processed) with the result of events not assembled by the GTK-PC. This because in the occurrence of a jump, the corresponding event fragment is paired to a wrong event number, and therefore assembled in the wrong event, while the missing event fragment prevents the GTK-PC to assemble the complete correct event. This problem can anyway be identified and rejected at reconstruction level, comparing the L0 trigger timestamps (25 ns granularity) paired to every event fragment composing a complete GigaTracker event. In case of mismatch the event should be rejected.

Finally, in the days before the end of the 2016 run, tests at increasing beam intensities (up to nominal) were performed, in order to study the behaviour of the GigaTracker DAQ system. Besides a pure functional test, the goal was to evaluate the occurrence of the half-board hit limiter with the 2016 firmware. Since events with limited half-chips should be rejected at analysis level, it is important to evaluate the fraction of these events. This has been done in 3 steps up to the nominal intensity. Results are reported in Table 4.1.
Secondly, a half-chips map of limited events can be drawn as in Figure 4.15 for the run at nominal intensity. Plotting then the corresponding hit map (Figure 4.16) one can identify an inefficiency region in correspondence of the most limited half chip. This points out the need to increase the hit limit from a half chip from 17 to some higher number, that still needs to be evaluated.

All the present open issues will be addressed before the start of the 2017 NA62 physics run.

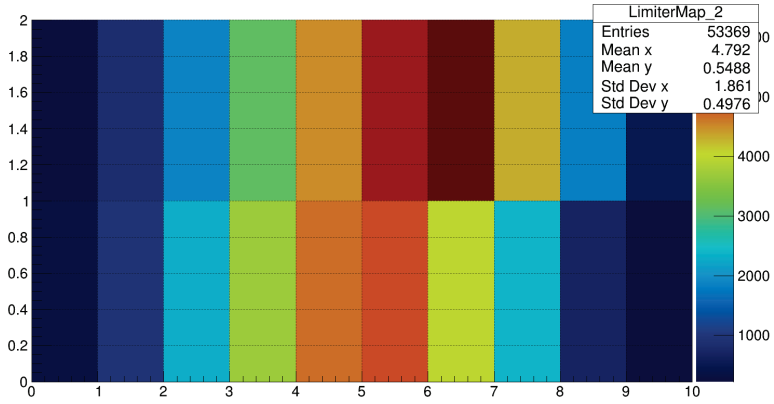


Figure 4.15: Map of half-chip hit limiters for 20 bursts at nominal intensity.

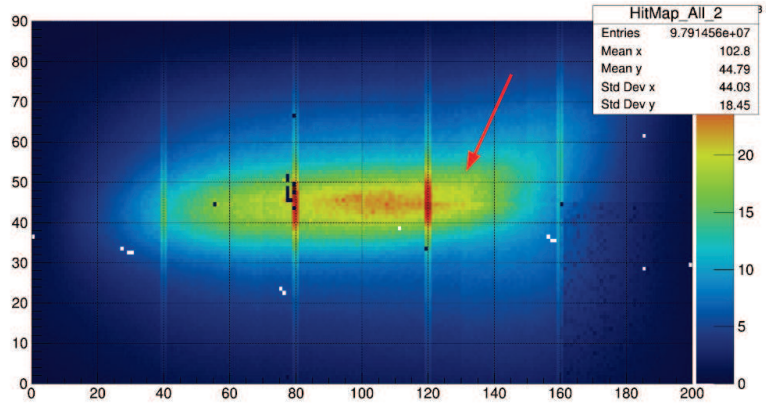


Figure 4.16: Hit map of 20 burst at nominal intensity. The red arrow points to an inefficient half chip, due to the hit limiter activation.

Chapter 5

GigaTracker Performances

After the commissioning of the GigaTracker system, the author contributed to analysis of the data, in particular on the time corrections and alignment of the GigaTracker, and the evaluation of efficiency of the detector and read-out system.

5.1 Time Alignment and Time Walk Correction

All NA62 detectors use the same synchronised clock but the cables lengths, the particles time of flight and others delays introduce constant time offsets among them. The offsets can only be corrected offline. In doing so all the hits belonging to an event are zeroed with respect to a reference time. Every GigaTracker pixel has its own time offset, that should be accounted for individually. This step is essential in the timing analysis. We will show that most of the offset can be traced back to specific groups of pixels (e.g. chip's row).
The GigaTracker front-end is based on a time-over-threshold discriminator which requires an offline time walk compensation. As we will see, calibration curves are extracted from the data. Given that each pixel front-end is unique, a specific correction curve should be needed for each pixel (we will show that corrections can be computed for an entire chip); the correction also depends on the detector operating conditions. Moreover, the ageing of the sensor will affect the charge collection properties. For the reason stated above, the correction curve has to be recomputed regularly.
In order to exploit the potential hit time resolution of the GigaTracker, corrections must be applied at data reconstruction level in order to take care of:

- Station and chip (board) time offsets (or T0s).
- Pixel time offsets.
- Time-walk corrections.

The previous are referred to some time reference, being in the present study the KTAG Candidate time.

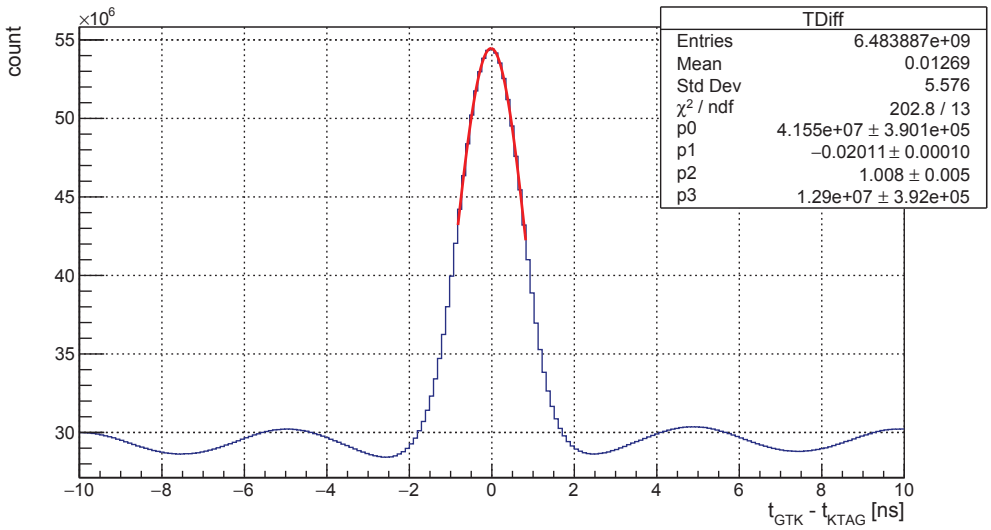


Figure 5.1: Raw time resolution after automatic T0 computation. The histogram shows the time difference between hits in the GigaTracker and the KTAG candidate time. The fit is performed with a gaussian + a 0th degree polynomial functions.

5.1.1 Automatic T0 Reconstruction Computation

The NA62 Reconstruction features an automatic procedure for Station and Mezzanines (TDCpix/Readout boards for the GigaTracker) T0s computation. The author implemented the code needed to include the GigaTracker in the latter procedure. This allowed to have hits belonging to all TDCpixs automatically time-aligned on a run by run basis directly in the reconstructed data.
This raw alignment alone allows to obtain a time resolution of $\sim$ 1000 ps including the KTAG candidate time resolution component as shown in Figure 5.1.

5.1.2 Timing corrections

Finally in order to obtain the design time resolution, fine corrections should be applied. We studied different procedures to compute T0s and Time walk correction for pixels (or groups of them) taking into account the trade-off between resolution itself and available statistics of data as well as computing resources.
In general, results presented hereafter, are based on $\sim$ 1000 bursts and using the chip's row of pixels as smallest group for T0 evaluation.

For what concerns time walk, the idea behind the correction method is presented in Figure 5.2. Two timestamps are recorded when a shaped pulse crosses a predefined threshold, the first on the signal rising edge (T_L) and the second on the signal falling edge (T_T). The time-over-threshold ($T_T - T_L$) is proportional to pulse height and therefore indirectly to the amount of energy deposited in the

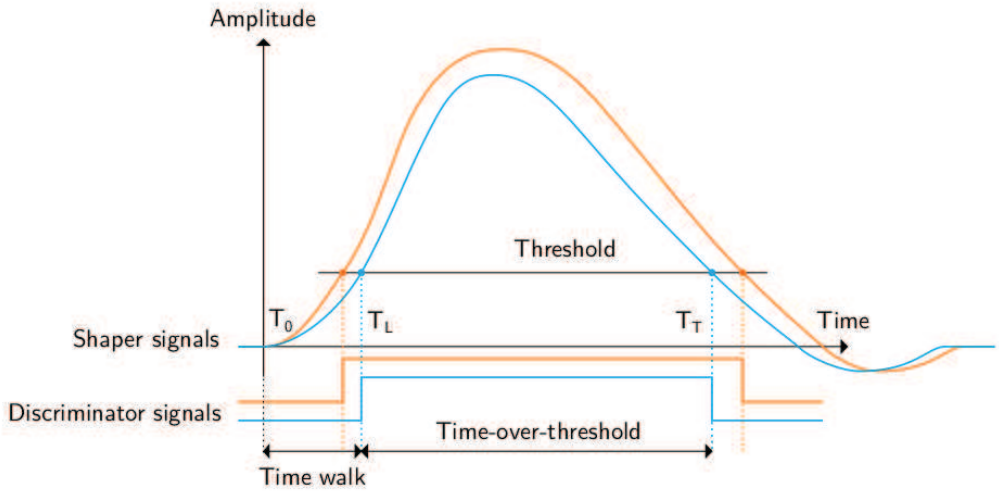


Figure 5.2: Illustration of the relation between the time walk and the time-over-threshold. Higher amplitude signals lead to bigger time-over-threshold and vice versa.

pixel. Bigger time-over-threshold leads to smaller time walk and vice versa, one can use this relation to compensate for the time walk. The relation is fairly linear for medium energy deposits but non-linear behaviours appears for low and high energy depositions [27].

Chip's time walk + pixel T0

The first method is driven by the present GigaTracker private database configuration:

- 3×18000 pixel time offsets.
- 3×10 2nd degree polynomial function parameters to account for chip's Time walk.

The procedure consists in the following steps:

1. Create histograms with the time difference between GTK hits and KTAG candidate for each chip's row of pixels.
2. Fit these histograms in order to find row's pixel time offsets.
3. Create 2D histograms per chip, with hit time difference (corrected for row's T0) against hit Time-over-Threshold (Time-walk plots).
4. Fit the Time-walk plots using a slice and fit procedure in order to extract the 2nd order polynomial parameters (Figure 5.3).
5. Refine row T0s or pixel T0s (if enough statistics is available) applying Time walk corrections and reiterating steps 1 and 2.

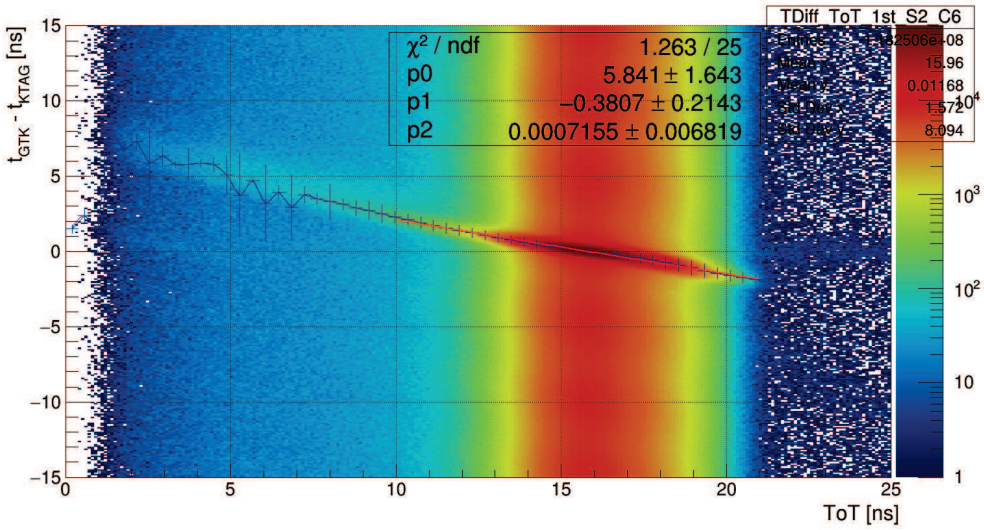


Figure 5.3: Example of a time-walk fit.

This procedure allows to obtain a hit time resolutions of ~ 230 ps, including the ~ 70 ps KTAG candidate time resolution (Figure 5.4).

An alternative solution for Chip's time walk correction is based on a time-over-threshold bin-by-bin mapping of the time walk. Each bin is 98 ps due to the TDC's specifications. Before the evaluation of time walk, the T0 correction for row is performed. In this case, the T0 is not extracted using the integrated distribution of time difference between GTK hits and KTAG candidate over the all ToT range but instead using a ToT slice in correspondence of the ToT peak of the chip. In this way the T0 is independent from any change in the time-walk distribution due to radiation damage.
After T0 extraction, the usual 2D histogram is filled for every chip, and the distribution peak for all ToT bins is extracted (see Figure 5.5). After T0 and time-walk correction, it is possible to obtain a hit time resolution in line with the method described above. It is also possible to refine the T0 corrections at the single pixel level, further improving the hit time resolution.
This last method is the one currently employed for the time corrections in the GigaTracker reconstruction analyser. The number of parameters to store for the time-walk corrections is 256 values (equivalent to a 25 ns ToT range) for each chip.

Chip's row time walk

A second strategy needs less steps but requires to save 30×45 2nd degree polynomial function parameters. The procedure consists in the computation of the Time walk corrections for each one of the 30×45 chip's row of pixels. This corrects for time walk itself and for the T0 of the row.
Time hit resolution after correction is applied is shown in Figure 5.6.

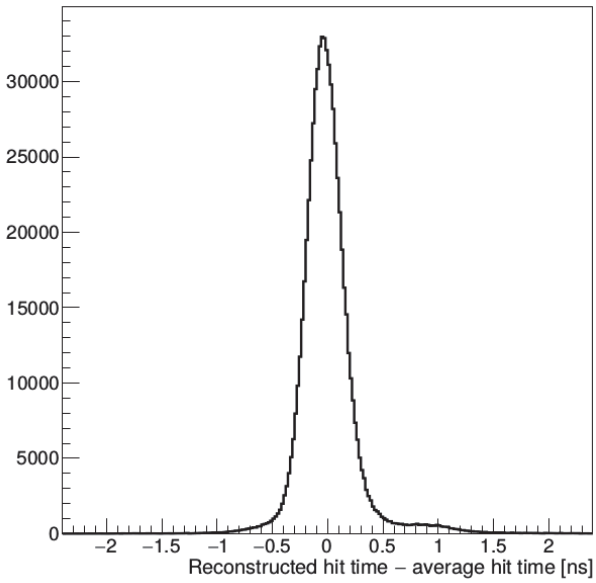


Figure 5.4: KTAG performance measured with the 2015 data. Time resolution of a typical PM signal; a Gaussian fit to the central peak gives a resolution of 160 ns; this leads to kaon time resolution of 70 ps

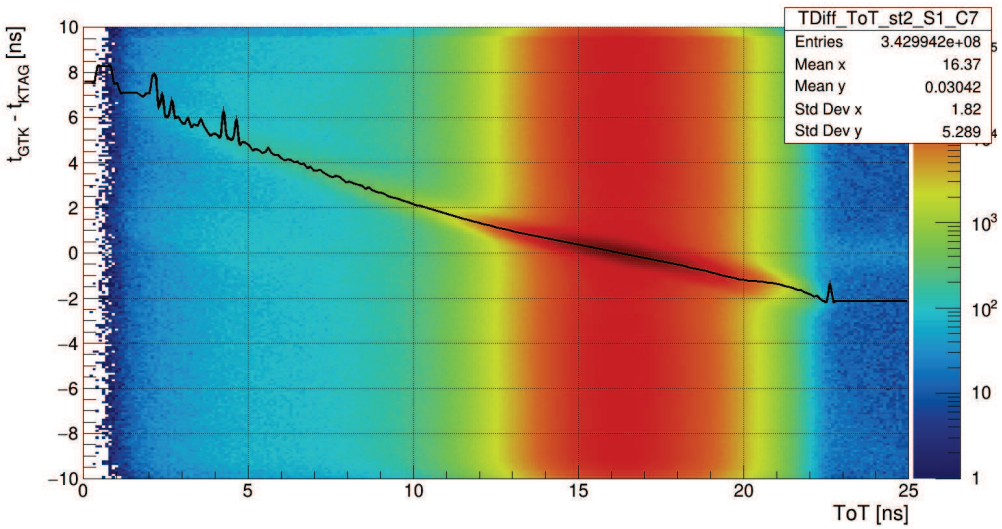


Figure 5.5: Time walk distribution with the overlayed points of its bin-by-bin mapping.

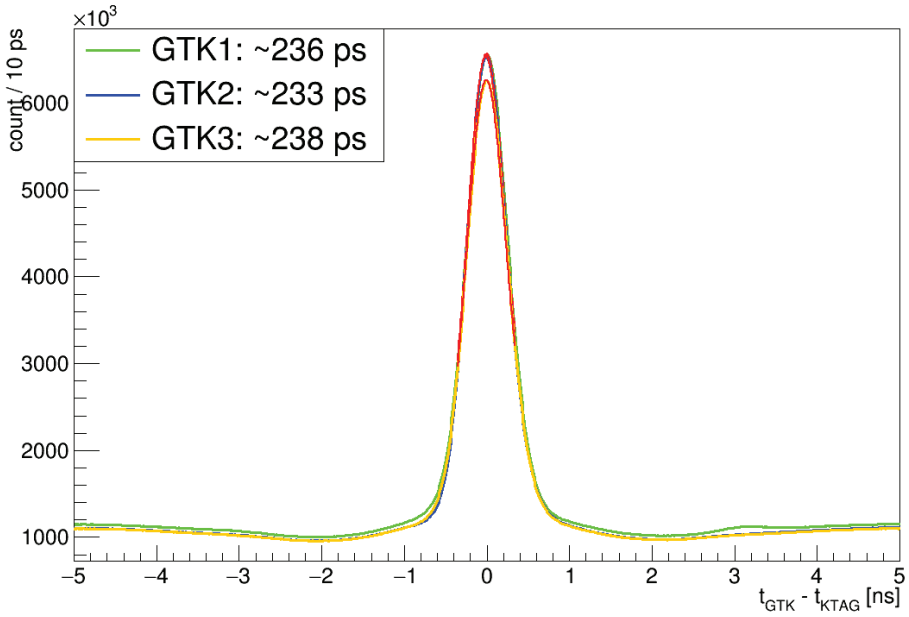


Figure 5.6: Fine time resolution after Time walk correction per chip's row is applied. The histogram shows the time difference between hits in the GigaTracker and the KTAG candidate time. The fit is performed with a gaussian.

5.2 Spatial Alignment

The spatial alignment of the GigaTracker is relatively straightforward, since the stations are mechanically very well constrained by the vessel and the only relevant degrees of freedom are in X and Y plane. Nevertheless small offsets can be introduced during the assembly of all the components hence the alignment must be carefully checked.

The strategy to extract the X-Y corrections of the 3 stations is based on the downstream reconstruction of $K^+ \to \pi^+\pi^-\pi^+$ decays using the information of the Straw spectrometer. Let us define "downstream K^+" the kaon track reconstructed from the 3 pion tracks, as opposed to the GigaTracker-reconstructed kaon track. The reconstructed downstream K^+ (momentum and direction) can be then projected back to the Z position of the 3 stations in order to compare it with the expected hit position from the GigaTracker data.

The kaon initial position and momentum are reconstructed as the vertex of a filtered 3 π event. The downstream K^+ is then propagated through the "Blue Tube" field back to the GigaTracker station 3 position. Taking in consideration the magnet setup of the beam line (sketched in Figure 5.7) it is then required to remove the kick of TRIM5 and bending magnets in order to extrapolate back the position in stations 2 and 1.

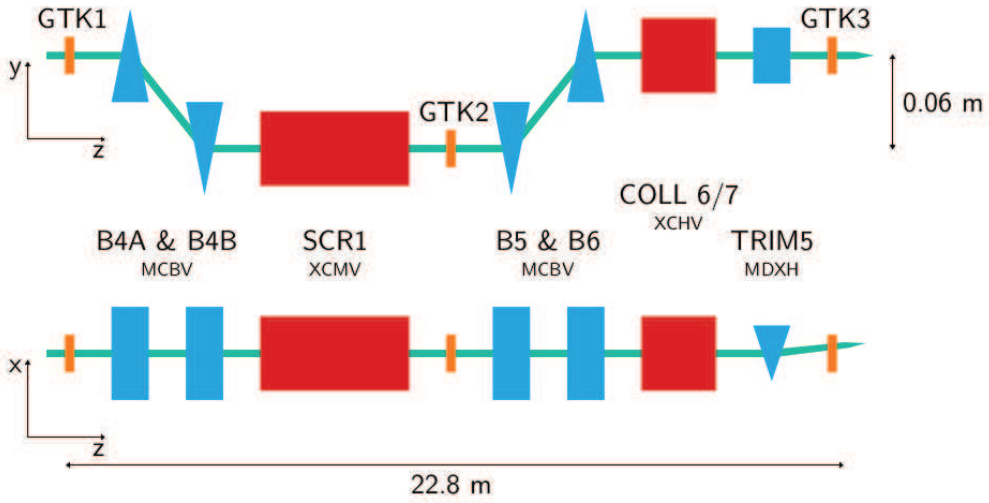


Figure 5.7: Scheme of the beam line in the GigaTracker region. The magnets B4A, B4B, B5 and B6 are standard dipoles. The TRIM5 is a short dipole magnet.

In general the shift due to the TRIM5 magnet is computed as:

$$dX = c \cdot Bl \cdot \frac{\Delta Z}{P} \tag{5.1}$$

where Bl is the integrated magnetic field, ΔZ is the distance between the evaluation Z position and the magnet's Z position and finally P is the kaon momentum. All these quantities are known from database (lengths and magnetic field strengths) and from the reconstruction of the 3π vertex.
The same equation and principle applies on the Y-axis for the dipole bending magnet induced displacement.

The selection of the 3π event is based on a standard 3-track selection with the addition of:

- only three tracks in the event
- no MUV3 candidate
- $E/p < 0.8$ in the Lkr in order to reject electrons
- one good KTAG candidate
- CHOD and NewCHOD candidates associated with the tracks
- $(t_{KTAG} - t_{K3\pi}) < mean \pm 3\sigma$

where $t_{K3\pi}$ is the weighted mean of CHOD and NewCHOD times for the three tracks.
In this way it is possible to use the KTAG candidate time to match hits in the 3 GigaTracker station and compute the X and Y difference between GigaTracker

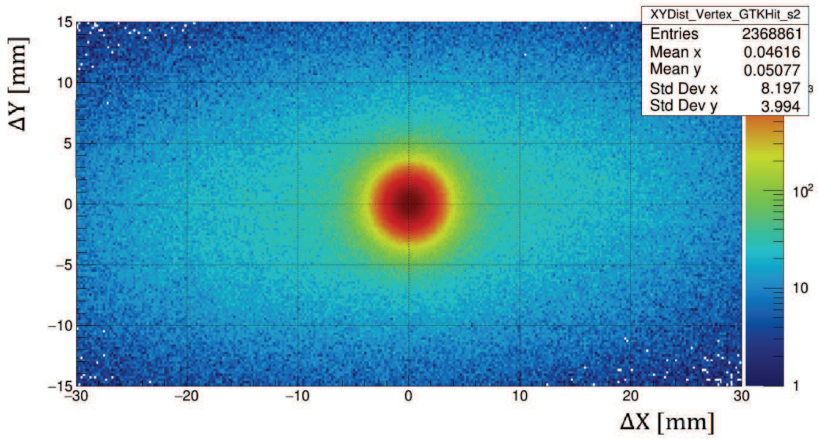


Figure 5.8: X-Y distribution of the space difference between GigaTracker hits and $K3\pi$ extrapolated position in GTK3.

hits and expected $K3\pi$ position in the corresponding station.

Fitting the distribution of space offsets, the corrections and the position resolution on X and Y can be extracted for the 3 stations. The corrections are detector-dependent in the sense that they change in general when different GigaTracker assemblies are installed on beam, and they are usually in the (0.5 - 3.0) mm range for both X and Y. Obtained position resolutions are $\sim 1.5mm$ for both X and Y for GTK3 and they worsen extrapolating to GTK2 and GTK1 because of magnets' corrections.
In Figure 5.8 an example of the X-Y hit space difference after offset corrections.

5.3 Track association

After time and spatial corrections it is then possible to reconstruct GigaTracker candidates. The procedure requires to select triplets of in-time GigaTracker hits (0.7 ns time window) and build the track using standard reconstruction routines. The parameters of the reconstructed GigaTracker track can then be compared with the corresponding ones of the $K \to 3\pi$ reconstructed downstream K^+ in order to evaluate their agreement.
Meaningful quantities to compare are:

- difference in reconstructed momenta ($|p_{GTK}| - |p_{K3\pi}|$) (Figure 5.9)
- dx/dz (θ_x) vs x (Figure 5.10)
- dy/dz (θ_y) vs y (Figure 5.11).

Moreover, one can evaluate a series of discriminants to select a clean sample of matched $K - 3\pi$ tracks:

- GTK - K3π difference in momenta ($|p_{GTK}| - |p_{K3\pi}|$)

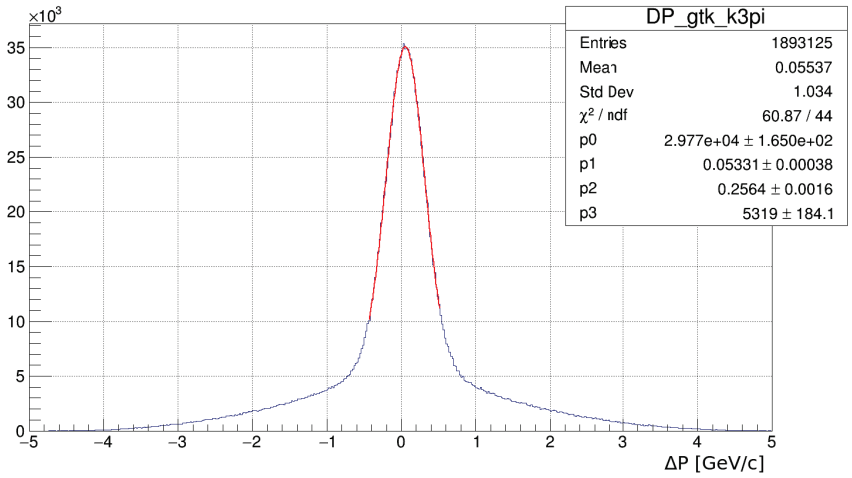


Figure 5.9: Difference in reconstructed momenta ($|p_{GTK}| - |p_{K3\pi}|$).

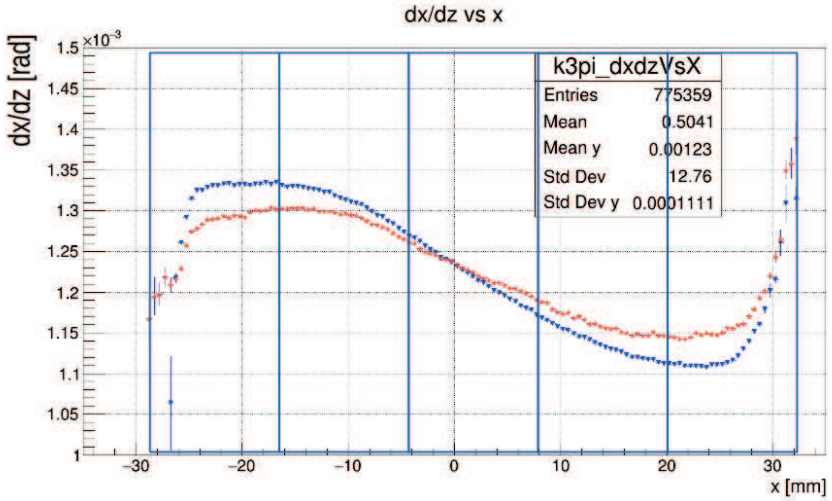


Figure 5.10: θ_x vs x. GigaTracker markers in red and $K3\pi$ in blue. The horizontal extension of the detector is divided in 5 parts in order to show the dependence on the 5 chip colomns.

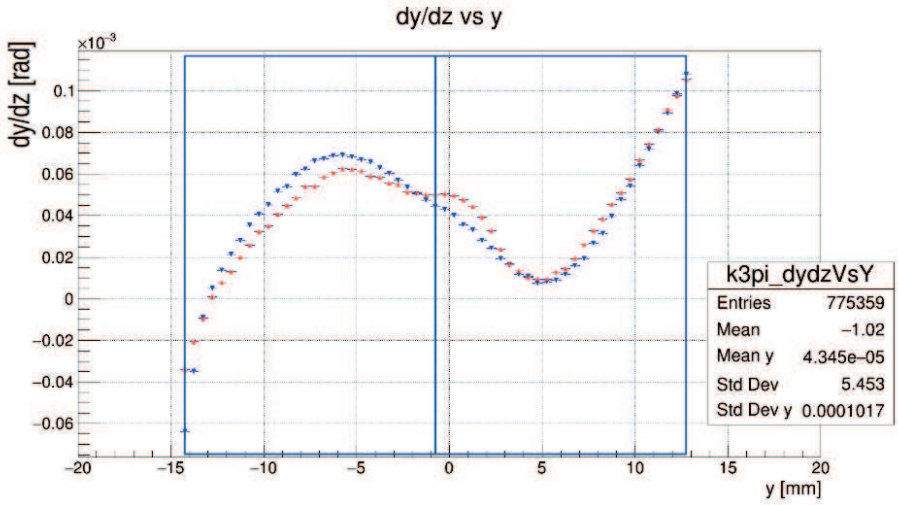


Figure 5.11: θ_y vs y. GigaTracker markers in red and $K3\pi$ in blue. The vertical extension of the detector is divided in 2 parts in order to show the dependence on the 2 chip rows.

- GTK - K3π difference in θ_x and θ_y
- GTK - K3π difference in x and y for station 3
- time resolution with respect to the associated KTAG candidate.

Resolutions on the listed quantities, extracted from Run 6683, are:

- $\sigma_p \sim 0.25$ GeV/c
- $\sigma_{\theta_X} \sim 23.5$ µrad
- $\sigma_{\theta_Y} \sim 27.2$ µrad
- $\sigma_X \sim 1.395$ mm
- $\sigma_Y \sim 1.496$ mm
- $\sigma_t \sim 150$ ps .

Cutting on around 3σs for all the above quantities on can appreciate the clean selection of $K3\pi$ events showed in Figure 5.12. A simple hit-or-miss check can then be performed on each station, populating a map with matched GigaTracker hits with respect to the $K3\pi$ (Figure 5.13) and missed 3π downstream K^+ position (Figure 5.14). In this example with data from Run 6683, it is possible to appreciate the link between missed $K3\pi$ and inefficiency in matched GigaTracker hits.

Finally a raw estimate of the combined inefficiency of the GigaTracker's readout and reconstruction can be measured by a simple counting of selected $K3\pi$ events without any GigaTracker candidate in time and with $|p_{GTK}| - |p_{K3\pi}| < 0.3$

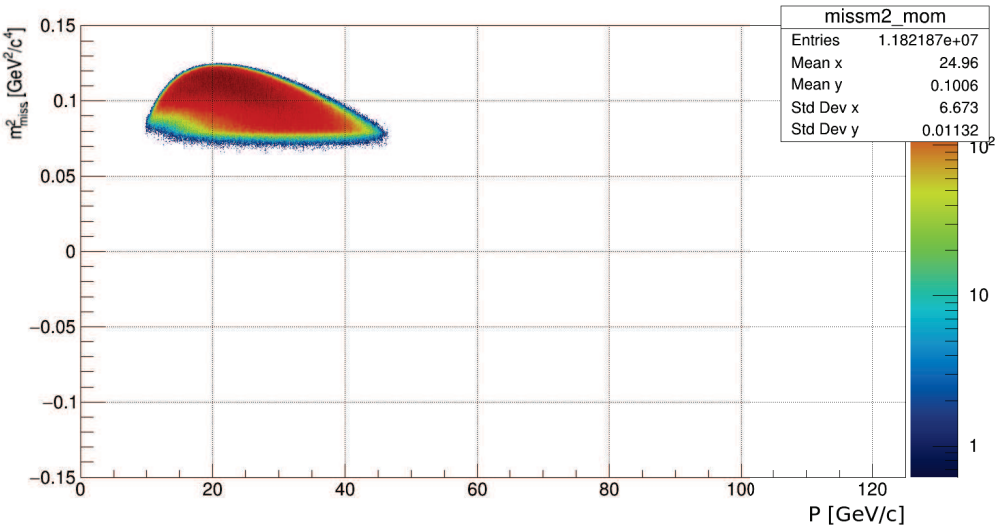


Figure 5.12: Distribution of the missing mass squared vs kaon momentum for all pions after 3π selection and 3σ cut on discriminant quantities.

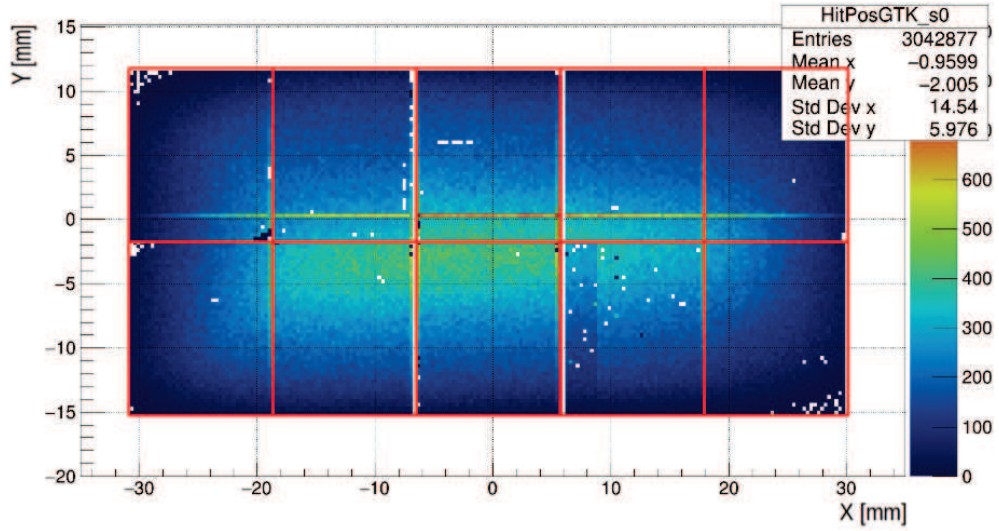


Figure 5.13: Matched GigaTracker hit map. In red the boundaries of the TDCpix chips are displayed. One can note an inefficient band (quarter chip) in the 4th chip from the left on the bottom.

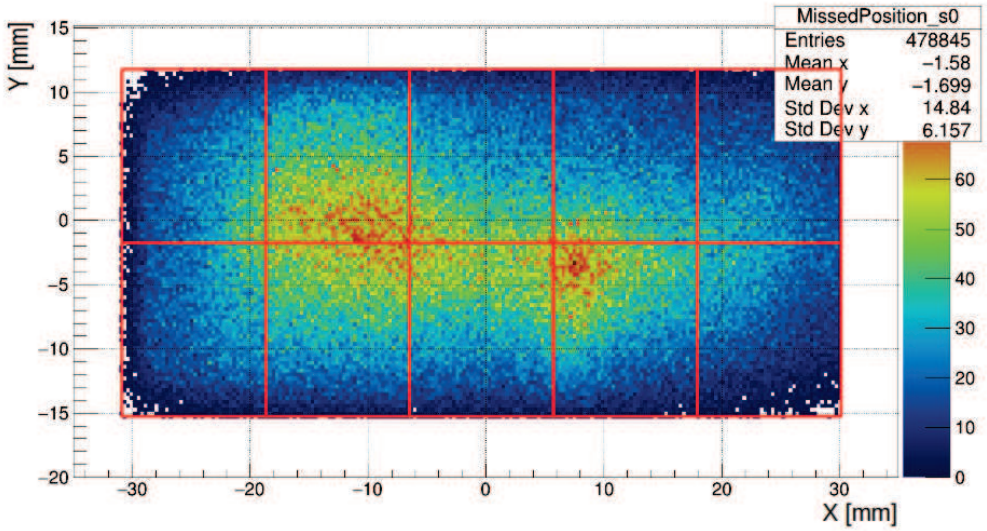


Figure 5.14: Missed 3π downstream K^+ projected on the GigaTracker detector. In red the boundaries of the TDCpix chips are displayed. Hot regions are due to inefficiencies (in this case a bandwidth saturation due to noisy pixels.

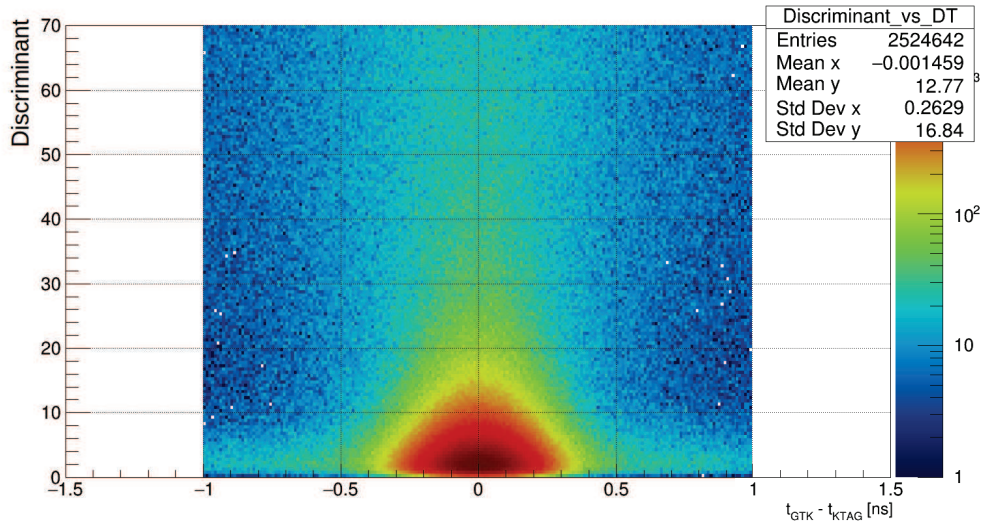
GeV/c. An inefficiency of $\sim 10\%$ is estimated from Run 6683. This is above the 3% inefficiency requirement. Although precise alignment in time and space plays a key role in this respect, investigations on data acquisition and reconstruction are foreseen in order to decrease the inefficiency.

5.3.1 Track matching based on discriminants

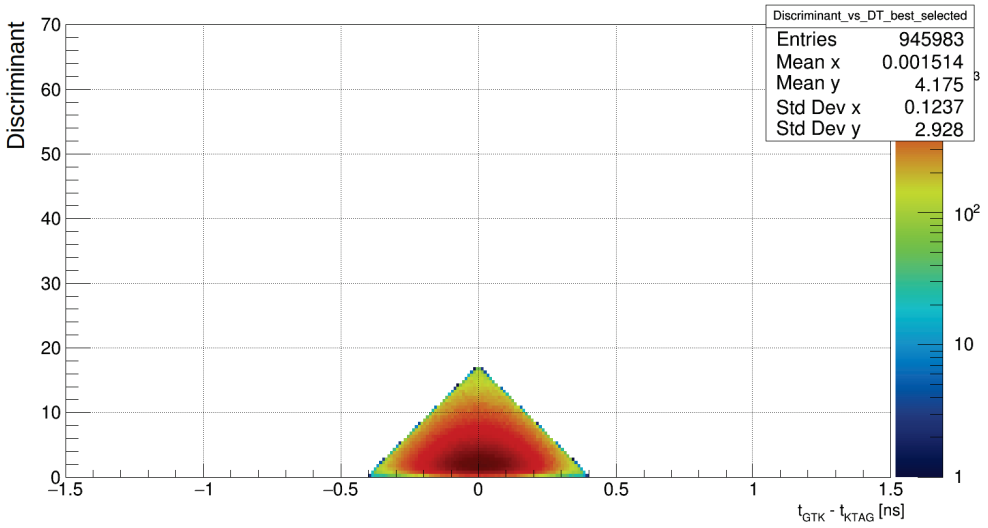
In order to associate the $K3\pi$ event to the right GigaTracker candidate, a discriminant is evaluated, based on the resolutions of the quantities listed above.

$$D = \left(\frac{|p_{GTK}| - |p_{K3\pi}|}{\sigma_p}\right)^2 + \left(\frac{\theta_{X(GTK)} - \theta_{X(K3\pi)}}{\sigma_{\theta_X}}\right)^2 + \left(\frac{\theta_{Y(GTK)} - \theta_{Y(K3\pi)}}{\sigma_{\theta_Y}}\right)^2 + \left(\frac{X_{GTK} - X_{K3\pi}}{\sigma_X}\right)^2 + \left(\frac{Y_{GTK} - Y_{K3\pi}}{\sigma_Y}\right)^2 \tag{5.2}$$

One can define the best GigaTracker candidate associated to a $K3\pi$ event by looking for the candidate with the minimum value of the discriminant D. The latter is defined as "best" GigaTracker candidate. It is also necessary to further clean the sample applying a cut, based on the the discriminant itself and the time difference between the GigaTracker candidate and the KTAG candidate associated to the $K3\pi$ event. Due to the shape of the obtained distribution, a triangular cut is applied (Figure 5.15).
This allows to work with pool of events with a GigaTracker candidate matched to a 3π event and to therefore study a technique to match single downstream tracks (the 3 tracks of the $K3\pi$ event) to a GigaTracker candidate using available observables.



a)



b)

Figure 5.15: (a) Distribution of discriminant D vs. GTK-KTAG time difference. (b) Triangular cut applied to the distribution.

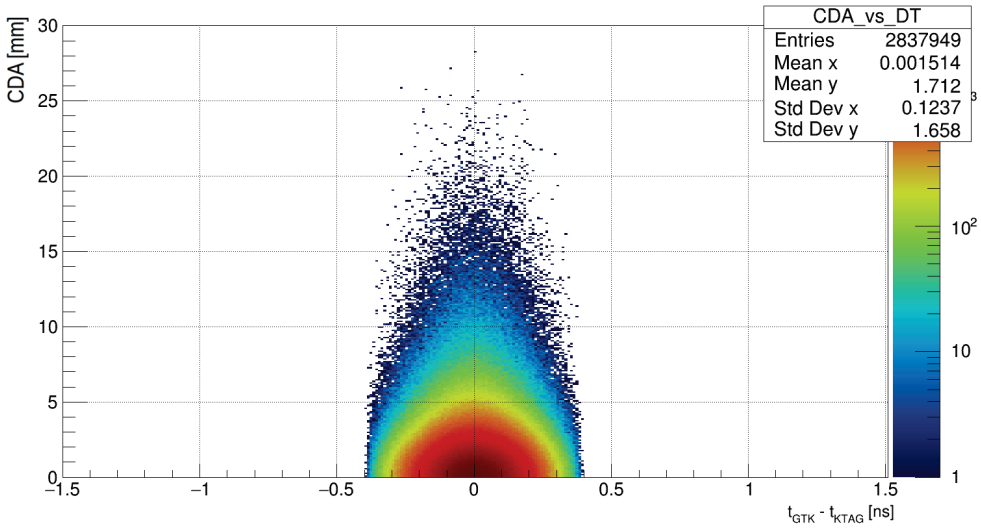


Figure 5.16: Distribution of CDA vs. time difference for single downstream tracks part of matched $K3\pi$ events. The match is based on the discriminant cut for "best" GigaTracker candidates.

In order to achieve the single track matching, the closest distance of approach (CDA) together with the time difference is used. These quantities are computed with the GigaTracker track and the single downstream track (in case of the downstream track, the associated KTAG time is used). A 2D distribution of CDA against time difference is populated (Figure 5.16) and a parabolic cut used to discriminate the single track matching (Figure 5.17).
The application of the CDA vs. time difference cut, results in the rejection of some single tracks participating to matched $K3\pi$. In particular, the $\sim$ 91.5% of matched best candidates has 3 selected single tracks as shown in Figure 5.18. This leads to a single track miss ratio of $\sim$ 3%.
Moreover, it is possible to independently evaluate the ratio match vs. mismatch based on the CDA vs. time difference using all GigaTracker candidates (as opposed to previous studies based on the best candidate). The match is defined as a single downstream track matched to the best GigaTracker candidate for that $K3\pi$ event, and a mismatch is a single downstream track matched to a GigaTracker candidate not being the best one. The result using a non-optimised cut is a mismatch probability of $\sim$ 3.8%. Obviously the CDA vs. time difference can be narrowed, although increasing the miss probability.

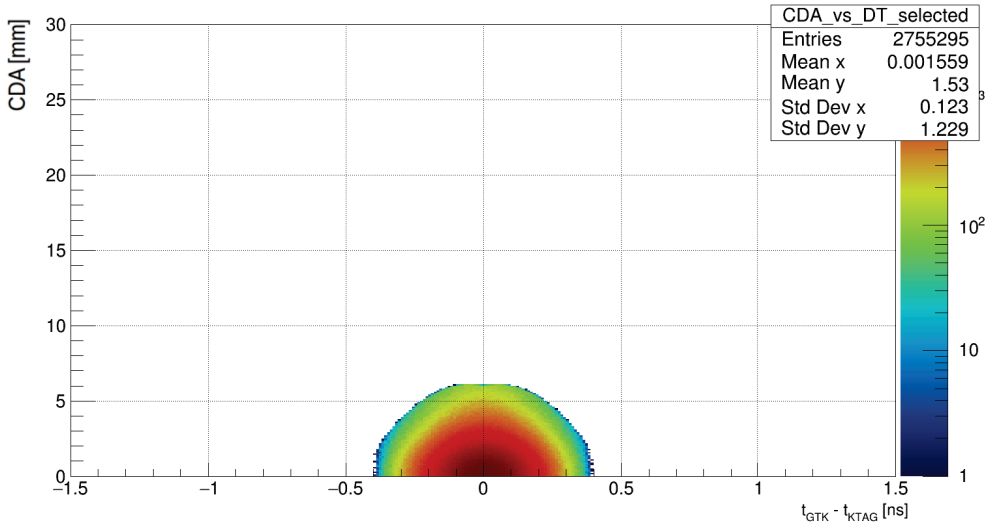


Figure 5.17: Parabolic cut of the CDA vs. time difference distribution.

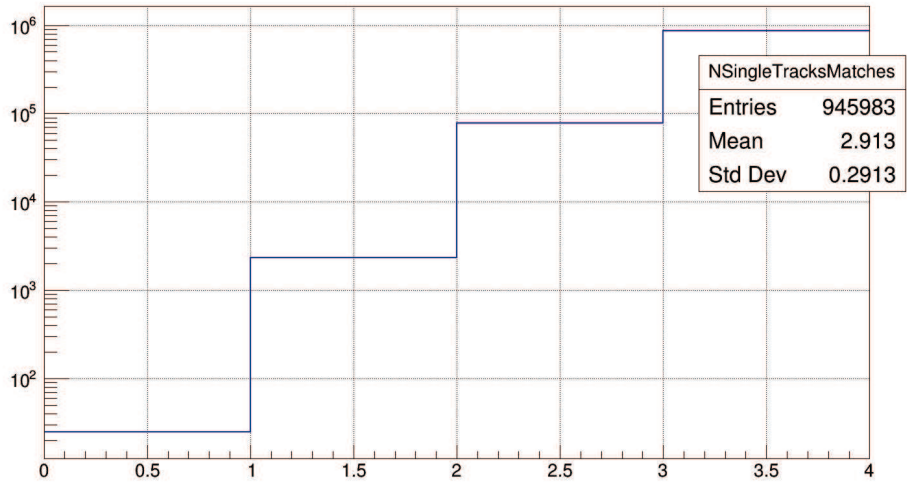


Figure 5.18: Number of single track matches passing the CDA vs. time difference cut per best GigaTracker to 3π match.

Conclusions

The GigaTracker is a key detector for the NA62 experiment, which main goal is the measurement of the Branching Ratio of the ultra-rare $K^+ \to \pi^+ \nu\bar{\nu}$ decay, a powerful tool to test the validity of the Standard Model. The GigaTracker is a flagship project of CERN due to its unique features in terms of rate capabilities, time resolution, radiation hardness and cooling technology.

This thesis describes the development, commissioning and testing of the GigaTracker's data acquisition and control systems, as well as the analysis of its data in order to evaluate time corrections, space offsets and quality of the data.

The author had a key role in the integration of the off-detector readout electronics and TDCpix chip. In particular, he designed an acquisition and control software tuned on the requirements of the evolving system at all the commissioning steps, and provided constant debugging support for firmware and hardware developers.
The software of the PC-based stage of the data acquisition chain was developed in the context of this thesis. The system allows to receive, process and temporarily store more than 450 MB/s from five off-detector readout boards per each of the six GigaTracker sub-detector PCs, while performing L1 trigger matching.
A software control system, crucial for the operation of the whole data acquisition system of the GigaTracker, has also been developed by the author. It manages of all the procedures to configure, synchronise and operate the various components of the off-detector and front-end electronics providing as well an interface to the NA62 experiment run control.

After the phase of commissioning, the author performed an analysis of the detector data, aimed at extracting time corrections and at estimating its timing performance, as well as the spatial offsets and data quality using reference decay channels.
The design of the GigaTracker front-end electronics allows to achieve a resolution better than 200 ps on the hit time. In order to fully exploit the potential hit time resolution, time walk correction and time alignment are mandatory. The author explored different approaches for the computation of the corrections to apply to the acquired data. This allowed to measure the actual time resolution of the GigaTracker, that corresponds to the design specification of 150 ps on the track time.
The total inefficiency on the track reconstruction was also evaluated, resulting in

$\sim 10\%$ on the analysed run. This value currently exceeds the requirements. As a consequence, further tuning of the reconstruction and debugging of the GigaTracker data acquisition system are needed.

This thesis work, and in particular the development and commissioning of the GigaTracker's data acquisition and control systems, has been crucial for the complete commissioning of the GigaTracker detector and its successful employment in the NA62 data taking in 2016 and the years to come.

Appendix A

Single Event Upset Monitoring

As reported in Section 3.2, registers of the TDCpix on the beam path are triplicated. In order to understand the occurrence of Single Event Upsets (SEU) during a particle burst, a series of C++ classes were developed and included in the GigaTracker Control software, featuring readback of the triplicated registers in 3 slices in continuous or error-triggered modes.
The single slices are composed of bits coming from either the registers a, b or c that partecipate in the majority vote of the triplicated register output. These slices can then be compared to the loaded configuration file in order to spot bit flips in registers using a set of analysis tools.
Pixel matrix configuration and end-of-column configuration registers are triplicated: per column pair 2×45 (pixels) $\times 8$ bits + 22 bits + 43 bits for a total of 15700 triplicated bit registers taking into account 20 column pairs per chip.

At the end of the 2016 run, exploiting the tests at nominal intensity, a pool of 117 burst-equivalent slices have been acquired in continuous mode. This means that the slices were read back from the TDCpix hardware regardless of the SEU error bit being set or not (in order to acquire also triple SEU). The read-back was active in all 30 chips. The results are shown in Figure A.1.
It is possible to compute a table of SEU probabilities per chip (all register bits) in a burst (Table A.1 and per single register bit (Table A.2.

SEU type	SEU probabily/chip/burst
Single	~ 0.37
Double	$\sim 2 \times 10^{-3}$
Triple	$< 3 \times 10^{-4}$

Table A.1: SEU Probabily of different SEU types per chip in a burst.

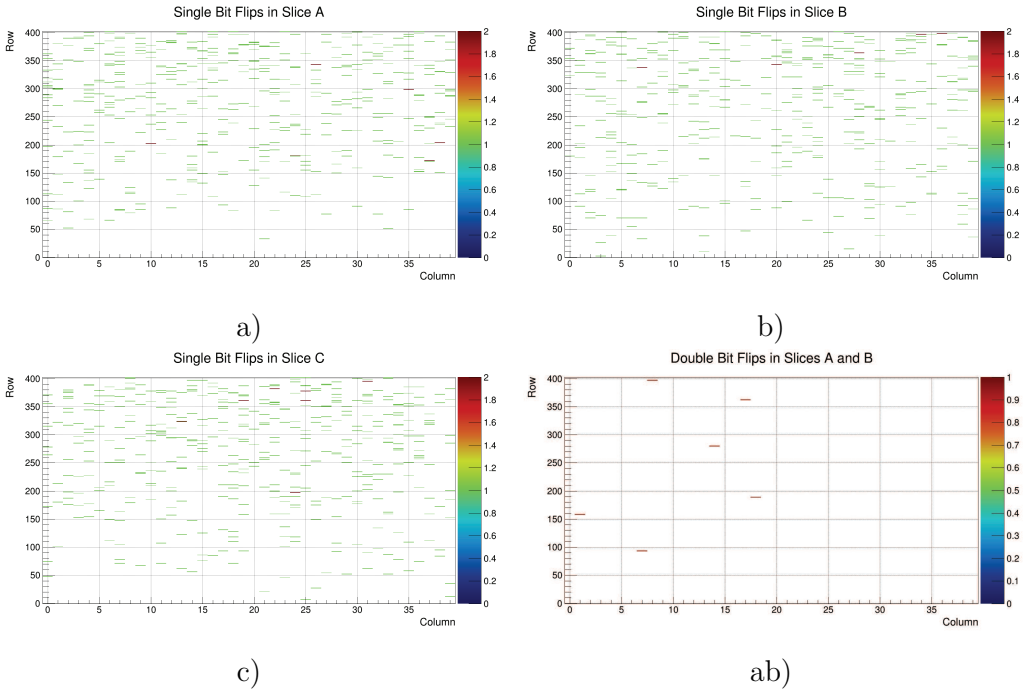


Figure A.1: SEUs recorded on 117 bursts. The plots show the integrated count for the 117 bursts and the 30 chips. a,b,c) are Single SEUs respectively of the bits in the first, second or third slice. ab) represents Double SEUs, in this particular case a flip of the same bit in first and second slice.

SEU type	SEU probabily/bit/burst
Single	$\sim 2.3 \times 10^{-5}$
Double	$\sim 10^{-7}$
Triple	$< 2 \times 10^{-8}$

Table A.2: SEU Probabily of different SEU types per single register bit in a burst.

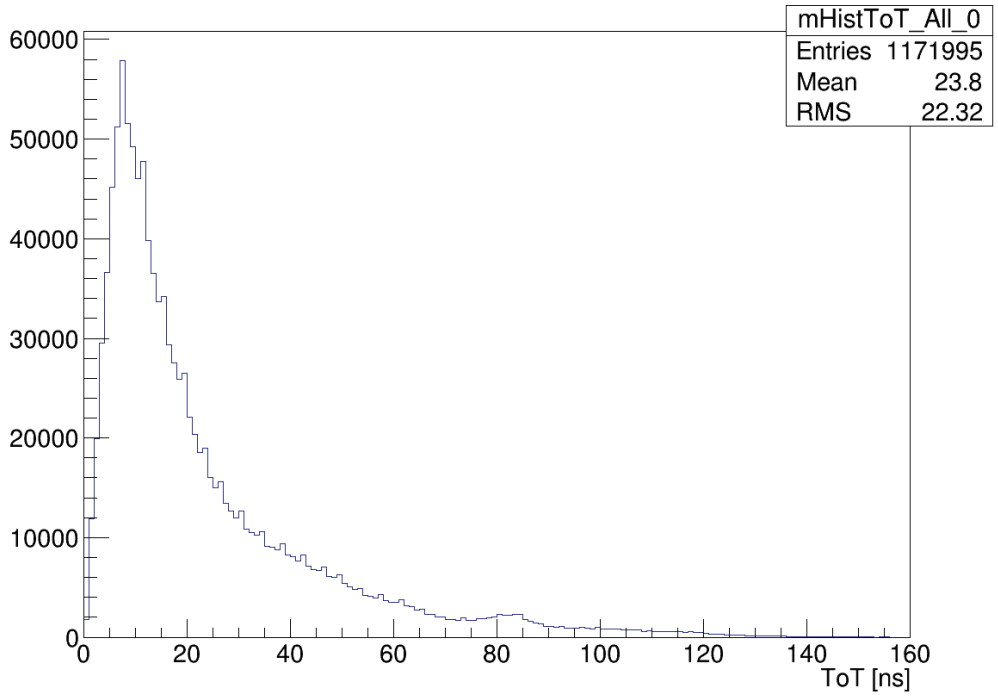
Appendix B

Noise identification

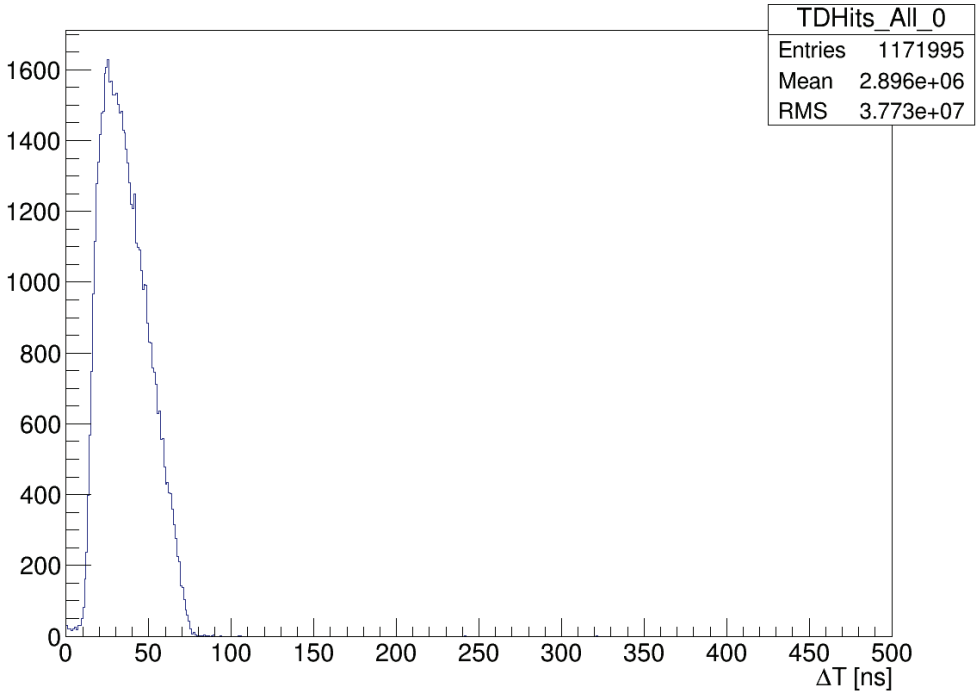
During 2015 run the first detectors with $\sim 70\%$ working chips were used during data taking. These detectors started to present the appearance of noisy pixels after some time of exposure to the hadron beam. These noisy pixels were changing hit frequency throughout a run, and outnumbering the physics hit rate by orders of magnitude. Moreover, a small number of noisy pixels in a quarter chip can fill the bandwidth of the 3.2 Gbps link, causing therefore a noticeable inefficiency. This made the initial analysis of data extremely challenging. In order to be able to time align and measure a preliminary time resolution of the detector, some strategies for tagging noisy pixels during data analysis were defined by the author, as well as providing the tools to mask heavily affected pixels directly in the pixel matrix configuration.

An example of analysed noise data can be seen in Figure B.1, acquiring during a dedicated run without beam. The distribution of time-over-threshold shows a tail in the high ToT region, usually not populated by physics hits, while the distribution of time differences between successive hits shows a peak around ~ 30 ns, corresponding to ~ 30 MHz hit rate, well above the peak rate for a central pixel at nominal intensity (114 kHz).

One strategy for noise tagging is based on the counting of hits per pixels during a burst. These counts are ordered per increasing number (Figure B.2) and an estimation of the distribution profile is made based on bins in the first 3/4 (assuming they aren't affected by noise). This allows to extrapolate the maximum number of hits in the hottest pixel (noise excluded) and therefore set a limit for the number of physics hits in a pixel. Pixels with more hits (including an additional safety factor) are tagged as noisy.



a)



b)

Figure B.1: Noise data from Run 4173. (a) Distribution of time-over-threshold. (b) Distribution of time differences between successive hits in the same pixel.

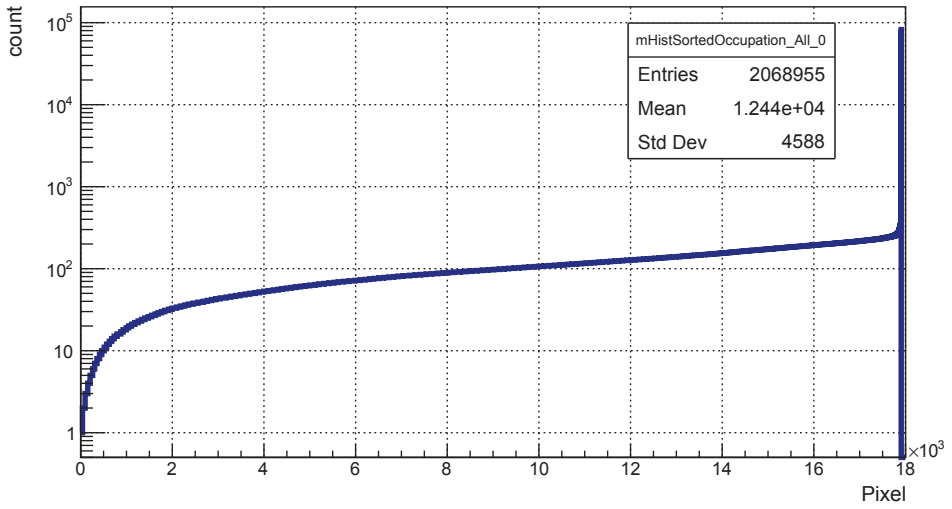


Figure B.2: Example of the distribution of ordered hit per pixel before the cut. One can note the peak that spans two orders of magnitude above the bulk of the distribution. This is due to the noisy pixels targeted by the described cut. Burst from Run 6497.

Appendix C

Level 0 Trigger Processor

A major activity carried on during the first year of PhD was the continuation of the work on development and testing of an alternative Level 0 Trigger Processor (L0TP) design, featuring a hybrid PC-FPGA system [40].

Primitives from sub-detectors, collected in Multi Trigger Packets (MTPs), are asynchronously sent via Ethernet links (using the UDP protocol) to the L0TP. MTPs are sent periodically with default period of 6.4 µs and contain the primitives produced in that time interval. The theoretical input rate limit is related to the Gigabit Ethernet link capability, i.e. 14 MHz.
The time of the event is fundamental to align primitives coming asynchronously. It is stored in a 32-bit unsigned integer (Timestamp), relative to which all individual channel times are to be interpreted and made available to each sub-system through the Timing Trigger and Control (TTC) system [10] by a dedicated receiver. The Timestamp is uniquely related to the event number within a burst, this latter being the particle spill from the SPS. The LSB equals the period of the master clock, 24.95 ns. A Fine Time 8 bit information is also stored in the packet. The lowest significant bit is 1/256 of the main clock period (97.47 ps), allowing a more precise data alignment and a tighter trigger coincidence window. Nonetheless detectors precision can be different from one to another, and therefore Fine Time information should be used accordingly and in combination with meaningful matching time windows. After the trigger decision is taken, triggers are synchronously sent to the TTC system with fixed latency for broadcasting to detectors.

Both the baseline (FPGA-based) and alternative (FPGA-PC or PC-based) design make use of a commercial development board, Terasic DE4 mounting an Altera Stratix IV FPGA. The DE4 board features 4 gigabit Ethernet links as default plus 4 available on High Speed Mezzanine Cards (HSMC). 7 links are used as detector inputs while the last is reserved to send trigger information to the PC farm or the support PC. An auxiliary board mounting the TTC receiver module is used to convert optical signals, coming from the SPS, into digital levels to transmit the clock and start/end of the spill signals.

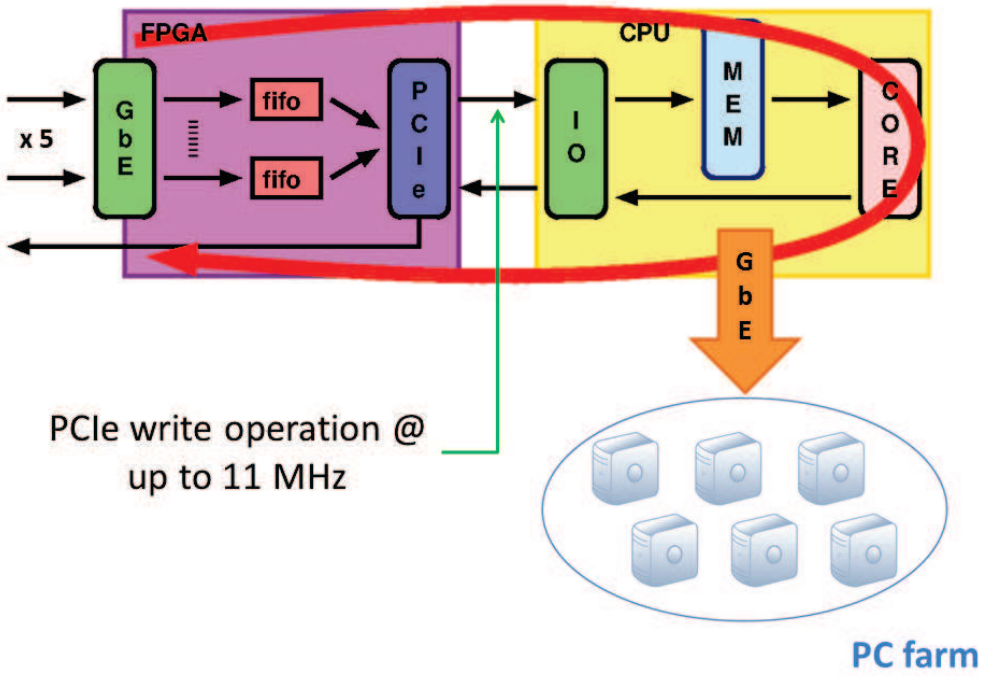


Figure C.1: Overview of the core FPGA-PC implementation of the L0TP. It is possible to follow the data path of primitives information from Gigabit Ethernet (GbE), through PCIe, to the CPU core (left to right). After trigger decision is taken, the trigger Timestamp follow the path back toward the FPGA in order to be shipped to the TTC system with fixed latency (right to left).

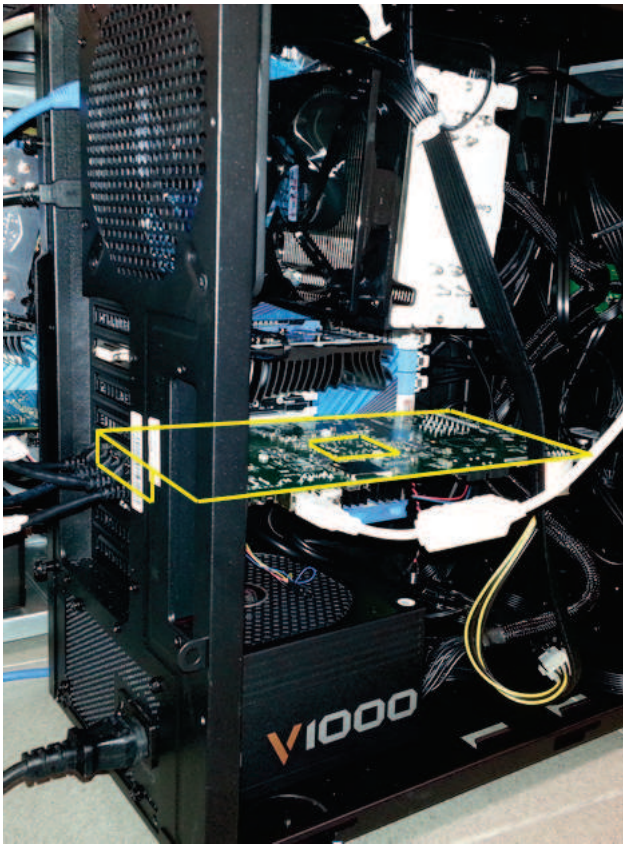


Figure C.2: The DE4 board hosted in the PC case while plugged to the PCIe bus.

In the alternative design described here, the DE4 board is paired to a common PC as shown in Figure C.2. The latter also features a 8x PCI Express Gen. 2 bus which in this case is used to deliver data directly to the RAM memory of the PC. The PC takes advantage of an Intel Core i7-4930K CPU @ 3.40 GHz with Scientific Linux 6 kernel. This system can exploit the entire memory of the PC without any problem of synchronization of circular buffers as in the FPGA-based solution, since all primitive information is stored for the whole length of the spill. On the FPGA firmware side, this project features similar DE4 remote control, primitives reception, TTC signals management and trigger shipping to detector at fixed latency, with the addition of PCIe access to the PC memory. On the PC software side, the CPU directly reads primitives from memory and, by using a single-threaded algorithm, aligns them looking for overlapping time windows in real-time. After time-alignment, Primitive IDs are compared with pre-set masks and selections are applied as in the FPGA-based solution. Trigger decisions are then shipped back to the FPGA via PCIe and fixed latency is applied for transmission to the TTC system for broadcasting.
Overview of the PC-based system is sketched in Figures C.1 and C.3.
Since all primitive information is accessible by the matching algorithm it is possible to exploit all bits of the Timestamp and Fine Time. The best time granularity in this way is 97 ps. This allows to precisely time-align the primitives exploiting the full Fine Time precision and specifying different time-windows for each source in order to reflect the actual sub-detector sensitivity.

Feasibility studies have been carried out to measure the time needed to take the trigger decision with realistic primitive generators and input rates up to 14 MHz proving that the trigger latency time is below the maximum admitted 1 ms.

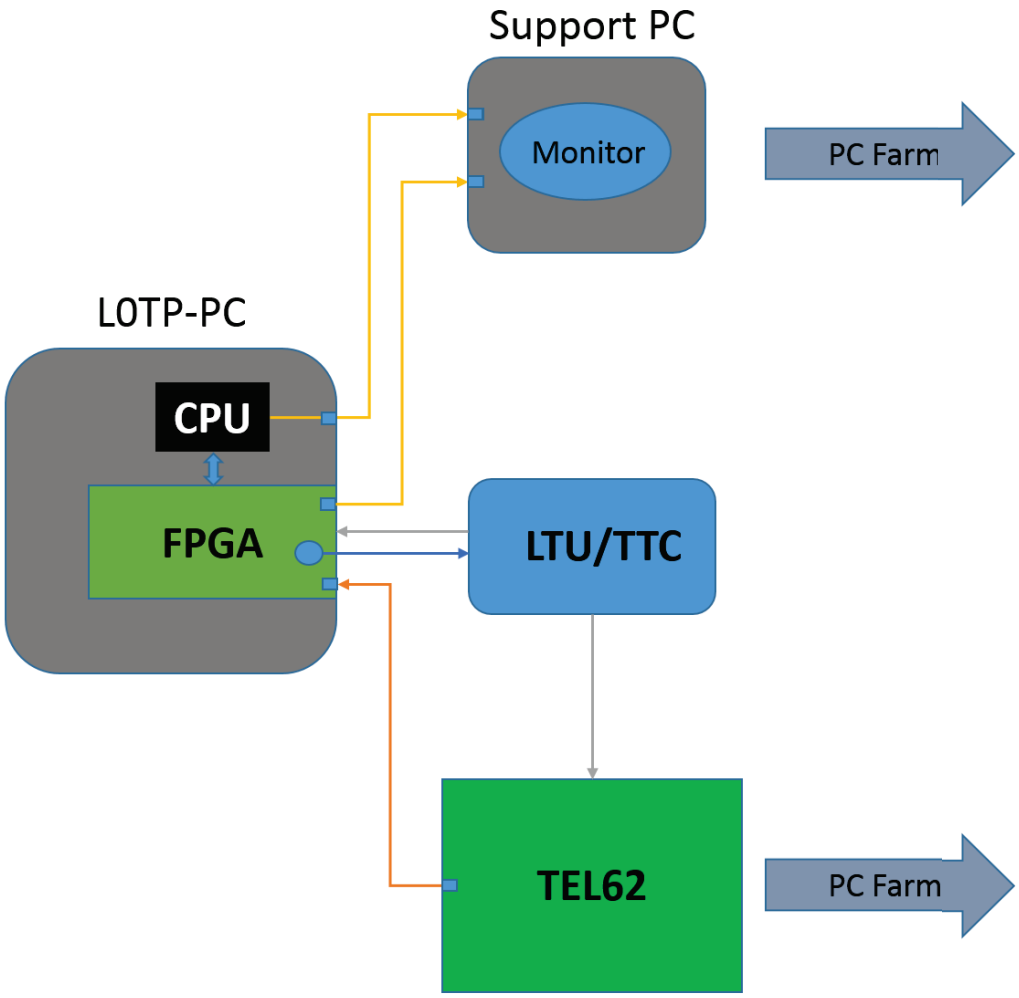


Figure C.3: Overview of the tested trigger system, including the PC-based L0TP and the other key trigger sub-systems. The support PC software has been developed in order to provide a layer of processing between the raw FPGA output and the PC Farm.

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