The Phase-I Upgrade of the ATLAS First Level Calorimeter Trigger

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Abstract. The ATLAS Level-1 calorimeter trigger is planning a series of upgrades in order to face the challenges posed by the upcoming increase of the LHC luminosity. The trigger upgrade will benefit from new front-end electronics for parts of the calorimeter that provide the trigger system with digital data with a tenfold increase in granularity. This makes possible the implementation of more efficient algorithms than currently used to maintain the low trigger thresholds at much harsher LHC collision conditions. The Level-1 calorimeter system upgrade consists of an active and a passive system for digital data distribution, and three different Feature Extractor systems which run complex algorithms to identify various physics object candidates. The algorithms are implemented in firmware on custom electronics boards with up to four high speed processing FPGAs. The main characteristics of the electronic boards are a high input bandwidth, up to several TB/s per module, implemented through optical receivers, and a large number of on-board tracks providing up to 12.8 Gb/s high speed connections between the receivers and the FPGAs as well as between the FPGAs for data sharing. Prototypes have been built and extensively tested, to prepare for the final design steps and the production of the modules. The contribution will give an overview of the system and present the module designs and results from tests with the prototypes.

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1 Introduction

During the Run 3 data-taking period (starting in 2021), the Large Hadron Collider (LHC) will increase the current instantaneous luminosity by almost a factor of two (i.e. to $\sim 2.5 \times 10^{34} cm^{-2} s^{-1}$), to substantially enhance its physics potential. The luminosity upgrade will lead to a higher number of interactions per bunch-crossing at the ATLAS detector [1] than the design values of the current trigger system. In order to maintain a high event selection efficiency in the increased luminosity environment, the ATLAS Level-1 calorimeter trigger (L1Calo) [2] will be upgraded with new object-finding processors. These will run more efficient identification algorithms on finer granularity calorimeter information than is currently available, preserving the low energy trigger thresholds of the current Run 2 system [3]. This paper presents an overview of the Phase-I upgrade of the L1Calo system for LHC Run 3 and the development status of the new L1Calo hardware components.

2 L1Calo Phase-I Upgrade

L1Calo is a hardware-based, pipelined system that identifies various physics object candidates in the Liquid Argon (LAr) and Tile calorimeters.

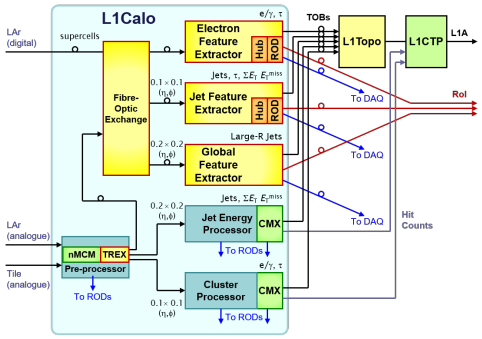

Fig. 1. L1Calo architecture in Run 3. Components shown in yellow and orange are part of the Phase-I upgrade [4].

In Run 2, the object identification is based on coarse-granularity analogue trigger-tower input, which describes transverse energy (E_T) deposits in calorimeter areas of typically $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The system consists of a Pre-Processor, which digitises the trigger-tower signals and extracts the E_T value from each pulse, a Cluster Processor (CP) and a Jet/Energy-Sum Processor (JEP), which respectively use 0.1×0.1 and 0.2×0.2 E_T input to identify e/γ, τ's and jets and to compute various global energy sums and the missing E_T.

After Run 2, the L1Calo system will be upgraded with three new Feature Extractor (FEX) systems, to increase the discriminatory power of the trigger at the higher LHC luminosity: the electromagnetic Feature Extractor (eFEX), the jet Feature Extractor (jFEX) and the global Feature Extractor (gFEX) (see Fig.1). The input to the FEXes will be entirely digital. The front-end electronics of the LAr calorimeter will also be upgraded during Phase-I, providing L1Calo with finer granularity digital information. For each trigger-tower, ten so-called SuperCells will provide E_T information from the four longitudinal calorimeter layers [5]. The Tile front-end electronics will not be upgraded to send digital data until Phase-II. To accommodate these plans, Tile Rear Extension (TREX) [6] modules will be developed and installed in the PreProcessor system, providing the FEXes with Tile digitised results. In total, the FEXes will receive the digital calorimeter data via ∼7100 high-speed optical links running at up to 12.8 Gb/s. A Fibre-Optic Exchange (FOX) plant will have the task of reorganising the optical fibre input, from the mapping employed by the source systems to the one required by each destination FEX.

The eFEX and jFEX will perform similar investigations to the CP and JEP, but with more complex sliding-window algorithms that make use of higher granularity input. The eFEX will use the SuperCell data from $|\eta| < 2.5$ to better isolate and analyse the electromagnetic shower shapes, while the jFEX will run Gaussian-weighted algorithms to improve jet identification using mostly 0.1×0.1 digital trigger-tower data from $|\eta| < 4.9$. In total, 24 eFEX modules in two ATCA shelves and 7 jFEX modules in one ATCA shelf will be needed for the

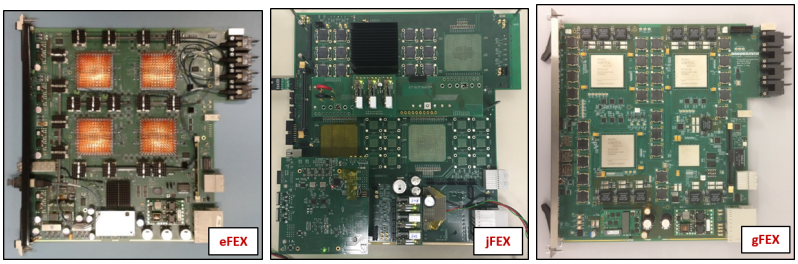

Fig. 2. The FEX prototype modules [4].

complete system. The gFEX [7] will receive 0.2 × 0.2 E_T-sum data from the entire calorimeter in a single ATCA module, to identify large-radius jets and compute various global event observables. All of the FEXes will send results in the form of Trigger Objects (TOBs) to the Level-1 Topological Trigger Processor (L1Topo), and read out data to the Data Acquisition (DAQ) system, via optical links running at 12.8 Gb/s and 9.6 Gb/s, respectively. On the eFEX and jFEX, the transfer of TOBs and readout information is realised via custom ATCA Hub-ROD boards (see Fig.1).

3 Prototype Modules and Tests

Prototype modules for each FEX processor have been manufactured and assembled (see Fig.2), and their functionality has been verified. Each module is a highly-dense ATCA board design, hosting a large number of high-speed devices that have to handle and process an input bandwidth of up to several TB/s.

The eFEX prototype is a 22-layer board with four processing FPGAs (Xilinx Virtex-7 XC7VX550T), one readout FPGA (Xilinx Virtex-7 XC7VX330T), 17 MiniPOD optical transceivers, and up to 450 on-board multi-Gb/s differential signals. In addition, 94 high-speed electrical buffers duplicate the input calorimeter data between the processing FPGAs, as required by the eFEX sliding-window algorithms [3]. Three eFEX prototypes have been manufactured and tested. The high-speed optical links were tested at up to 11.2 Gb/s, both at CERN using a LAr Digital Processing System (DPS) prototype and a FOX demonstrator, to emulate the Run 3 configuration, and in the laboratory environment using custom FEX Test Modules (FTMs) as data sources. On 99% of the input links the observed bit error rate was less than 10^{-14}. For the other links, the errors were traced to a few broken high-speed buffers, to sensitive fibre connections and to poor routing on one input. Additional functionality such as the readout and the Timing, Trigger and Control (TTC) distribution, the IPBus and IPMC operation or the simultaneous transmission over ∼360 on-board differential pairs was successfully tested. The module power consumption was measured to be ∼280W, with all of the FPGA Multi-Gigabit Transceivers (MGTs) active. The maximum recorded module temperature was ∼67°C, with all three prototypes fully powered and in adjacent slots.

The jFEX prototype is a 24-layer board that hosts four processing FPGAs (Xilinx Virtex UltraScale XCUV190), 12 MiniPODs, and up to 540 on-board multi-Gb/s differential tracks. The board control is implemented via an extension mezzanine, which hosts among others a Xilinx Zynq-7000 FPGA based card. Input data duplication is realised within each processing FPGA using the Physical Medium Attached (PMA) loopback. One jFEX prototype has been manufactured and so far only partially assembled and tested. Preliminary link tests at up to 12.8 Gb/s, with the LAr DPS and the FTMs or in loopback mode, showed very good and stable operation for all the tested inputs.

Two gFEX prototype versions have been manufactured. The last version, shown in Fig.2, is a 26-layer board with three processing FPGAs (Xilinx Virtex UltraScale XCUV160), one control and monitoring FPGA (Xilinx Zynq XC7Z100), 28 MiniPODs and a large number of on-board high-speed interconnections. All of the optical I/O links of the prototype were successfully tested at the maximum specified speeds with both the LAr DPS and in loopback mode. The module's power consumption was measured to be $\sim$300W (with all MGTs active), while the maximum recorded FPGA temperature was $\sim$67°C. The design of the next gFEX hardware iteration, the pre-production module, has been recently completed. This features an increased number of PCB layers (30) and MiniPODs (35), and newer generation FPGAs (UltraScale+).

The TREX prototype is currently being manufactured. This will be an 18-layer VME rear transition module, mainly hosting one Xilinx Kintex UltraScale FPGA (KU115) and four Samtec FireFly optical transmitters for sending data to the FEXes.

4 Outlook

The prototyping and testing of the L1Calo modules for Phase-I will continue during 2017, to guide preparation of the final designs. The installation of the final modules in the experiment will be during the LHC long shutdown starting in 2019, with the aim of being fully commissioned before the start of Run 3 in 2021.

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