CLICdp-Note-2017-003
13 June 2017

Finite-element simulations of coupling capacitances in capacitively coupled pixel detectors

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Abstract

Capacitively coupled hybrid silicon pixel-detector assemblies are under study for the vertex detector at the proposed future CLIC linear electron-positron collider. The assemblies consist of active CCPDv3 sensors, with 25 μm pixel pitch implemented in a 180 nm High-Voltage CMOS process, which are glued to the CLICpix readout ASIC, with the same pixel pitch and processed in a commercial 65 nm CMOS technology. The signal created in the silicon bulk of the active sensors passes a two-stage amplifier, in each pixel, and gets transferred as a voltage pulse to metal pads facing the readout chip (ROC). The coupling of the signal to the metal pads on the ROC side proceeds through the capacitors formed between the two chips by a thin layer of epoxy glue. The coupling strength and the amount of unwanted cross coupling to neighbouring pixels depends critically on the uniformity of the glue layer, its thickness and on the alignment precision during the flip-chip assembly process. Finite-element calculations of the coupling capacitances were performed, based on a detailed 3-dimensional implementation of the geometrical layout for various alignment parameters. We present the simulation setup and results of coupling and cross-coupling capacitance extractions for the current chip versions (CCPDv3 and CLICpix), as well as results for new chips with optimised designs (C3PD and CLICpix2).

This work was carried out in the framework of the CLICdp collaboration

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1 Introduction

Hybrid silicon pixel detectors are widely used in High Energy Physics for vertex and tracking detectors, and also in medical imaging applications. They are also considered for the vertex detector under development for the future high-energy linear electron-positron Compact Linear Collider (CLIC). The hybridization process allows the signal-collecting sensors and the signal-processing read-out chips (ROC) to be developed and produced with different technologies, optimizing individually the sensor and the ROC. Both parts are bonded together, creating the final pixel detector.

The standard hybridization process uses bump-bonds ($\approx 20\ \mu$m diameter solder balls) to connect each pixel on the sensor to its corresponding pixel on the ROC. In this one-to-one connection, the signal from the sensor is transmitted via a DC coupling (through the bump-bond) to the ROC. A schematic illustration is shown in Figure 1. The bump-bonding process is expensive, limiting the construction of pixel detectors with large areas. Moreover, standard bump-bonding techniques for single dice are not commercially available for very small pixel pitches of 25μm, as required for the vertex detector at CLIC.

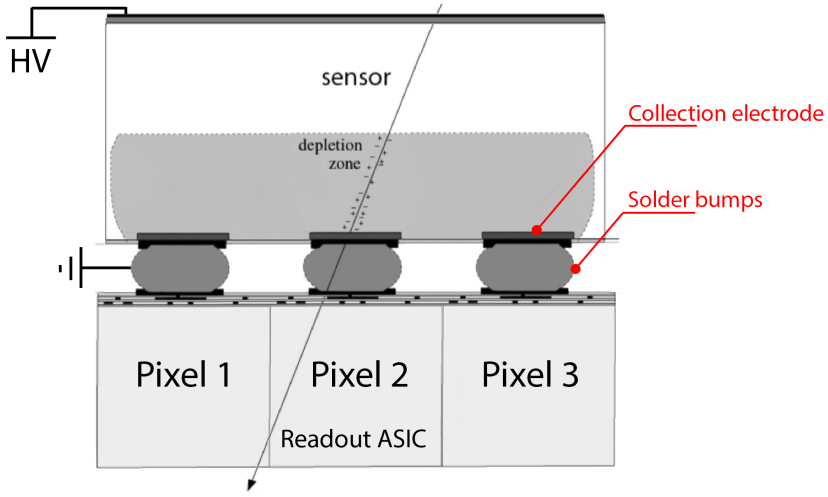

Figure 1: Ilustrative cross section of a hybrid pixel detector, consisting of a planar sensor interconnected via solder bumps to a ROC, and a Minimum Ionizing Particle (MIP) interacting with the sensor and generating charge inside the depletion zone.

A new hybridization technique based on capacitive coupling was developed in order to overcome the limitations of the fine-pitch bump bonding process. In this concept of capacitive coupled pixel detectors (CCPDs), the signal created in the sensor bulk is amplified in a CMOS circuit inside the collection electrode of the pixels and sent to the sensor output pad that is coupled capacitively (AC), through a thin layer of glue, to the input pad of the pixel in the ROC [1]. This active sensor is implemented in a commercial High-Voltage CMOS (HV-CMOS) process.

The HV-CMOS process allows the application of a high voltage to deplete the silicon substrate above the CMOS circuitry which is shielded inside deep implanted doping wells that, at the same time, act as signal collecting electrode. A schematic cross section of the technology is shown on Figure 2.

Through the AC connection, a voltage signal from the sensor pixel pad induces a charge signal in the ROC pixel input pad, that is further amplified by its charge sensitive amplifiers, digitized and read out. The pixel pads of both chips should be precisely aligned in order to have a capacitance high enough to establish the electrical AC connection. An illustration of a capacitively coupled assembly is shown in Figure 3

As the method of signal transfer between the sensor and the ROC is via a capacitive injection, potential crosstalk to neighbouring pixels must be considered. For that, a 3D simulation of the coupling between

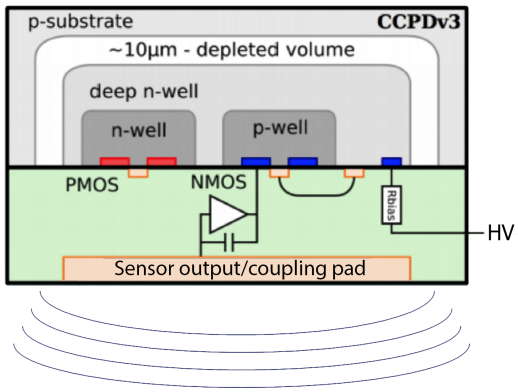

Figure 2: Illustrative cross section of the HV-CMOS sensor technology.

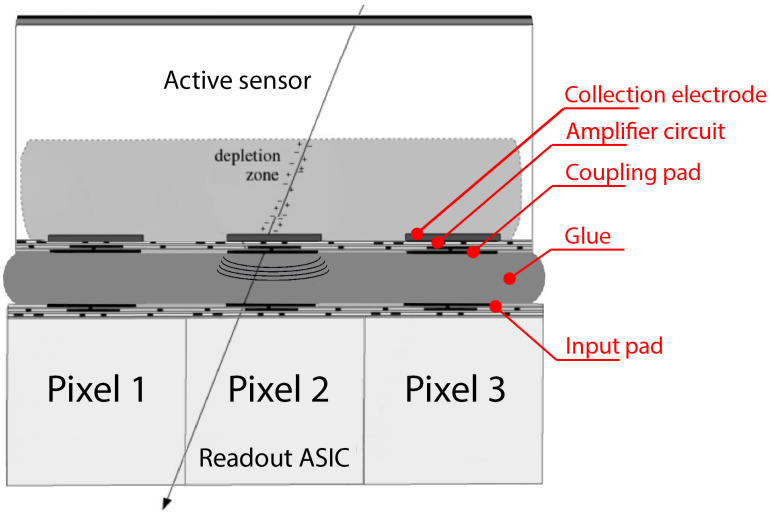

Figure 3: Illustrative cross section of a capacitively coupled hybrid pixel detector with a Minimum Ionizing Particle (MIP) interacting with the sensor and generating charge inside the depletion zone. The capacitive connection of the pixel pads is done via the glue layer. An illustration of the CMOS circuitry, needed for the AC coupling, is also present on the sensor side.

the pixel pads is performed with the COMSOL Multiphysics software [2], using the Finite Element Analysis method. The effect of different glue layer thicknesses, pixel misalignment and different pixel pad designs was also simulated.

2 CLIC Capacitively Coupled Pixel Detectors

A vertex-detector concept based on hybrid pixel sensors is under development for the proposed high-energy linear e^+e^- collider CLIC. In the context of this project, prototype assemblies of CLICpix readout ASICs capacitively coupled to CCPDv3 active HV-CMOS sensors have been produced.

The CLICpix chips were produced in a commercial 65 nm CMOS process. They are composed of a matrix of 64x64 pixels with 25 μm pitch. Each CLICpix pixel contains a Charge Sensitive Amplifier (CSA), discriminator, and digital logic to record the arrival time and charge deposited of each hit. The

CCPDv3 sensors were produced in a commercial 180 nm HV-CMOS process and contain a pixel matrix matching the pixel footprint of the CLICpix chips. Each pixel contains a charge sensitive amplifier and a second inverting amplifier stage. Figures 4 and 5 show the CLICpix chip and the CCPDv3, respectively.

CLICpix+CCPDv3 glue-assemblies were produced and wire bonded to printed circuit boards (PCBs) as shown in Figure 6. The chips were assembled using a flip-chip machine, by depositing the glue on top of one of the chips and bringing the other into contact with a controlled force (of 5N) and temperature (100 °C) applied for 6 minutes. The alignment precision of the final assembly is of the order of ± 2 μm, as measured on a few samples with destructive cross section pictures.

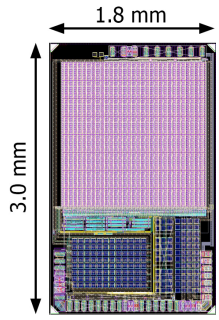

Figure 4: CLICpix

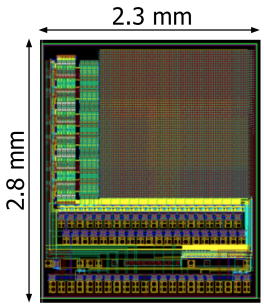

Figure 5: CCPDv3

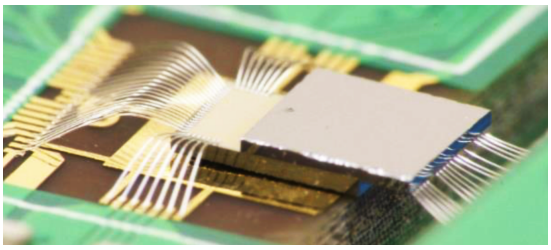

Figure 6: CLICpix+CCPDv3 assembly.

Cross section measurements of the assemblies were done by the CERN EN-MME-MM group with a scanning electron microscope. The measurements revealed a glue layer thickness of about 0.2 μm, which is constant over the pixel matrix. The total distance of $\approx$3 μm, between the CCPDv3 and CLICpix pads, includes the passivation layers of the respective chips and the glue layer. Figure 7 shows a cross section picture of one of the assemblies. The top chip in the picture is the CCPDv3, and the bottom is the CLICpix.

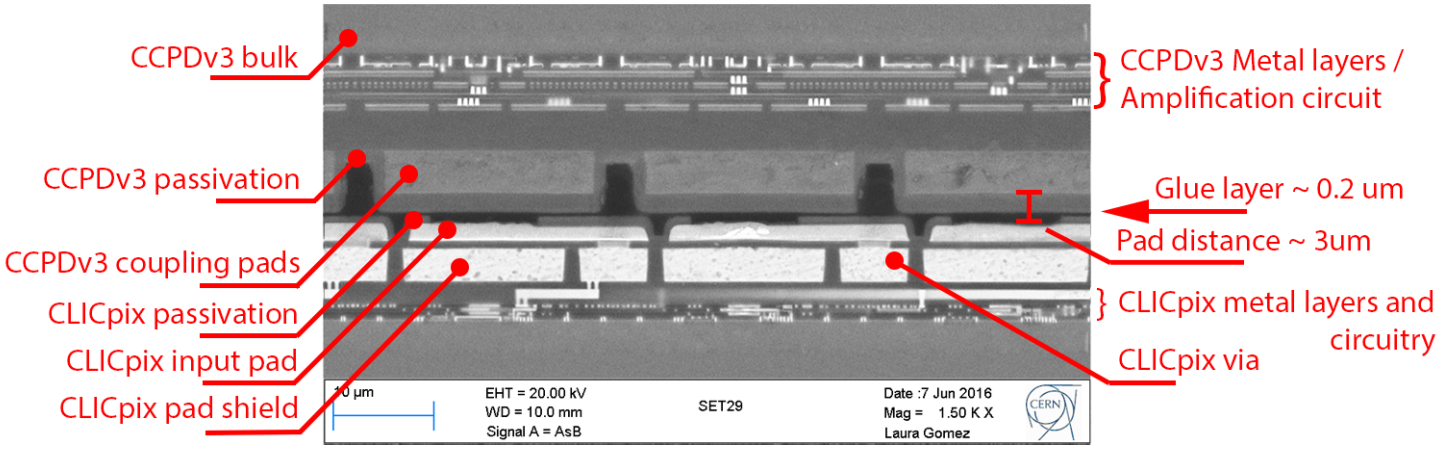

Figure 7: Scanning electron microscopy of CLICpix+CCPDv3 assembly cross section.

Testbeam measurements with prototype assemblies [3] revealed a dependency of the measured signal on the uniformity of the glue layer and on the alignment precision. The simulations presented in the following will be used to understand and quantify the capacitive signal-transfer and to optimise the layout of future capacitively coupled assemblies.

3 Coupling Simulation

In order to understand the coupling and the cross talk between neighbouring pixels through the glue layer, a simulation was carried out using the Finite Element Analysis software COMSOL Multiphysics.

3.1 COMSOL Multiphysics

COMSOL Multiphysics is used in this work to formulate and solve the differential form of Maxwell's equations together with a set of initial and boundary conditions using the Finite Element Method, and post-process the results to calculate derived values, such as capacitances.

The work flow is as follows. First the geometry is defined; materials are assigned to the volumes of the model; a *Physical Interface* is chosen with the model's respective boundary and initial conditions; the element mesh is created; a solver is selected and subsequently the results are computed. All these steps are accessible from the same interface.

The *Physical Interface* provides a set of partial differential equations, such as Maxwell equations and material laws, with the corresponding initial and boundary conditions. The mesh is used to divide the volume of the model into discrete parts where the equations will be computed. After the calculation for the mesh elements, the results are interpolated over the volume.

3.2 3D model

A 3D model of the detector assembly was created using SolidWorks [4]. A matrix of 3x3 pixels was created for each chip, based on their GDSII[2] design files. Each matrix was created as a *SolidWorks Part* and both *Parts* were brought together, with a nominal gap of 0.2 μm, forming a *SolidWorks Assembly*.

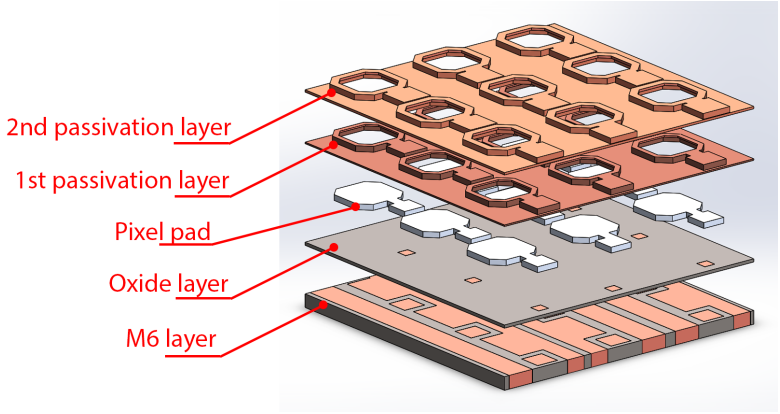

Figure 8: CLICpix pixel pads and M6 layer. Picture from SolidWorks. 1st and 2nd passivation layers are composed of SiO_2 and Si_3N_4, respectively.

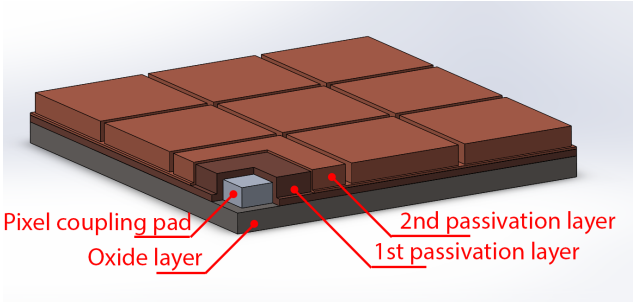

Figure 9: CCPDv3 pixel pads. Picture from SolidWorks. 1st and 2nd passivation layers are also SiO_2 and Si_3N_4, respectively.

The thickness of the different chip layers was extracted from the technology process manual used for each chip. Both ROC and sensor chip use two passivation layers after the pixel pads (on the CLICpix chip, the passivation has an opening so it can also be bump-bonded to other sensors). In the ROC, the M6 layer (last metal layer before the pixel pads) was also included in the model, in order to extract possible parasitic capacitances/loads for the CCPDv3 pixel output circuitry. The oxide layers, responsible for

[2] Industry standard format file for data exchange of integrated circuit.

isolating the metal layers, are also included in the model. The 3D geometries of the chips are shown in Figures 8 and 9 and a cross section of the assembly is shown in Figure 10.

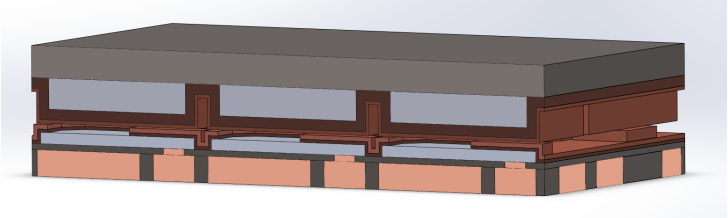

Figure 10: Chip assembly cross-section of CCPDv3 (top) and CLICpix (bottom) in SolidWorks.

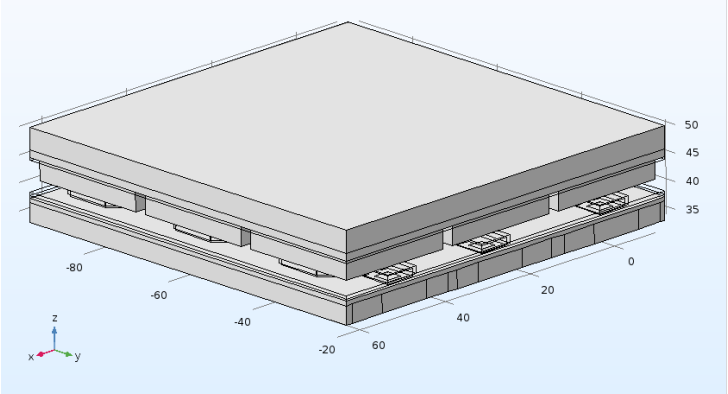

Figure 11: SolidWorks assembly imported into COMSOL Multiphysics. The grid scale is in μm.

It is possible to import 3D CAD files into COMSOL Multiphysics, and the imported SolidWorks assembly file of the detector is shown in Figure 11. The next step is to create the missing epoxy glue layer that will fill the gap between the two chips. It is easier to model the glue layer with COMSOL, as it offers some basic CAD tools, such as boolean operations (difference or intersection for example) between different parts of the geometry. The resulting glue layer is shown in Figure 12. It was defined by the volume surrounding both chips, subtracting the volume of the chips.

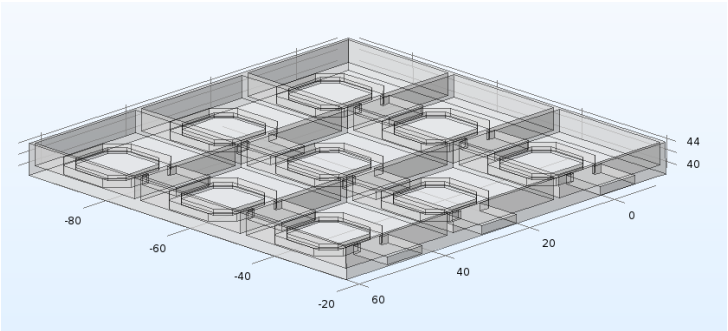

Figure 12: Gap volume between chips defined as the glue layer. The grid scale is in μm.

After the geometry is created, a material is assigned to each volume of the model, so that the corresponding material properties, such as the dielectric constant, are taken into account (in the electric field

calculation, for example). The materials used in the model are Aluminium for the pixel pads and metal lines + vias; silica glass for the material between the metal lines and between the metal layers; epoxy resin for the glue layer and SiO2 and Si3N4 for the passivation layers. Table 1 shows the dielectric constant for the materials listed above. The dielectric constant of the Araldite 2011 glue depends on the measurement frequency and is tabulated only up to 10 kHz. The CCPDv3 output pulse corresponds to a frequency of ≈10 MHz, for which the dielectric constant of the glue has to be confirmed with future measurements. The values for the dielectric constant of the passivation layers were extracted from the process technology manual from the corresponding foundry of each chip. In reality, only the pixel pads are made of Aluminium, with the other metal lines and vias being made of copper. However, as the pixel pads and metal lines are conductors, the different dielectric properties of Aluminium and Copper have no impact on the capacitance calculated, as checked with previous simulations[3]. Hence, Aluminium was chosen to represent all metals to simplify the model.

Table 1: Dielectric constants used.

	Material ID	Dielectric constant	Layers
	Aluminium	1.7	Pixel pads
	Silica Glass	2.09	Oxide layer and between metal lines
	Epoxy resin [5]	3.2 (at 10 kHz)	Araldite 2011 Glue layer
CLICpix	SiO_2	4.2	First passivation layer
	Si_3N_4	8.1	Second passivation layer
CCPDv3	SiO_2	3.9	First passivation layer
	Si_3N_4	7.5	Second passivation layer

3.3 Capacitance Simulation

For the simulations in this work, the COMSOL *Electrostatic interface* was used in a *Stationary Study* (time independent) for the capacitance calculation. The interface is responsible for connecting the geometry modelled with the equations of electrostatic physics by assigning respective Boundary Conditions (BC), such as a specific potential distribution, on the elements of the geometry (points, edges, surfaces or domains). The *Electrostatic interface* solves the Gauss' Law using the scalar electric potential, given by the BCs, in order to compute the electric field, electric displacement field, and potential distributions in dielectrics under the respective BC of the system modelled.

Capacitance is defined as a static property of the system, depending only on the geometry of the system and the dielectric constant of the media. A geometric formulation of the capacitance is given in reference [6]. COMSOL computes the capacitance as a lumped parameter. Lumped parameters are matrices describing electromagnetic properties of the system, such as resistance, inductance and capacitance. A column/row pair in the matrix represents two elements of the electric system and the matrix bins contain the capacitance, for example, between the corresponding elements. The capacitance matrix is described in reference [7].

In COMSOL, lumped parameters are calculated for and between the electrodes of the model. Hence, all pixel pads are modelled using the *Terminal BC*, which sets the electric potential as constant on all electrodes, each one being identified by a unique Terminal/Port number. Figure 13 and 14 show an example pixel domain boundaries selection to which the *Terminal BC* is applied.

The capacitance matrix elements, C_{ij}, are calculated using the so called *Energy Method*, explained in references [8] and [9]. In this method, to find the capacitance between pairs of terminals, it is important to

[3]The volume inside metal domains does not even need to be modelled or meshed, as it can be defined only by boundaries conditions on its surface.

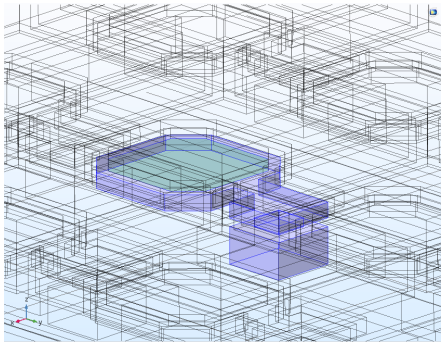

Figure 13: CLICpix pad boundary selection (in blue) for the *Terminal BC*. The blue selection is the metal from the CLICpix pixel pad + the copper via (through the oxide layer) + via in the M6 layer.

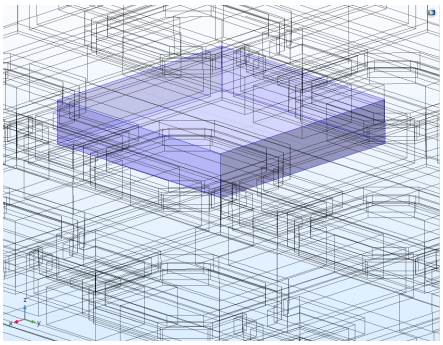

Figure 14: CCPDv3 pad boundary selection (in blue) for the *Terminal BC*. The blue selection is the metal from the CCPDv3 pixel pad, positioned above the CLICpix pad.

have only the electrode for which the capacitance is being calculated with a boundary potential different from zero, while all the other electrodes are set to 0V. In this way, the capacitance calculated from the energy density integral will not have "parasitic" contributions from other electrodes. A *Terminal Sweep* is done in order to loop the excitation (application of a potential or current) over the terminals and, hence, calculate the lumped parameter matrix elements.

There are three options when defining the BC of the metal lines. Their boundaries can be fixed to ground using the *Ground BC*. The *Floating Potential BC* models a conductive electrode at floating potential (with or without an initial charge deposited on it). The *Terminal BC* can be used to model the metal lines and vias, as they can also be modelled as electrodes. The *Terminal BC* allows also an extraction of the cross capacitance of the HV-CMOS pixel to the metal lines as it is computed in the capacitance matrix. Hence, for simplicity of the model, the same *Terminal BC* was assigned for all metal lines.

A periodic boundary condition was applied at the outer/external boundaries of the model and default boundaries conditions, like current conservation and electric insulation, were applied to the model.

After the model boundary condition assignment, a mesh of the modelled volume is created, in order to generate smaller domains (or sets of element equations) where the electric potential (and derivable quantities) will be calculated. After the calculations for each element, the results are recombined into a global system of equations for the final calculation. COMSOL contains advanced automatic meshing algorithms, making it possible to mesh the complex geometric volume with a small set of parameters in one step. The volume was meshed with tetrahedrals with minimum element size of 0.1 μm, maximum element size of 2.6 μm and maximum element growth rate of 1.35 (determining how fast a mesh element can grow from the minimum to the maximum size). An example of a resulting mesh is shown in Figures 15 and 16. The mesh was created in about 1 min.

COMSOL chooses automatically a solver sequence based on the physical interface and BCs created, although it is possible to manually choose the solver to be used. For this simulation, the conjugate gradient method was used, as an iterative algorithm, to find the numerical solutions of the compiled equations, set by the *Electrostatic interface*.

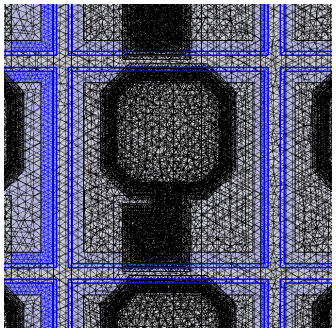

Figure 15: Top view of the volume mesh created.

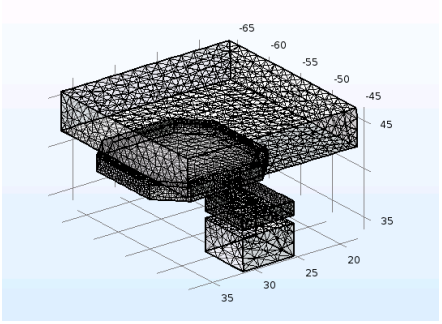

Figure 16: Mesh of the CCPDv3 (top) and CLICpix (bottom) pixel pads. The grid scale is in μm.

4 Simulation results

4.1 Results for nominal parameters

The electric field and the energy density are computed over the model and are used to derive the capacitance matrix of the system as described above. The electric field is calculated for each node element of the mesh and interpolated between the nodes such that it is known continuously inside the volume. The norm (or amplitude) of the electric field between the CCPDv3 and CLICpix pixel pad is shown in Figure 17. Regions of high electric field are visible in the corners. This is a feature of the simulation, as the simulated geometry has "perfect" (sharp) edges, while the physical implants have rounded edges.

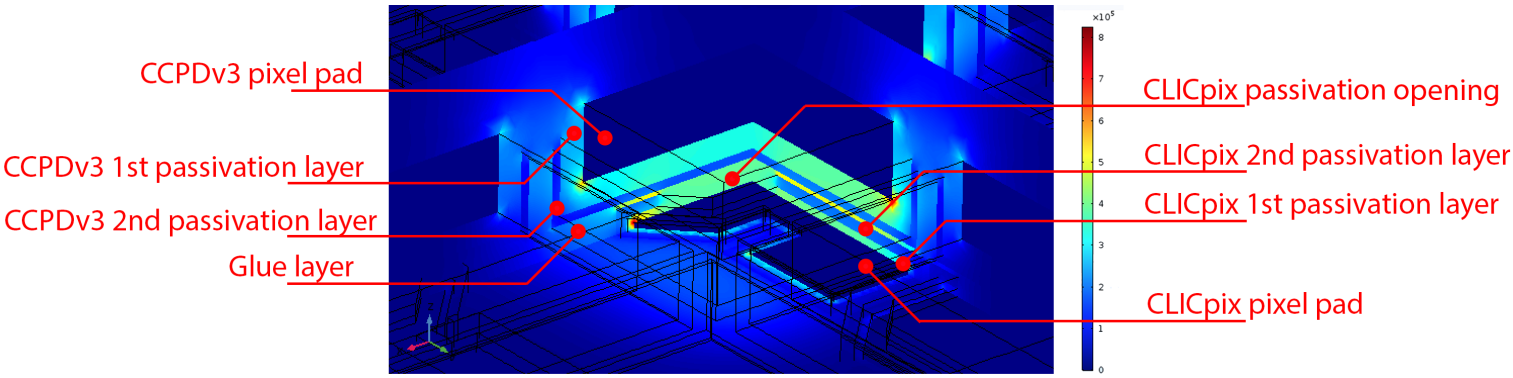

Figure 17: Norm of the electric field (in V/m) between pixel pads represented in the color scale.

Each column and row of the capacitance matrix represents one terminal. The matrix contains the self-capacitance of the terminals on its diagonal, and the capacitance between different pads outside the diagonal. The capacitance matrix, for nominal alignment, is shown in Table 2.

The terminals 1-9 are the pixels pads in the 3x3 matrix of the CLICpix ROC (first column and row pixel is terminal 1), see Figure 18. The terminals from 10 to 18 are the pixels in the CCPDv3 (enumerated in the same order as the corresponding CLICpix pads). Terminal 19 corresponds to the metal lines.

The aim of this simulation is an analysis of the signal propagation from the CCPDv3 sensor to the ROC through the glue layer. Hence, it is important to know the coupling capacitance between the pixels in the sensor and the pixels in the ROC. In the following, it will be analysed how the center pixel in the

Table 2: Capacitance matrix, for nominal alignment, extracted from COMSOL. Values are in fF.

	Terminal 10	Terminal 11	Terminal 12	Terminal 13	Terminal 14	Terminal 15	Terminal 16	Terminal 17	Terminal 18
Terminal 1	3.9494	0.15866	9.6283E-07	0.032963	0.0039841	2.7976E-07	2.5585E-07	1.3813E-07	1.0296E-09
Terminal 2	0.092502	3.9494	0.15864	0.0020867	0.032972	0.0039839	7.8366E-08	2.5445E-07	1.3817E-07
Terminal 3	4.2326E-07	0.092504	3.9495	1.6822E-07	0.0020874	0.032972	6.0781E-10	7.7733E-08	2.5516E-07
Terminal 4	0.033186	0.0039782	2.7836E-07	3.9486	0.15886	9.6997E-07	0.036263	0.0053793	4.5665E-07
Terminal 5	0.0021518	0.03319	0.0039718	0.092868	3.9487	0.15884	0.00085779	0.036284	0.0053807
Terminal 6	1.7186E-07	0.002151	0.03318	4.257E-07	0.092879	3.9485	9.0633E-08	0.00085789	0.036269
Terminal 7	2.1499E-07	1.4301E-07	1.0808E-09	0.030019	0.0045962	4.0977E-07	3.771	0.15175	9.1709E-07
Terminal 8	3.6192E-08	2.1394E-07	1.4199E-07	0.00078639	0.030063	0.0045969	0.089797	3.7718	0.15168
Terminal 9	2.6289E-10	3.6395E-08	2.1479E-07	8.7977E-08	0.0007869	0.030028	4.1552E-07	0.089842	3.7691

CCPDv3 sensor couples to the directly opposite pixel in the ROC and its surrounding 8 first neighbours. This corresponds to the first 9 rows (9 CLICpix pixels) at the "Terminal 14" column (central CCPDv3 pixel) in the capacitance matrix, as illustrated in Figure 18.

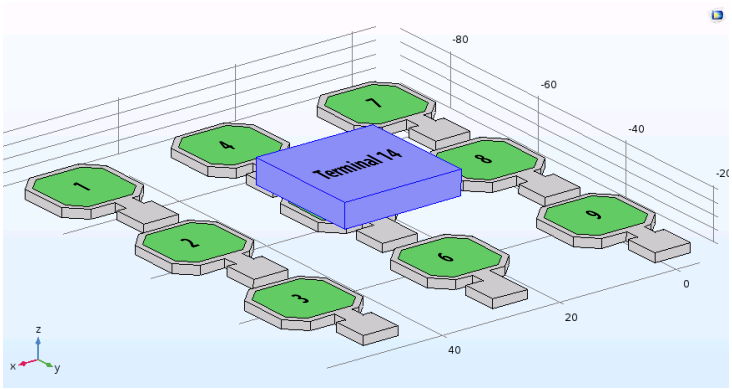

Figure 18: Illustration of the central CCPDv3 pixel and CLICpix pixels. The numbers on the pads indicate the *Terminal* number used in the simulation. The grid scale is in μm.

Figure 19 gives the coupling capacitance values of the central CCPDv3 pixel with the 9 pixels in the ROC. The biggest coupling capacitance is, as expected from the geometry, with the central pixel in the ROC matrix, with a capacitance value of 3.80 fF.

The cross coupling capacitance (coupling with the first neighbour pixel pads) is a value that is interesting to be analysed with respect to the "main" coupling capacitance, as it is important to know the parasitic charge fraction that would be created on the neighbours from a voltage pulse in the sensor pixel pad. Figure 20 shows the capacitance values normalized to the main capacitance. Only two pixels of the first neighbours obtain a significant fraction of the charge induced in the central pixel. These two neighbouring pixels could see a "parasitic" hit if the charge from the CCPDv3 pixel is high enough.

The coupling with the metal lines is 1.68 fF, or 44%. This high coupling capacitance is due to its area being much larger than the one of the pixel pads, causing a bigger overlap volume with the sensor pixel pad. This capacitance represents an additional load on the amplifiers inside the CCPDv3 pixels.

The geometry of the pixel pads leads to an asymmetric cross coupling with the neighbouring pixels. The CLICpix pixel pad has a rectangular aspect ratio. Therefore, the lateral pixels (1, 2, 3, 7, 8 and 9) have a much smaller capacitance than pixels 4 and 6. The asymmetry in the horizontal axis causes pixel 6 to have a capacitance 1.6 times larger than pixel 4. This asymmetry in the cross coupling was observed in testbeam data from [3].

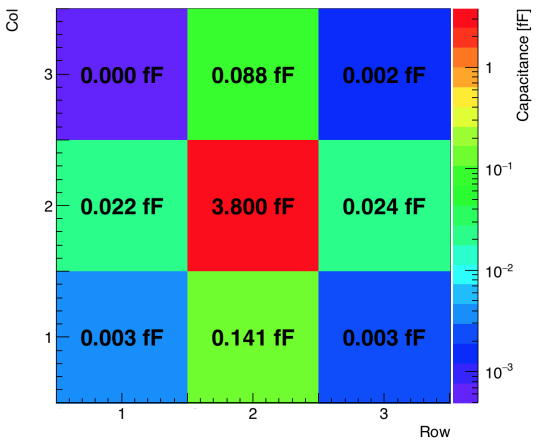

Figure 19: Capacitance of the central CCPDv3 pad with the 9 pads in the r/o chip.

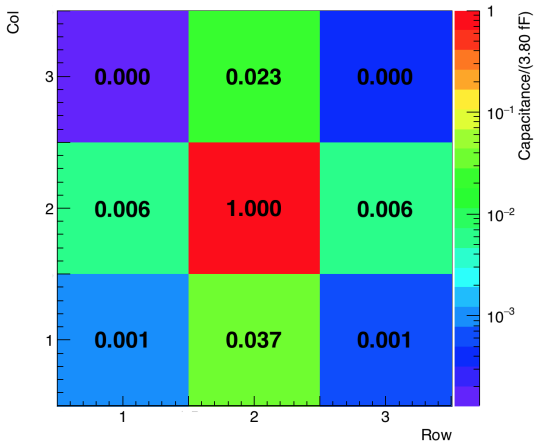

Figure 20: Coupling capacitance normalized to the main coupling.

4.2 Dependence on the glue layer thickness

The thickness of the glue layer, and consequently the distance between the pads, depends on the parameters of the flip-chip bonding process. Hence, it is important to know how the coupling capacitance changes with the distance between the pixel pads. The same simulation, as described above, was repeated while changing gradually the distance between the chips, using the *Parametric Sweep* feature of COMSOL. The distance between the pixel pads was changed from 3 up to 100 μm, in steps of 1 μm. The resulting pixel capacitances, and also the total capacitance, are shown in Figure 21 as function of the distance.

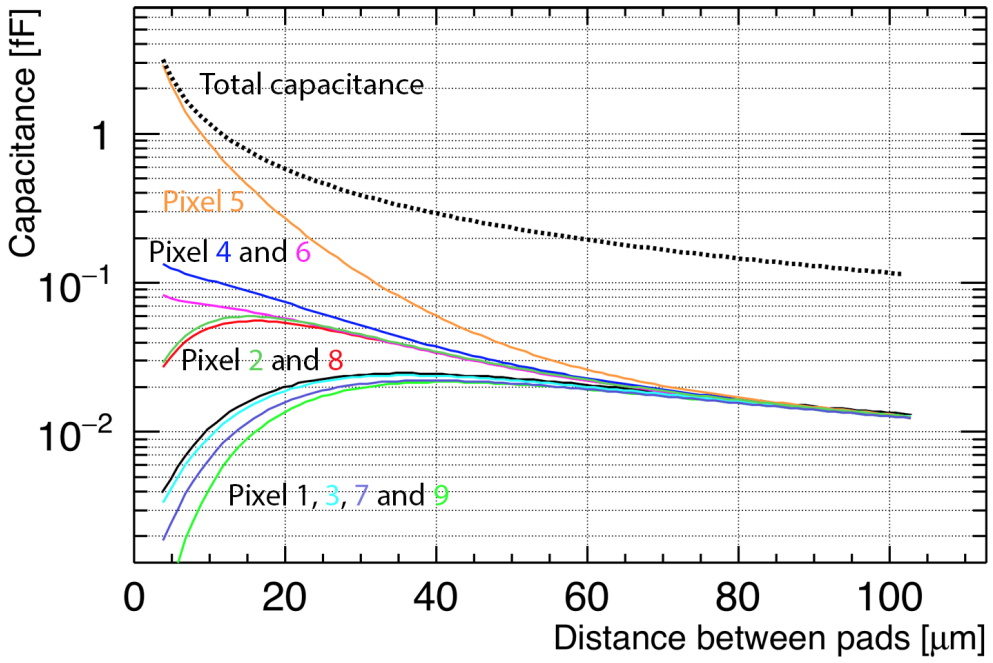

Figure 21: Capacitances of all pixel pads for different thickness of the glue layer.

As the distance increases, it is expected that the capacitance between the CCPDv3 pixel to the pixels on the CLICpix will decrease in absolute value, and that the relative difference between the capacitance to the closet pixel on CLICpix and its neighbours will get smaller, as the capacitance to the closest pixel is proportional to the gap between the pixel pads (called Z) and the capacitance to the neigbouring pixels are proportinal to Z/sinθ, where $\lim_{Z\to\infty} sin\theta = 1$.

In Figure 21 it is possible to see that with a 40 μm gap, the main coupling decreased by about two orders of magnitude, being about two times higher than the coupling to neighbouring pixels, instead of 25-50 times when compared with the nominal gap of 3 μm. It is also possible to see that for a typical gap between sensor and ROC in bump-bonded hybrid detectors ($\sim 20\mu$m), the capacitance to the closest pixel drops by about one order of magnitude while for 6 neighbouring pixels the absolute value of the capacitance increases.

This effect is due to the complex 3D geometry of the pixel pads. When the pixel pads are close to each other, part of the neighbouring pixel pads in the CCPDv3 chip and the adjacent CLICpix pixel pads act as a shield for the electric field, reducing the cross-coupling to the peripheral pixels in the CLICpix (see Figure 22). For small distances and as the chips move apart, the surface overlap between the pixels pad increases and, consequently, the shielding part of the pads gets smaller. This allows more field lines to reach the peripheral pixels, increasing the capacitance up to the point where the contribution of the larger overlap is counterbalanced by the larger distance, decreasing the capacitance.

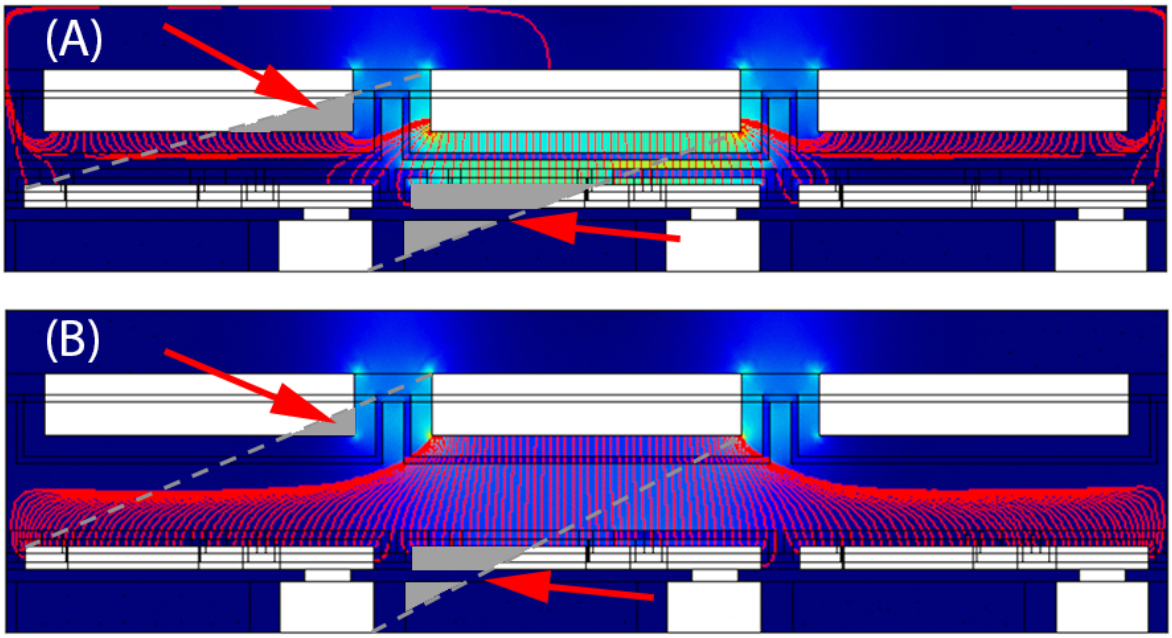

Figure 22: Comparison of overlap surface and electric field lines for 3 μm (A) and 5 μm (B) gap between CCPDv3 (top) and CLICpix (bottom) pixel pads. The area between the grey dashed lines indicates the overlap between the middle CCPDv3 pad and the neighbour CLICpix pad. The greyed areas, indicated by the red arrows, are the parts of the pixel pads that act as a shield. The red lines are the electric field lines.

In Figure 22, the pixel pad regions in grey color, indicated by the red arrows, are the shielding areas mentioned above. For a gap of 3 μm (Figure 22a) there are fewer field lines connecting the central CCPDv3 pixel to the neighbouring pixels in the CLICpix chip than for a 5 μm gap (Figure 22b). As the capacitance is proportional to the density of the electric field, the larger quantity of field lines reaching

the neighbouring pixel indicates a stronger coupling. Despite the gap being bigger, the bigger overlap (and more electric field lines) compensates and increases the capacitance.

This hypothesis was confirmed by a 2D simulation where the neighbouring pixels in the CCPDv3 chip were removed. The corresponding geometry is shown in Figure 23. In this case, the cross-coupling capacitance always decreases for increasing gaps between the chips.

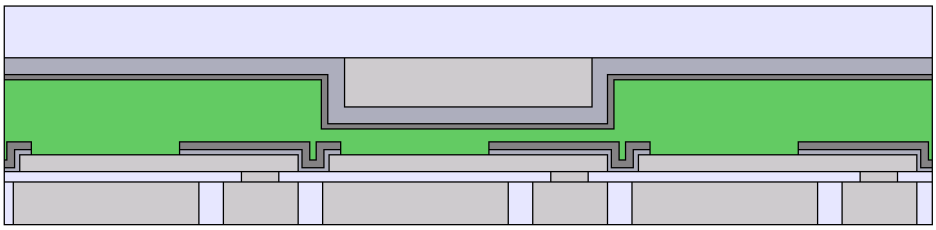

Figure 23: 2D geometry without neighbouring pixels in the CCPDv3 and for a gap of 1 μm.

4.3 Dependence on alignment

For the test samples produced so far, two different alignment schemes were used: the so called "pad+via alignment" and "pad alignment", illustrated in Figure 24(a) and (b), respectively. The nominal alignment chosen for the simulation model was pad+via alignment, while testbeam data exhibiting asymmetric cross coupling come from an assembly produced with pad alignment. The effective difference between the alignments is an offset of $\sim$4 μm in the row direction. Hence, this should be taken into account when analysing the results.

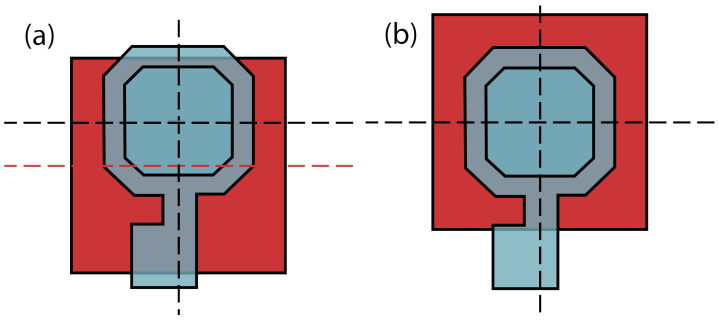

Figure 24: Pixel pad alignment scheme used for the production of test samples. (a) pad+via alignment. (b) pad alignment.

The alignment of the chips assembly relies on a prior alignment before the gluing, which can be done manually or by a pattern-recognition software, both methods using the images from the cameras of the flip-chip machine. It is therefore possible that the final alignment between the chips, after the gluing, is different from the aimed one due to imperfections of the alignment or the flip-chip process. Inspections of cross sections from different assemblies showed that the alignment precision is of the order of $\pm$2 μm in the X and Y axis. Ways to improve the alignment precision are being investigated.

4.3.1 One-dimensional misalignment offset

To simulate different alignment scenarios, the CLICpix chip was fixed in space and the CCPDv3 chip was moved from -13 μm to 13 μm, in steps of 1 μm, in the X (col) and Y (row) direction, from its

original position (via+pad alignment).

To maintain full overlap of the 3x3 area, a larger matrix with 5x5 pixels was created, where only the 3x3 central sub-matrix is analysed, as illustrated in Figure 25. The outer pixels were set together on the same *Terminal BC*. The glue layer was extended to the sides in order to fully fill the gap between the chips when they are with the maximum offset between each other.

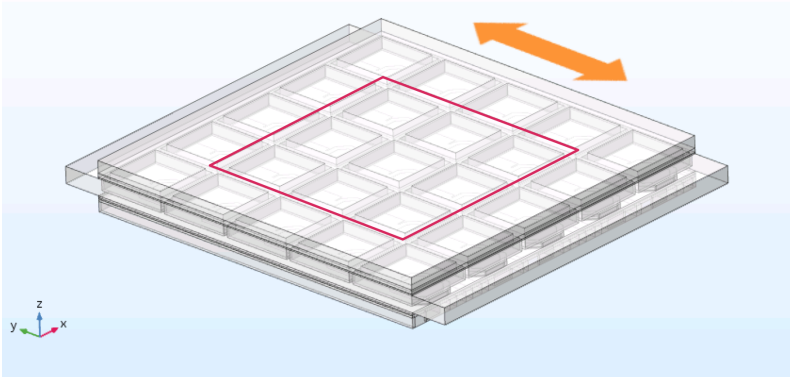

Figure 25: Extended 5x5 pixel matrix.

The results of the X, or column, scan are presented in Figure 26. The small box on the right hand side of the figure illustrates the position of each pixel in the matrix. The color bands represent the uncertainty of the capacitance at a given nominal position, due to the uncertainty of ± 2 μm from the flip-chip alignment, found after metrology measurements on real devices. It is visible that small misalignments (~ 2 μm), in the column direction, around the perfect pad+via alignment, do not affect the coupling with the closest pixel in the CLICpix chip (pixel 5) strongly, while increasing the cross coupling by about a factor of 3, as expected due to the geometric aspect of the CLICpix pixel pads.

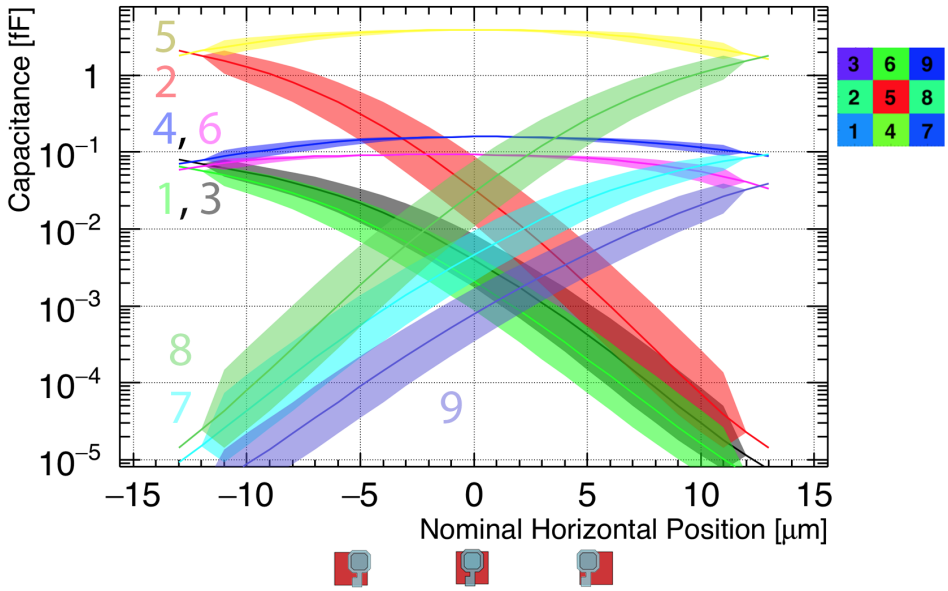

Figure 26: Coupling capacitances as a function of the matrix column (X) position. The uncertainty bands correspond to an assumed alignment precision of ± 2 μm. The bottom images of the pads indicate how the chips are moving with respect to each other.

The results for the Y, or row, offset scan is shown in Figure 27.

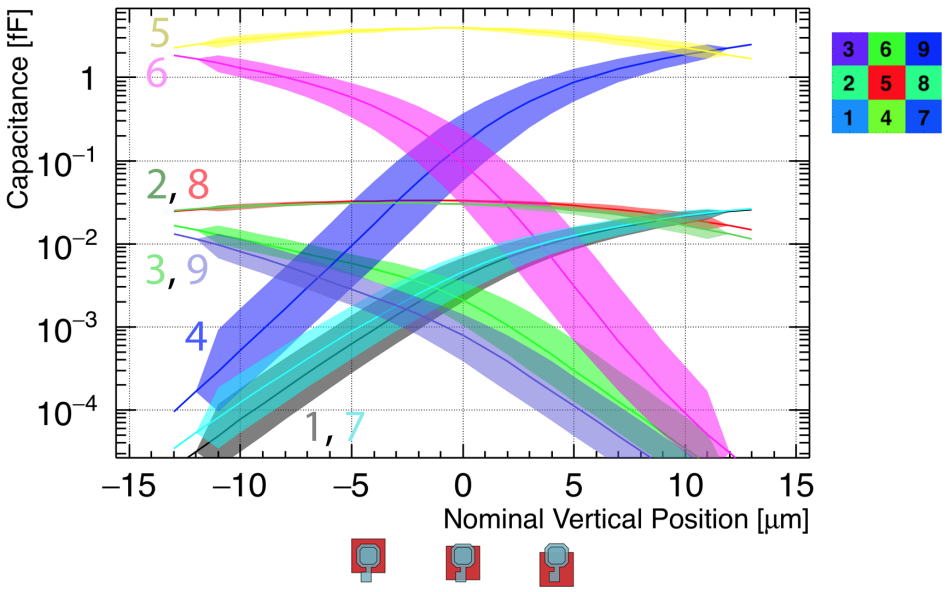

Figure 27: Coupling capacitances as a function of the matrix row (Y) position. The uncertainty bands correspond to an assumed alignment precision of ± 2 μm. The bottom images of the pads indicate how the chips are moving with respect to each other.

The asymmetric cross coupling capacitance to pixels 4 and 6 is visible for 0 μm offset (pad+via aligned position) where the cross coupling to pad 4 is almost twice as large as to pixel 6. This corresponds to the closer vicinity of the main pad area for pixel 4. To equalize the capacitance over these two pixels would require to move the CCPDv3 chip $\sim$0.6 μm in the direction of the pad alignment.

For the assemblies done with the pad alignment (-4.25 μm misalignment in Figure 27), one can expect relative capacitances of 0.4% and 12% for pixels 4 and 6, respectively. This result is yet to be confirmed with the analysis of the charge measured by the pixels during the testbeam campaign.

4.3.2 Two-dimensional misalignment

In order to visualize the effect of the alignment uncertainty, the simulations described above (with a scan of 26 μm in the horizontal and vertical directions) were combined in a 2-dimensional scan going from -2 up to 2 μm, in X and Y directions, creating a measurement plane with respect to the "pad+via alignment" (X=Y=0 position). Figure 28 illustrates the CCPDv3 pixel pad in the "pad+via alignment" and with the CCPDv3 pixel pad shifted -2 μm in the X direction and -1 μm in the Y direction. The inner segmented square represents the points where the CCPDv3 pixel pad was simulated with respect to the CLICpix pixel pad. Each point represents one bin in the 2D histogram in Figure 29.

Figure 29 shows the simulated capacitance for each position of the 2D scan. The simulation shows that in the worst simulated alignment case (+2 μm in X and Y), the coupling capacitance decreases by about 200 aF, or $\sim$5%. The asymmetry in the vertical direction is due to the shape of the CLICpix pixel pad. It is also possible to see that the coupling capacitance is maximized if the pad is shifted between 0.5 and 1 μm in the direction away from the via of the CLICpix pixel. This is due to, again, the complex geometry of the pixel pads. However, the capacitance difference between the "pad+via alignment" and the alignment with a -1 μm offset in the Y direction is $\sim$10 aF, and $\sim$12.5 aF from the optimal position (extracted from interpolation). Such a small capacitance difference corresponds to $\sim$0.3% and can be

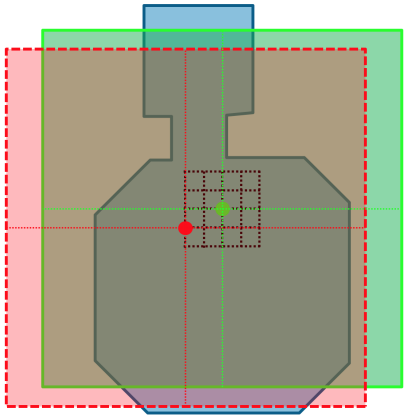

Figure 28: Illustration of the pixel pad alignments. In green, the "pad+via alignment". In red, the CCPDv3 pixel pad is shifted -2μm in the X direction and -1 μm in the Y, w.r.t. the "pad+via alignment". Each point in the black segmented square represents one position of the CLICpix pixel "center-of-mass" with respect to the center of the CCPDv3 pixel.

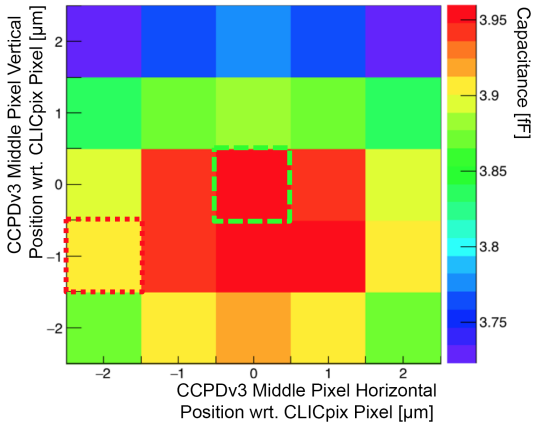

Figure 29: Calculated capacitances for different positions of the CCPDv3 pixel with respect to the CLICpix pixel. The dashed red and green squares represent the two positions illustrated in Figure 28.

neglected in practice.

The effect of the uncertainty on the position of the CCPDv3 pixel can also be calculated for the neighbouring pixels in the CLICpix chip, as in the previous simulations, in order to understand the global effect of the alignment precision on the couplings. Figure 30 shows the coupling capacitance of the 9 CLICpix pixels with the central CCPDv3 pixel in the 3x3 pixel matrix. As before, each bin represents one position in the 2-dimensional scan. Each 2D-histogram, in Figure 30, represents one pixel on the CLICpix. The color scale range is the same for all histograms and the values are in fF.

It is possible to see that the cross coupling capacitances are more affected by misalignment than the capacitance to the closest CLICpix pixel (pixel number 5). Within the ± 2 μm misalignment range, changes of cross coupling capacitances by about one order of magnitude are observed.

5 Simulations for new chip versions

A new read-out chip, CLICpix2, and a new HV-CMOS sensor, C3PD (CLIC Capacitive Coupled Pixel Detector) were designed based on the successful features of the previous chips.

The CLICpix2 chip is implemented in the same 65 nm CMOS technology and, among other new features, contains a larger pixel matrix with 128x128 pixels, with small changes in the dimensions of the pixel pads, and registers for the time-stamping and energy measurements of the particle hits with higher resolution. The C3PD is a new design with features based on the CCPDv3 chip and implemented in the same 180 nm HV-CMOS technology. A new main feature, relevant regarding the cross coupling, is a guard ring (GR) structure, surrounding the pixel pads, in order to decrease the cross coupling between the pixels.

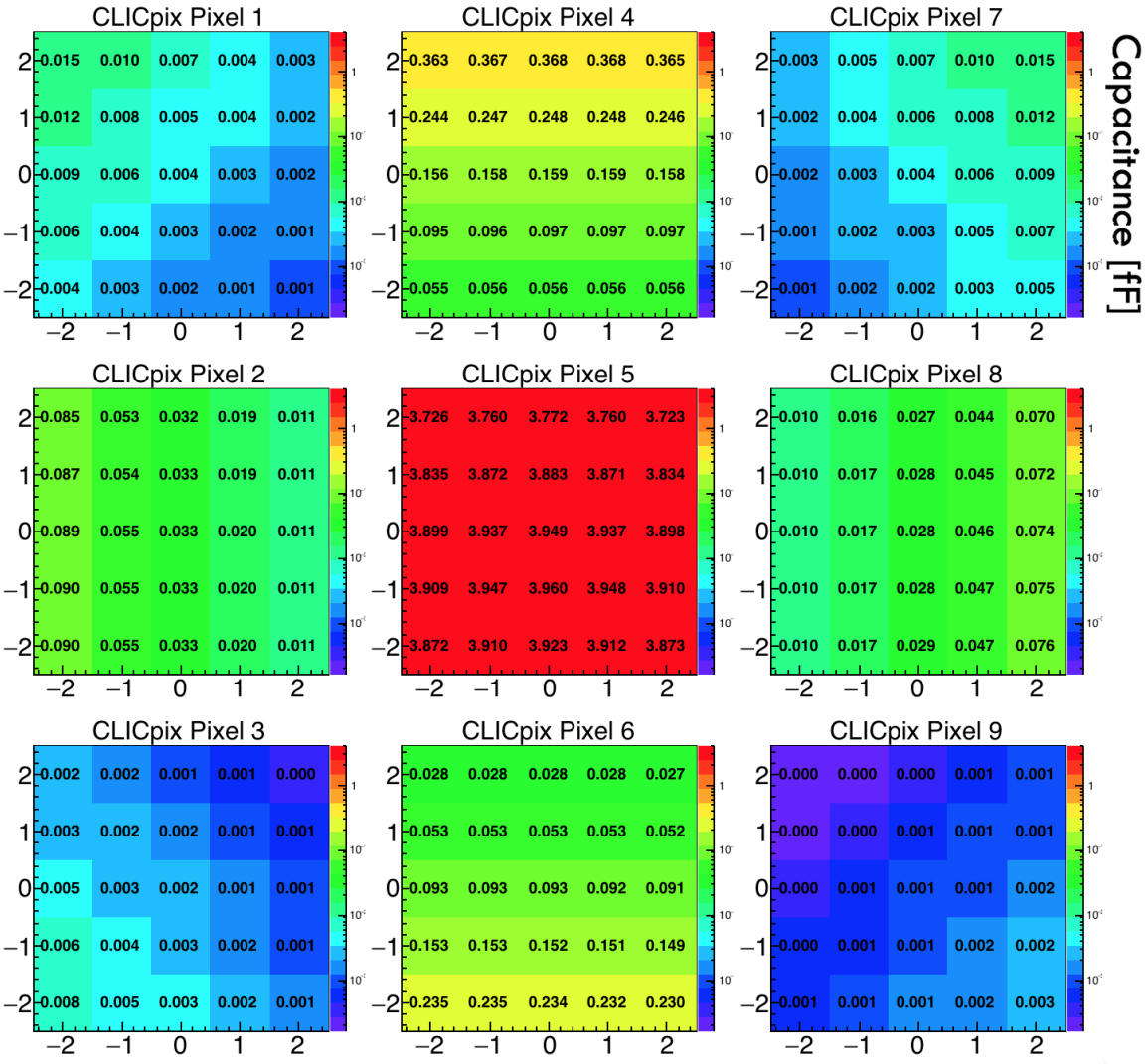

Figure 30: Coupling capacitances for the 9 pixels in the CLICpix matrix for different positions of the CCPDv3 pixel. The bins represents the position of the CCPDv3 pixel as in Figure 29.

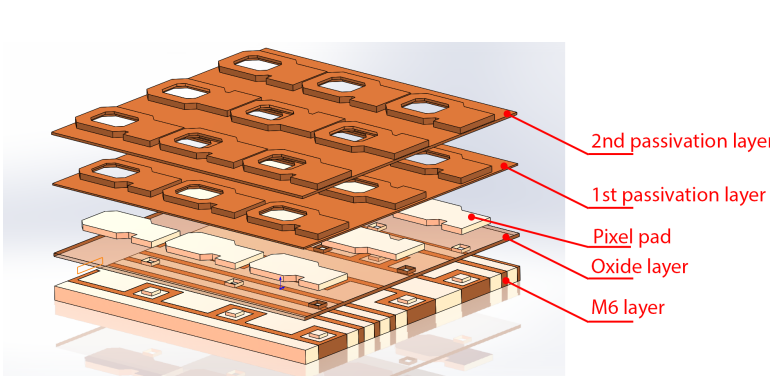

Figure 31: CLICpix2 chip layers.

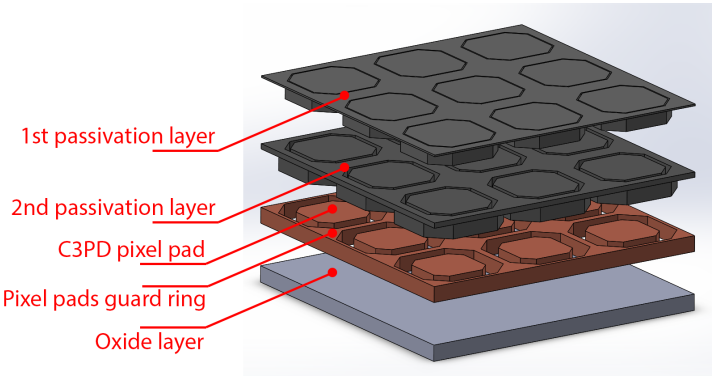

Figure 32: C3PD chip layers.

The SolidWorks 3D model of the new chips is shown in Figures 31 and 32. They were assembled with the same gap of 0.2 μm as before. The assembly was imported to COMSOL and the glue layer was created in the same way as before. As the chips were created with the same technology, the materials used in this model are the same. The *Electrostatics* physics interface was used here as well, with the addition of a new BC for the GRs. The GRs are inserted in order to shield the HV-CMOS pixel pads and its boundaries were defined with the *Terminal BC*. In order to compare the effect of the GR on the cross coupling, the C3PD was also modelled without the GR, maintaining the rest of the geometry identical.

The effect of the ROC metal line layers on the pixel pad coupling simulation was also analysed for the CLICpix+C3PD assembly. For this, in addition to the passivation, pixel pad and M6 layers, the M5 layer was also modelled. The M5 layer has a thickness that is four times smaller than the M6 layer and is further away from the C3PD pixel pads. Hence, it is expected that it has only a small influence on the coupling. The simulations were done progressively adding the metal layers (with the respective dielectric layer and vias in between), starting only with the passivation layers and pixel pads.

5.1 Simulation results on Guard Ring effects

The guard ring shields the C3PD pixel pads from the neighbouring pixels in the ROC by adding a conductor in between the pads. This decreases the coupling capacitance to the neighbours as it makes the overlap surface smaller. The effect can be seen looking at the potential and electric field distribution between the pixel pads shown in Figure 33. The cross section shows the middle C3PD pixel pad on the top and the CLICpix2 pixels 4, 5 and 6 (from left to right) on the bottom, marked by dashed lines.

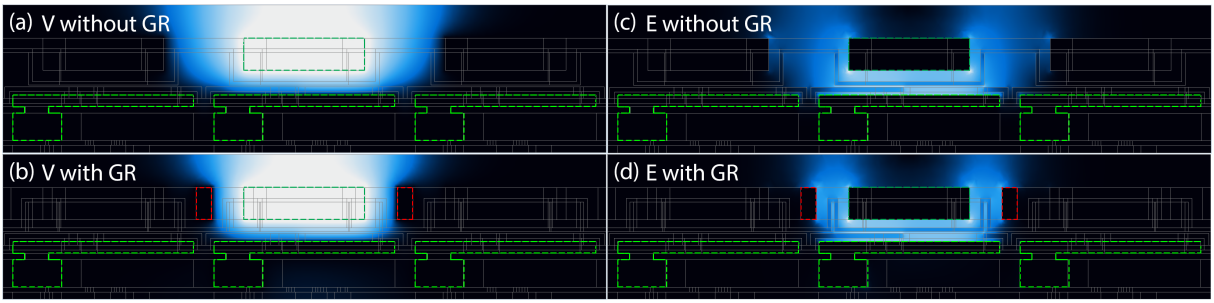

Figure 33: Electric potential ((a) and (b)) and electric field ((c) and (d)) distribution, without ((a) and (c)) and with ((b) and (d)) guard ring. The GR is grounded and is delimited by the dashed red line. The C3PD (top) and CLICpix2 (bottom) pixel pads are indicated by the green dashed lines.

Table 2 summarises the coupling capacitances found for pixels 4, 5 and 6 with and without GR. The GR blocks the potential and electric field from reaching the neighbouring pixels, decreasing the cross coupling by almost a factor of 10, while increasing the capacitance to the closest, or main, pixel by a few attofarads ($\sim$4%).

Table 3: Pixel 14 coupling capacitances, in fF, with and without guard ring.

	Pixel 4	Pixel 5	Pixel 6	Metal lines	GR
Without GR	96E-3	3.360	96E-3	854E-3	-x-
Grounded GR	12E-3	3.484	12E-3	398E-3	3.14

The GRs also helps to shield the metal lines from the sensor pixel, decreasing its coupling capacitance by almost half. On the other hand, it adds a parasitic capacitance, as the sensor pixel will also induce a charge on the GR. The result shows that the coupling capacitance is 3.14 fF, comparable with the

capacitance to the ROC pixel. This capacitance is relevant for the design of the pixel electronics, as it adds a non negligible load to the pixel output amplifiers.

5.2 Effect of deeper metal layers on simulation results

In order to simulate a system as realistic as possible it would be needed to simulate the complete chip, with all pixels and metal lines. To simulate all the possible capacitances, it is needed to simulate all metal lines on the ROC that could parasitically couple to the HV-CMOS pixel. There are 7 metal layers with the respective vias in between. The layers from M1 to M5 are thin, with M5 having 0.9 μm and the other layers ~ 0.2 μm. These layers are shielded from the pixel pads by the M6 layer (with 3.4 μm thickness). Therefore it is expected that the dominating parasitic capacitance comes from the M6 layer, which was included in the simulation model for all results shown in the previous sections. In order to quantify the contribution of the inner metal layers to the simulated capacitance values, two new simulation geometries were created. In one, the M6 layer was removed. In the other, the M5 layer and corresponding vias were added under the M6 layer. Figures 34 and 35 show the geometry of the model with M5 and M6 layers.

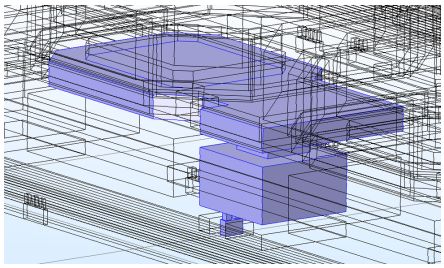

Figure 34: Pixel pad + via + M6 + via + M5.

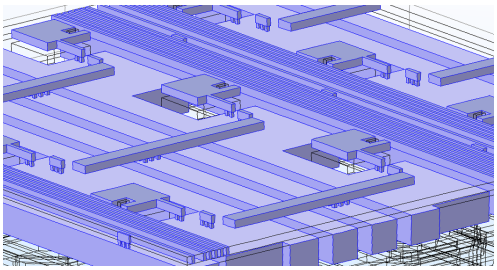

Figure 35: M5 and M6 layers and vias.

In order to simulate the different geometries (with and without metal layers) one mesh was created including all the layers. For the different geometries to be simulated, the volume enclosing the layers to be excluded from the calculation was excluded from the *Electrostatic interface*. Doing so, the mesh elements inside the volume excluded are not taken into account for the simulation.

Table 3 shows the simulation results for the 3 geometries. The addition of the M6 layer decreases the capacitance to the main pixel by 4% (130 aF). This is due the fact the the M6 layer increases the volume of the model, thereby decreasing the electric energy density and thus the total capacitance. The same trend is visible for the neighbouring pixels.

Table 4: Pixel 14 coupling capacitances, in fF, when different metal layers are included.

	Pixel 4	Pixel 5	Pixel 6	Metal lines
Without M6 and M5	15E-3	3.6151	16E-3	-x-
With M6	12E-3	3.4840	12E-3	398E-3
With M6 and M5	12E-3	3.4839	12E-3	398E-3

The addition of the M5 layer does not change the capacitances significantly. With this result, one can conclude that the modelling of the M6 layer is sufficient to provide an accurate simulation of the chips.

6 Summary and conclusions

In the context of the CLIC vertex detector project, glued hybrid assemblies of a CLICpix readout ASIC and a CCPDv3 active HV-CMOS sensor have been produced. As the signal transmission from the sensor

to the readout chip is done via capacitive coupling, the assembly has to be precisely aligned and the issue of cross coupling between different pixels needs to be considered.

Simulations using finite element method were carried out using COMSOL Multiphysics. A matrix of 3x3 pixels was modelled for the CLICpix readout chip and for the CCPDv3 HV-CMOS sensor. The model contains the passivation layers of the chip, pixel pads and metal lines with respective dielectric layers and vias in between, as well as the glue layer filling the gaps between the pixel pads.

The capacitance matrix was calculated for the pixel pads and metal lines. For nominal alignment parameters and a gap of 3 μm between the pixel pads, it shows a coupling capacitance of 3.80 fF for the HV-CMOS pixel with the readout pixel directly under it. The capacitance to the neighbouring pixels is considerably smaller. The two highest capacitances found for the neighbouring pixels are 0.068 fF (2.3% of main coupling) and 0.141 fF (3.7%). When increasing the distance between the pixel pads to 20 μm, the coupling capacitance drops by about one order of magnitude

Simulations with different alignments were also done to study the effect of possible misalignments during the bonding process. The chips were moved horizontally between -13 and +13 μm with respect to the center of each other, in the X (column) and Y (row) direction in a 1D scan, and from -2 up to +2 μm in X and Y directions in a 2D scan. The results show that small offsets in the X direction do not have a major effect on the cross coupling between the pixel pads. However, misalignments in the Y direction are more relevant, as the Y spacing between different pads is smaller. Hence, the capacitance to the two closest neighbour pixels can change significantly within the achievable alignment accuracy of $\sim \pm 2$ μm. It was also shown that the alignment can induce an asymmetry in the cross coupling, as observed in testbeam measurements.

Assemblies with the new readout chip CLICpix2 and the new C3PD HV-CMOS sensor were simulated. The results show that the newly introduced guard ring around the C3PD pixel pads helps to decrease the cross coupling by almost a factor of 10, while keeping the main coupling essentially unchanged. The new chips were also simulated by including the metal layers in the model. It was shown that the M6 layer, together with the pixel pads and passivation layers, is sufficient to create an accurate model of the assembly for the simulation.

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