An IPMI-compliant control system for the ATLAS TileCal Phase-II Upgrade PreProcessor module

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***Abstract*–The electronics of the hadronic calorimeter of the ATLAS detector (TileCal) is being redesigned as part of the works that will lead to the High Luminosity Large Hadron Collider (HL-LHC).**

TileCal electronics is divided in front and back-end sub-systems. While the front-end is inside the detector, the back-end is located off-detector inserted in an ATCA shelf. The main objective of this paper is to describe the work being carried out in the hardware management aspects of the back-end electronics of TileCal.

I. Introduction

TileCal is the Tile hadronic calorimeter of the ATLAS experiment at the Large Hadronic Collider (LHC). The LHC upgrade program, currently under development, will culminate in the High Luminosity LHC (HL-LHC), which is expected to operate at about five times the LHC nominal instantaneous luminosity. Under this scenario, the readout electronics of the Tile calorimenter is being redesigned introducing a new read-out strategy in order to cope with the new HL-LHC parameters [1,2].

The data generated inside the detector at every bunch crossing will be transmitted to the PreProcessor (PPR) boards [3] before any event selection is applied. The PPRs, planned to be located off-detector, will provide preprocessed trigger information to the ATLAS first level trigger (L1).

The PPR is the main interface between the data acquisition, trigger and detector control systems and the on-detector electronics, therfore, being an important part of the readout system, it needs to be remotely controlled and monitored to prevent failures or, in case some failure occurs, to accurately diagnose the problem. With that purpose in mind, the PPR is included in an Advanced Telecommunications Computing Architecture (ATCA) [4] shelf that, not only provides high speed communication capabilities, but also includes an Intelligent Platform Management Interface (IPMI) compliant [5] out-of-band control architecture.

The main subject of this document is to show the hardware management features being implemented in the back-end electronics of the Phase-II Upgrade of the Tile calorimeter of ATLAS.

In Section II the main aspects of the TileCal upgraded electronic architecture is described, in Section III ATCA shelves and some of there hardware management aspects are introduced; the main aspects of the PPR are also explained. Section IV describes the main aspects of the IPMI system software designed at the Instituto de Física Corpuscular (IFIC). In Section V the conclusions are presented.

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II. TileCal Phase-II Upgrade

TileCal is an iron-scintillator calorimeter essential for measuring the presence, incident angle and energy of hadrons produced as in the LHC collisions inside the ATLAS detector.

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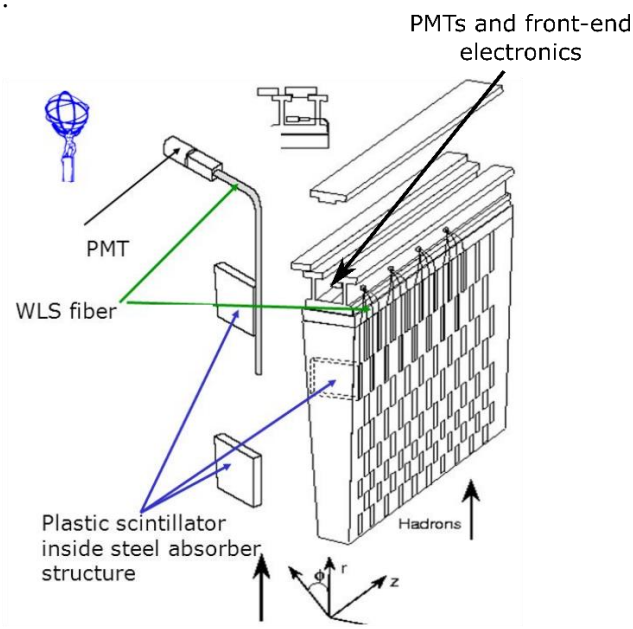

Fig. 1 Illustration of the composition of a TileCal module.

TileCal is divided into barrels, which are then divided into modules. A diagram of one of the modules can be seen in Fig.1 where its components are described. Every 25ns LHC particle bunches cross each other inside ATLAS. When the particles from the collisions hit the scintillator material, light is produced. This light signal is collected by Wave-Length Shifting (WLS) optical fibers and amplified by a photomultiplier (PMT). The PMTs deliver to the front-end electronics an analog electronic signal that is conditioned, digitized, properly formatted and transmitted off-detector to the

back-end electronic system. A schematic view of the readout electronics is depicted in Fig.2.

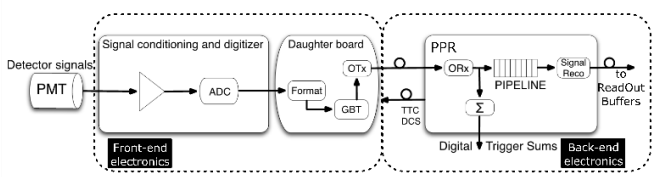

Fig. 2 Functional scheme of the TileCal Phase-II Upgrade readout, where DCS means Detector Control System, TTC is Timing and Trigger Control and GBT stands for GigaBit Transciever.

In the back-end, the PPR provides preprocessed information to L1 and stores the digital samples in pipelined memories. If a certain event is selected by the trigger system, its samples are processed and transmitted to the ATLAS global data acquisition (DAQ) system.

III. Hardware Management in ATCA Shelves and TileCal Back-End Electronics

The core of the back-end electronics for the Phase-II Upgrade are the PPR boards. This device has been designed to operate within an ATCA shelf.

A. ATCA shelf and PICMG set of specifications

The ATCA is defined by a set of PCI Industrial Computer Manufacturers Group (PICMG) specifications, denoted as PICMG 3.x [4,6], that propose an open multi-vendor architecture targeted to fulfill the requirements for carrier grade high-performance communications equipments.

Besides the high-performance communications links, the PICMG 3.x specifications include extensive in-band and out-band hardware control and management capabilities. This aspect of the ATCA specification is mainly based on the IPMI specification [5].

An ATCA crate is a shelf structure that includes several ATCA-compliant boards with different communications and computing functionalities that are interconnected via the same hardware platform management bus. In the IPMI environment, this is an I2C bus called Intelligent Platform Management Bus (IPMB).

Fig.3 shows the structure of the ATCA being used at CERN and IFIC laboratories to test and develop the TileCal Phase-II Upgrade hardware/firmware back-end electronic system.

The Shelf Manager assures proper operation of the shelf and is responsible of monitoring and control over the other boards in the crate. The Single Board Computer (SBC) is a general purpose computer board, while the ATCA carrier controls and gives connectivity services to a set of Advanced Mezzanine Cards (AMC) inserted in it. Intelligent Platform Management Controllers (IPMCs) are intelligent devices, usually implemented in small microcontrollers, embedded in ATCA boards with hardware management features.

The Shelf Manager Controller (ShMC) and the Module Management Controller (MMC) are also hardware management controller devices. While all share some basic functionality, they have different levels of responsibility within the IPMI infrastructure.

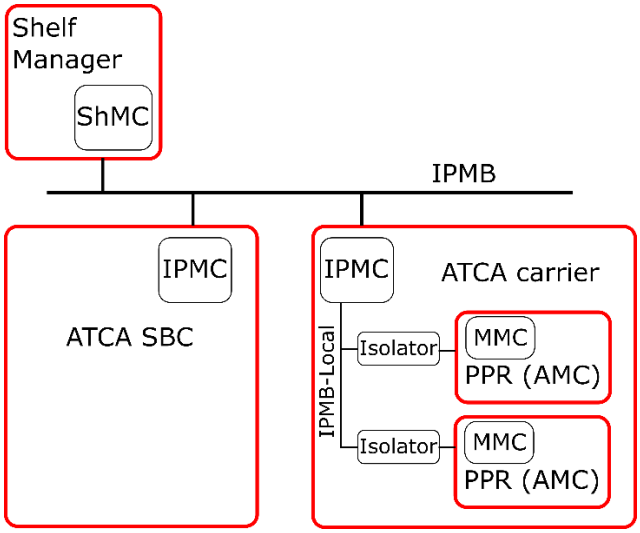

Fig. 3 Illustration of the ATCA shelf infrastructure.

The PPR prototype was designed in an AMC-compliant format.

B. PPR prototype board

The PPR prototype board, depicted in Fig.4, is a custom design module which includes one Virtex7 and one Kintex7 FPGAs for data processing.

With a bidirectional bandwidth of 260 Gbps is able to process one TileCal front-end drawer equipped with up to 48 PMTs. It includes 4 QSFP connectors, which provide full duplex communication with the front-end electronics. The 16 input optical links, running at 10.24 Gbps, are used to receive the PMTs data as well as to monitor information from the on-detector electronics. The 16 output optical links running at 4.8 Gbps are used to transmit configuration and control commands to the front-end electronics.

The design includes a series of sensors that allow monitoring its status continuously. Table I shows a list of sensors and the number of bytes needed to read their state records.

As shown in Fig.4, a small board with an ATMega128 microcontroller fulfills the functionalities of IPMI-MMC. Through the MMC, via the IPMB, the status of the different sensors can be retrieved and configuration commands to different devices in the PPR can be issued. A list of control/configuration devices is included in Table I.

IV. System Software for Hardware Management

An IPMI system software was designed at IFIC. The main goals of this software are:

- To visualize, in real time, the state of the ATCA crate boards, sensors and alarms.
- To send orders and commands, via the IPMI hardware management links, to the PPRs inserted in the crate.
- To keep historical records of the performance (power consumption, communications links failure,

temperature, etc.) of the different boards, in particular of the PPR.

The software relies on OpenIPMI and IpmiTool libraries for the IPMI connectivity features and on MySQL database for recording all collected data. The graphical user interface (see Fig.5) is based on Qt-C++ libraries.

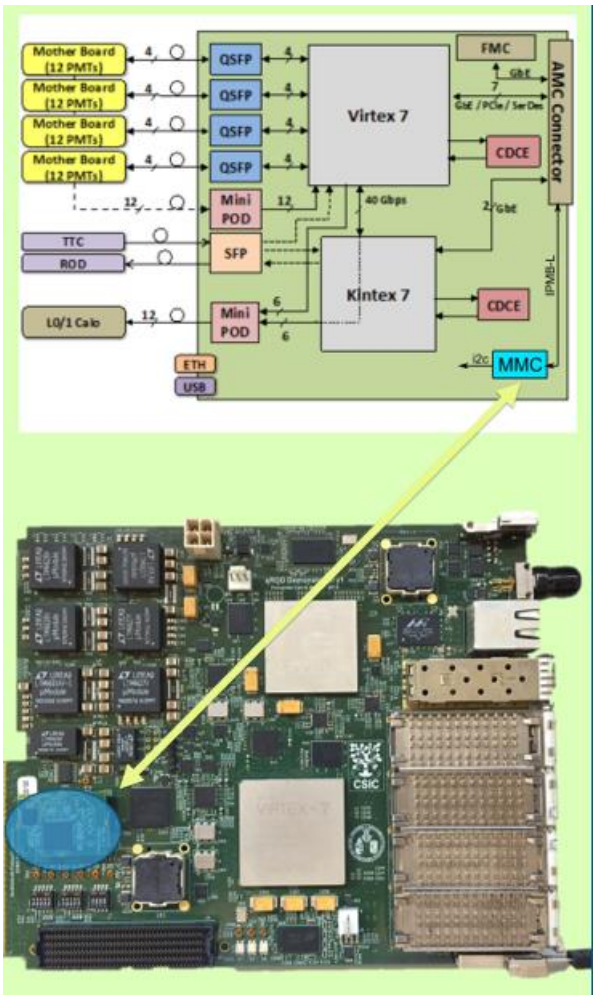

Fig. 4. Schematic representation and picture of PPR prototype board.

The PPRs are not directly connected to the main IPMB link, but are accesible only by bridging messages through the IPMC of the ATCA carrier to the IPMB-Local (see Fig.3 and [6]).

V. Conclusions

The electronic systems of the barrel hadronic calorimeter of the ATLAS detector, TileCal, is being redefined as part of the Phase-II Upgrade process. The core component of the back-end electronics, the PPR, has been designed to operate inside an ATCA shelf. One of the main features of ATCA crates is the IPMI-compliant hardware management infrastructure. In this work, the IPMI hardware management features of the back-end electronics developed for the TileCal Phase-II Upgrade have been described. Under this project, a custom MMC board (hardware and firmware) has been designed and implemented at CERN so that it operates embedded in the PPR. A system software that gathers all the information of the ATCA shelf (sensors, boards and blades presence and status, alarms and events) specifically oriented to communicate, configure and read the status of the PPR has been designed at IFIC.

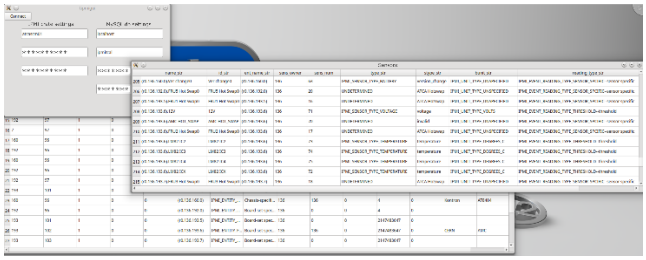

Fig. 5. IPMI System Software graphical interface.

TABLE I. PPR SENSORS AND CONFIGURABLE/READABLE DEVICES VIA IPMB

Device	N.devices x N.registers per device
Supply voltage	8x1 (sensor, r)
Supply Current	8x1 (sensor, r)
QSFP (link on/off state)	(4x4) links x1 (control, r/w)
QSFP (link optic. pwr)	(4x4) links x1 (sensor, r)
SFP (on/off state)	1x1 (control, r/w)
SFP (optical power)	1x1 (sensor, r)
MiniPOD (on/off state)	2x12 (control, r/w)
MiniPOD (optical power)	2x12 (sensor, r)
Temperature Sensor	6x1(sensor, r)
Clock config.registers	4x4 (control, r/w)
Jitter cleaners Normal	2x2 (control, r/w)
FPGAs remote reset	3x1 (control, w)
PPR id EEPROM	1x1 (configuration, r/w)

References

[1] The ATLAS Collaboration, “Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment”, CERN-LHCC-2012-022. LHCC-I-023, Dec.2012.

[2] F. Tang et al., “Design of the front-end readout electronics for the ATLAS tile calorimeter at the sLHC,” IEEE Trans.Nuc.Science, V.60, N.2.1255-1259, Apr.2013.

[3] F. Carrió et al. “The PreProcessor for the ATLAS Tile Calorimeter Phase II Upgrade”, IEEE NSS 2015, San Diego (USA-CA) Oct./Nov.2015.

[4] PICMG 3.0 Revision 2.0 AdvancedTCA Base Specification. http://www.picmg.org.

[5] Intelligent Platform Management Interface Specifications v1.5 and v2.0. http://www.intel.com/content/www/us/en/servers/ipmi/ipmi-home.html

[6] PICMG Advanced Mezzanine Card (AMC) Base Specification. https://www.picmg.org/openstandards/advanced-mezzanine-card/