An IPMI-compliant control system for the ATLAS TileCal Phase-II Upgrade PreProcessor module

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***Abstract*–The electronics of the hadronic calorimeter of the ATLAS detector (TileCal) is being redesigned as part of the work that will lead to the High Luminosity Large Hadron Collider (HL-LHC).**

TileCal electronics is divided in front and back-end sub-systems. While the front-end will be inside the detector, the back-end is planned to be off-detector inserted in an ATCA shelf. The main objective of this paper is to describe the work being carried out in the hardware management aspects of the back-end electronics of TileCal.

I. Introduction

TileCal is the central hadronic calorimeter of the ATLAS experiment at the Large Hadronic Collider (LHC) [1]. The LHC upgrade program, currently under development, will culminate in the High Luminosity LHC (HL-LHC), which is expected to operate at about five times the LHC nominal instantaneous luminosity. Under this scenario, the readout electronics of the Tile calorimeter is being redesigned introducing a new read-out strategy in order to cope with the new HL-LHC parameters [2,3].

The data generated inside the detector at every bunch crossing will be transmitted to the PreProcessor (PPR) boards [4] before any event selection is applied. The PPRs, planned to be located off-detector, will provide preprocessed trigger information to the ATLAS first level trigger (L1) [5].

The PPR is the main interface between the Trigger and Data Acquisition System (TDAQ) and Detector Control System (DCS) and the on-detector electronics, it needs to be remotely controlled and monitored to prevent failures or, in case some failure occurs, to accurately diagnose the problem. With this purpose in mind, the PPR is included in an Advanced Telecommunications Computing Architecture (ATCA) [6] shelf that, not only provides high-speed communication capabilities, but also includes an out-of-band control architecture compliant with the Intelligent Platform Management Interface (IPMI) [7] specification.

This document describes the hardware management features being implemented for the back-end electronics Phase-II upgrade of the Tile calorimeter.

In Section II the main features of the TileCal upgraded electronic architecture are described, in Section III the ATCA shelves and some of the hardware management aspects are introduced; the main characteristics of the PPR are also explained. Section IV describes the IPMI system software being designed at the Instituto de Física Corpuscular (IFIC). In Section V the conclusions are presented.

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II. TileCal Phase-II Upgrade

TileCal is a steel-scintillator calorimeter essential for the triggering and reconstruction of hadrons produced in the LHC collisions inside the ATLAS detector.

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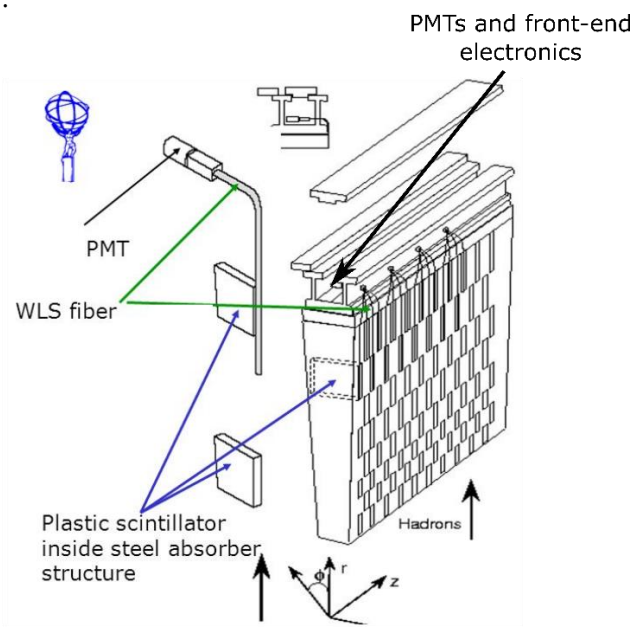

Fig. 1 Principle of a TileCal module.

TileCal is divided into 4 barrels, which are then divided into 64 modules each. A diagram of one of the modules can be seen in Fig.1 where its components are described. Every 25ns LHC particle bunches collide inside ATLAS. When the particles from the collisions hit the scintillator material, light is produced. This light signal is collected by Wave-Length Shifting (WLS) optical fibers and amplified by a photomultiplier (PMT). The PMTs deliver to the front-end electronics an analog electronic signal that is conditioned, digitized, properly formatted and transmitted off-detector to the back-end electronic system. A schematic view of the readout electronics is depicted in Fig.2.

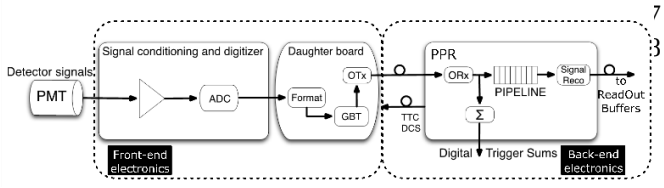

Fig. 2 Functional scheme of the TileCal Phase-II readout, where TTC is Timing and Trigger Control and GBT stands for GigaBit Transceiver.

In the back-end, the PPR provides preprocessed information to L1 trigger and stores the digital samples in pipelined memories. If a certain event is selected by the trigger system, its samples are processed and transmitted to the ATLAS global data acquisition (DAQ) system.

III. Hardware Management in ATCA Shelves and TileCal Back-End Electronics

The core of the back-end electronics for the Phase-II Upgrade are the PPR boards. This device has been designed to operate within an ATCA shelf.

A. ATCA shelf and PICMG set of specifications

The ATCA is defined by a set of PCI Industrial Computer Manufacturers Group (PICMG) specifications, denoted as PICMG 3.x [6,8], that propose an open multi-vendor architecture targeted to fulfill the requirements for carrier grade high-performance communications equipments.

Besides the high-performance communications links, the PICMG 3.x specifications include extensive in-band and out-band hardware control and management capabilities. Out-of-band management guarantees the access to the hardware even when the operative system (OS) is powered off or unresponsive. This is achieved by setting up a direct network connection to the hardware rather than to the OS. This aspect of the ATCA specification is mainly based on the IPMI specification [7].

An ATCA crate is a shelf structure that includes several ATCA-compliant boards with different communications and computing functionalities that are interconnected via the same hardware platform management bus. In the IPMI environment, this is an I2C bus called Intelligent Platform Management Bus (IPMB).

Fig.3 shows the structure of the ATCA being used at CERN and IFIC laboratories to test and develop the TileCal hardware/firmware back-end electronic system.

The Shelf Manager assures proper operation of the shelf by managing its power, cooling, interconnects, responding to event messages and performing monitor and control tasks over the other boards in the crate. The Single Board Computer (SBC) is a general purpose computer board, while the ATCA carrier controls and gives connectivity services to a set of Advanced Mezzanine Cards (AMC) [8] inserted in it. Intelligent Platform Management Controllers (IPMCs) are intelligent devices, usually implemented in small microcontrollers, embedded in ATCA boards with hardware management features.

The Shelf Manager Controller (ShMC) and the Module Management Controller (MMC) are also hardware management controller devices. While all share some basic functionality, they have different levels of responsibility within the IPMI infrastructure.

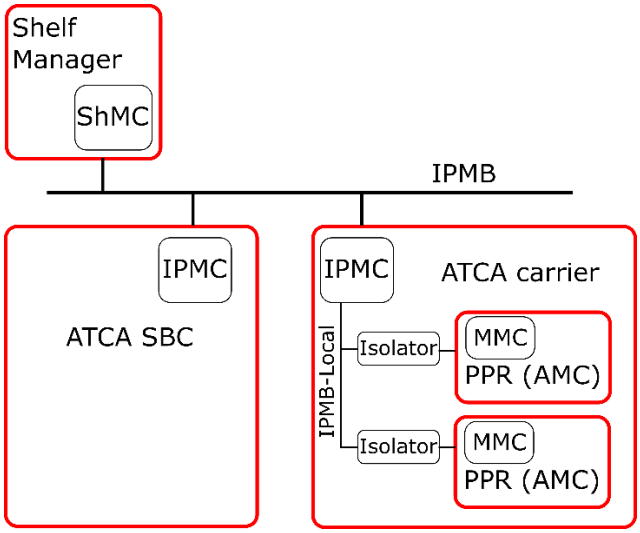

Fig. 3 Illustration of the ATCA shelf infrastructure.

The PPR prototype was designed in an AMC-compliant format.

B. PPR prototype board

The PPR prototype board, shown in Fig.4, is a custom design module which includes one Virtex7 and one Kintex7 FPGAs for data processing.

With a bidirectional bandwidth of 280 Gbps is able to process one TileCal front-end drawer equipped with up to 48 PMTs. It includes 4 QSFP connectors, which provide full duplex communication with the front-end electronics. The 16 input optical links, running at 9.6 Gbps, are used to receive the PMTs data as well as to monitor information from the on-detector electronics. The 16 output optical links running at 4.8 Gbps are used to transmit the clock and configuration and control commands to the front-end electronics.

The PPR design includes a series of sensors that allow monitoring its status continuously. Table I shows a list of sensors and the number of bytes needed to read their state records.

The hardware management devices and links of the PPR are highlighted in Fig.4. A small board with an ATMega128 microcontroller fulfills the functionalities of IPMI-MMC. The temperature sensors, the EEPROM that holds the PPR id number, a GPIO chip -accessible via I2C protocol and labelled as Digital Switch in Fig.4- used to activate the reset signals of the three FPGAs and the Spartan-6 FPGA are directly connected to one of the I2C buses of the MMC. QSFP, MiniPOD and SFP connectors, the jitter cleaners, the I/V sensors and the XTALs configuration are connected to one of the I2C buses of the Spartan-6, therefore, when the MMC needs to communicate with these devices, the messages have to be bridged through the Spartan-6 FPGA.

Through the MMC, via the IPMB, the status of the different sensors can be retrieved and configuration commands to different devices in the PPR can be issued. A list of control/configuration devices is included in Table I.

IV. System Software for Hardware Management

An IPMI system software was designed at IFIC. The main goals of this software are:

- To visualize, in real time, the state of the ATCA crate boards, sensors and alarms.
- To send commands, via the IPMI hardware management links, to the PPRs inserted in the crate.
- To keep historical records of the performance (power consumption, communications links status and failure, temperature, etc.) of the different boards, in particular of the PPR.

The software relies on OpenIPMI and IpmiTool libraries for the IPMI connectivity features and on MySQL database for recording all collected data. The graphical user interface (see Fig.5) is based on Qt-C++ libraries.

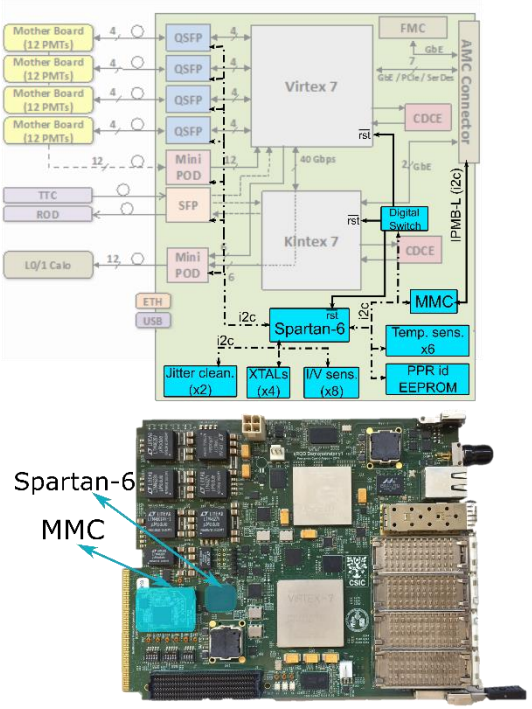

Fig. 4. Schematic representation and picture of the PPR prototype board. Hardware Management devices and links are highlighted in the schematic.

The PPRs are not directly connected to the main IPMB link, but are accessible only by bridging messages through the IPMC of the ATCA carrier to the IPMB-Local (see Fig.3 and [8]).

V. Conclusions

The electronic systems of the hadronic calorimeter of the ATLAS detector, TileCal, is being redesigned for the operation at the HL-LHC. The core component of the back-end electronics, the PPR, has been designed to operate inside an ATCA shelf. One of the main features of ATCA crates is the IPMI-compliant hardware management infrastructure. In this work, the IPMI hardware management features of the back-end electronics developed for the TileCal Phase-II Upgrade have been described. Under this project, a custom MMC board (hardware and firmware) has been designed and implemented at CERN so that it operates embedded in the PPR. A system software that gathers all the information of the ATCA shelf (sensors, boards and blades presence and status, alarms and events) specifically oriented to communicate, configure and read the status of the PPR has been designed at IFIC.

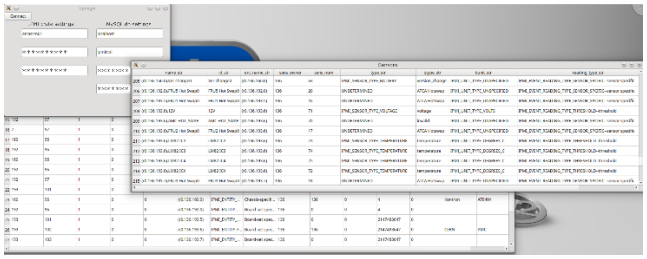

Fig. 5. IPMI System Software graphical interface.

TABLE I. PPR sensors and configurable/readable devices via IPMB

Device	N.devices x N.registers per device
Supply voltage	8x1 (sensor, r)
Supply Current	8x1 (sensor, r)
QSFP (link on/off state)	(4x4) links x1 (control, r/w)
QSFP (link optic. pwr)	(4x4) links x1 (sensor, r)
SFP (on/off state)	1x1 (control, r/w)
SFP (optical power)	1x1 (sensor, r)
MiniPOD (on/off state)	2x12 (control, r/w)
MiniPOD (optical power)	2x12 (sensor, r)
Temperature Sensor	6x1(sensor, r)
XTALs config.registers	4x4 (control, r/w)
Jitter cleaners	2x2 (control, r/w)
FPGAs remote reset	3x1 (control, w)
TOTAL OF 'read' BYTES	125
TOTAL OF 'write' BYTES	65

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