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The ATLAS Fast TracKer- input and output data preparation

J. Adelman,[a] **J. Anderson,**[b] **A. Armbruster,**[c] **N. Asbah,**[d] **R. Blair,**[b] **A. Bolz***,[e] **E. Brost,**[a] **G. Drake,**[b] **S. Gkaitatzis**[f] **T. Iizawa,**[g] **N. Ilic,**[c] **Z. Jiang,**[c] **Y. Kawaguchi,**[g] **N. Kimura,**[f] **K. Kordas,**[f] **C .L. Sotiropoulou,**[h] **J. Love,**[b] **T. Mitani,**[g] **E. Mpochoridis,**[f] **S. Nikolaidis,**[f] **Y. Okumura,**[i] **J. Proudfoot,**[b] **S. A. Thayil,**[c] **L. Tompkins,**[c] **R. Wang,**[b] **R. Watari,**[g] **J. Webster,**[b] **K. Yorita**[g] **and J. Zhang**[b]

[a] *Northern Illinois University, DeKalb IL, United States of America*
[b] *High Energy Physics Division, Argonne National Laboratory, Argonne IL, United States of America*
[c] *Department of Physics, Stanford University, Stanford CA, United States of America*
[d] *DESY, Hamburg and Zeuthen, Germany*
[e] *Physikalisches Institut, Ruprecht-Karls-Universität Heidelberg, Heidelberg*
[f] *Aristotle University of Thessaloniki, Thessaloniki, Greece*
[g] *Waseda University, Tokyo, Japan*
[h] *University of Pisa and INFN, Pisa, Italy*
[i] *International Center for Elementary Particle Physics, The University of Tokyo, Tokyo, Japan*
E-mail: abolz@physi.uni-heidelberg.de

The ATLAS Fast TracKer (FTK) is a custom hardware system for fast, associative memory based track reconstruction. It will provide tracking information within the full acceptance of the inner tracking detectors to the High Level Trigger at a rate of up to 100 kHz. At the first stage of the FTK, the Data Formatter subsystem clusters inner detector hits and organizes them into 64 η-ϕ trigger regions. At the last stage, the FTK to HLT interface cards repackage track records and send them to the High Level Trigger computing farm. This report aims to give an overview over the functionality of the two systems, their hardware implementation in the Advanced Telecommunications Computing Architecture standard, and the status of their integration into ATLAS.

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*Speaker.

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1. Introduction

As an integral part of the upgrades to the ATLAS detector [1] trigger system for the ongoing LHC Run 2, the Fast TracKer [2] (FTK) will provide hardware based tracking at the trigger level. It is designed to reconstruct tracks above a transverse momentum threshold of 1 GeV in the full acceptance of the tracking detectors for all events accepted by the hardware based Level-1 Trigger (L1) at a rate of up to 100 kHz. The FTK tracks are then to be provided to the software based High Level Trigger (HLT) with a latency below 100 µs. Full tracking information is expected to boost the performance of many HLT algorithms, in particular for b-tagging and τ-identification. The ATLAS trigger layout is illustrated in Figure 1 (left).

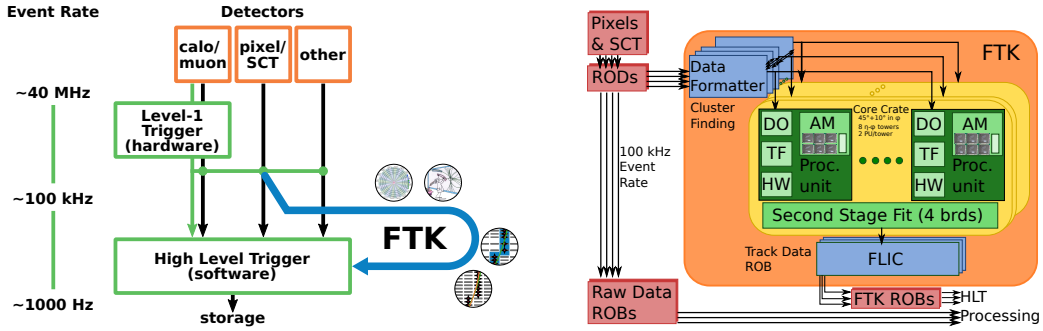

Figure 1: The figure shows (left) a diagram of the ATLAS trigger system and (right) the functional overview over the FTK. Right figure from [2].

FTK is a pipeline of dedicated, custom made hardware as illustrated in Figure 1 (right). It will process hits from the ATLAS inner detector, which is comprised of silicon strip (SCT) and pixel detectors (Pixel), including an new Insertable B-Layer (IBL), with roughly 100 million channels combined. To manage the large amount of data to be expected from the LHC, in particular under high instantaneous luminosity and induced high pile-up, in the short available time window, FTK is designed as a highly parallel system performing track finding in 4×16 η-ϕ regions simultaneously. These so-called "towers" overlap in order to reduce inefficiencies at their respective boundaries. Track finding is performed in two steps. First, to reduce the combinatoric problem, coarse hit patterns are compared to predefined possible patterns using fast associative memory [3]. Secondly, more precise track parameters are calculated in a linearised helix fit using the full resolution hits.

The amount of data to be processed and the parallel structure of the FTK impose strict requirements on the input data preparation. Output data must be merged into the ATLAS data stream and be easily accessible by the HLT. A brief overview over the FTK input and output subsystems is given in this report. Their respective functionality and their hardware and firmware is described in Section 2. The status of ongoing efforts to integrate the input and output subsystems into ATLAS is summarised in Section 3. A recent overview over the FTK tracking system is given in [4].

2. Input and Output Data Preparation

The design of the FTK input interface system is guided by data formatting requirements. Data from the SCT, Pixel, and IBL detectors are transmitted to the FTK's Data Formatters (DF). Incoming hits are clustered using a custom algorithm [5] with the simultaneous goals of reducing the

amount of data to be processed and improving the coordinate resolution. Cluster centroids are then used as "hits" by the downstream system. The DFs map the detector readout structure to the 64 FTK η-ϕ towers and distribute hits to the appropriate tracking engines. Special consideration is given to hits that fall into the overlap regions and need to be shared between multiple towers.

After tracks are reconstructed by the FTK tracking system, FTK event fragments containing hit and track information are re-formatted into the standard ATLAS event format at the last stage of the FTK. As the FTK uses its own coordinate system for hit clustering, local identifiers have to be converted to the global ATLAS identifiers before FTK events are passed on to the HLT.

2.1 Hardware and Firmware Implementation

The FTK input interface system is realised by 32 DF boards implementing the Advanced Telecommunications Computing Technologies (ATCA) standard. Two ATCA racks with two shelves host 8 boards per shelf, each. The combined system is controlled by means of a custom micro-controller installed on each board [6]. In particular these controllers also implement the functionality to download the board's firmware over Ethernet. Each DF board consists of 3 components: the ATCA front board, 4 Input Mezzanine (IM) cards and a Rear Transition Module (RTM). An example production board is shown in Figure 2 (left).

The IM cards are connected to the DF mother boards via an FMC connector. They receive raw hits from the tracking detector read out drivers (RODs) through 4 optical links per card. A total of 128 IMs are employed by the FTK input system establishing around 400 input links which process data at up to roughly 500 Gb/s. Clustering is performed by two Field Programmable Gate Arrays (FPGAs) directly on the IMs. Each FPGA is responsible for one strip and one pixel link. Two IM production versions exist that host two Artix-7 or two Spartan-6 FPGAs, respectively. As the IMs operate independently, event synchronisation has to be taken care of by the DF mother boards.

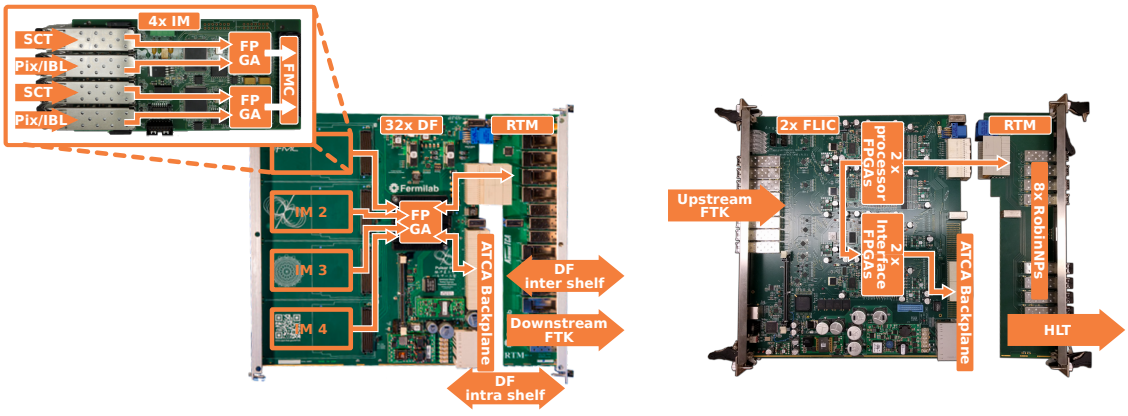

Figure 2: (Left) a DF production board including an IM card and the RTM and (right) a FLIC including the RTM. The main components of systems and the respective dataflow is illustrated on top of the pictures. Pictures provided by the FTK Collaboration.

The DF main boards contain a Virtex-7 FPGA on board, which is responsible for mapping the ATLAS inner detector structure onto the FTK towers, sharing hits in overlap regions and sending them to the downstream FTK tracking boards. Even after optimizing the input cabling, this requires

a large amount of real-time data sharing between the boards. High bandwidth, low latency data sharing within the ATCA shelves is achieved over the ATCA backplane. The Fabric Interface of the full mesh backplane allows for 6.25 Gb/s point-to-point communications between all slots. Further connectivity is provided by pluggable optical links through the RTM. These links are both used to connect DFs on different shelves, as well as to connect the DFs to the downstream FTK tracking system. In total, the DF system implements about 500 inter-board connections and 1000 output fibres. An illustration of the data flow through a DF board is given in Figure 2 (left).

The FTK output interface system is also ATCA based and consists of two FTK to HLT interface cards (FLICs). The cards are hosted independently from the DFs on a dedicated shelf and are both extended by an RTM card. Track and cluster information is received from the upstream FTK tracking system through 8 optical links per card at 2 Gb/s per link. Two Virtex-6 FPGAs per board process the incoming data. They convert the local FTK into global ATLAS identifiers and repackage the event records into the ATLAS event format. The event records are then sent to the HLT read out system via 8 optical links on each RTM. Two additional FPGAs exist on the FLICs that can provide monitoring functionality through the ATCA backplane.

3. System and Integration Status

Commissioning of the FTK has started in late 2015 with the goal to install the FTK hardware at the ATLAS experimental site and integrate the system into the ATLAS trigger and data acquisition. Since then, 16 DF production boards have been installed of which 4 are fully equipped with IM cards and 8 include the RTM. The remaining hardware is ready and awaits installation. In the meantime, the available system has been used for extensive dataflow tests using both real data from the ATLAS SCT, Pixel and IBL detectors, as well as simulated events. With some debugging still ongoing, the goal is to establish stable data flow of real ATLAS data from the IMs through the DFs to the downstream system, including data sharing between DFs, by the end of 2016. The two production FLIC boards have been installed. Sending FTK output data to the ATLAS data acquisition system has been demonstrated using simulated events.

Commissioning of the full FTK will be achieved in steps, where at first the system will reconstruct tracks in the barrel region only. It will then be gradually upgraded until it meets it's full design specifications in 2018.

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