Tile Rear Extension Module for the Phase-I Upgrade of the ATLAS L1Calo PreProcessor System

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ABSTRACT: After the Phase-I ATLAS upgrade the Tile calorimeter will have to provide its data via fast optical links to the new Feature Extractor (FEX) modules of the L1Calo trigger system. In order to provide the FEXes with digitised Tile data, new Tile Rear Extension (TREX) modules need to be developed and installed in the existing L1Calo PreProcessor system. The TREX modules are highly complex PCBs, with state-of-the-art FPGAs and high-speed optical transmitters working at rates up to 14 Gbps. The prototype design of TREX and first corresponding test results will be presented.

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Contents

1 Introduction

The ATLAS experiment [1] at the Large Hadron Collider (LHC) explores the vast variety of physics resulting from the collisions of proton bunches at a centre-of-mass energy of 13 TeV and an instantaneous luminosity of more than 10^{34} cm^{-2} s^{-1}. With about 10^8 readout channels, the ATLAS detector produces a few PBytes of raw data every second, a rate that cannot be sustained for mass storage even with the most recent technology. To overcome this, the ATLAS Trigger reduces the initial bunch-crossing rate of 40.08 MHz down to a more manageable storage rate of ~1 kHz, while efficiently retaining the interesting physics events in real-time.

The ATLAS Trigger achieves the reduction via two stages of successive event selection: Level-1 (L1) and High-Level Trigger (HLT). The L1 trigger is a hardware-based system, which uses coarse-granularity calorimeter data and dedicated muon chambers to reduce the 40.08 MHz bunch-crossing rate to 100 kHz. The HLT is software-based, running on large computer farms consisting of commercial hardware, and has access to the full-granularity calorimeter and muon detector data, as well as to the tracking data, to further reduce the event rate down to the storage rate of ~1 kHz.

The L1 trigger consists of four main subsystems: a Calorimeter Trigger (L1Calo), a Muon Trigger (L1Muon), a Topological Trigger Processor (L1Topo) and a Central Trigger Processor (CTP). The CTP combines the results of the other three subsystems to reach a final L1 trigger decision with respect to each event.

1.1 L1Calo Trigger System

The L1Calo trigger [2] is a pipelined system designed to identify high-pT objects in approximately 2 μs after the proton-proton collision has occurred, based on a coarse-granularity analogue input from the ATLAS Liquid Argon (LAr) and Tile Calorimeters. The analogue input signals, also referred to as trigger-tower signals, describe transverse energy (E_T) deposits in multiple calorimeter cells, having a typical granularity of 0.1×0.1 in pseudorapidity (η) and azimuthal angle (ϕ) coordinates.
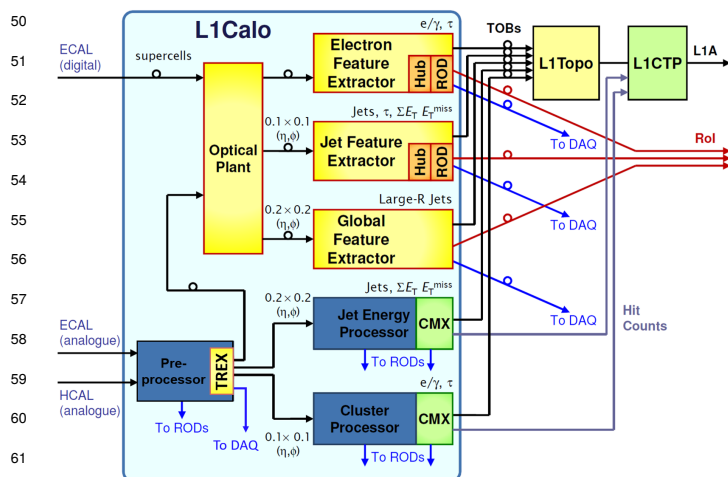
Figure 1. The architecture of the ATLAS L1Calo trigger system. Components shown in blue and green and the L1Topo are part of the current system, while the others shown in yellow and orange will be added during the Phase-I upgrade (modified from [3]).

L1Calo consists of three subsystems: the PreProcessor, the Cluster Processor (CP), and the Jet/Energy-Sum Processor (JEP) (see Figure 1). The PreProcessor receives, digitises and processes 7168 trigger-tower signals from the entire AT-LAS calorimetry, and transmits digital data, representing the E_T deposited for the identified bunch-crossing (BC), to the subsequent processors. The CP identifies isolated clusters of electrons, photons and taus, while the JEP identifies jets and computes global sums of total and missing E_T. Both the processor systems produce results in the form of Trigger Objects (TOBs), which describe the location, energy and type of identified physics objects. The TOBs are sent to the L1Topo, which receives similar information also from the L1Muon trigger. L1Topo forms combined trigger objects, based on the full event topology, and sends this information to the CTP, which also receives object multiplicities from the CP and JEP subsystems. Based on all of this information the CTP takes a final L1 trigger decision for each BC. If positive, then the CTP issues a Level-1 Accept (L1A) signal to all of the ATLAS sub-detectors and readout electronics. Upon the reception of the L1A, all of the L1Calo subsystems transmit event related data to the ATLAS Data Acquisition (DAQ) system. The CP and JEP simmultaneously produce Region-of-Interest (RoI) information that describes the η-ϕ coordinates of the detector regions where the interesting physics signatures have been identified and send it to the HLT.

1.2 L1Calo Phase-I Upgrade

After 2018 the LHC plans to increase the current instantaneous luminosity by a factor of two, in order to enhance the physics discovery potential. For the ATLAS trigger, the luminosity upgrade will lead to higher event rates and harsher pile-up conditions. In order to maintain a high efficiency of the event selection, L1Calo will be extended during the Phase-I upgrade (2019-20) with three subsystems: the electromagnetic Feature Extractor (eFEX), the jet Feature Extractor (jFEX) and the global Feature Extractor (gFEX) [3] (see Figure 1). The eFEX and jFEX will perform similar investigations to CP and JEP, but with more efficient and sophisticated algorithms, while the gFEX will identify large jet objects. The input to the FEX processors will be entirely digital. New dedicated LAr Calorimeter electronics will directly provide digital trigger data via optical fibres. Also, the digital input from the LAr Calorimeter will be of finer granularity than the similar analogue input, i.e. ten super-cells per trigger-tower, in order to help L1Calo improve the event selection. The Tile Calorimeter will continue to send analogue trigger-tower signals to the PreProcessor until the Phase-II upgrade (2023-25) is implemented. In order to also provide the FEX processors with

Tile digitised results, new digital modules, called Tile Rear Extension (TREX), will be developed and installed in the PreProcessor system. The main task of each TREX will be to extract copies of the Tile digitised results from the legacy trigger data path and transmit them optically to the FEXes. The functionality of the TREX module is presented in detail in section 3.

After the performance of the new FEX processors has been validated, the part of the Pre-Processor system that digitises and processes analogue signals from the LAr Calorimeter, and the entire CP and JEP subsystems will be decommissioned and dismantled. The remaining part of the PreProcessor system, including the TREX modules, will be kept in operation until the Phase-II upgrade, when it will be replaced by a dedicated Tile digital pre-processing system.

2 The PreProcessor

The PreProcessor is a highly modular system consisting of 124 hardware-identical PreProcessor Modules (PPMs), which are organised into eight 9U VME crates. The modules in two crates process analogue trigger-tower signals from the Tile Calorimeter, while the other modules process signals from the LAr Calorimeter. Apart from PPMs, each crate is equipped with a 'Timing Control Module' (TCM) that distributes over the VME backplane information from the 'Timing, Trigger and Control' (TTC) system (e.g. 40.08 MHz bunch-crossing clock, L1A signal from CTP, etc.), and a single board computer, acting as VME controller, for the purpose of setting up, controlling and monitoring the operation of the PPMs.
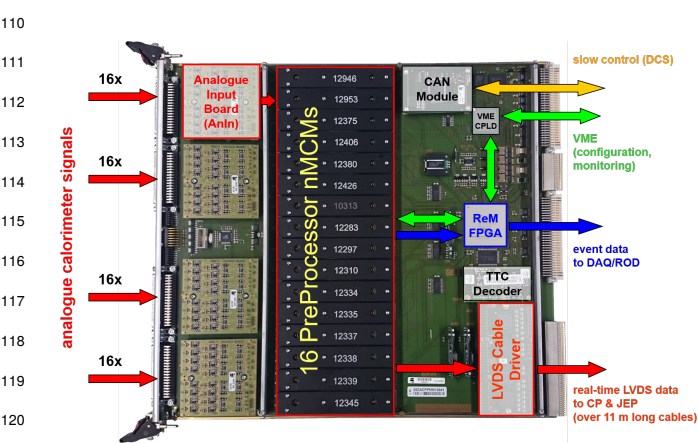

Figure 2. The PreProcessor Module.

Each PPM is designed to receive and process 64 analogue signals and carries 23 daughter cards and several programmable devices (see Figure 2). The analogue signals are received in differential form through the front-panel, and have amplitudes up to 2.5 V that correspond to an E_T deposition range of 0-256 GeV. Four 16-channel Analogue Input (AnIn) boards convert the differential signals to single-ended form, and apply a fixed gain and a programmable pedestal to match the signals into the 1 V digitisation window.

The main signal processing takes place on 16 four-channel Multi-Chip Modules (MCMs). These were upgraded to new MCMs (nMCMs) during the first LHC long shutdown (2013-14), to improve the performance of the trigger algorithms at high pile-up levels [3] [4]. On each nMCM, the analogue signals are first digitised with 10-bit resolution at 80 MHz (double the LHC bunch-crossing frequency). The resulting digital streams are then routed to a Field Programmable Gate Array (FPGA) device, which performs the trigger-specific tasks:

- synchronisation of pulses originating from the same collision, to correct for the different time-of-flight of the particles from the interaction point to the calorimeter and for the different path-lengths of the signals from the calorimeter to the PPM input;

- BC-wise, dynamic pedestal correction for each trigger channel to suppress the physics pile-up effects.

- identification of the E_T deposits per trigger channel and of the corresponding BC in time (Finite-Impulse-Response Filter and PeakFinder for pulses in linear range, dedicated algorithms for saturated pulses);

- separate noise suppression, pedestal subtraction and fine-calibration of the extracted E_T values for each destination processor (CP, JEP). The calibrated E_T values are 8 bits wide, with a resolution of 1 GeV per count.

- multiplexing into one serial stream of the 8-bit E_T results from two trigger channels adjacent in ϕ, to halve the number of links to CP (BC multiplexing);

- pre-summing of the four 8-bit calibrated E_T values into a 9-bit 0.2×0.2 jet element for the JEP, to reduce the number of links between the two systems.

The digital E_T results are sent in real-time from the nMCMs to the L1Calo processors as Low-Voltage Differential Signaling (LVDS) signals, at a rate of 480 Mbit/s. The transmission is realised via an LVDS Cable Driver (LCD) daughter card and 11 m long parallel pair cables connected to the rear side of the PPM.

In order to allow the verification of the L1 trigger decision, the PPM provides raw digital values and E_T results related to accepted events to the DAQ system. The event data is continuously accumulated in pipeline memories on the nMCMs. Upon the receipt of an L1A from the CTP, the event data are first collected and formatted by an on-board Readout Manager (ReM) FPGA, then they are presented to a Rear G-Link Transmitter Module (RGTM), mounted on the back side of the crate, and finally they are sent to the DAQ via an external Readout Driver (ROD) module. The L1A signal and all the other TTC protocol signals are decoded by a 'TTC Decoder' daughter card and distributed on the board by the ReM FPGA.

The configuration and control of the PPM are realised via a standard VME interface. The data transfer between the VME controller and the on-board programmable locations is handled by a Complex Programmable Logic Device (CPLD) and the ReM FPGA. The latter device also has the task to collect and provide monitoring data to VME. The operating conditions of the PPM are permanently monitored by the ATLAS Detector Control System (DCS). A Fujitsu micro-controller collects information about the temperatures and voltages on the board, and sends it to the DCS via a CAN-bus interface on the backplane and the TCM module in the crate.

3 Tile Rear Extension Module

After the Phase-I upgrade the Tile Calorimeter will send analogue trigger-tower signals to the PreProccessor system. In order to also supply the FEXes with digital trigger data from the Tile Calorimeter, TREX modules will be developed and installed in the two PreProcessor crates that digitise and process Tile analogue signals, to extract copies of the real-time pre-processing results from the legacy trigger data path, and transmit them optically to the FEXes. The following sections present the functionality of the TREX and the development of the prototype module.
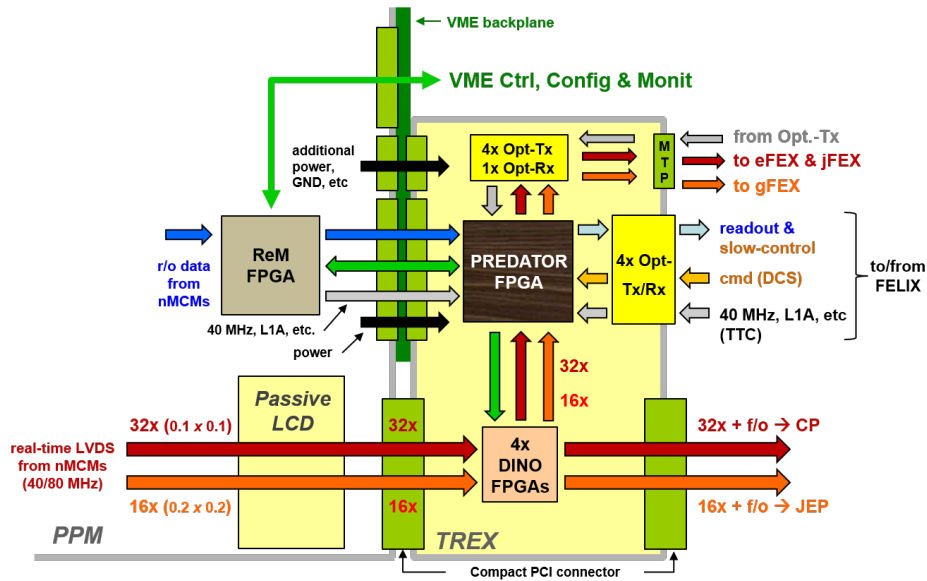
Figure 3. Schematic representation of the TREX functionality.

3.1 Functionality

The TREX will be a rear transition module in the PreProcessor VME crate, acting as a physical extension of the PPM in the corresponding crate slot (see Figure 3). The PPM real-time data path will be extended to the TREX, to facilitate the extraction of signal copies for the FEX processors. The cable driver functionality, currently implemented on the LCD card, will be re-located to the TREX, to provide continuity in the trigger operation.

The real-time input from the PPM consists of 48 LVDS data streams, where 32 of them transport 8-bit 0.1×0.1 E_T results for the CP, while the other 16 provide 9-bit 0.2×0.2 jet sums for the JEP. Four 'Data In-Out' (DINO) FPGAs on the TREX will receive the LVDS signals and produce an appropriate number of copies for the CP, JEP and FEX processors. The signal copies for the CP and JEP will be sent via the existing 11m long electrical cables to the respective processor systems, while the copies for the FEXes will be routed on the board to another FPGA, called the 'PreProcessor Data Collector' (PREDATOR). On the PREDATOR, the input LVDS signals will first be de-serialised, and then the resulting parallel data will be replicated and formatted as required by each destination FEX. The eFEX and gFEX processors require only 0.1×0.1 E_T values and 0.2×0.2 jet sums respectively, while the jFEX requires both data sets. The data will then be serialised and sent to the FEXes, using up to 48 high-speed optical links. The baseline rate for these links has been established by the L1Calo and LAr groups to 11.2 Gbps, but other choices, like 9.6 Gbps or 12.8 Gbps, have been kept as possible alternatives.

Once the performance of the FEX processors has been validated during the commissioning phase, and the CP and JEP subsystems have been decommissioned, the PPM can be configured to double the output data rate on the real-time path, i.e. to 960 Mbit/s. This operational mode will permit either the BC-multiplexing of the 0.1×0.1 E_T results to be removed or additional information to TREX to be sent, if needed. In order to enable this mode, a rework of the LCD daughter card

is required. The current LCD card, which was designed more than a decade ago, is based on old generation FPGAs that cannot cope with the higher rate. The new LCD design will be simplified to include only passive components, and the functionality of the card will be reduced to route only the LVDS signals to the PPM output connector.

The TREX also will have the task of collecting, formatting and transfering the PPM event data to the DAQ system. In the current configuration of the PreProcessor, the event data is collected and formatted by the ReM FPGA, and sent to the DAQ via the rear-mounted RGTM card and an external ROD module. In the Phase-I configuration, the RGTM card has to be removed, to insert the TREX, and the data collecting and data formatting tasks will be re-located from the ReM FPGA to the PREDATOR FPGA. The transfer of event data from TREX to DAQ will be then realised via one optical link running at 9.6 Gbps and a Front-End Link Exchange (FELIX) device [5]. The TREX will also interface to FELIX to transfer local slow-control data to DCS, and to receive protocol signals from the TTC and specific commands from DCS. The slow-control data will be collected by the PREDATOR FPGA from various on-board locations and transferred to FELIX together with the event data via the same optical link. The information from TTC and DCS will be received and decoded by the same PREDATOR FPGA via a separate multi-Gb/s link.

For configuration, control and monitoring purposes the TREX will be connected to the VME controller via the PPM. The communication will be realised using a custom parallel interface between the ReM and the PREDATOR FPGA.

For testing and diagnostic purposes, the TREX also will have the capability to receive and analyse data from up to 12 high-speed optical links. This operational mode is mostly intended for the prototype module, to allow verifications of the high-speed transmissions in standalone mode; it may be removed in future hardware iterations.

3.2 Prototype Module

The TREX prototype module is currently being developed at the 'Kirchhoff Institute for Physics' (KIP) Heidelberg. The design is based on the most recent PCB design technologies, FPGA devices and high-speed optical transmitters. The prototype module will be an 18-layer PCB with a standard 9U VME height of 366 mm and a width of 150 mm (see Figure 4).
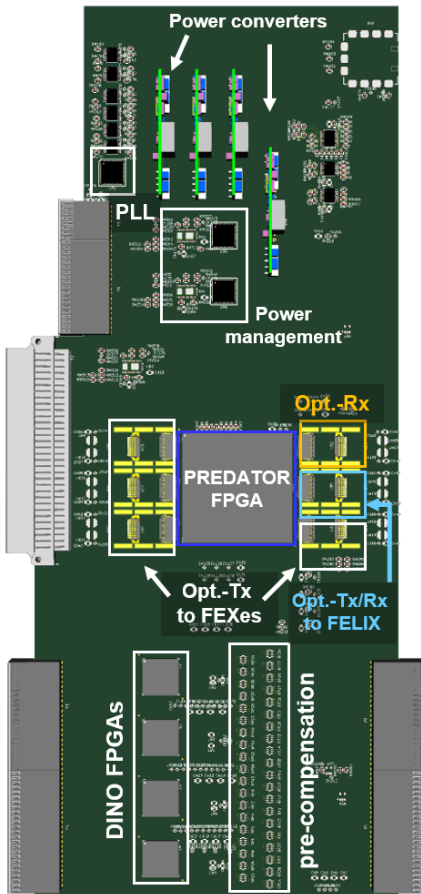
The four DINO FPGAs will be implemented using Xilinx Artix-7 35T devices [6]. The two dominant factors that have motivated this choice were the small form factor ($15 \times 15 mm^2$) and the small input-to-output routing delay obtained after placing and routing the firmware designs (i.e. less than 10 ns). The LVDS signals are received from the PPM and sent to the CP and JEP through identical Compact PCI connectors. The mapping of the signals on the output connector will be identical to that currently implemented on the PPM, to ensure a full replication of the legacy system. Also, the inherent signal losses due to transmission over long parallel pair cables will be pre-compensated in the same way as currently done on the LCD card.

The PREDATOR FPGA will be a Xilinx Kintex UltraScale KU115 device [7]. The FPGA features 64 GTH Gigabit transceivers, that support data rates up to 16.3 Gbit/s, and a sufficiently large number of additional internal resources (BRAMs, DSPs, FFs, LUTs, etc.) to implement all the functionality foreseen for this device.

The optical transmission and reception will be realised with Samtec FireFly devices [8]. Four 12-channel FireFly transmitters will be used to transfer the digitised Tile trigger data to the FEX

processors, while one 12-channel FireFly receiver will serve for testing the optical transmission for diagnostic purposes. An additional 4-channel FireFly duplex transceiver will be used to implement the bi-directional communication with the FELIX devices. All FireFly optical transceivers are 7 mm high and can handle data rates up to 14 Gbps/channel at low power consumption (maximum 3.6 W per transceiver pair in an operating range from $0°C$ to $70°C$). The height of the transceivers is an important parameter, as the effective available space between two neighbouring TREX PCBs will be only 16 mm.

Figure 4. Front side of the TREX prototype module (3D layout view).

In future hardware iterations of the module, the 12-channel optical receiver, used for diagnostic purposes in standalone mode, may be removed. Consequently, a smaller Kintex UltraScale device (KU085) may be used for the the PREDATOR FPGA. The smaller FPGA will have the same package as the larger device, to minimise modifications in the board design, and will feature only 56 GTH Gigabit transceivers that can support the same maximum data rate of 16.3 Gbps.

The prototype design also includes a 10-channel PLL to generate low-jitter clock signals for the multi-Gb/s transmission. The reference clock will be either the BC clock pulse received via FELIX or the same signal received via the legacy TTC system and the PPM. A jitter-clean version of the input clock will be then distributed to both the PPM and the TREX. The PLL chip also will have the task to supply the TREX and the PPM with 40.08 MHz based clock signals in the absence of the TTC system, i.e. in the laboratory environment.

The various power supply values needed by the devices on the board are derived from two inputs, i.e. +5V and +3.3V. The +5V input supply will be received from the PPM, while the +3.3V will be received via one of the backplane connectors. Two programmable power managers will accurately monitor the input supplies and the on-board voltages, and take appropriate measures in case of detected misbehaviours. Also, the power management on the TREX is coupled to the hot-swap mechanism available on the PPM, to power on and off the module at the same time as the front PPM. A fully equipped crate, in the current configuration of the PreProcessor system, consumes ~47% of the total power budget. With 16 TREX prototype modules, the power consumption in the crate is expected to increase to ~85%.
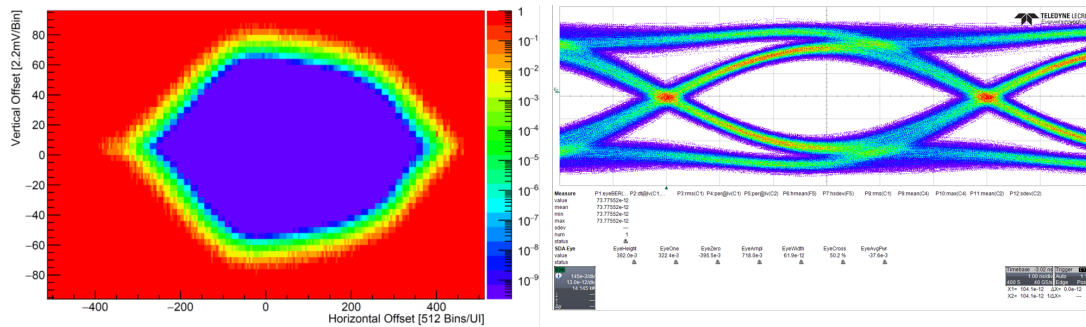
The high-speed serialisation and transmission has been successfully tested with a Kintex Ultra-Scale based development board (XCKU040), using SFP+ optical transceivers (up to 10.125 Gbps) and in loopback mode (electrical transmission over the PCB, up to 12.8 Gpbs). In both cases, the observed bit error rate (BER) was smaller than 10^{-13}. The quality of the data links can be observed in Figure 5.

Figure 5. Gigabit BER test results with Kintex UltraScale based development board. The test results were recorded using Xilinx integrated statistical eye tools (*left*) and oscilloscope (*right*).

4 Outlook

The TREX modules will provide digital Tile trigger data from the PreProcessor to the L1Calo FEX processors. A TREX prototype module is currently under development. The main challenge of the design is to integrate a high density of components while maintaining the signal integrity required to achieve a sufficiently low bit error rate on the Gigabit links. The TREX prototype board will be manufactured in the last quarter of 2016. Intensive and thorough testing, together with the FEX processors and the FELIX devices, will be carried out at CERN during 2017. The final TREX modules will be installed at CERN, in the electronics cavern of the ATLAS experiment, during 2018-19, upon the successful completion of all design and production procedures.

Acknowledgments

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