

Timing distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

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Abstract– The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment at the Large Hadron Collider (LHC). The upgraded High Luminosity LHC will deliver five times the current nominal instantaneous luminosity. The ATLAS Phase II upgrade will upgrade the readout electronics of the TileCal for the HL-LHC. The majority of the front- and back- end electronics will be redesigned with a new read out strategy.

In the upgraded read out architecture for Phase II, the front-end electronics consist of the Front-End Boards, MainBoards and the DaughterBoards. The MainBoard digitizes the analog signals coming from the Front-End Boards (FEBs) connected to the PhotoMultiplier Tubes (PMTs), provides integrated data for minimum bias monitoring and includes electronics for PMT calibration. Three different FEB options with different signal acquisition strategies are under study: new 3-in-1 cards, QIE4 chip and FATALIC chip. The DaughterBoard receives and distributes Detector Control System commands, clock and timing commands to the rest of the elements of the front-end electronics as well as collects and transmits the digitized data to the back-end electronics at the LHC frequency (~25 ns).

In the back-end electronics, the TileCal PreProcessor (TilePPr) receives and stores the digitized data from the DaughterBoards in pipeline memories to cope with the latencies and rates specified in the new ATLAS DAQ architecture. The TilePPr interfaces between the data acquisition, trigger and control systems and the front-end electronics. In addition, the TilePPr distributes the clock and timing commands to the front-end electronics for synchronization with the LHC clock.

I. INTRODUCTION

THE Tile Calorimeter (TileCal) [1] is the hadronic calorimeter of the ATLAS [2] experiment at the Large Hadron Collider (LHC) at CERN. TileCal is a sampling detector using steel plates as absorber and plastic scintillator tiles as active material; it covers the central part of the ATLAS experiment. This detector is divided into four sections along the beam direction, each of which is segmented azimuthally into 64 modules (Figure 1a). The Photomultiplier Tubes (PMTs) and the front-end electronics are located in mechanical structures called “drawers”, placed in the outermost part of the modules (Figure 1b). The complete readout of the TileCal cells comprises a total of 9852 PMTs.

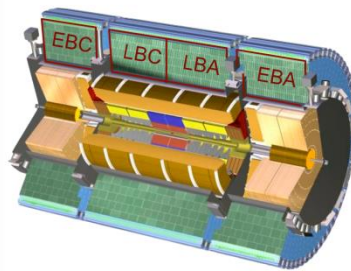


Fig. 1a. Tile Calorimeter detector.

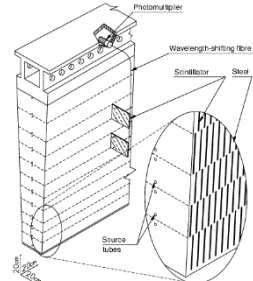


Fig. 1b. Tile Calorimeter module.

II. CURRENT READOUT ARCHITECTURE

In the present front-end electronics, the analog signals produced by PMTs are conditioned and amplified in the 3-in-1 cards with two gains, and digitized by the Digitizer chips at the LHC frequency. The digitized data are stored in pipelined memories in the Digitizers until the reception of a Level-1 trigger acceptance signal (L1A). When an L1A signal is received, the Interface board collects the selected events and sends them to the Readout Drivers (RODs) [3] in the back-end electronics through a dedicated optical link. RODs are responsible of processing the incoming data at a maximum average rate of 100 kHz.

Parallel to this process, the analog signals coming from the 3-in-1 cards are analog summed in towers every bunch crossing and transmitted to the Level 1 Calorimeter trigger system (L1Calo) for the selection of potentially interesting events. Figure 2 shows the data flow of the TileCal architecture.

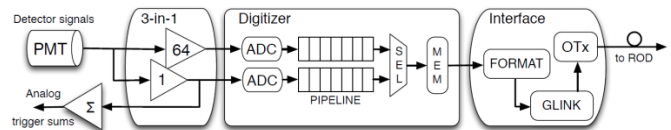
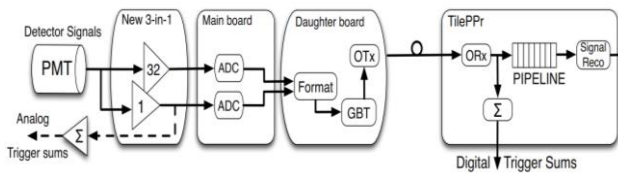


Fig. 2. Diagram of the current readout architecture of the Tile Calorimeter.

67 After the ATLAS Phase II Upgrade [4] in 2024, the High
68 Luminosity LHC (HL-LHC) will deliver a nominal
69 instantaneous luminosity of $5\text{-}7\cdot 10^{34}\text{ cm}^{-2}\text{s}^{-1}$ with a pileup
70 close to 200 events per bunch crossing providing a total
71 integrated luminosity of 3000 fb^{-1} in ten years.

72 The Phase II Upgrade requirements make necessary a full
73 redesign and replacement of the readout architecture and
74 trigger systems to improve the event selections and cope with
75 the new radiation levels, latency and high data rates.

76 Figure 3 shows a diagram of the readout architecture for the
77 ATLAS Tile Calorimeter Phase II Upgrade. The new readout
78 architecture requires a fully digital trigger system where the
79 front-end electronics will transmit all the digitized samples
80 the Tile PreProcessors (TilePPr) in the back-end electronics at
81 the LHC frequency.



83 Figure 3. Diagram of the TileCal Phase-II Upgrade readout electronics.

84 Table 1 shows a comparison between the data bandwidth
85 requirements for the current readout system and for the Phase
86 II Upgrade readout system.

88 TABLE I. TILE CALORIMETER READOUT FEATURES COMPARISON

89	Current	Phase II Upgrade	142
90 Total BW	~205 Gbps	~40 Tbps	144
91 N. fibers	256	8192	145
92 BW/module	800 Mbps	160 Gbps	146
93 Nb. boards	32	32	147
94 Nb. crates	4 (VME)	4 (ATCA)	148
95 In BW/board	6.4 Gbps	1.28 Tbps	149
96 Out BW/board _{DAQ}	2.56 Gbps	40 Gbps	150
97 Out BW/board _{L1/L0}	Analog	500 Gbps	151

98 IV. THE TILE CALORIMETER DEMONSTRATOR PROJECT 152

99 The Demonstrator Project aims to evaluate and qualify the
100 proposed readout architecture before its full replacement
101 during the Long Shutdown 3 (2024--2027). As part of the
102 Demonstrator activities the new system is being validated
103 several Test Beam campaigns at CERN during 2015 and 2016.
104 It is hoped that at the end of 2016 a complete TileCal module
105 with the upgraded electronics will be inserted in the ATLAS
106 detector.

107 The Demonstrator module comprises on a single frame, the
108 front-end upgraded electronics needed for the digitization of
109 signals coming from the PMTs, the calibration circuitry and
110 high speed data communication with the back-end electronics,
111 and the electronics needed for the distribution and monitoring
112 of high voltage to the PMTs. Since the full digital trigger
113 system will not be present until Phase II, the Demonstrator
114 module will also provide analog trigger signals to the current
115 L1Calo system.

A. Front-end boards

Three different FEB options are being evaluated for the
ATLAS Phase II Upgrade. The first FEB option is an
improved version of the current 3-in-1 card [5] used in TileCal.
This FEB has been designed using Commercial Off-The-Shelf
components and provides analog outputs with two different
gains, as well as calibration capabilities for PMTs. The new 3-
in-1 card shows better linearity and lower noise and has
passed successfully the radiation certification. The modified 3-
in-1 card has been chosen as FEB for the Demonstrator
module, since it is the only FEB providing analog outputs
required for the current trigger system.

The second option is a custom ASIC called Charge
Integrator and Encoder (QIE) [6]. This ASIC divides the
signal coming from the PMTs with a current splitter followed
by a gated integrator providing four different ranges (16/23,
4/23, 2/23, 1/23). In the same chip, a 6-bit flash ADC digitizes
the selected range covering a dynamic range of 17 bits.

The third option for the FEB is a mixed ASIC called Front-
end for ATLAS TileCal Integrated Circuit (FATALIC) [7].
FATALIC includes analog and digital processing blocks. A
current conveyor connected to three shaping stages with
different gains covers the full dynamic range of the PMT
signal. The conditioned signals are digitized using three 12-bit
ADCs also present in the ASIC, and stored in a pipelined
memory. A digital processing block performs the auto-
selection between low- and high-gain data and transmits the
auto-selected and the medium gain data through a high speed
serial link.

B. Main Board

The Main Board interfaces the Daughter Board and the
FEBs. It is responsible for the control, monitoring and readout
of the FEBs.

TileCal modules will include four Main Boards, where one
Main Board will host and manage up to 12 FEBs. Three
different types of Main Board will be designed in order to
accommodate the three FEB options.

A Main Board capable to accommodate and operate up to
12 new 3-in-1 cards has been designed for the Demonstrator
module. This board includes four Altera Cyclone IV FPGAs to
control and to configure the FEBs, while 12-bit ADCs digitize
the analog shaped signals coming from the new 3-in-1 cards.

Each half of the Main Board is powered with a separate low
voltage power supply, where power connections from one half
are diode-ORED with the other half. Figure 4 shows a picture
of the Main Board prototype for the Demonstrator.

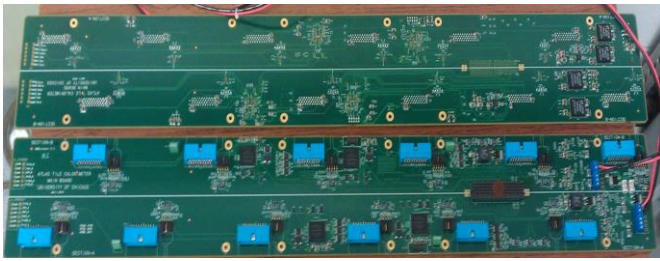


Fig. 4. Photograph of the Main Board.

C. Daughter Board

The Daughter Board [8] is the interface between the front- and back-end electronics. The Daughter Board receives and deserializes low- and high- gain data samples from the 12 FEBs connected to the Main Board at the LHC frequency. Data sampled is packed and transmitted to the back-end electronics using redundant high speed links at data rates of 9.6 Gbps.

The Daughter Board used in the Demonstrator includes two Xilinx Kintex 7 FPGAs, two Quad Small Form-factor Pluggable (QSFP) optical modules, two GBTx [9] chips and an FPGA Mezzanine Connector (FMC) for the communication with the Main Board. Figure 5 shows a picture of the Daughter Board version 4.



Fig. 5. Photograph of the DaughterBoard version 4.

VI. UPGRADED BACK-END ELECTRONICS

The TilePPr will be the main component of the back-end electronics after the ATLAS Phase II Upgrade. This module will provide a high speed link for the readout, operation and monitoring of the front-end electronics. Moreover, the TilePPr will send calibrated information to the ATLAS trigger systems with improved granularity and precision.

High speed links will distribute the Trigger, Timing and Control (TTC) information and the Detector Control System (DCS) commands towards the TileCal front-end electronics.

The TilePPr will be designed in an ATCA [10] form factor, where each TilePPr will manage up to eight TileCal modules, each one containing up to 48 PMTs. A total of 32 TilePPr will be required for the complete readout of the TileCal detector.

A Rear Transition Module (RTM) called TDAQ-I, will interface the TilePPr with the ATLAS trigger and data acquisition (TDAQ) readout system.

The TDAQ-I will receive event data from the TilePPr every bunch crossing and will transmit preprocessed trigger information to the calorimeter and muon trigger systems at the LHC frequency.

For every bunch crossing, the TilePPr boards will receive, decode and store event data in circular pipeline memories, until the reception of a trigger acceptance

signal. The selected data will be transmitted to the Front End Link eXchange [11] (FELIX) system, for proper event data decoding and transmission to the next trigger level.

Figure 6 shows a preliminary diagram of the TilePPr for Phase II Upgrade.

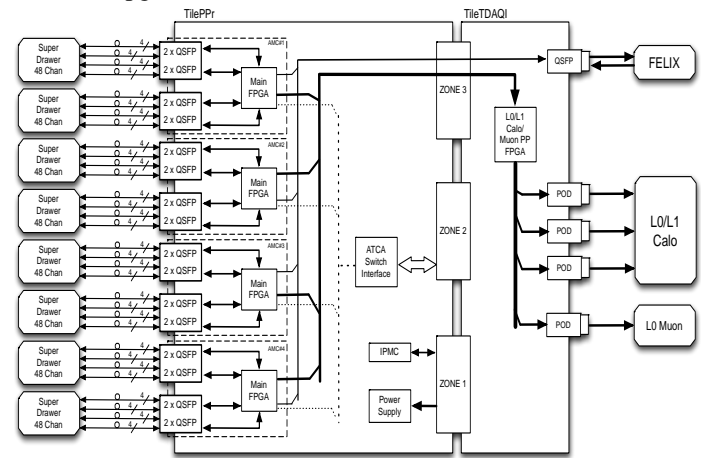


Fig. 6. Diagram of the TilePPr for Phase II Upgrade.

A. The TilePPr prototype

The TilePPr prototype [12] has been designed and produced in the framework of the Demonstrator project. The TilePPr demonstrator is responsible for the reception, processing of the digital data coming from the Demonstrator module, as well as for the distribution to the front-end electronics of TTC data for synchronization with the LHC clock. It represents one eighth of the final TilePPr board.

The TilePPr prototype has been designed as a double mid-size Advanced Mezzanine Card (AMC) and is populated with 4 QSFPs connected to the Virtex 7 FPGA and jitter cleaners. Figure 7 shows a picture of the TilePPr demonstrator.



Fig. 7. Photograph of the TilePPr prototype.

The high speed communication path between the front-end and back-end electronics is implemented through 16 GigaBit Transceiver (GBT) [13] links at 4.8 Gbps for the downlink (TilePPr to front-end electronics) and 9.6 Gbps for the uplink (front-end electronics to TilePPr).

The downlink is used to send DCS and TTC commands at the standard data rate of the GBT protocol (4.8 Gbps) with Forward Error Correction (FEC). Each DaughterBoard receives 4 GBT links, with one link connected to a GBTx chip

236 for clock recovery and remote configuration and the other
237 three links connected to the Kintex 7 FPGAs for command
238 reception and clock distribution to the MainBoard.

239 In the uplink, the GBT firmware has been adapted
240 operate at 9.6 Gbps in order to have enough data bandwidth
241 read out all the channels of the Demonstrator module every
242 bunch crossing. The received data is stored in pipeline
243 memories upon the reception of a L1A when the data is
244 packed and transmitted to the FELIX prototype system and
245 the present RODs, thus providing compatibility between the
246 current architecture and the Demonstrator module.

247 In order to achieve synchronous communication between
248 the front-end and the back-end electronics at the LHC
249 frequency, the TilePPr recovers the LHC clock from the TBC
250 stream and cleans it with a jitter cleaner reducing the jitter
251 levels up to the required values for error-free data
252 transmission.

253 VII. CONCLUSIONS

254 A new readout architecture with a fully digital trigger will
255 be implemented to fulfill the new requirements of the HL-LHC
256 LHC during the ATLAS Phase II Upgrade. The increase of the
257 radiation levels and the larger data bandwidth implies the
258 complete redesign of the front-end and back-end electronics
259 of the TileCal.

260 This contribution shows a description of the data flow and
261 timing distribution in the new read out architecture for the
262 TileCal Phase II Upgrade and presents the status of the

hardware and firmware developments of the upgraded front-
end and back-end electronics.

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