fig EHS

P. Meinke

CERN/EF/EHS/TE 78-2
14 February 1978

TESTS OF THE VIENNA DRIFT CHAMBER ELECTRONICS

N. Bosco, Ch. Ljuslin, G. Neuhofer, M. Pernicka, H. Stradner

1. DESCRIPTION OF THE MODULES

1.1 Clock-module and Converter Module

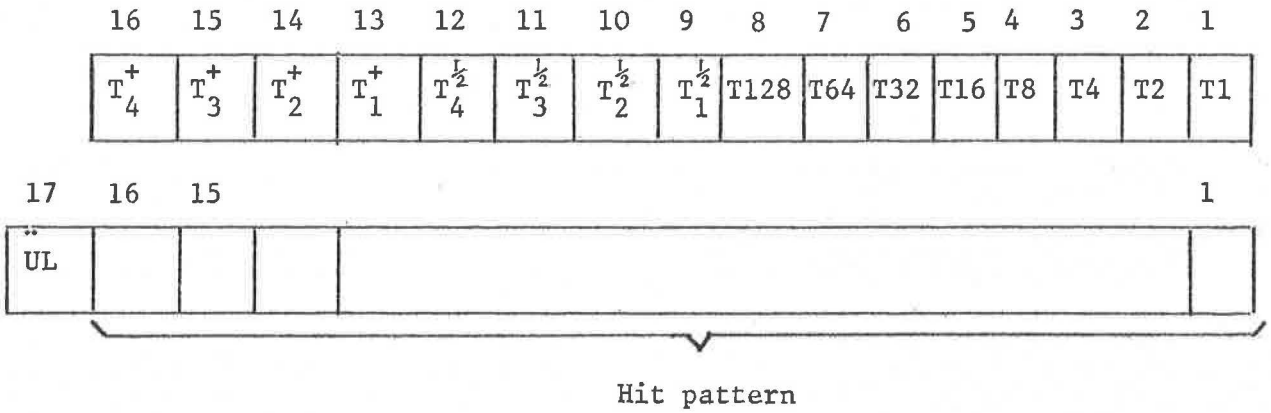
These are already described in note CERN/EF/EHS/TE 77-5.

1.2 Clock-stop-module (CSM)

This module, from the performance and the logic point of view, is unchanged, but the clock distribution has been moved to the crate-controller.

1.3 Drift-time-module (DTM)

This is a single slot CAMAC module with card-edge connector, 16 inputs, 1 clock input and external test input. A block diagram is shown in Fig. 1. The module allows one to measure drift times up to ~ 1.5 µs with a bin width of 3 ns. The major difference compared to the prototype module is that the number of interpolators and correction bits have been increased. Four adjacent inputs share one interpolator. This is a major improvement for multihit events. The memory is 33 bits wide and 16 words deep.
The words read out have the following format :



16 bits are used for the hit pattern and 8 bits for the coarse time measurement. There are 4 $T^{\frac{1}{2}}$ bits which are the measurements of the 4 interpolators and there are 4 T + bits which indicate when two hits in one interpolator were close together. They are used as correction bits. There is also 1 bit $\ddot{U}L$ (overflow) which acts as a time out bit.

1.4 Controller

The controller conforms to CAMAC standards. Seen from the CAMAC branch highway, it looks like a normal CAMAC-crate-controller. It serves also for clock-distribution. It accepts the following CAMAC commands: Start, Stop, Reset, Set, read $\ddot{U}L$-pattern

2. SET-UP

The set-up (Fig. 2) of the test is the following: all modules are located in a modified CAMAC crate, which is connected to the computer via the controller.

A test-cycle is started with a computer-generated signal SA and stopped with the coincidence signal of SB and the random source (switches A and C closed) or with a signal from the random source alone. Signal SB arrives about 2 ms after SA. The output of this coincidence acts also as an event generator for the DTM.

3. RUNNING UP

No discrepancies between write-up and hardware were observed, but the controller generated non-standard BTB signals.

4. TEST RESULTS OF THE CLOCK-STOP-MODULE (CSM)

4.1 Test of the Interpolator

The CSM was started via the computer and after some delay stopped randomly. The last 3 bits of the time-counter were histogrammed (Fig. 3).

The distribution should be flat in an ideal case. The maximum deviation from the expected 750 ps is about 200 ps. No further timing tests were done.

4.2 Thermal Stability

The pattern reproduced within statistics even after a long power off.

5. TEST RESULTS OF THE DRIFT-TIME-MODULE (DTM)

5.1 Maximum Input Rate

Data were lost only at input frequencies higher than 100 MHz !!

5.2 Cross-talk Test

All, except one channel, were fired at the same time. In 5000 events the open channels showed no hits. Only channels 5 and 6 showed some 0.3% cross-talk.

5.3 Interpolator Test

The least significant bit of each channel was histogrammed. Two typical cases are shown in Fig. 4. Interpolators 1 and 4 were not very well tuned.

5.4 Time Resolution

The time difference between the pulse to the DTM and the stop-pulse is constant, but the pulses arrive at random with respect to the clock pulses. The value "Stop-time - Drift-time" was histogrammed (Fig. 5): the bin-width is 0.75 nsec. The expected theoretical distribution should be 5 bins wide. The measured distribution shows a full width of 5 to 6 bins, which means there are nowhere essential jitters in the circuitry.

5.5 The "3 - 9 nsec Problem

The electronics set-up is shown in Fig. 2. 7 series of measurements have been performed in the following way:

(a) ΔT_2 delay was set such that one just saw an even number for the drift-time, which means one had just crossed the edge of the clock-pulse,

(b) ΔT_3 was set to the same value and then stepped up by 1 ns increments, the time difference between input A and B was registered. After 20 - 25 increments →

(c) ΔT_2 was incremented by 1 ns. Point 2 was repeated; after 7 series one is sure that one has covered the range of a full clock-pulse.

The results are given in the following table which shows the measured time differences in ns.

$\Delta T_3 - \Delta T_2$ [ns]	ΔT_2 [ns] 0	1	2	3	4	5	6
0	0	0	0	0	0	0	0
1	0	0	0	0	0	9+	0
2	0	0	0	0	9+	|	0
3	0	0	9+	9+	|	|	0
4	0	0	|	|	|	|	0
5	0	12+	|	|	|	9+	0
6	12+	|	|	|	9+	9	12+
7	|	|	9+	9+	9	|	|
8	|	12+	9	9	|	9	|
9	|	12	|	|	|	12	12+
10	12+	|	|	|	9	|	12
11	12	|	9	9	12	|	|
12	|	12	12	12	|	|	|

The symbol + indicates that the T^+ bit was on. One has to correct these values by 6 nsec.

5.6 Hang-up Test

The system was started and stopped within a short time interval (100 ns) with a repetition rate of ~ 2 s. No hang-ups were observed.

6. CONCLUSIONS

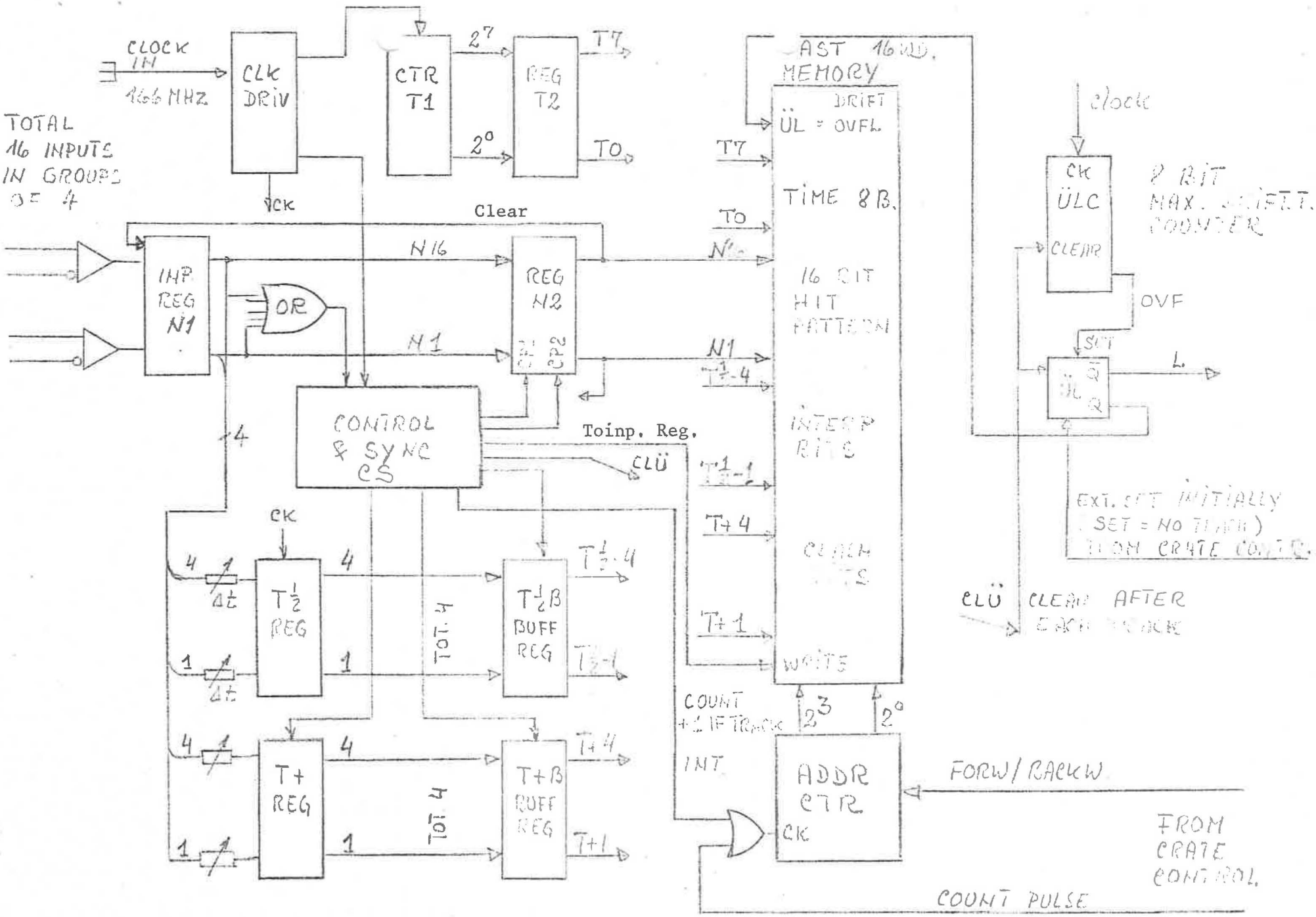
6.1 Clock-stop Module

This module works very well, the stability is good.

6.2 Drift-time Module

The "3 - 9 nsec" problem looks much better than the last test in July 1977.

In addition, it is worth mentioning that its occurrence is strongly reduced by using 4 interpolators. A minor bug was found, namely that the T^+ turns on already with the first word. But this error is recoverable by software.



VIENNA DRIFT-TIME MODULE - PRINCIPLE

FIG. 1

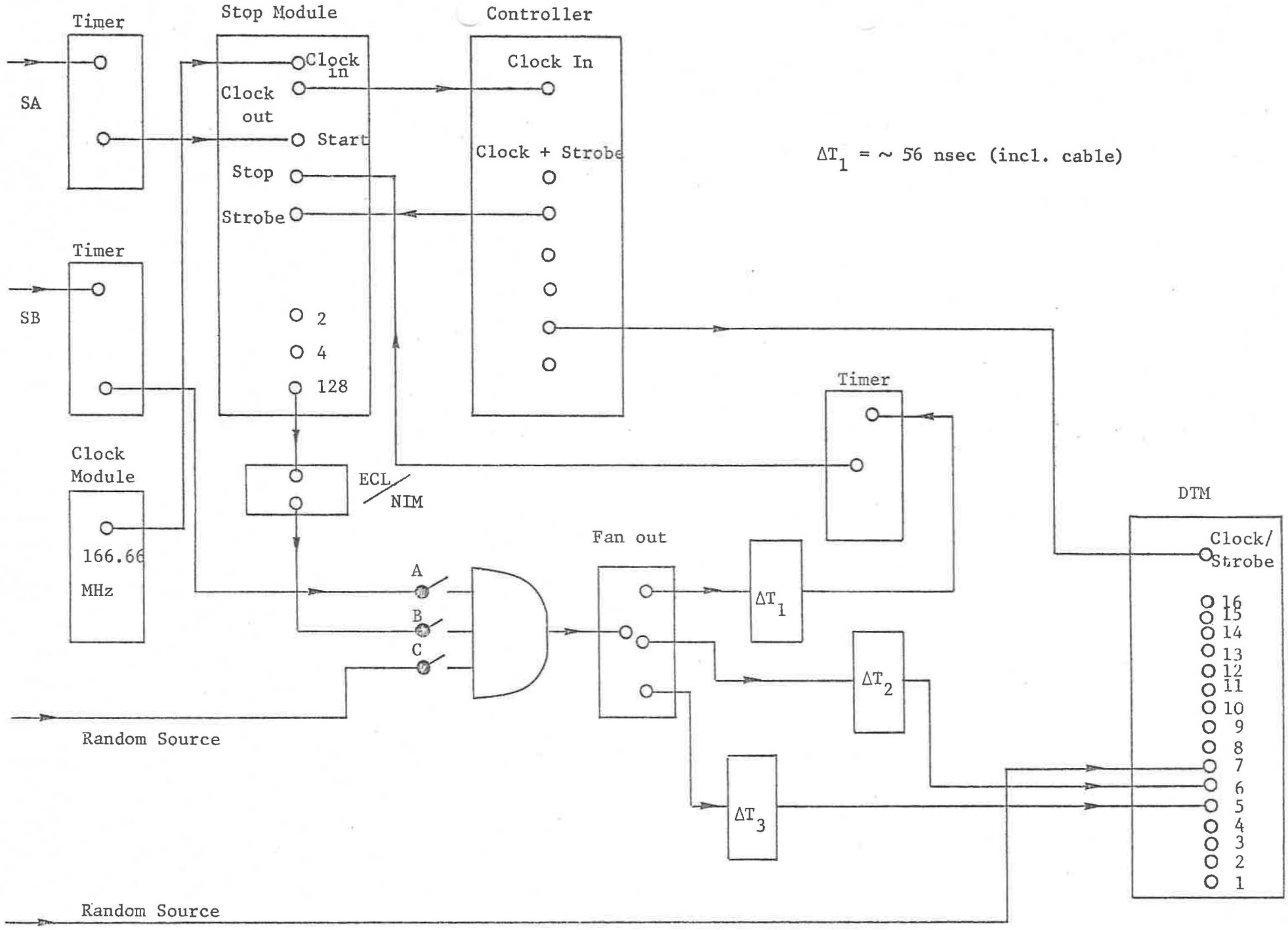

Timer
SA
Stop Module
Clock in
Clock out
Start
Stop
Strobe
2
4
128
Controller
Clock In
Clock + Strobe
ΔT_1 = ~ 56 nsec (incl. cable)
Timer
SB
Timer
Clock Module
166.66 MHz
ECL
NIM
A
B
C
Fan out
ΔT_1
ΔT_2
ΔT_3
DTM
Clock/ Strobe
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
Random Source
Random Source

Fig. 2

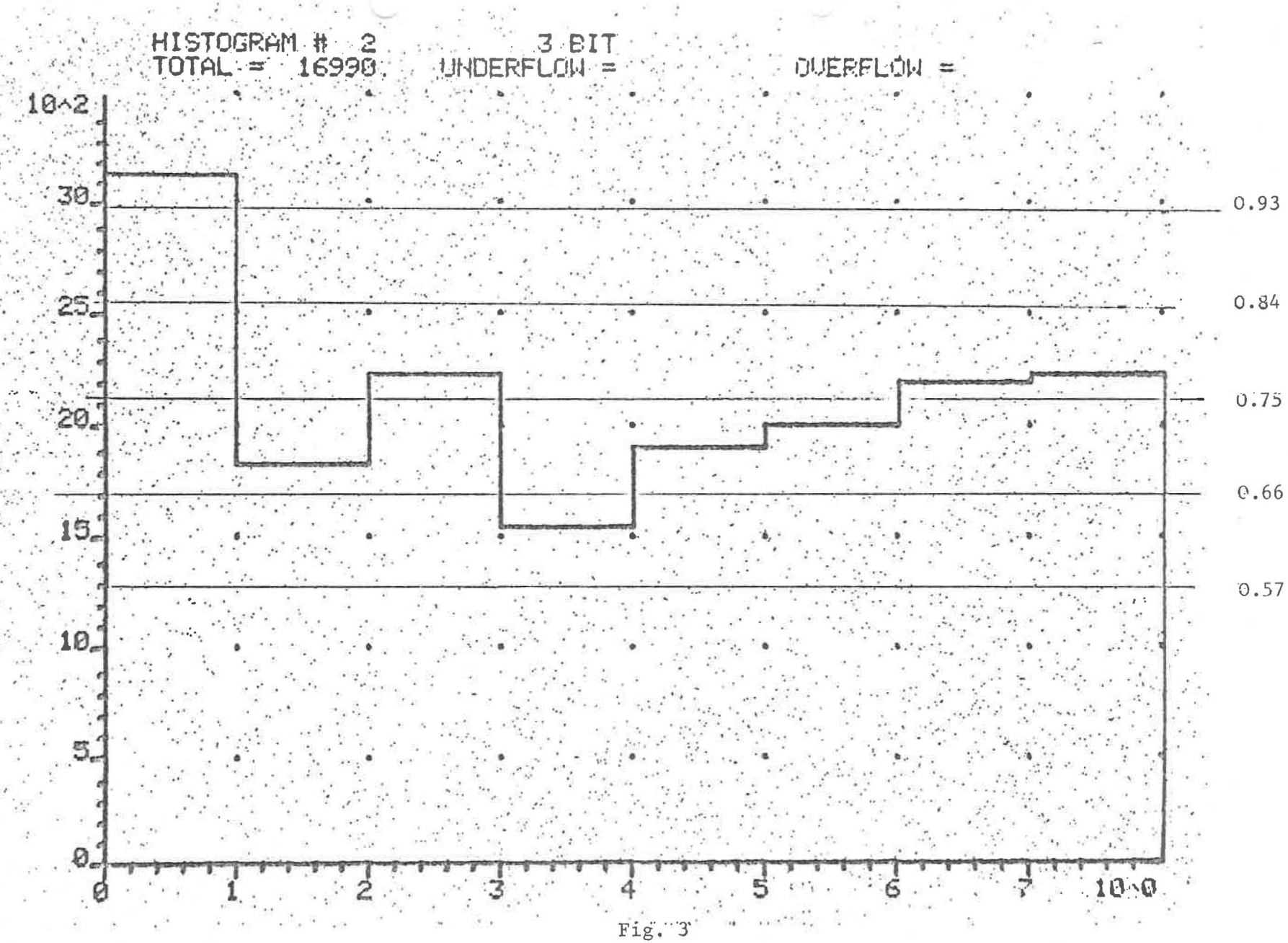

HISTOGRAM # 2 3 BIT
TOTAL = 16990. UNDERFLOW = OVERFLOW =
10^2
30
25
20
15
10
5
0
0
1
2
3
4
5
6
7
10^0
0.93
0.84
0.75
0.66
0.57

Fig. 3

```
HISTOGRAM # 31      LAST 2 BIT DTM CH 3

CHAN.  LW.EDGE  CONT.                  1111111111111111222222222222222233333333333333334444444444444444555555555
                              112334456677899001223345566788990112234455677889900112334456677899001223345566788990112234455
                             6284062840628406284062840628406284062840628406284062840628406284062840628406284062840628

                             ----------------------------------------------------------------------------------------
   1       .000     467.  I***************************************************************************5
   2      1.000     533.  I*************************************************************************************5
          2.000             ----------------------------------------------------------------------------------------
                   1000.  TOTAL NUMBER OF EVENTS
                      6   PER * (FULL CASE)
                      0   UNDERFLOW ,NOT INCLUDED
                      0   OVERFLOW  ,NOT INCLUDED
          1.033           MEAN VALUE OF THE DISTRIBUTION


HISTOGRAM # 26      LAST 2 BIT DTM CH 7

CHAN.  LW.EDGE  CONT.                111111111111222222222222233333333333334444444444444555555555555566666666666667777 7
                              1234456788901223456678900123445678890122345667890012344567889012234566789001234456788901223 4
                             8642086420864208642086420864208642086420864208642086420864208642086420864208642086420864

                             ----------------------------------------------------------------------------------------
   1       .000     655.  I********************************************************************************7
   2      1.000     345.  I******************************************1
          2.000             ----------------------------------------------------------------------------------------
                   1000.  TOTAL NUMBER OF EVENTS
                      8   PER * (FULL CASE)
                      0   UNDERFLOW ,NOT INCLUDED
                      0   OVERFLOW  ,NOT INCLUDED
           .845           MEAN VALUE OF THE DISTRIBUTION
```

Fig. 4

```
        HISTOGRAM # 15      CH13

 CHAN.  LW.EDGE  CONT.                            1111111111111111111111111222222222222222222222222233333333333333333
                            1122233444556667788899900011222334445566677888990001122233444556667788899000112223344455666 7
                          482604826048260482604826048260482604826048260482604826048260482604826048260482604826048260482

                          ---------------------------------------------------------------------------------------------
   1     70.000        . I
   2     71.000        . I
   3     72.000        . I
   4     73.000        . I
   5     74.000       1. I1
   6     75.000        . I
   7     76.000        . I
   8     77.000        . I
   9     78.000        . I
  10     79.000        . I
  11     80.000        . I
  12     81.000       8. I**
  13     82.000     227. I********************************************************3
  14     83.000     210. I****************************************************2
  15     84.000     300. I***************************************************************************
  16     85.000     213. I*****************************************************1
  17     86.000      30. I*******2
  18     87.000        . I
  19     88.000        . I
  20     89.000       5. I*1
  21     90.000       2. I2
  22     91.000       1. I1
  23     92.000       2. I2
  24     93.000       1. I1
  25     94.000        . I
  26     95.000        . I
  27     96.000        . I
  28     97.000        . I
  29     98.000        . I
  30     99.000        . I
  31    100.000        . I
  32    101.000        . I
  33    102.000        . I
  34    103.000        . I
  35    104.000        . I
  36    105.000        . I
  37    106.000        . I
  38    107.000        . I
  39    108.000        . I
  40    109.000        . I
        110.000          ---------------------------------------------------------------------------------------------
                  1000.  TOTAL NUMBER OF EVENTS
                     4   PER * (FULL CASE)
                     0   UNDERFLOW ,NOT INCLUDED
                     0   OVERFLOW  ,NOT INCLUDED
         84.144          MEAN VALUE OF THE DISTRIBUTION
```

Fig. 5