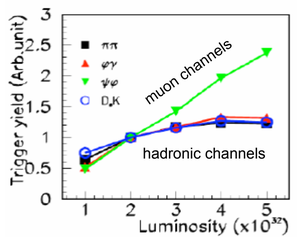
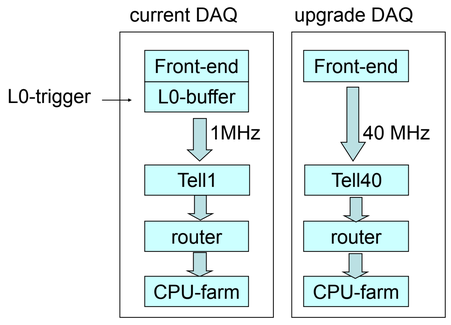
VeloPix ASIC for the LHCb VELO Upgrade

LHCb Upgrade Motivation

After collecting ~10 fb^{-1} at the standard luminosity of 2*10^{32}/cm^2/s, the time-to-double-statistics will be 3 years. LHCb wants to increase the b-event yield by a factor >10 to efficiently address remaining open physics questions and aims to collect 50 fb^{-1} in 5 years. Increasing the luminosity x 10 is rather 'easy' for LHCb (enhanced beam focusing can be introduced at 'any' time and does not require an LHC-upgrade).



But : many b-event yields do not increase with luminosity, rather saturate ...!
LHCb has a (single !) hardware trigger level (L0), necessary to reduce the event-rate to 1 MHz, which is a built-in limitation of the front-end electronics readout.
To handle an increased collision rate, but constant output rate, the L0-rejection must be increased by raising the thresholds, leading to **less signal efficiency** (especially calorimeter triggers).



Solution: Only a more sophisticated trigger can maintain good efficiencies. Decided not to rebuild new & more complex L0-trigger electronics, but execute the trigger algorithms on all data in software.

A new **DAQ** system must transfer all, zero-suppressed front-end data straight into a large computer farm, through a huge optical network & router.

All **front-end electronics** must be adapted or rebuilt to digitize, zero-suppress and transmit event data at 40MHz. Since the FE-electronics of the trackers (IT,OT,TT and VELO) and of the RICH is integrated on detectors, this requires new, enhanced detectors. Calorimeters and muon detectors can be retro-fitted with new FE electronics.

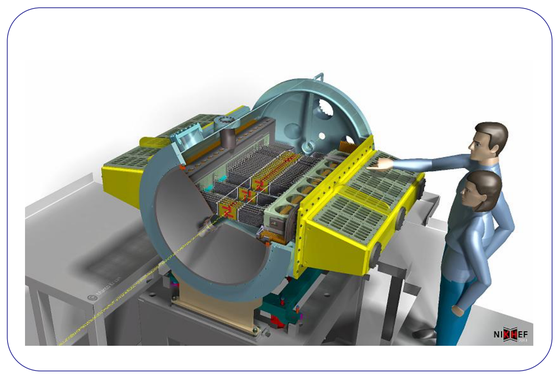
Note: the mean number of interactions per 'non-empty' event only increase from 1.2 to 4 for a factor 10 increase in luminosity. Detector granularities are largely sufficient and the upgrade focus is mainly on the FE electronics and DAQ.

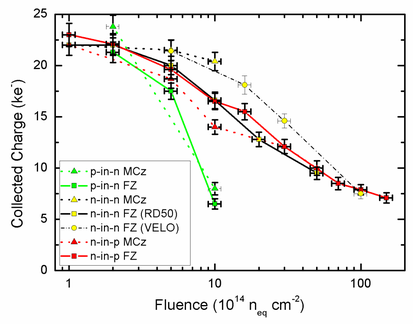
The upgraded detector is scheduled for installation in 2019/2020.

VELO Upgrade concept

The Upgraded VELO silicon vertex detector will be a lightweight hybrid pixel detector.

- The detector contains 41 million 55 µm x 55 µm pixels readout by an array of 52 modules equipped with the custom developed VeloPix front end ASIC
- The square pixel size results in equal spatial precision in both directions, removing the need for a double sided modules and saving a factor 2 in material
- Cooling is provided by evaporative CO2 circulating in micro channel cooling substrates
- In order to get the best possible impact parameter resolution the material must be minimised and the first pixel brought as close as posible to the interaction vertex. The new pixels will approach to within 5.1 mm of the collision point, and the ASICs and sensors will be thinned to 200 µm.
- The data rate from the entire VELO will reach 2.7 Tbit/s





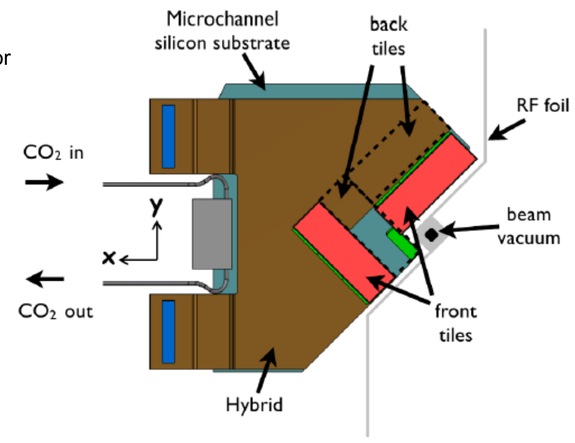
Severe irradiation environment:
At 5 mm from beam the TID will be 370 MRad or 8 x 10^{15} n$_{eq}$/cm^2.

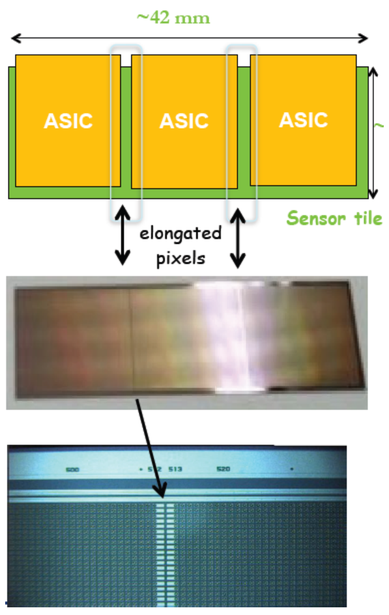
Recent RD50 studies have shown that silicon irradiated at these levels still delivers a **signal** of ~ 8ke$^-$ / MIP

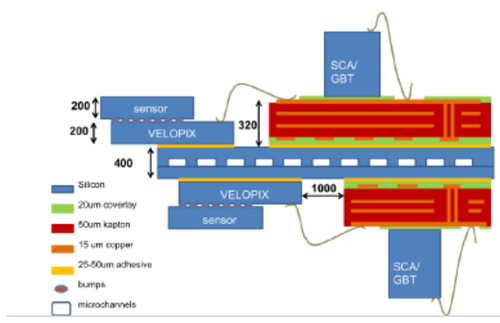
VeloPix Module

Each of the 52 modules

- Is equipped with 4 sensor tiles, each with 3 VeloPix
- For a total of 624 VeloPix ASICs in the whole detector
- The ASIC is designed in 130 nm TSMC technology
- Readout is data driven



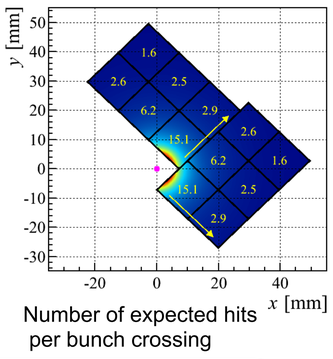




Timepix3 VeloPix

The VeloPix Chip

- a development building on the Timepix series, with a close relationship to Timepix3
- radiation resistant and with an enhanced data rate to cope with the upgrade levels
- Operational temperature -10ºC
- Must be able to compensate leakage current after irradiation of up to 20 nA / pixel



Number of expected hits per bunch crossing

VeloPix

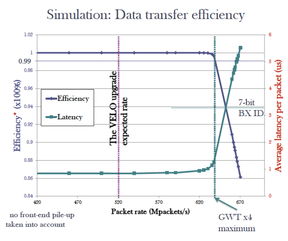
- Chip dedicated for LHCb
- Binary readout
  - ToT readout at low rate
- Extreme data rate
  - ~900 Mhits/s
  - 20 Gbit/s output bandwidth
- Optimised for electron collection
- Radiation hard / SEU robust
- Reduced time resolution (25 ns)

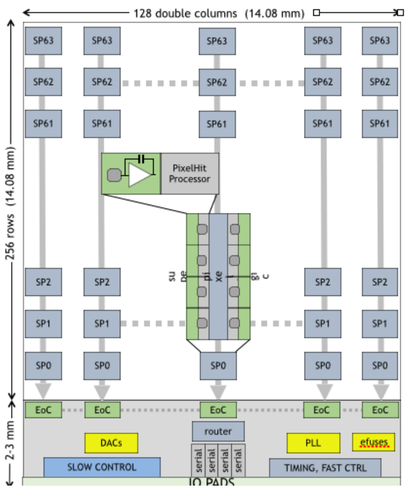
Timepix3

- General purpose chip
- "Analog" (ToT) readout
- Many modes / features
- High data rate
  - 80 Mhits/s, 5 Gbit/s
- Excellent chip for sensor characterisation

VeloPix Outline

- Pixel Matrix:
  - 65536 pixels 55 µm x 55 µm:
    - 128 double columns
    - Each double column of 2 x 256 pixels
- Analog Front end
  - Krummenacher scheme
  - Pile-up losses at tip < 1.6%
- Pixel grouping for sharing bunch id and super pixel ID; reduction in data rate ~ 30%
- Output electrical link: 4 x 5.12 Gbps





ASIC specifications

Pixel size	55 µm x 55 µm
Pixel matrix	256x256
Chip size	14 mm x ~16 mm [note 1]
Input charge	Optimized for e- (h+ if possible)
Input coupling	DC
Leakage current compensation	20 nA per pixel [notes 2-4]
Input referred noise (ENC)	σ < 100 e- (Cdet < 50 fF, planar silicon)
Minimum threshold, full chip	<800 e-
Threshold spread after equalisation	σ < 30 e-
Timewalk	< 25 ns for 1 ke-
Time over Threshold	No, binary readout, ToT only for monitoring [note 5]
ToT: pixel to pixel spread	< 5 %
Average max. hit rate	> 590 (880) MHits/s [note 6]
Allowed hit loss at max. rate	< 1% [note 7]
Technology	130 nm CMOS
System clock frequency	40 MHz
Output data format	Data-driven, zero-suppressed, grouping of hits to reduce bandwidth (superpixel concept)
Data output	At least 4 GWT links [note 8]

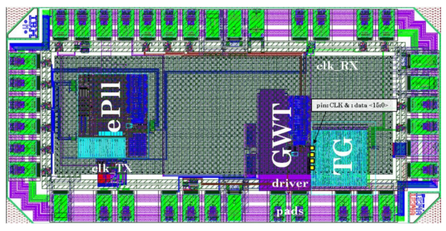
Operational temperature range	**-40 'C to + 60'C**
Startup temperature range	-60 'C to + 60'C [note 9]
Power consumption	< 3W/ full chip
Radiation hardness	> 400 MRad [note 10]
SEU protection	yes [note 11]
Timing and fast control (TFC)	See note 12
Slow control	Compatible with LHCb ECS: e.g. SPI over GBT [note 13]
Monitoring	Voltage, temperature
Error/status counters	see note 14
Front-end disable	yes (shutter-like mode), see TFC
Fast (data) reset / clear buffers	yes
Bump pad window diameter	12 µm, like Timepix3
IO signal levels	SLVS
Global (trigger) OR	Yes
Calibration	Internal and/or external testpulse (1-2 ns time resolution), internal delay in case of external TP.
Power on reset (pin)	Yes

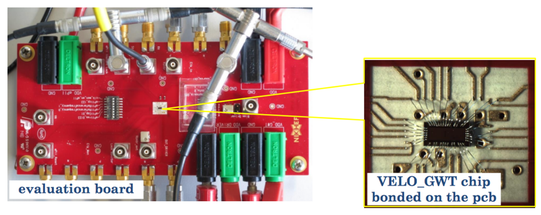
Output stage and R/O

GWT: 5.12 Gbps serializer Wireline Transmitter

- Low power topology : serializer < 10 mW, wireline transmitter < 35 mW
- Delay locked loop (DLL) based topology
  - lower phase noise (no jitter accumulation)
  - lower power

Velo_GWT test chip in IBM 130nm technology

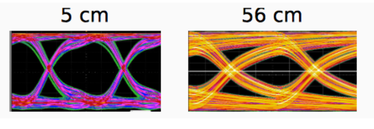




Proof of principle submission
Tests underway - good performance
SEU confirmed acceptable

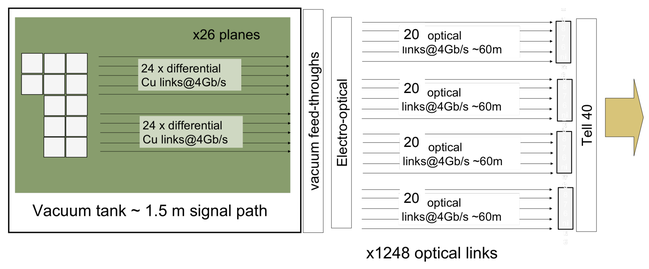
Readout Challenges

- Time reordering at 40 MHz
- Fast electrical transmission in vacuum



Prototype cable tests

Readout of one VELO half



x1248 optical links