The PreProcessors for the ATLAS Tile Calorimeter Phase II Upgrade

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***Abstract*–The Large Hadron Collider has envisaged a series of upgrades towards a High Luminosity LHC delivering five times the LHC nominal instantaneous luminosity. The ATLAS Phase II Upgrade will accommodate the detector and data acquisition system for the HL-LHC. In particular, the Tile Hadronic Calorimeter will completely replace front-end and back-end electronics using a new read-out architecture. The digitized detector data will be transferred for every beam crossing to the PreProcessors located in off-detector counting rooms with a total data bandwidth of roughly 80 Tbps. The TilePPr implements larger pipelines memories and must provide pre-processed digital trigger information to Level 0/1 trigger systems. The TilePPr system represents the link between the front-end electronics and the overall ATLAS data acquisition system. It also implements the interface between the Detector Control System and the front-end electronics which is used to control and monitor the high voltage distribution system. The TilePPr is responsible of transmitting the commands to configure, control and monitor the front-end electronics.**

I. Introduction

The Tile Calorimeter (TileCal) [1] is the hadronic calorimeter of the ATLAS [2] experiment at the Large Hadron Collider (LHC) at CERN. TileCal is a sampling detector using steel plates as absorber and plastic scintillator tiles as active material. This detector covers the central part of the ATLAS experiment and it is divided into four sections along the beam direction, each of which is segmented azimuthally into 64 modules (Figure 1a). The Photomultipliers Tubes (PMTs) and the front-end electronics are located in the super-drawers in the outermost part of the modules (Figure 1b). The complete read-out of the TileCal cells comprises a total of 9852 PMTs.

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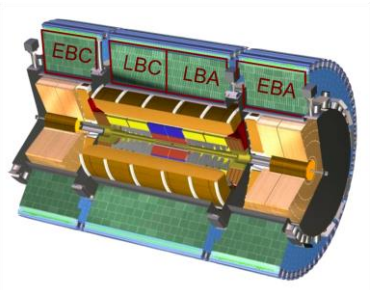

Fig. 1a. TileCal detector.

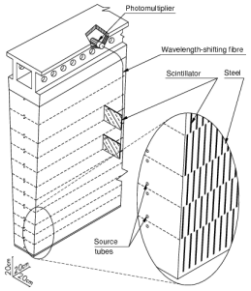

Fig. 1b. TileCal module.

In the front-end electronics, the analog signals coming from the PMTs are shaped and amplified with two different gains. The shaped signals are digitized and stored in the front-end electronics at the LHC frequency of 25 ns. Moreover, the analog signals are summed in towers and transmitted to the Level 1 Calorimeter trigger system (L1Calo) for the selection of potentially interesting events. Figure 2 shows the data flow of the TileCal architecture.

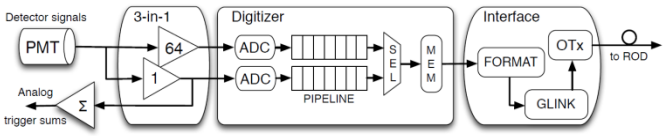

Fig. 2. Diagram of the current read-out architecture of the Tile Calorimeter.

Digitized data is stored in the front-end electronics until the reception of a Level-1 trigger acceptance signal, when the Interface boards send the selected events to the Read-Out Drivers (RODs) [3] in the back-end electronics. RODs are responsible of processing the incoming data at a maximum average rate of 100 kHz.

II. The ATLAS Tile Calorimeter Phase II Upgrade

After the ATLAS Phase II Upgrade [4] in 2024, the High Luminosity LHC (HL-LHC) will provide a nominal instantaneous luminosity of $5\text{-}7\cdot10^{34}$ $cm^{-2}s^{-1}$ with a pileup close to 200 events delivering a total integrated luminosity of 3000 fb^{-1} in ten years.

The Phase II Upgrade requirements imply the complete redesign of the read-out architecture and trigger systems to improve the event selections and cope with the new radiation levels, latency and high data rates.

Figure 3 shows a diagram of the read-out architecture for the ATLAS Tile Calorimeter Phase II Upgrade. The new read-out architecture points to a fully digital trigger system where the front-end electronics will transmit all the digitized samples

to the Tile PreProcessors (TilePPr) in the back-end electronics at the LHC frequency.

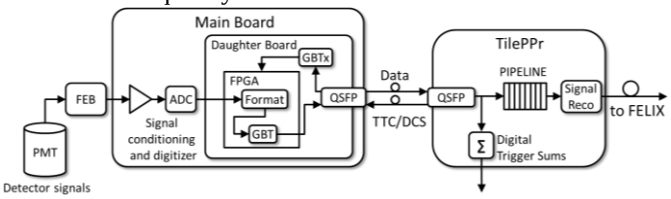

Fig. 3. Diagram of the Phase II read-out architecture of the Tile Calorimeter.

A. *The Tile Calorimeter Demonstrator Project*

The Demonstrator project aims to evaluate the new read-out architecture and trigger system interfaces before the complete replacement of the electronics during the ATLAS Phase II Upgrade.

The performance of the upgraded front-end electronics will be evaluated with test beam during 2015, and with the insertion of one Demonstrator module containing all the new electronics into the ATLAS detector at the end of 2016.

Figure 4 shows a diagram of the read-out architecture for the Demonstrator, where the Demonstrator module provides analog trigger signals to the L1Calo system as the fully digital trigger system will not be present until Phase II. The Demonstrator module also will contain all the electronics needed for the digitization of analog signals, the calibration circuitry and high speed data links with the TilePPr, as well as, all the electronics needed to operate and distribute the high voltage to the PMTs.

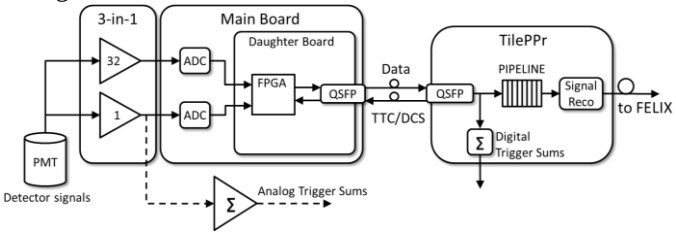

Fig. 4. Diagram of the read-out architecture of the Tile Calorimeter Demonstrator.

III. The Tile Calorimeter PreProcessors

The TilePPr will be the main component of the back-end electronics after the ATLAS Phase II Upgrade. This module will provide a high speed link for the read-out, operation and monitoring of the front-end electronics. Moreover, the TilePPr will send calibrated information to the ATLAS trigger systems with improved granularity and precision.

High speed links will be used to distribute Trigger, Timing and Control (TTC) information and Detector Control System (DCS) commands towards the detector.

Figure 5 shows a preliminary diagram of the TilePPr for Phase II Upgrade. The TilePPr will have an ATCA [5] form factor, where each TilePPr will operate up to 8 TileCal modules, each one containing up to 48 PMTs. A total of 32 TilePPr will be needed for the total read-out of the TileCal detector. A Rear Transition Module (RTM) will allow the TilePPr to interface with the FELIX [6] system and trigger systems.

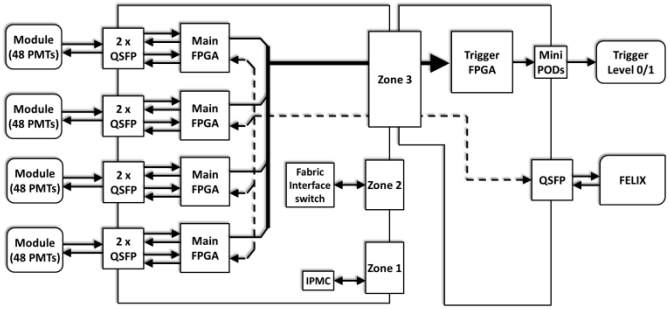

Fig. 5. Preliminary diagram of the TilePPr.

A. *The TilePPr prototype*

The TilePPr prototype [7] has been designed and produced in the framework of the Demonstrator project. This prototype is able to read out and operate the Demonstrator module providing compatibility between the current architecture and the Demonstrator module. Figure 6 shows a picture of the first prototype of the TilePPr.

Fig. 6. Photograph of the TilePPr prototype.

Four QSFP optical modules are used to interface the TilePPr with the Daughter Boards [8] in the front-end electronics. The Xilinx Virtex 7 FPGA [9] implements 16 high speed asymmetric links using the GigaBit Transceiver (GBT) [10] protocol for the high speed communication. All the incoming data is decoded in the Virtex 7, which also performs the Cyclic Redundancy Check (CRC) calculation and stores the events in circular pipeline memories until the reception of a trigger acceptance signal. When the trigger acceptance signal is received, the selected events are extracted from the pipeline memories, packed and sent to the RODs to keep backward compatibility with the present architecture.

The Virtex 7 FPGA decodes the TTC commands and extracts the clock from the TTC stream distributing them to the front-end electronics. The extracted TTC clock is cleaned with a high performance jitter cleaner which provides the reference clock to the GBT links.

The uplink (back-end to front-end electronics) is used to send DCS and TTC commands at the standard data rate of the GBT protocol (4.8 Gbps). The downlink has been modified to operate at 9.6 Gbps in order to have enough data bandwidth to

read out all the channels of the Demonstrator module every bunch crossing (~25 ns).

An Avago MiniPOD TX connected to the Kintex 7 FPGA will be use to interface the TilePPr with the Level 0/1 trigger systems. The Kintex 7 FPGA will receive read-out data from the Virtex 7 and will send pre-processed trigger information to the trigger systems.

The TilePPr prototype is also intended as a platform to test new algorithms for energy reconstruction, time and quality factor for the Phase II Upgrade.

IV. Conclusions

A new read-out architecture with a fully digital trigger will be implemented to cope with the new requirements of the HL-LHC during the ATLAS Phase II Upgrade. The increase of the radiation levels and the larger expected data bandwidth implies the complete redesign of the front-end and back-end electronics of the Tilecal.

As part of the Demonstrator project, the TilePPr prototype has been designed and produced. The first TilePPr prototypes have been tested successfully. The test results confirm the expected performance of the prototype.

The TilePPr prototype will be used to evaluate the Demonstrator module in the test beam campaigns during 2015-2016 and to operate and read out the new electronics that will be inserted in the ATLAS detector at the end of 2016.

References

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