A 12 bit 40 MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS LAr calorimeter readout

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ABSTRACT: We present a SAR ADC with a generalized redundant search algorithm offering the flexibility to relax the requirements on the DAC settling time. The redundancy also allows a digital background calibration, based on a code density analysis, to compensate the capacitor mismatch effects. The total number of capacitors used in this architecture is limited to a half of the one in a classical SAR design. Only 2^{11} unit capacitors were necessary to reach 12 bit resolution, and the switching algorithm is intrinsically monotonic. The design is fully differential featuring 12 bit 40 MS/s in a CMOS 130 nm 1P8M process.

KEYWORDS: SAR ADC; Non-binary; Redundancy; Switching algorithm; Digital calibration.

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Contents

1. Introduction

Particle detectors, such as liquid argon (LAr) calorimeters used in the ATLAS experiment at the LHC (Large Hadron Collider), generate very large dynamic signals which require a sophisticated front-end electronics. This readout includes the noise optimization stages (low noise preamplifier, and analog multi-gain filters) [8]. A critical task is the design of the following stage of Analog to Digital Converter (ADC). The minimum requirements for this converter are 40 MS/s at 12 bit resolution. In this configuration, pipeline architecture was widely used in the past. However following the scaling of CMOS processes, Successive Approximation Register (SAR) architecture appears to be more suitable in terms of power dissipation. In this paper, a redundant SAR ADC is proposed, to achieve the high resolution required despite the capacitor mismatching. The paper is organized as follows. In Section II, the conventional SAR ADC limitations are reviewed. Section III introduces the generalized non-binary search algorithm. Section IV presents the proposed redundant SAR ADC. In Section V, the simulations of the design are discussed.

2. Conventional SAR ADC limitations

Recently, SAR ADCs have been widely used for high-resolution, medium sampling rate, and low-power applications [1]. SAR ADCs are actually known to achieve very low power consumption owing to the extensive use of switching capacitor based circuits.

The conventional SAR ADCs uses a binary search algorithm following a binary-weighted capacitive DAC which is also used to perform the sample-and-hold function [2]. The drawback of the binary search algorithm is that it makes the ADC sensitive to decision errors due to capacitor matching limitations, incomplete DAC settling, parasitic capacitors, etc. In case of an intermediate wrong decision, the following digitization process cannot recover. In Fig.1 the first comparison is wrong and this drives away the DAC output (V_{DAC}) from the analog input signal (V_{in}), which results in an error at the end of the conversion. Therefore one needs to guarantee an

accuracy of 0.5 LSB at each step of the SAR ADC processing. In the standard CMOS process a 12 bit resolution, for instance, is not achievable even after a big effort in solving matching problems in the layout.

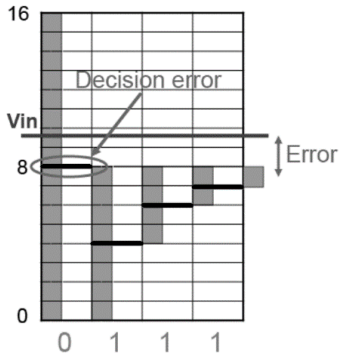

Figure 1: Example of decision error due to incomplete DAC settling. Taken from Ref. [3]

We have created a Matlab model to evaluate just the capacitor matching limitations effects on a 12 bit SAR-ADC. Simulation results are shown in Fig.2.

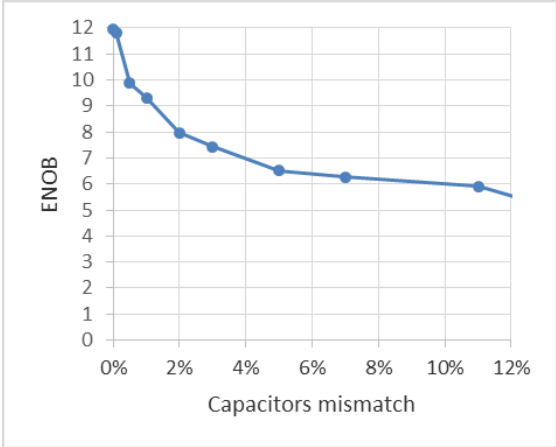

Figure 2: Matlab simulations results for capacitors mismatch limitations on a 12 bit SAR ADC.

The pure binary search algorithm requires a strict and monotonic DAC section which is hard to combine with high density of integration that dramatically impacts the capacitor matching performances. To overcome these limitations, one possible solution is to move from the conventional binary search algorithm to a non-binary one.

3. Generalized non-binary search algorithm

A non-binary search algorithm makes the SAR ADC tolerant towards incomplete DAC settling errors, and it allows a digital correction algorithm for the capacitor mismatch errors, which is identified to be the main limiting factor for high resolution ADCs.

By using overlapped search ranges (for redundancy), the non-binary search algorithm compensates the comparison decision errors made in earlier conversion steps as long as the error made is within a certain tolerance range. To achieve a N-bit resolution using a redundant search algorithm, the SAR ADC requires M comparison steps (M>N) to determine the output digital bits. The idea is to have 2^M possible comparison combinations and 2^N possible digital output

combinations, and since M>N, therefore $2^M>2^N$. In other words, for a given output level D_{out}, there can be multiple comparison patterns leading to the same final result. Thus even if it happens for a comparison decision to be wrong, there is nevertheless a room for recovering a correct ADC output codes after the following steps. Fig. 3 illustrates a 4 bit SAR ADC using 5 redundant steps.

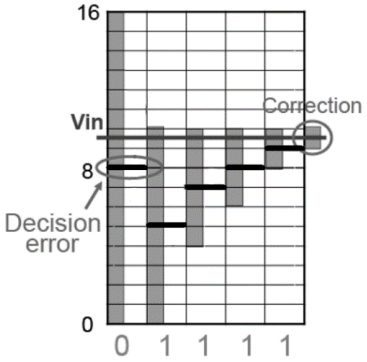

Figure 3: Operation of a redundant search algorithm of a 4-bit 5-step SAR ADC. Taken from Ref. [3]

Although the redundant search algorithm adds extra clock cycles to the conversion phase, the duration of these conversion steps can be made shorter (thanks to incomplete DAC settling) [4] and the overall conversion speed is preserved.

A SAR ADC implementing the non-binary search algorithm can use radix $r=2^{N/M}$ such as presented in [4] and [5]. An alternative method called "*a generalized non-binary search algorithm*" has been presented in [3] without restricting to a radix of $2^{N/M}$. We explain hereafter this alternative algorithm.

At each conversion step (*k*), to define the k-th bit, the analog input voltage is compared to a reference voltage generated by the DAC according to a redundancy vector *p*. For a normalized input voltage in the range $[0, 2^N]$, the reference voltage used in k-th step (*Vref (k)*) to define the k-th bit (*b(k)*), as given in [3], as follows:

$$V_{ref}(k) = 2^{N-1} + \sum_{i=2}^{k} s(i-1) * p(i) \qquad (1)$$

Where:

- *k = 1, 2. . . M.*
- *s(i-1)=1* if *b(i-1) = ''1''* **or** *s(i-1)=-1* if *b(i-1) = ''0''.*
- *p(i)* is the i-th element of what we can call the redundancy vector *p*.

The vector *p* must satisfy the following conditions :

$$p(1) = 2^{N-1} \qquad (2)$$

$$\sum_{i=1}^{M} p(i) = 2^N - 1 \qquad (3)$$

At the end of the conversion, the actual ADC digital output is extracted following the equation:

$$D_{out} = 2^{N-1} + \sum_{i=2}^{M} s(i-1) * p(i) + \frac{1}{2}(s(M) - 1) \qquad (4)$$

The comparison error range which can be corrected by the redundancy in k-th step is defined as follows:

$$q(k) = -p(k+1) + 1 + \sum_{i=k+2}^{M} p(i) \qquad (5)$$

The equations (6) and (7) show an example of the values of the redundancy vector *p* and the vector, of the acceptable errors, *q* in each step of conversion for a 12 bit 14 step SAR ADC.

p = [2048, 1012, 456, 252, 144, 80, 46, 26, 14, 8, 4, 2, 2, 1] (6)

q = [24, 124, 76, 40, 24, 12, 6, 4, 2, 2, 2, 0, 0, 0] (7)

4. Proposed architecture

To implement the generalized non-binary search algorithm for a N-bit conversion, based on a M-step redundant SAR ADC, a series of corresponding reference voltages must be generated and then compared to the incoming voltage signal. In other words, the ADC must perform the additions/subtractions, between *Vref(k-1)* and *p(k)*. For these operations a digital architecture approach is possible [3], but this strategy comes with an increase of the overall complexity of the design, and some extra delay and power consumption in the digital part of the ADC. Another approach is to perform the operations in the analog domain by using a DAC [6]. Each value of *p(k)* is then stored in capacitor values. This strategy presents the advantage of a reduced and simplified digital part of the circuit, which leads to reduced power consumption, compared to the one proposed in [3].

In this paper, we propose a fully differential N-bit M-step redundant architecture that implements the generalized non-binary search algorithm in the analog domain, a new structure is designed so as to use only 2^{N-1} unit capacitors in the DAC instead of 2^N in conventional solutions. This allows reducing the dynamic power consumption as well as the total capacitance compared to the architecture proposed in [6]. Fig.4 shows the proposed architecture.

During the sampling phase, the differential input signal (V_{in+} and V_{in-} respectively) are stored in a capacitor array. After this phase, in each step, the ADC compares the input signal with the corresponding *Vref(k)* generated, by switching the corresponding capacitor, following the switching algorithm explained hereafter. The DAC is not segmented in order to optimize the linearity features and to avoid the limitations associated with split-capacitor structures such as the parasitic capacitance at the sub-DAC output and the fractional value of the bridge capacitor. The high-speed and low-noise comparator is implemented by using a multi-stage differential pair as shown in Fig.5.

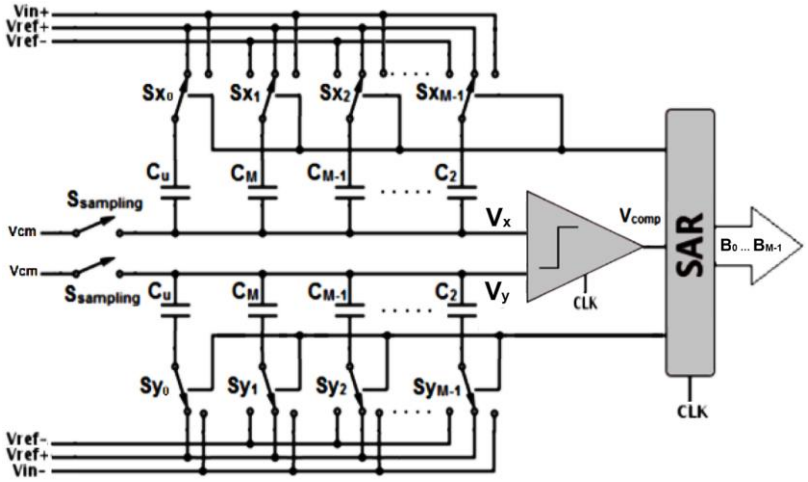

Figure 4: The proposed N-bit M-step SAR ADC architecture (where C_k=*p(k)C_u and k = 2, 3. . . M).**

4.1 Proposed switching algorithm

The proposed redundant SAR ADC uses a monotonic switching algorithm (see Fig. 6) which requires much less dynamic power consumption compared to the conventional switching algorithm.

One may notice that there is no switch-back operation and over the whole ADC, only one capacitor is switched at each bit-cycle step, providing inherent immunity to the skew of the switch signals. At the end of the conversion, the N-bit digital output is calculated from the M-bit data. This proposed switching algorithm is also valid for the SAR ADC using the binary search algorithm, when N=M and $C_k=2^{N-k}*C_u$; $2 \leq k \leq N$.

4.2 Digital Calibration

A foreground digital calibration algorithm was developed based on Ref. [7]. It uses the original ADC core without adding any extra analog hardware on-chip or any additional reference channel in the design. It is based on a statistical approach using a code density measurement to estimate the actual step sizes which map accurately the M-bit output into a final N-bit digitalized output. At present, this algorithm is out of chip.

In our case, a calibration signal is used to simplify the calibration algorithm presented in [7]. During the calibration phase a full-scale ramp is sent to the ADC input to create a histogram of the 2^M possible output codes. After having normalized this histogram for the number of samples, an equation associated with each code bin is formulated, then an equations system is obtained by subtracting the neighbouring equations. To calculate the estimated value of the step sizes, the algorithm searches for a solution in this equations system.

5. Simulation results

Using the proposed architecture and the coefficients of the equation (6), we designed in the 130 nm 1P8M IBM CMOS a fully differential 12 bit redundant SAR ADC working at 40 MSPS with a 2 V_{pp} full-scale input range. Fig. 7 shows a photograph of the chip received and to be tested. The power consumption of the core ADC is about 11 mW from a 1.5 V / 1.2 V supply. Fig.8 shows the simulation results for the successive DAC approximation signal at the comparator input. In Fig.8 (a) after all settlings are completed, the ADC performs the conversion without any decision error, and the D_{out} calculated from the 14 bits, according the equation (4), is 3031. But in the configuration of Fig.8 (b) a wrong decision has been made in the second step due to an incomplete settling. However one can see how the ADC is capable to recover in the following steps, and D_{out} obtained finally is the same as in Fig.8 (a) (case without error). This illustrates the robustness of our redundancy architecture.

To evaluate the digital calibration regarding capacitor mismatch error, a 5% capacitors mismatch error was inserted in the DAC and a 1.0546875 MHz full-scale sine wave input was converted at 40 MSPS with 4096 samples, to simulate the static and dynamic performance. Fig.9 and Fig.10 show respectively the simulated INL and dynamic performance without and with calibration. Without calibration the maximum INL errors are +56.5/-56.8 LSB and the ADC achieves 38.25 dB of SNR, 40.53 dB of SFDR and 5.56 b ENOB. After calibration the maximum INL errors is reduced to +1.6/-1.7 LSB and the ADC achieves 69.54 dB of SNR, 64.23 dB of SFDR and 11.15 b ENOB.

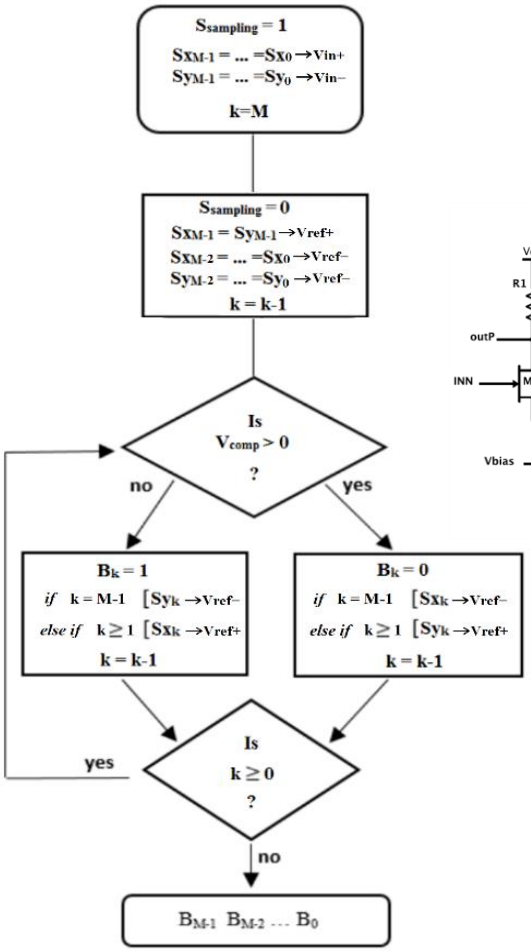

Figure 6: Switching algorithm for the proposed SAR ADC.

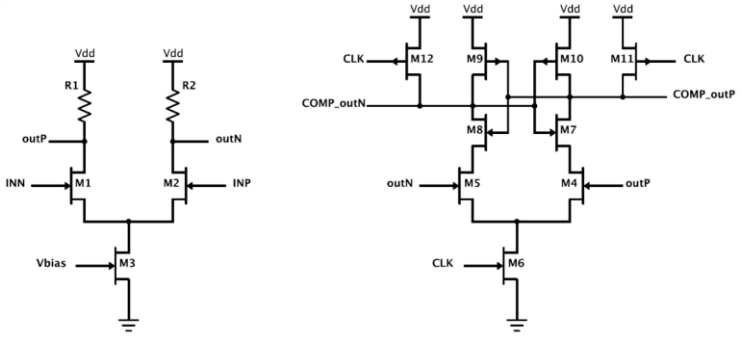

Figure 5: Multistage comparator.

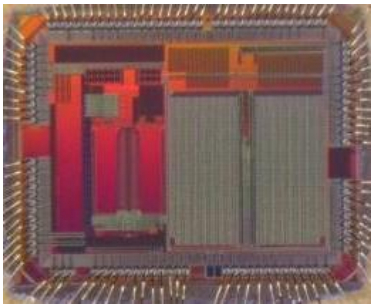

Figure 7: Photograph of the chip die to be tested.

(a)
Complete settling

(b)

Incomplete settling in the second step

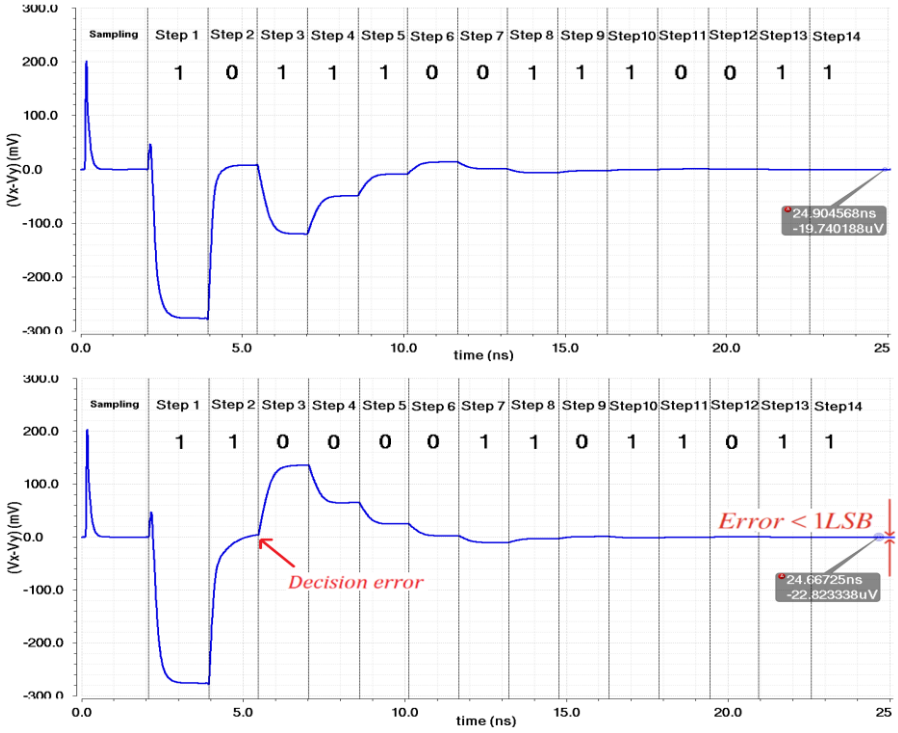

Figure 8: The simulated DAC output voltage difference (V_x-V_y) of the proposed redundant architecture.

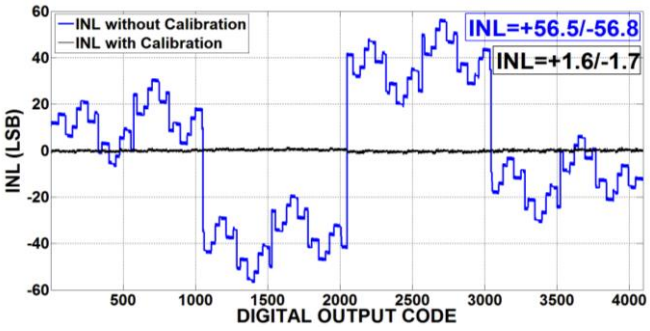

Figure 9: The simulated INL.

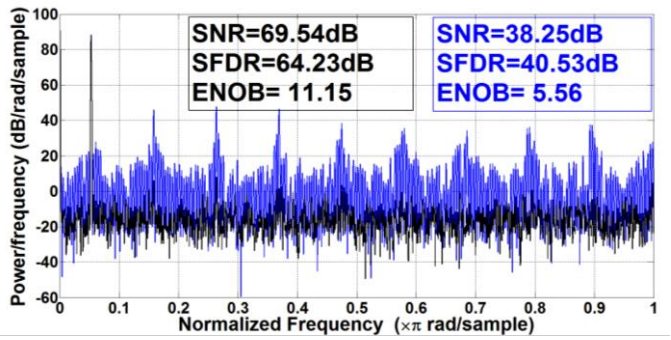

Figure 10: The simulated FFT spectrum.

6. Conclusion

The design of a redundant SAR ADC has been presented with an efficient switching algorithm, and a digital calibration algorithm. The design of a generalized non-binary search algorithm is explained. Compared to previous works, this architecture presents the advantage of simplicity and minimizes the value of total capacitance. A design of a 12 bits, 40 MS/s configuration and its simulation results confirm the robustness of the proposed structure. The circuit is under test, and testing results will be published later.

References

[1] B. Murmann, *ADC Performance Survey 1997-2014*, [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[2] J. McCreary, P. Gray, *ALL-MOS charge redistribution analog-todigital conversion techniques*, IEEE J. Solid-State Circuits, vol. SC-10, no. 12, pp. 371-379, Dec. 1975.

[3] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, S. A. N. Hao, T. Matsuura, and Y. Katsuyoshi, *SAR ADC algorithm with redundancy and digital error correction*, IEICE transactions on fundamentals of electronics, communications and computer sciences, vol. 93, no. 2, pp. 415–423, 2010.

[4] F. Kuttner, *A 1.2 V 10b 20MSample/s non-binary successive approximation ADC in 0.13/spl mu/m CMOS*, Solid-State Circuits Conference, 2002. Digest of Technical Papers, ISSCC. 2002 IEEE International, 2002, vol. 1, pp. 176–177.

[5] M. Hesener, T. Eichler, A. Hanneberg, D. Herbison, F. Kuttner, and H. Wenske, *A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13 pm CMOS*, Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International, 2007, pp. 248–600.

[6] A. Arian, M. Saberi, S. Hosseini-Khayat, R. Lotfi, and Y. Leblebici, *A 10-bit 50-MS/s redundant SAR ADC with split capacitive-array DAC*, Analog Integrated Circuits and Signal Processing, vol. 71, no. 3, pp. 583–589, 2012.

[7] Chang, A.H.; Hae-Seung Lee; Boning, D., *A 12b 50MS/s 2.1mW SAR ADC with redundancy and digital background calibration*, ESSCIRC (ESSCIRC), 2013 Proceedings of the , vol., no., pp.109,112, 16-20 Sept. 2013.

[8] N J Buchanan., *ATLAS liquid argon calorimeter front end electronics*, Journal of Instrumentation, vol. 3, no. 9, pp. P09003, 2008.