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MILESTONE REPORT

DESIGN AND FABRICATION OF AMC MODULES FOR CONTROLLING STEP MOTORS, PIEZO AND WAVEGUIDE TUNERS

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Abstract:

FLASH accelerator is using superconducting RF cavities to accelerate electron beam. These cavities must be precisely tuned to RF frequency due to very high Q factor (~10^9 unloaded Q and ~10^6 loaded Q). They are tuned by slight dimension change (particularly length) induced by tuners driven by step motors. For high gradients (~20MV/m and more) the cavities are dynamically detuned during RF pulse due to Lorentz Force Detuning (LFD). To keep them in resonance the fast tuners with piezos are used. Both slow and fast tuners need the control integrated with the LLRF system.

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1. INTRODUCTION

Both the step motors and piezos control require relatively high voltage and current electrical signals. In the ATCA based control system it was foreseen to integrate these systems in a form of plug-in cards (for ATCA crate) using the ATCA power supply (48V), which was freely available. This way it was possible to fit most of the LLRF system into single ATCA crate. When the hardware platform was changed from ATCA to uTCA this concept had to be revised. The uTCA plug-in card (AMC module) is to small to fit on it many channels with high voltage and current supplied. In addition the 48V is not available in the uTCA crate (only 12V is available).

Therefore the control system for the step motors and piezos was realized in the form of external 19 inch box connected to the LLRF controller with communication link.

2. STEP MOTOR CONTROL

The controller is built based on the AVR microcontrollers and uses the MODBUS protocol. The integration of 16 drivers on a single PCB makes possible to service 16 stepper motors controlling the RF (Radio Frequency) phase shifters. The following description applies to a single channel controller – 16 identical channels on a single PCB will be used in the target system. The control board has been designed and currently is being manufactured.

2.1. STEP MOTOR DRIVER

The driver is controlled by the AVR RISC ATmega8 microcontroller with 8 kB Flash memory and 1 kB of RAM in its structure. Measurements of the step motor voltage and current consumption force to use the TQFP version that contains (in relation to the DIP version) additional 10-bit A/C converter. The microcontroller operates in the configuration of the external 6MHz quartz resonator to ensure the stability of the clock signal used for serial transmission and the microcontroller engine speed setting. Connector in Kanda standard allows programming the ISP microcontroller.

The signals that control the motor windings from microcontroller ports are sent to two ULN2803 chips via optocouplers. The ULN2803 chips contain 8 transistors in Darlington's configuration with a maximum current of Ic = 0.5A each, equipped with additional protection diodes. Individual transistors are connected in parallel, thereby generating outputs with maximum current efficiency of about 2A. Due to the fact that the transistors are placed in a single structure and the same parameters of individual transistors are provided, the output power amplifiers are connected directly to each other without additional resistors compensating currents in individual branches.

The initial state of the controller can be determined on the basis of the signal produced by three LEDs. When the driver moves the engine to the left, then the yellow LED starts blinking. The blinking of the green LED indicates right engine speed. When the limit switches stop the engine, the selected direction diode lights up with steady light (towards the right - green, in left direction - yellow). The red LED signals the emergency situation in the driver. It

begins to blink when the voltage is outside the set range or when current drawn by the motor exceeds the nominal value.

The schematic diagram of the microcontroller part of the controller is presented in Figure 1. Based on the MODBUS protocol, the controller is remotely supervised and driven by the host computer. However, there is a possibility to control the stepper motors using 3-buttons control panel, which requires the driver to be set up by the host beforehand. The front panel buttons allows steering the rotation direction and speed. The motor is operating until it is stopped by stop button or the end position is reached.

2.2. CONTROL INTERFACE

For communication with the host the MODBUS RTU protocol is used. All controlling registers are stored in the volatile SRAM memory and their contents are lost when voltage is switched off.

Control Registers

Symbol	Description of the registry functions	Address register	Registry Size in bytes	Read Operation Type - R Write - In	No. of MODBUS
VOLTAGE	Supply Voltage (at 10 mV)	A100	2	R	3
CURRENT	Supply current (mA)	A101	2	R	3
STATUS	Engine status register	A102	2	R	3
CURR_POS	The current motor position in steps	A103	4	R/W	3/16
TARGET_POS	Motor target position motor in steps	A105	4	R/W	3/16
SPEED	Register of motor speed in steps / s	A107	2	R/W	3/16
COMMAND	The register of motor's driver's commands	A108	2	R/W	3/16

All configuration registers are stored in nonvolatile memory, so their content is stored even after switching off the voltage.

Configuration Registers

Symbol	Description of the registry functions	Address register	Registry Size in bytes	Read Operation Type - R Write - In	No. of MODBUS
MODBUS_ADR	MODBUS address of the driver	A500	2	R/W	3/16
CONFIG	Controller configuration register	A501	2	R/W	3/16
U_LOW_LIMIT	The lower limit of supply voltage (at 10 mV)	A502	2	R/W	3/16
U_HI_LIMIT	Upper limit of supply voltage (at 10 mV)	A503	2	R/W	3/16
I_LIMIT	Limit of the supply current in mA	A504	2	R/W	3/16
SPEED_LIMIT	Maximum permitted engine speed	A505	2	R/W	3/16
CORRECT_U	Voltage control register	A506	2	R/W	3/16
CORRECT_I	Power control register	A507	2	R/W	3/16

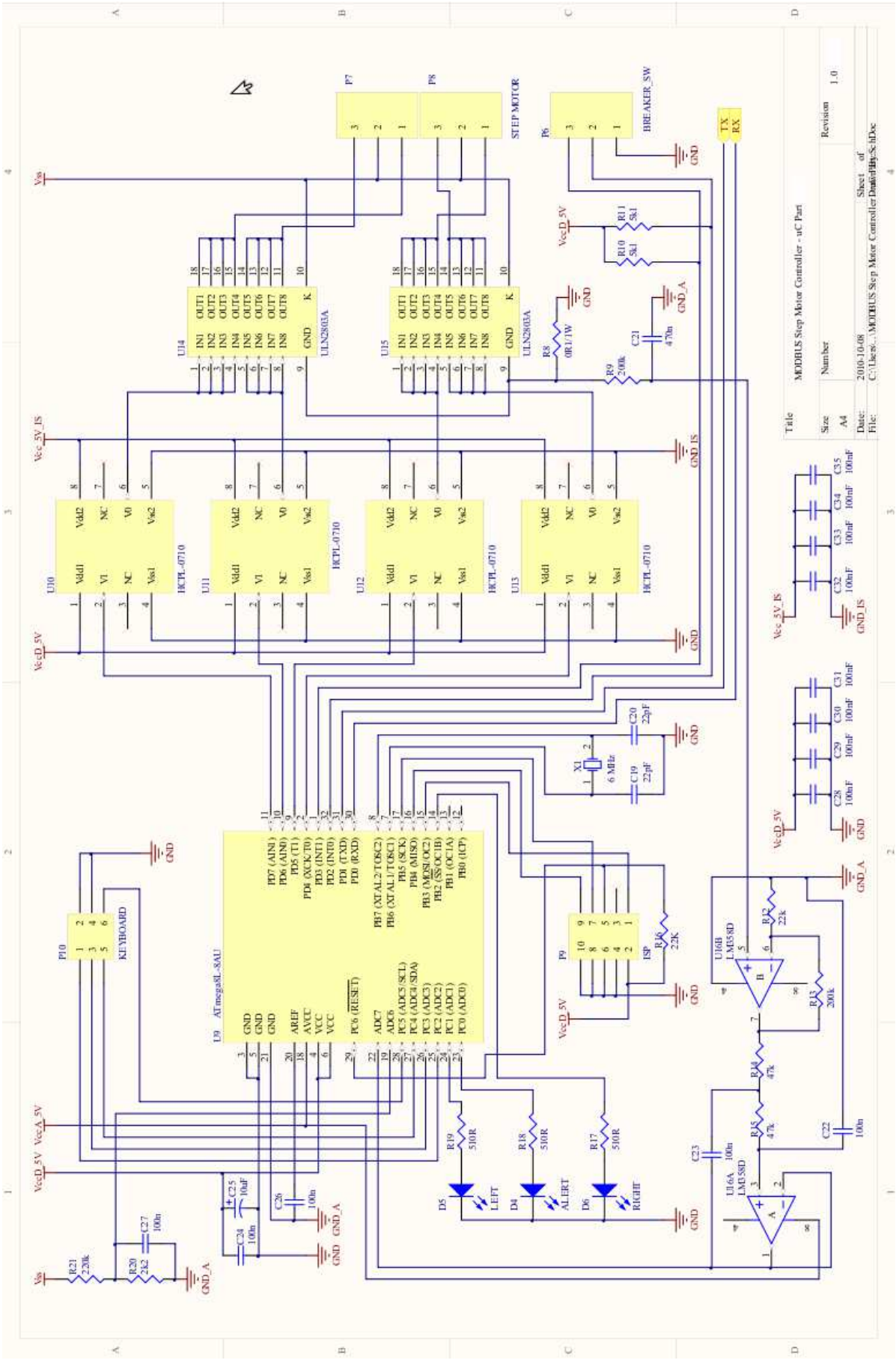


Figure 1 Schematic diagram of step motors driver - microcontroller module

The content of the STATUS register (A101) allows for specification of the state of the driver. The meaning of individual bits is presented below.

The importance of the STATUS register bits (A101)		
Bit No.	**Symbol**	**Function Description**
0	is_run	The engine is running
1	target_pos	The engine stopped in the target position
2	left_sig	Left marginal signal was active
3	right_sig	Right marginal signal was active
4	u_alarm	Supply voltage out of range of engine operation
5	i_alarm	Exceeded the maximum allowable motor current

The alarm flags are automatically reset after sending a new command to the engine. If the engine moves to the left and the right alarm final signal is given, it means that the breakers are damaged. CONFIG (A501) register allows the customization of the controller to the type of engine and selection of the type of control.

The importance of bits in CONFIG register (A501)		
Bit No.	**Symbol**	**Function Description**
0	**mot_4_phase**	1 - 4-phase motor 0 - engine 2 - phase winding in the middle
1	**mot_half_step**	1 – half-step control 0 - full stepper control
2	**kbd_control**	1 - control the operation of the engine with the keyboard 0 - control the operation of the engine via the host
3	**nc_left_pol**	1 - left NC (Normal Closed) signal switch 0 - left NO (Normal Open) marginal signal
4	**nc_right_pol**	1 - right NC (Normal Closed) marginal signal 0 - right NO (Normal Open) marginal signal
5	**stop_left_pwr**	1 – stopping the engine leaves voltage (torque) 0 – stopping the engine does not leave the voltage (torque)

COMMAND (A108) register is used to control motor movement. Record Registry is possible when kbd_control bit is 0, which means that the engine is controlled by the host.

The meaning of bits of the COMMAND register (A108)		
Command	**Symbol**	**Function Description**
0	**STOP**	The order to stop the engine
1	**POS**	The order of movement to a designated position
2	**LEFT**	The order of movement to the left to the extreme signal
3	**RIGHT**	The order of movement to the right to the limit signal
4	**SAVE_POS**	The command of writing the motor position in EEPROM memory

Setting the COMMAND register does giving an order to the motor controller. It is possible only when the driver does not execute any command (the controller is in STOP state) except the STOP command that is always possible.

3. PIEZO CONTROL

The main purpose of piezo control module is to provide electrical signals for driving piezos in superconducting accelerating module of FLASH. The piezos are used to compensate Lorentz Force Detuning of the superconducting cavities excited by high electromagnetic field and in limited range to tune the cavities. The electrical bias of the piezo results in changes of piezo dimensions and cavity itself and consequently in changes of cavity resonant frequency.

Some of the FLASH accelerating modules are equipped with double piezos at each cavity – one can be used as an actuator and at the same time the second one as a vibrations sensor. The piezo controller must support both modes of piezo operation.

The main requirements for piezo control come from a high voltage needed to excite piezo and relatively high capacitance of the piezo element. Therefore the piezo control system must be able to provide required voltage and current with parameters adjusted to the operating condition of the cavity. The lifetime of the piezo depends on the voltage applied and other operating conditions. Therefore the control should be realized in a way using lowest possible and limited to the safe region voltage levels, lowest possible and limited to the safe region current and smooth rising up and falling down of current to avoid overvoltage generation in parasitic cable inductance. The control should also allow maximization of the lifetime by periodically swapping the piezos (actuator and sensor).

In order to fulfill all these goals the piezo control board has been designed.

3.1. DESIGN OF PIEZO CONTROL SYSTEM

The block diagram of the designed piezo control board is presented in Figure 2. The main functionality (driving piezos) is realized by 16 power amplifiers (PZD) driven by 16-channels DAC. The signal from piezo sensors is conditioned in instrumentation amplifiers (PZS) and sampled by 16-cannels ADC. The switching between actuators/sensors is provided by 16 relays. The control logic and communication interfaces are realized by FPGA Spartan 6 device. The voltages and temperature monitoring is realized by AD converters and temperature sensors connected to the central FPGA. The temperature is monitored in 3 places at the PCB – one of them is a middle point of power amplifiers area. The system is powered by power supply unit from Vicor.

The PCB board is placed in 2U, 19 inch box. The cooling air is provided by fans assembled in the front and back panel sides forcing the air flow from front to back. The digital input/output connectors as well as status LEDs are placed on the front panel side.

The piezo control system communicates with outside world using fast serial LVDS links. Optionally the communication can be also provided through optical links. The connectors are placed at the front panel.

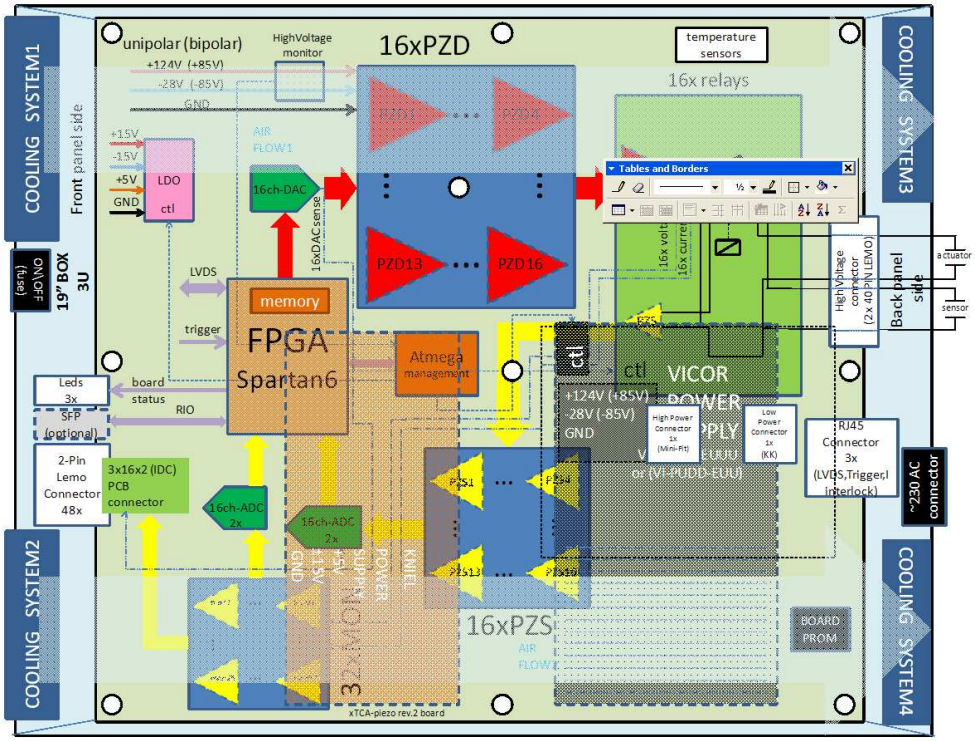


Figure 2 Basic block diagram of sixteen-channel Piezo module

3.2. ANALOGUE PART OVERVIEW

The single channel piezo drive consists of pre-amplifier and power amplifier stages. The global gain of the circuit is adjusted using external resistors. The output voltage is sensed using voltage dividers and sampled by monitoring ADC. The output current is measured using additional 1 Ω resistor and also sampled by monitoring ADC.

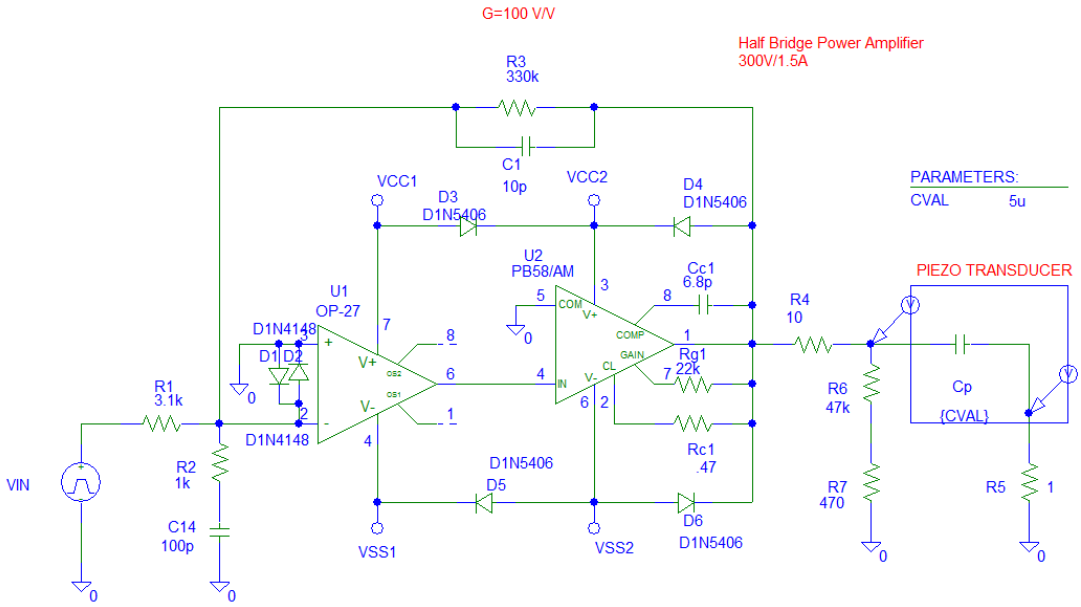


Figure 3 The block diagram of single channel Piezo Driver

3.3. DIGITAL PART OVERVIEW

The digital controller consists of integral interface component, 16-channel DAC component, low-latency link component, DAC-SPI component, ADC_MUX component, 16-channel ADC component and synchronization component. Integral interface component is used to communicate with outside world using rs232 interface. It allows using bits, registers and memory blocks directly defined inside FPGA device. The memory blocks are used to store the waveform for each DAC channel as well as data acquisition from each piezo sensor. The registers are used to set i.e. the each channel DC voltage offset or AC amplitude. Low-latency link component is used to communicate with outside world using fast serial links, i.e. multi-gigabit transceiver (MGT). 16-channel DAC component is used to control external DAC device with the samples stored inside FPGA memory block. The DAC_SPI component is used to communicate with external DAC device with serial peripheral interface (SPI). The synchronization component is used to generate trigger signal and strobe signal. The trigger signal is used to indicate the start of RF field pulse. The strobe signal is used to read the sample from memory block and send it to DAC device through serial link. The 16-channel ADC component is used to control external ADC and multiplexer devices. The controller block diagram is shown in Figure 5.

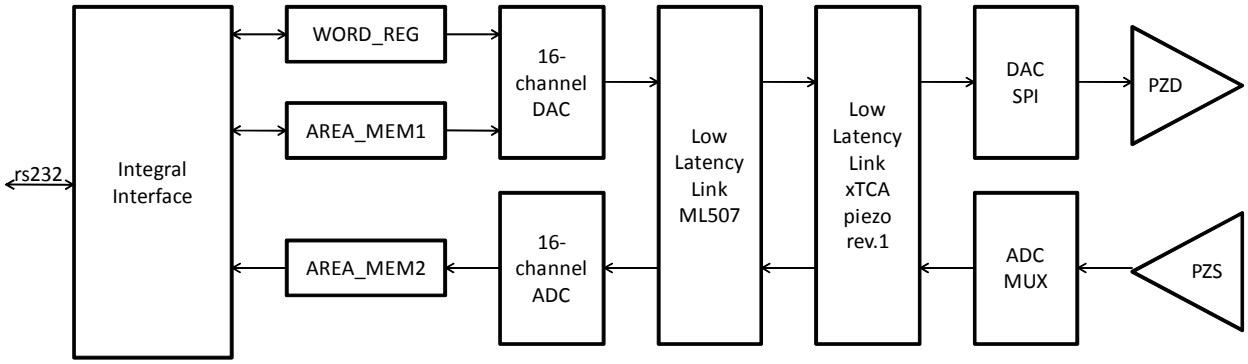


Figure 4. Block diagram of the piezo controller

3.4. 16-CHANNEL PIEZO DRIVER

The piezo control system can be operated using bipolar and unipolar control schemes. For the bipolar control mode the excitation is sinusoidal shape type. The unipolar control mode the excitation is generated using cosinusoidal function. In both modes the number of pulses, frequency, amplitude and DC voltage piedestal can be adjusted. The waveforms of output voltage and currents for both control modes are shown in Figure 5.

The power consumption of the piezo control board in idle conditions (without any driving signals applied) is about 70 W (at the supplying voltages ±96 V). That means the single power amplifier is taking about 20 mA of the quiescent current. The power consumption during normal operation depends on the parameters settings but one have to count few hundreds of watts dissipated in the power amplifiers. Therefore the module has to be equipped with airflow cooling system.

a) *b)*

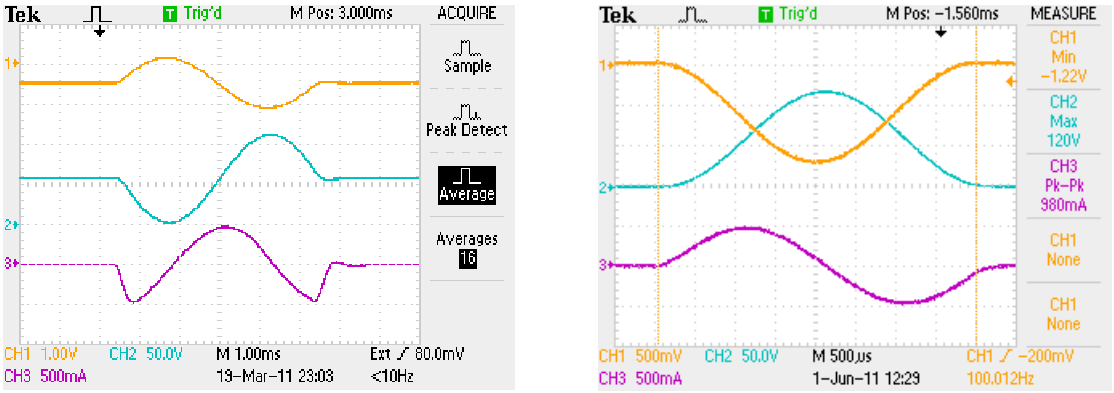
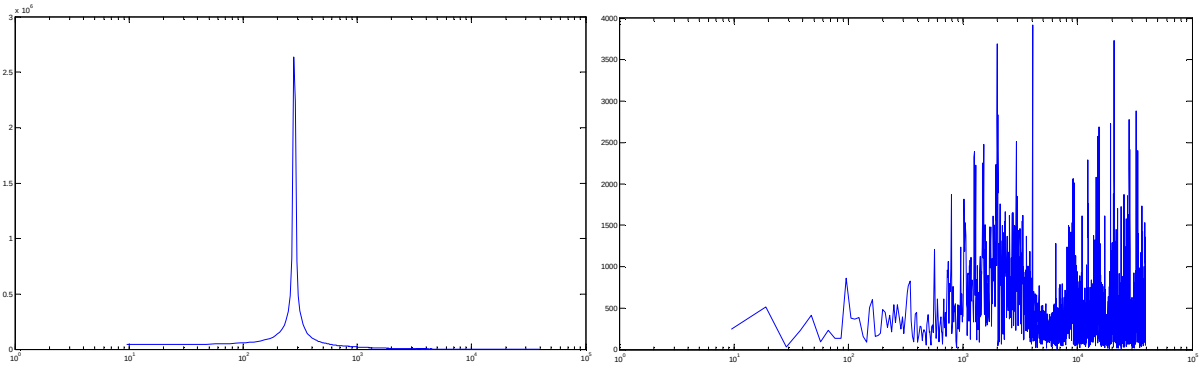


Figure 5. The piezo control schemes: a) bipolar mode – waveform no.1 means amplitude of the input signal, waveform no. 2 means amplitude of output signal, waveform no. 3 means amplitude of the output current; b) unipolar mode – waveform no. 1 means amplitude of the input signal, waveform no. 2 means amplitude of the output signal, waveform no. 3 means amplitude of the output current

3.5. 16-CHANNEL PIEZO SENSOR CIRCUIT

The 16-channel Piezo sensor circuitry tests have been carried out to investigate the maximum switching frequency of the multiplexer used to switch between Piezo sensor channels. The first tests have been carried out to measure the signal to noise ratio of the ADC and chosen piezo sensor channel. The input sinusoidal waveform of frequency of 300 Hz and amplitude of the 5Vp-p has been applied. The FFT analyses of the chosen piezo sensor channel with and without driving signal are shown in Figure 6. The tests results of the other Piezo sensor channels are summarized in Tab. 4.



a b

Figure 6. FFT of captured signal at channel 1. The number of 8192 data points have been taken for analyses, signal to noise ratio is more than 60 dB
a) – channel driven with continuous sinusoidal wave of 300 Hz and amplitude of 5Vp-p
b) left open

4. SUMMARY

The prototypes of the circuits for resonance control of the superconducting cavities at FLASH have been designed and currently they are being manufactured. They are designed to cooperate with uTCA based LLRF system designed for FLASH application. The tests of the whole system at FLASH are foreseen to be performed after June 2012.