

Upgrade of the Trigger System of the ATLAS Liquid Argon Calorimeters

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Abstract—The ATLAS detector was designed and was built to study proton-proton collisions produced at the LHC at centre-of-mass energies up to 14 TeV and instantaneous luminosities up to $10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The ATLAS Liquid Argon (LAr) calorimeters produce a total of 182,486 signals, which are digitized and processed by the front-end and back-end electronics for each triggered event. In addition, the front-end electronics sums analog signals to provide coarse-grained energy sums, called trigger towers, to the first-level trigger system, which is optimized for nominal LHC luminosities. In 2020, instantaneous luminosities of $(2-3)\times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ are expected, far beyond that for which the detector was designed. In order to cope with the increased trigger rate, an improved spatial granularity of the trigger primitives is proposed, to improve the identification performance for trigger signatures at high background rejection rates. For these purposes, a new LAr Trigger Digitizer Board (LTDB) is being designed to receive higher granularity signals, digitize them on-detector and send them via fast optical links to a new digital processing system (DPS). The DPS applies digital filtering and identifies significant energy depositions in each trigger channel. The general concept of the upgraded LAr calorimeter trigger and expected performance as well as the various electronics components to be developed are described.

I. INTRODUCTION

THE ATLAS detector [1] is a general-purpose particle physics detector, designed to study proton-proton collisions produced at the Large Hadron Collider (LHC) at CERN [2]. Successful operation of both the LHC machine and the detectors established the discovery of the Higgs boson in 2012. Two upgrade programs of the LHC, Phase-I (2018-2019) and Phase-II (2023-2025) have been planned. The detectors need to be upgraded to explore the full physics potential of the LHC experiments, further probing of the electroweak sector in the Standard Model and searches for new physics.

II. ATLAS CALORIMETER

The ATLAS calorimeter system [3] is composed of an electromagnetic sector covering pseudorapidity range of $|\eta| < 3.2$, a barrel hadronic calorimeter with $|\eta| < 1.7$, an end-cap hadronic sector with $|\eta| = 1.5 - 3.2$, and a forward calorimeter covering $|\eta| = 3.1 - 4.9$.

The electromagnetic (EM) calorimeter has lead absorbers and liquid argon (LAr) as active material. The calorimeter

absorbers are folded in accordion shape geometry, providing gap free coverage in ϕ . The calorimeter has good energy and position resolution, excellent particle identification capability and fine granularity to minimize the electronics and pileup (multiple interactions per beam bunch crossing) noise contributions. The barrel hadronic sector is a sampling calorimeter of iron and plastic scintillating tiles. The hadronic endcap sector is a LAr sampling calorimeter with copper plate absorbers. The forward sector consists of a LAr calorimeter with rod electrodes in tungsten and copper matrices to achieve narrow LAr gaps to limit the development of space charge at higher luminosities. Fig. 1 shows a cut-away view of the ATLAS calorimeter system. Highly segmented LAr calorimeters comprise 182,486 readout cells in total. The calorimeter system is also used for online event selection (trigger). Fast response and a good timing resolution of a few ns at 1 GeV are required to identify the bunch crossing to which a given event belongs.

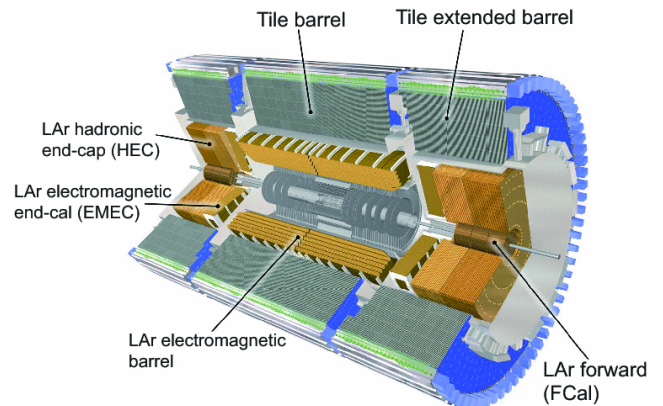


Fig 1. Cut-away view of the ATLAS calorimeter system, depicting the different calorimeter technologies.

III. CALORIMETER TRIGGER SYSTEM

When a charged particle traverses and ionizes the liquid argon in the gap between a LAr electrode and absorbers, an ionization current signal is produced, which is then pre-amplified, shaped, buffered and digitized by the front-end boards (FEBs) installed on the detector. The FEBs send the digitized pulse via optical links to the Readout Drivers (ROD), which are installed in a radiation free area (USA15) next to the detector cavern (UX15). Each ROD receives the data from up

Manuscript received May 22, 2014.

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to 8 FEBs and calculates the energy deposit, the time of the detection and a quality factor of the signal, using an optimal filtering algorithm [4]. RODs send data to the Readout Buffers (ROBs) hosted on PCs (Readout Subsystem, ROS). In parallel analog trigger sum signals are formed on front-end electronics boards and sent to the receiver system before interface to the Level-1 calorimeter trigger system (L1Calo). The LAr calorimeter front-end electronics system is installed on detector in 58 Front End Crates (FEC), which house 1,524 FEBs and other electronics boards. The back-end electronics system consists of 16 back-end crates and 68 ROS PCs, and there are total 192 RODs plugged in back-end crates.

The current ATLAS trigger system has been designed to work up to the LHC design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and produce an average output rate of 200 Hz [5]. It comprises the hardware based L1 and software based High-level trigger (HLT) systems for fast trigger algorithms. The L1 trigger rate is limited by the readout bandwidth of the front-end detector electronics to about 100 kHz while the L1 trigger latency is limited by the depth of the front-end detector pipeline memories up to 2.5 μs . The majority of the ATLAS front-end electronics will remain unchanged at Phase-I upgrade, while the instantaneous luminosity will be increased up to $(2-3) \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ in 2020, exceeding the LHC nominal design luminosity. The HLC system has full granularity and full precision information, and able to maintain an acceptable trigger rate by using offline-like algorithm to minimize the impact of the pileup efficiently. On the other hand, it is not feasible at the current L1 system due to the limited granularity information available. The strategy of the L1Calo trigger upgrade for Phase-I is to use high-granularity and high-resolution digitized data from the LAr EM calorimeter, in order to run more effective algorithms, improving electron/photon separation from jets while retaining the low transverse energy (E_T) threshold.

The geometrical representation of an EM trigger tower in the η - ϕ plane is illustrated in Fig. 2. In the current system, a total of 64 readout cells are summed to form the EM trigger tower. The new finer granularity scheme (Super Cell), which provides the information of each calorimeter layer with improved spatial granularity, $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ in the front and middle layers of the EM calorimeter in $|\eta| < 2.5$. The digitization precision of the Super Cell signals is improved by at least a factor 4 compared to the current L1Calo. The quantization scale and dynamic range of the digitizers are optimized in each η -region and for each layer of the calorimeter, to achieve sensitivities at the level of the Super Cell electronic noise or better.

The performance of the following shower shape quantities has been studied as discriminating variables:

R_η : Given a 3×2 group of Super Cells in $\eta \times \phi$ centered on the highest-energy Super Cell in the middle layer, R_η is defined as the transverse energy measured in the 3×2 group divided by the transverse energy measured in a 7×2 group.

f_3 : The ratio of the transverse energy measured in the back EM layer in an area of size $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ to that deposited in all three layers. The energies in the front and

middle EM layers are reconstructed in the area $\Delta\eta \times \Delta\phi = 0.075 \times 0.2$.

$\omega_{\eta,2}$: The spread of the shower in the middle EM layer in a 3×2 Super Cell region, defined as an energy weighted root-mean-square.

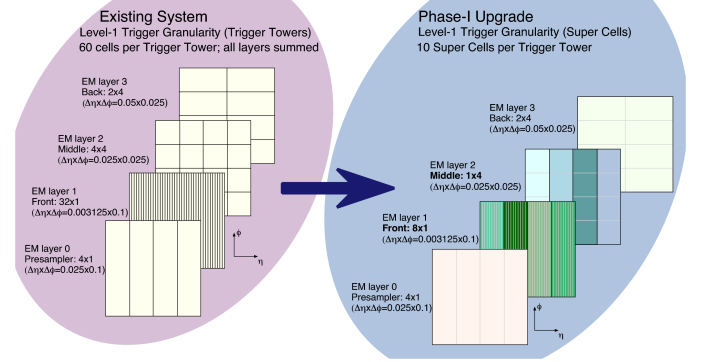


Fig. 2. Geometrical representation in (η, ϕ) space of an EM trigger tower in the current system, where the transverse energies in all four layers are summed (left) and of the Super cells proposed for the Phase-I upgrade, where the transverse energy in each layer is retained in addition to the finer granularity in the front and middle layers (right).

Fig. 3 shows the dependence of the single-electron trigger rate as a function of the E_T threshold for different run conditions. It is important to retain a low lepton E_T threshold for some physics processes and the detector calibration. The use of the shower shape variables reduces E_T threshold from 28.5 GeV to 21.5 GeV (efficiency of 95 %) for a given baseline bandwidth of 20 kHz.

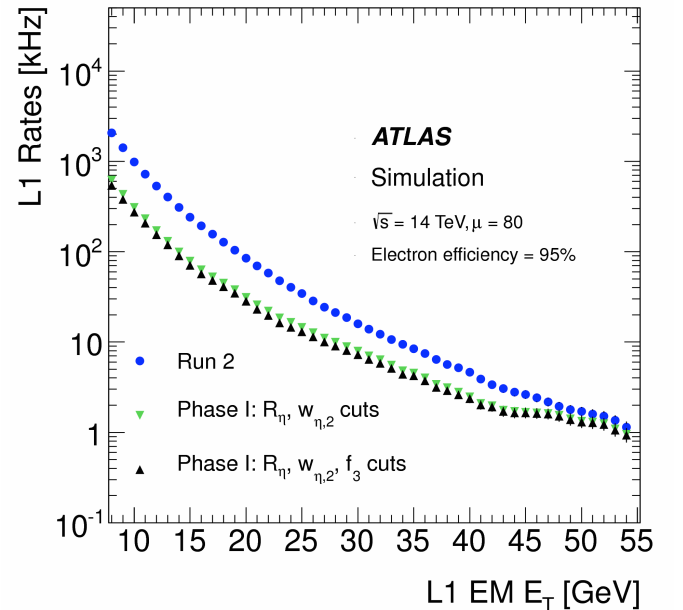


Fig 3 Trigger rates for the luminosity of $3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ as a function of E_T thresholds for different conditions; without Super Cells (blue points) and using Super Cells with different sets of discriminating variables (green and black points).

IV. NEW TRIGGER READOUT ARCHITECTURE

Fig. 4 shows a schematic diagram of the proposed upgrade electronics [6]. The use of the scheme based on Super Cells requires a replacement of the Layer Sum Boards (LSBs) for the front and middle layers. The new LAr Trigger Board Digitizers (LTDBs) will be added to receive analog signals from LSBs, to build analog sums as input for the Trigger Builder Boards (TBBs), to digitize Super Cell analog signals and finally to serialize data and send them to off-detector using high speed optical links. Each LTDB will process up to 320 Super Cell signals. The high performance ADC components for this board are under development. They will have a 12-bit dynamic range and must operate at 40MHz with low power consumption. One commercial option is under test and two series of custom circuits are being designed.

The LTDB design will incorporate a high-speed serializer and allow a least significant bit of 32 MeV in the front layer and 125 MeV in the middle layer. The base planes of the FECs will be rebuilt to handle the modified signal routing between LSBs, TBBs and LTDBs.

The LAr Digital Processing System (LDPS) will receive the digital signals from the 124 LTDBs and transmit the data to the L1Calo trigger system. There are planned to be FPGA based processing units, which apply digital filtering techniques to convert raw ADC sampling data to a calibrated transverse energy. The LDPS is made up of 31 LAr Digital Processing Blades (LDPBs) housed in three ATCA (Advanced Telecom Computer Architecture) shelves. Each LDPB consists of one carrier board equipped with four Advanced Mezzanine cards (AMCs), for a total of 124 AMCs. The AMC is designed around a powerful FPGA with high speed transceivers that will process the data up to 320 Super Cells within the latency budget (425 ns for LDPS). In addition to receiving ~ 25 Tb/s for 34,000 Super Cells, the LDPS transmits ~ 41 Tb/s over optical fibers to L1Calo system. The efficient handling of the large data volume is challenging.

V. R&D FOR THE ELECTRONICS UPGRADE

The following sections describe some of main R&D activities for LAr calorimeter readout electronics upgrades.

A. Mixed signal front-end ASICs

Super Cell signals must be digitized at 40 million samples per second (MSPS) by the ADC on the LTDB. This ADC must meet the stringent requirements listed in Table 1. The main challenge is to cover the full 16-bit dynamic range with one or more ADCs per channel. A commercial off-the-shelf option (the Texas Instruments ADS5272) has been identified as a candidate for the LTDB. There are also two series of custom ASIC developments based on the IBM CMOS8RF (130nm) technology, a 4-stage SAR-based pipeline ADC and a full SAR-based architecture ADC.

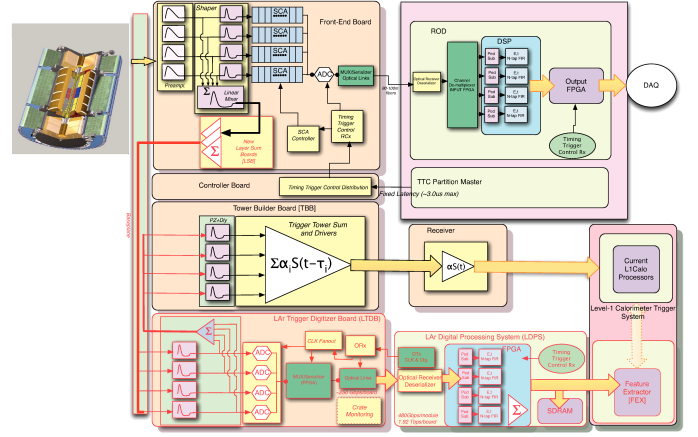


Fig. 4. Schematic block diagram of the Phase-I upgrade LAr trigger readout architecture. The new components are indicated by the red outlines and red arrows.

The latter ADC is named PEALL (Power Efficient and Low Latency) with the following characteristics: 4 channels, short latency (25ns), 12-bit resolution, 40 MSPS sampling speed and low power consumption (below 10 mW per channel without the reference voltage). One innovative feature of this chip is a high-speed clock internally generated by the ADC from a regular external 40MHz clock. In comparison to a classical successive approximation register ADC design, this feature helps to save significant power consumption. The final decision will be taken, based on the development work and test results.

Parameters	Requirement	ADS5272
Sampling rate	≥ 40 MSPS	40 MSPS
Dynamic range	12 bits	12 bits
Resolution (ENOB)	≥ 11	11.5
Differential Nonlinearity	≤ 1 lsb	0.3 lsb
Integral Nonlinearity	≤ 1 lsb	0.4 lsb
Latency	≤ 200 ns	162.5 ns
Power consumption	≤ 145 mW	113 mW

Table 1 Specifications for the ADC. The latency is the time between the first sample and the last bit out. The power consumption is given per ADC channel at 40MSPS.

B. High-speed off-detector FPGA based DPS units

In order to perform the required functions of the AMC, the FPGA must have 54 transceivers, sufficient DSP processing power, and ample memory in RAM blocks. The FPGA is associated to external memories like Flash, DDR3 (Double Data Rate type-III) or SDRAM (Synchronous Dynamic Random Access Memory) for firmware and temporary buffering. The FPGA transceivers must run at compatible link speeds, 5.12 Gb/s for the receivers and 10 Gbps for the transmitters. Table 2 shows the estimate of the total required resources for the FPGA. The expected FPGA resources are evaluated by coding one overall VHDL infrastructure for the full 320 channels. This includes all aspects of AMC operation,

where a FIR filter with χ^2 maximum detection is implemented to compute transverse energies (16 DPS blocks needed to evaluate one Super Cell). The resources needed for the AMC FPGA seems to be fulfilled with two high-end FPGAs expected to be available in 2014-2015. The crucial limit of 150 ns processing time is fulfilled by the Wiener filtering with the active forward out-of-time pileup correction, which is one promising technique for improving energy resolution.

The reception (transmission) of the ADC data from the LTDB (to L1Calo) is performed through high-density optical receiver (transmitter). The baseline design is that each AMC will handle 48 fibers for reception (Rx) and 48 fibers for transmission (Tx) to maximize the density of components, and to minimize the size of the system. The baseline choice for the 12-fold fiber connector is the MicroPOD optical connector. It has a package dimension of 7.6 mm (L) \times 7.6 mm (W) \times 3.9 mm (H), but must be embedded in a heat sink due to its significant power consumption (less than about 3W per component). Fig. 5 shows the results of transmission test between two test boards.

The test board is equipped with two sets of Rx and Tx microPOD connectors, and mounted in on the Xilinx evaluation kit, KC705, and evaluated with the Xilinx IBERT (The LogiCORE Integrated Bit Error Rate), which can evaluate up to 12.5 Gb/s. No error was observed in 2.6-days run, corresponding to a bit error rate of less than 1×10^{-15} .

Resource	Estimated Requirement	Specification	
		FPGA-I	FPGA-II
Register [10^3]	184	1424	1300
LUT [10^3]	120	712	900
TX/RX	54	96	96
DSP	778	3360(*)	1518(*)
BlockRam [Mbit]	13.5	67.7	57.0

Table 2 Summary of the total estimated resources required for the firmware running in the AMC FPGA and specifications of the two commercial FPGAs, Xilinx Virtex-7(FPGA-I) and Altera ARRIA-10 (FPGA-II). (*) The numbers of DSP cells between the two types of FPGAs are not directly comparable since they are integrated in multi-functional processing blocks.

VI. SUMMARY

An upgrade of the trigger readout for the ATLAS LAr calorimeters is essential for running at high luminosity and pileup conditions. The improved spatial granularity of the trigger primitives can reduce the trigger rate by improving the identification performance and energy resolution. The R&D studies are in progress towards Phase-I and Phase-II upgrades. The full system test of the upgrade electronics is going smoothly at CERN, and in-situ demonstrator is foreseen for the run starting in 2015.

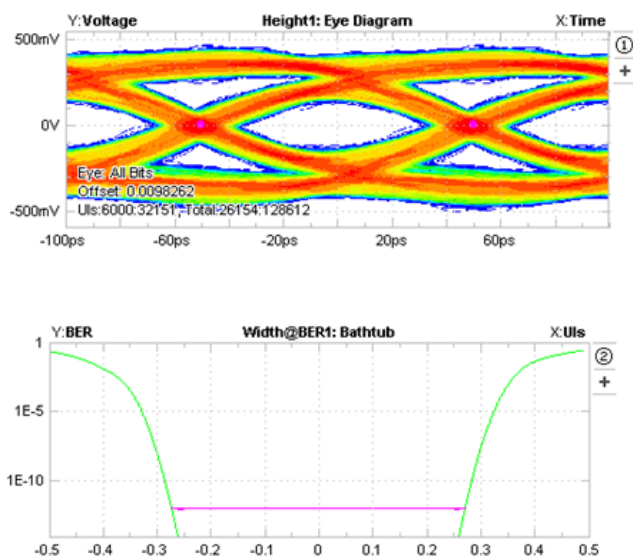


Fig. 5. Result of microPOD transmission test with route length of 69 and 25 mm for the carrier board and daughter boards and with 5 vias, “eye-diagram” (top) and “bathtub curve” (bottom).

ACKNOWLEDGMENT

The work presented in the paper has been performed within the ATLAS collaboration, and the author would like to thank to the collaboration members for the important contributions and useful comments.

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