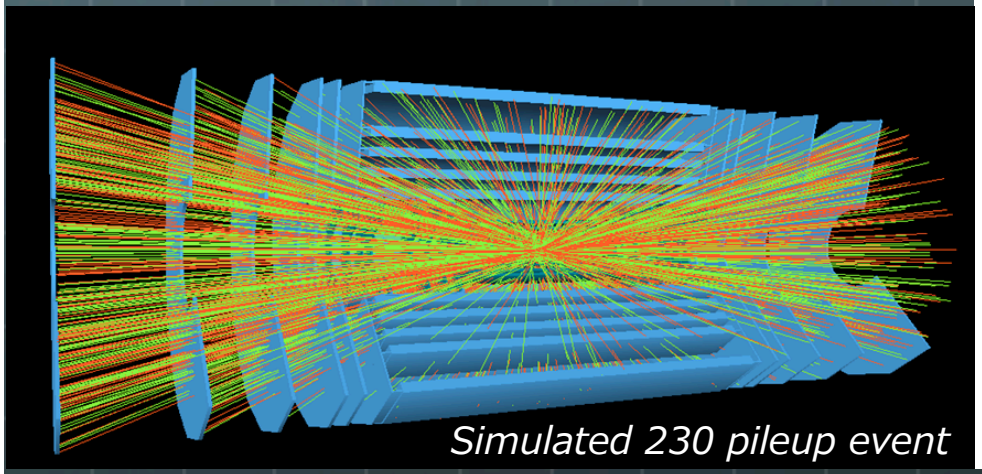
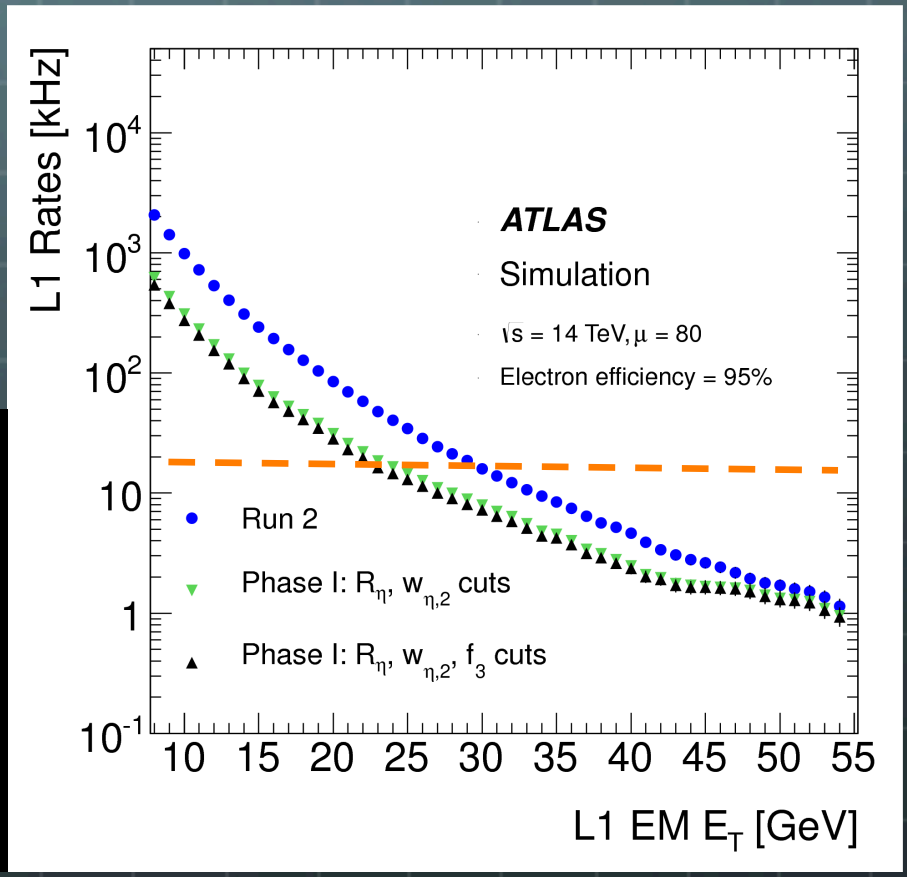
Upgrade of the Trigger System of the ATLAS Liquid Argon Calorimeters

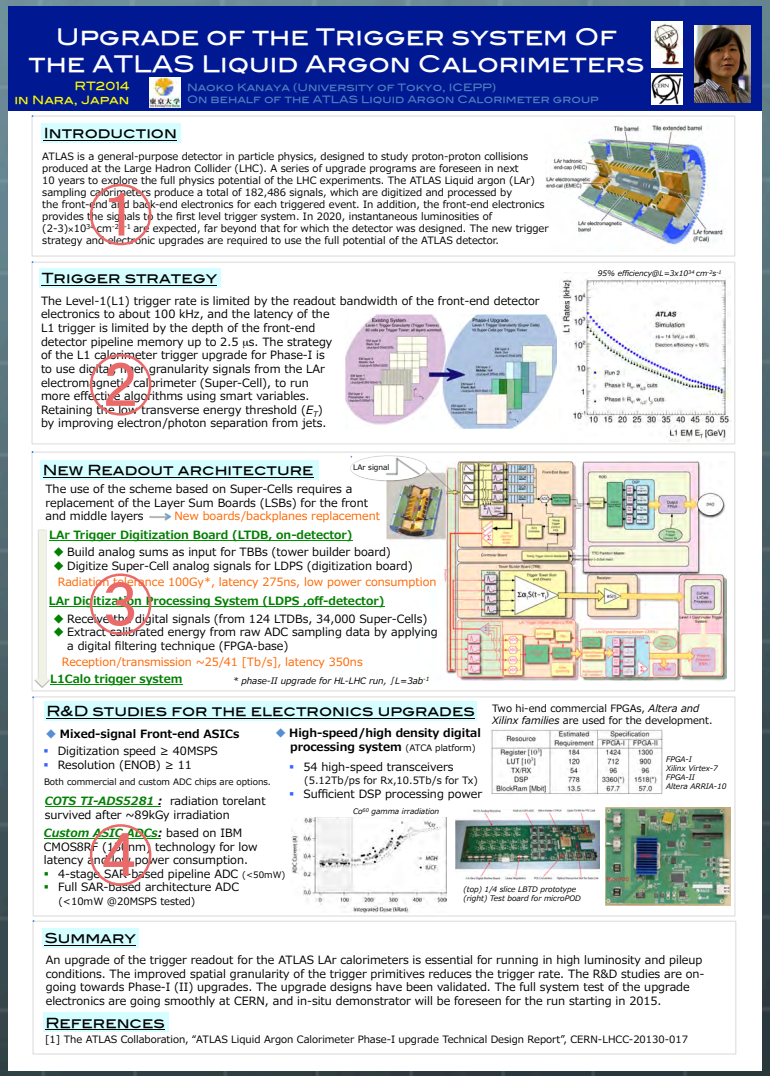
The ATLAS detector is a general purpose detector in particle physics, designed proton-proton collisions at the Large Hadron Collider (LHC) at CERN.





Naoko Kanaya on behalf of the ATLAS Liquid Argon Calorimeter group

Poster



UPGRADE OF THE TRIGGER SYSTEM OF THE ATLAS LIQUID ARGON CALORIMETERS

RT2014 IN NARA, JAPAN

NAOKO KANAYA (UNIVERSITY OF TOKYO, ICEPP)
ON BEHALF OF THE ATLAS LIQUID ARGON CALORIMETER GROUP

INTRODUCTION

ATLAS is a general-purpose detector in particle physics, designed to study proton-proton collisions produced at the Large Hadron Collider (LHC). A series of upgrade programs are foreseen in next 10 years to explore the full physics potential of the LHC experiments. The ATLAS Liquid argon (LAr) sampling calorimeters produce a total of 182,486 signals, which are digitized and processed by the front-end and back-end electronics for each triggered event. In addition, the front-end electronics provides the signals to the first level trigger system. In 2020, instantaneous luminosities of (2-3)x10^{34} cm^{-2}s^{-1} are expected, far beyond that for which the detector was designed. The new trigger strategy and electronic upgrades are required to use the full potential of the ATLAS detector.

TRIGGER STRATEGY

The Level-1(L1) trigger rate is limited by the readout bandwidth of the front-end detector electronics to about 100 kHz, and the latency of the L1 trigger is limited by the depth of the front-end detector pipeline memory up to 2.5 μs. The strategy of the L1 calorimeter trigger upgrade for Phase-I is to use digital fine granularity signals from the LAr electromagnetic calorimeter (Super-Cell), to run more effective algorithms using smart variables. Retaining the low transverse energy threshold (E_T) by improving electron/photon separation from jets.

NEW READOUT ARCHITECTURE

The use of the scheme based on Super-Cells requires a replacement of the Layer Sum Boards (LSBs) for the front and middle layers → New boards/backplanes replacement

LAr Trigger Digitization Board (LTDB, on-detector)
- Build analog sums as input for TBBs (tower builder board)
- Digitize Super-Cell analog signals for LDPS (digitization board)

Radiation tolerance 100Gy*, latency 275ns, low power consumption

LAr Digitization Processing System (LDPS ,off-detector)
- Receive the digital signals (from 124 LTDBs, 34,000 Super-Cells)
- Extract calibrated energy from raw ADC sampling data by applying a digital filtering technique (FPGA-base)

Reception/transmission ~25/41 [Tb/s], latency 350ns

L1Calo trigger system

* phase-II upgrade for HL-LHC run, ∫L=3ab^{-1}

R&D STUDIES FOR THE ELECTRONICS UPGRADES

Two hi-end commercial FPGAs, *Altera and Xilinx families* are used for the development.

Resource	Estimated Requirement	Specification FPGA I	Specification FPGA II	
Register [10^3]	184	1424	1300	FPGA-I Xilinx Virtex-7 FPGA-II Altera ARRIA-10
LUT [10^3]	120	712	900	
TX/RX	54	96	96	
DSP	778	3360(*)	1518(*)	
BlockRam [Mbit]	13.5	67.7	57.0	

◆ **Mixed-signal Front-end ASICs**
- Digitization speed ≥ 40MSPS
- Resolution (ENOB) ≥ 11

Both commercial and custom ADC chips are options.

COTS TI-ADS5281 : radiation torelant survived after ~89kGy irradiation

Custom ASIC ADCs: based on IBM CMOS8RF (130nm) technology for low latency and low power consumption.
- 4-stage SAR-based pipeline ADC (<50mW)
- Full SAR-based architecture ADC (<10mW @20MSPS tested)

◆ **High-speed/high density digital processing system** (ATCA platform)
- 54 high-speed transceivers (5.12Tb/ps for Rx,10.5Tb/s for Tx)
- Sufficient DSP processing power

Co^{60} gamma irradiation

(top) 1/4 slice LBTD prototype
(right) Test board for microPOD

SUMMARY

An upgrade of the trigger readout for the ATLAS LAr calorimeters is essential for running in high luminosity and pileup conditions. The improved spatial granularity of the trigger primitives reduces the trigger rate. The R&D studies are on-going towards Phase-I (II) upgrades. The upgrade designs have been validated. The full system test of the upgrade electronics are going smoothly at CERN, and in-situ demonstrator will be foreseen for the run starting in 2015.

REFERENCES

[1] The ATLAS Collaboration, "ATLAS Liquid Argon Calorimeter Phase-I upgrade Technical Design Report", CERN-LHCC-20130-017

① LHC upgrades & motivation

RUN2 : 2015-2017
Phase-I upgrade :2018-2019 ←
RUN3 : 2020-2022
Phase-II upgrade 2023-2025
HL-LHC : 2026~

② New event trigger strategy and improved performance expected.

③ Required electronics upgrades for the new trigger strategy

④ R&D studies for electronics upgrades (also towards Phase-II upgrades)

- Fast signal sampling (on-detector)
- FPGA-based digital processing system
- High-density optical Tx/Rx

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