Radiation tolerance of a SLVS receiver based on commercial components

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ABSTRACT: The capability of ProASIC3L FPGAs to receive SLVS signals has been studied in laboratory condition and after irradiation.

KEYWORDS: SLVS; ProASIC3; radiation.

CERN-OPEN-2013-043
22/12/2013

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Contents

1. SLVS signaling protocol

SLVS is a standard signalling protocol with a nominal VOL of 0V (ground) and a nominal VOH of 400 mV [1]. It finds application in data communications and image displays requiring high-speed and low-power. It is gaining some popularity in data acquisition systems for High Energy Physics experiments, an example is described in [3]. Although it has been standardized in 2001, it is still difficult to find commercial electronic components capable to translate SLVS to or from other protocols. As of today, no studies are known to the authors about the radiation tolerance of such commercial components. In this article we present our first results in this respect.

1.1 Component selection

This paper presents a series of tests of SLVS reception capabilities and their radiation tolerance in a Flash-based FPGA, the 0.13-um ProASIC3L product family (A3PL). Nominally this family of FPGAs supports LVDS but does not support SLVS. According to the Table 2-174 of reference [2], the electrical characteristics of the LVDS input buffers are:

Input Common Mode Voltage Min	50 mV
Input Differential Voltage Min	100 mV

According to these electrical characteristics, the LVDS input buffers appear to be capable to receive SLVS signals. We have then tested this hypothesis.

2. Electrical Tests

Electrical tests in a normal lab environment were performed to verify the capability to receive SLVS signals. We have used the Cortex-M1 ProASIC3L Development Board (Part Number M1A3PL-DEV-KIT sold by Actel) together with an test card shown in Figure 1. This card has a socket U1 with an LVDS-SLVS translator ASIC (CRT758) developed by CERN and described on section IV.C of reference [3].

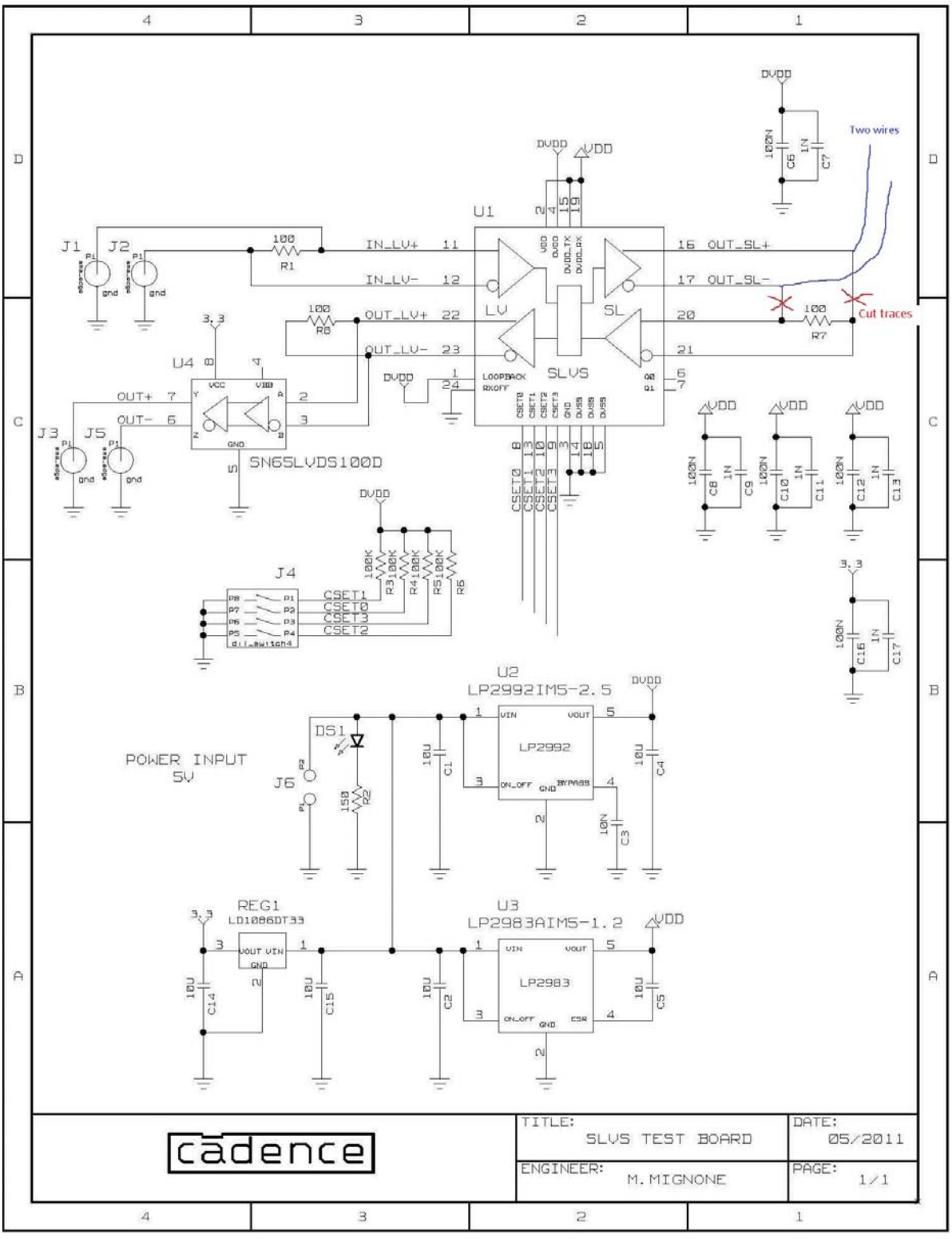

Figure 1: SLVS test board (Courtesy of INFN Torino) modified for the purpose of the test.

The concept of the test is to generate a signal in the FPGA, send it out as LVDS to the translator (and send out a copy as CMOS to an oscilloscope), then the translator converts it to an SLVS signal which is sent back to the FPGA. The FPGA receives it with an LVDS input buffer, then the resulting signal is sent out to a scope as CMOS for comparison. Figure 2 shows a block diagram of the test apparatus

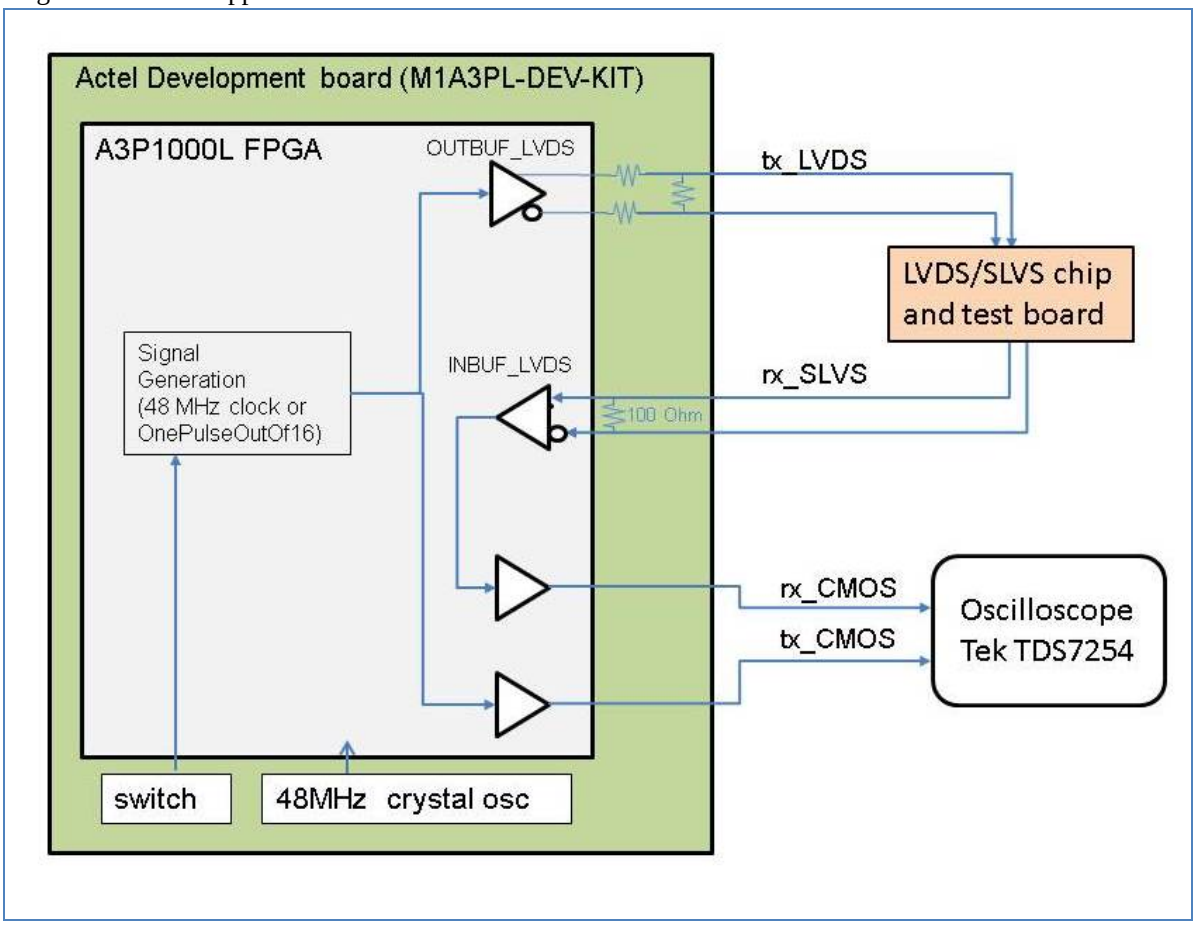

Figure 2: Apparatus for the electrical test. The oscilloscope is used with single-end active probes.

No particular effort has been done to minimize the electrical noise of the apparatus, shown on photography on **Error! Reference source not found.**. The LVDS signal is transmitted over two coaxial cables into two SMA connectors; the shields of the coaxial cables are connected to the ground of the Actel board (brown wire). The SLVS signal is transmitted over two unshielded wires into a header connector on the Actel board. The two active probes are connected to tx_CMOS and rx_CMOS.

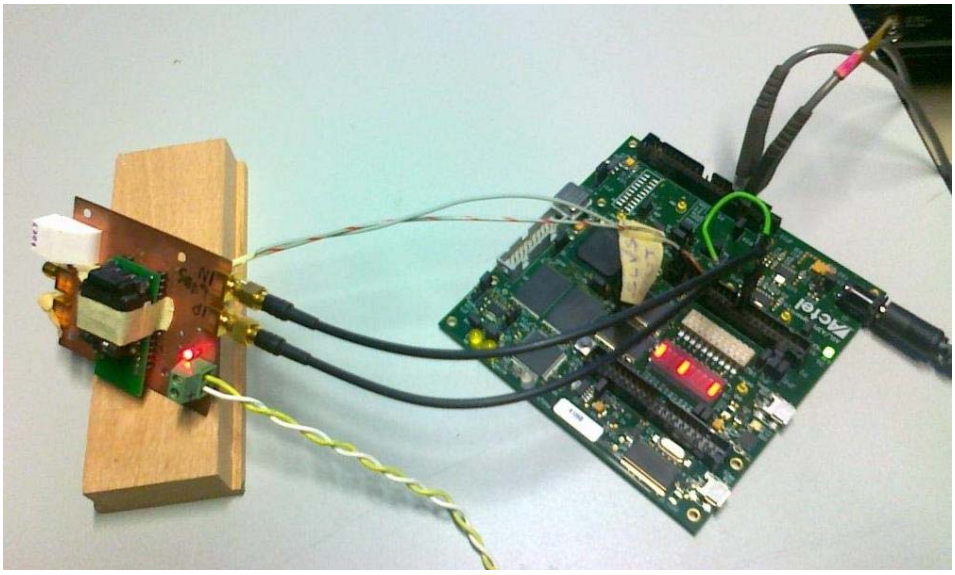

Figure 3: apparatus for the electrical tests, the LVDS/SLVS translator chip is on a socket on the left side.

We have created an Actel project following the scheme in Figure 2. The FPGA doubles the frequency of the 48MHz clock signal with one of its PLL and generates an internal 96MHz clock (period of ~10.4 ns), used to generate synchronous signals. Based on the position of the on-board switch, the FPGA can generate a different signals, including a clock-like signal (shown on Figure 4) or a signal with a positive pulse of about 10.4 ns followed by about 156ns (15 cycles of the 96MHz clock) where the signal remains low. This signal emulates applications with fast synchronous commands. The resulting generated signal is shown on Figure 5. In all cases, the FPGA has shown to be able to receive correctly the SLVS signal.

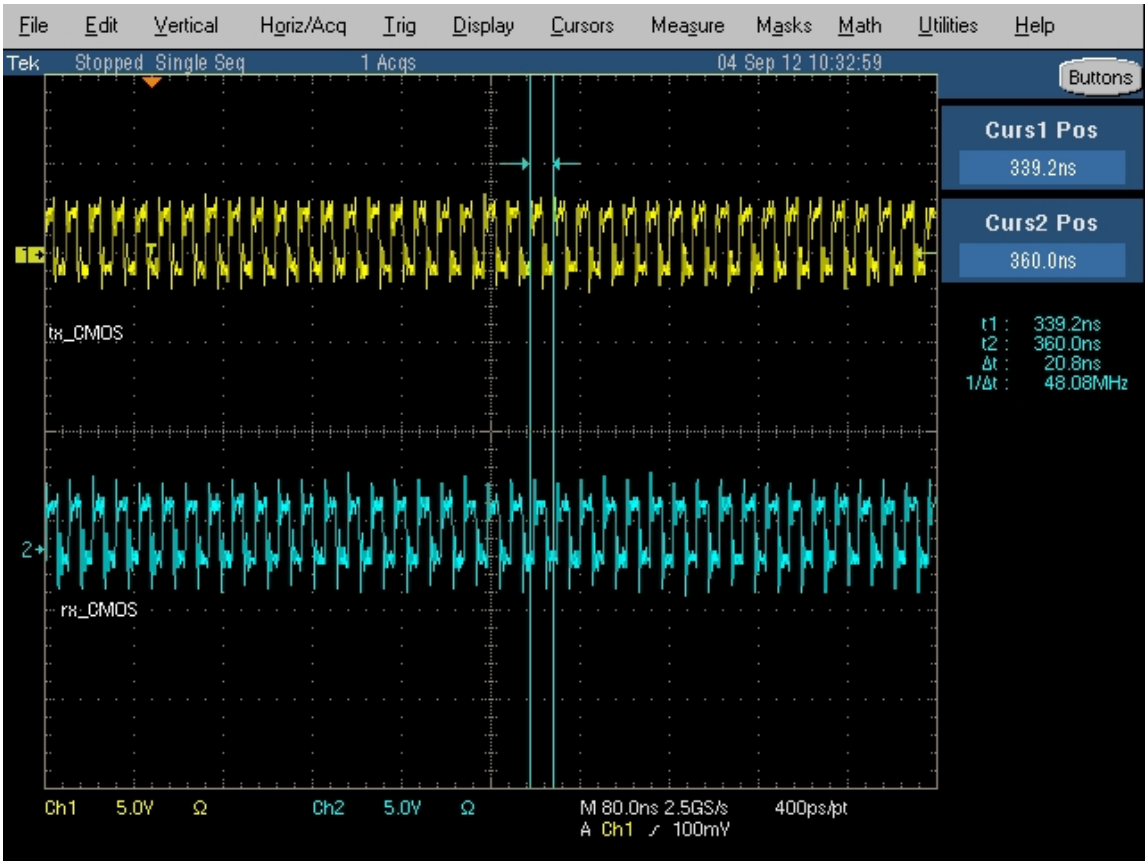

Figure 4: 48MHz signals at the beginning and at the end of the chain.

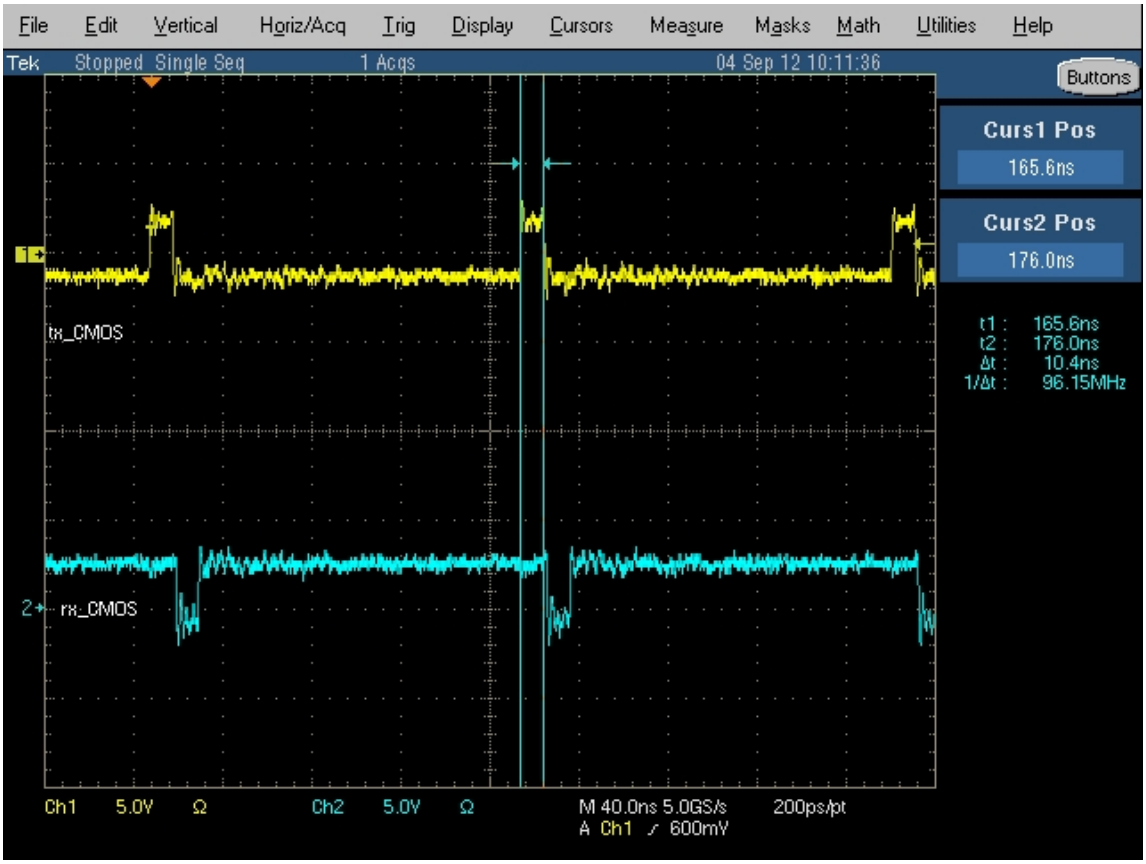

Figure 5: a non DC-balanced signal at the beginning and at the end of the chain.

The SLVS board has a 4-bit switch which allows modulating the output current between 0.5mA and 2mA. The ProASIC3L FPGA receives correctly the SLVS signal for all values of the current in this range. Note that the termination on the Actel board is 100 Ohm, thus setting the current at 2mA generates a voltage swing of 200mV per wire, which corresponds to the standard SLVS levels. Setting the current to 0.5mA generates a swing of only 50mV per wire (100mV Input Differential Voltage, which correspond to the low end of the LVDS characteristics of the ProASIC3L).

The electrical tests show that the ProASIC3L FPGA is capable to receive a 48MHz SLVS signal using an LVDS input. The test setup described here is not suitable for fine measurements of jitter and noise margins.

3. Irradiation tests

Having verified that ProASIC3L FPGAs can receive SLVS signals in a normal lab environment, we have tested the same capability on a radiation environment. The ProASIC3L FPGA has already been tested under radiation [6], but none of the previous tests has verified the SLVS capabilities. In the test of SLVS reception capability, we do not need to test SEU because SEU is a concern for memory elements, which is not the case of the circuitry used to receive SLVS. So we only need to test the tolerance to TID. A test apparatus different from what described in the previous sections has been prepared. The Device Under Test (DUT) is a A3P250L FPGA from the ProASIC3L family of Microsemi. It is mounted on the tests card shown in Figure 6.

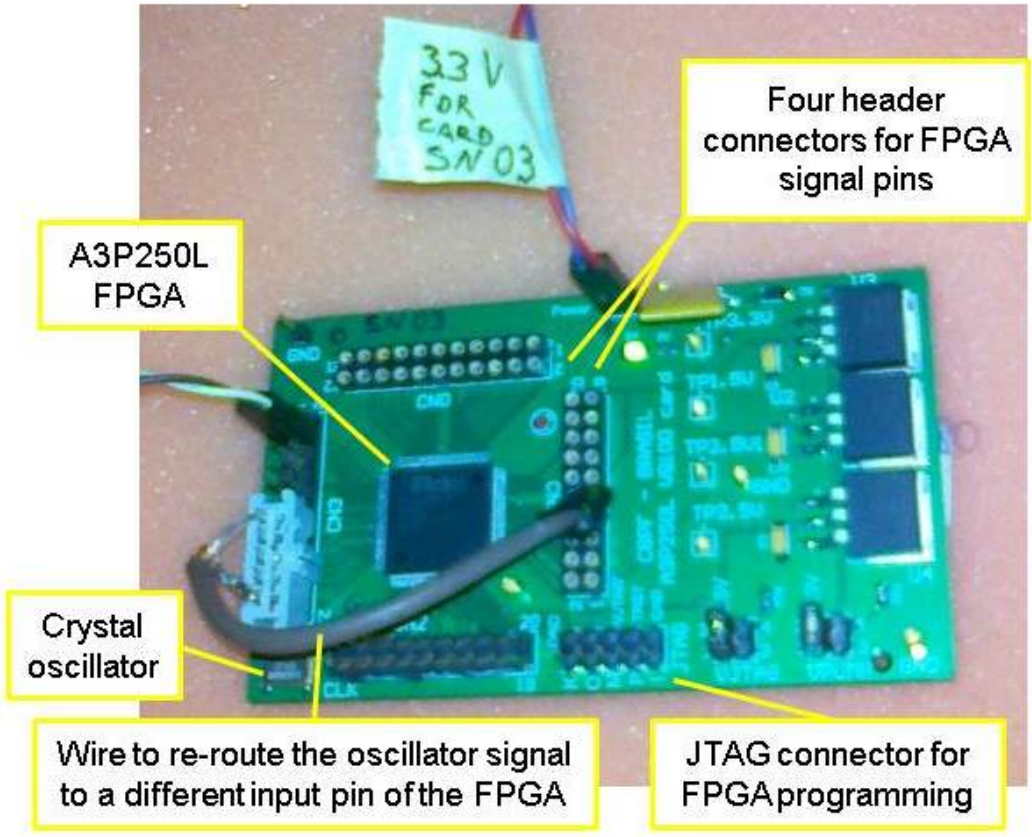

Figure 6: test card designed by CBPF (Brazil).

The FPGA has been programmed with a simple design which has four LVDS inputs connected to four LVDS outputs, without any logic or memory element in between.

The irradiation facility used is the Gamma Irradiation Facility (GIF) at CERN [4] During the irradiation, the DUT has always remained powered up, one of the input was constantly fed with a toggling SLVS signal generated by the card on Figure 1 via a 3-meter network cable, two of the inputs were fed with toggling LVDS signals (via the same network CAT6 cable) and the forth input was left unconnected. This apparatus has been mounted on the Gamma Irradiation Facility, as shown in **Error! Reference source not found.**. While leaving the setup mounted on the GIF facility, we have periodically stopped the irradiation and we have measured the activity on the outputs, using the cable labelled "OUT" on **Error! Reference source not found.**.

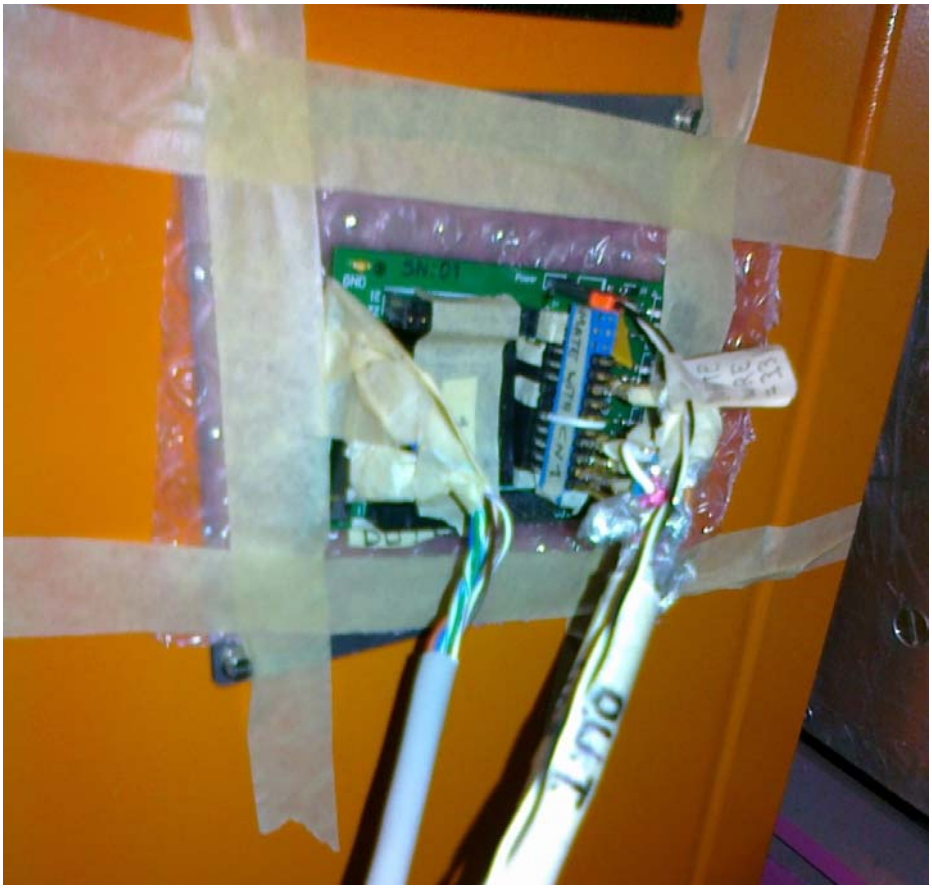

Figure 7: DUT mounted on a window of the GIF Cesium source at CERN.

To measure the Total Ionizing Dose absorbed by the DUT, we have used dosimetric films of the same type described on section III.B of reference [5]. The strips were mounted on the side of the DUT away from the source (so the DUT was in between the source and the films).

After a Total Dose of at least 201 Gy, we have removed the DUT from the radioactive environment and measured its capability to receive SLVS. We have connected the SLVS driver via the same 3-meter cable used during the irradiation sequentially to the four LVDS inputs of

the DUT, and we have measured the rise time at the corresponding outputs. The SLVS signal after the 3-meter cable appeared to have a reduced swing of about 100 mV, as shown on Figure 8.

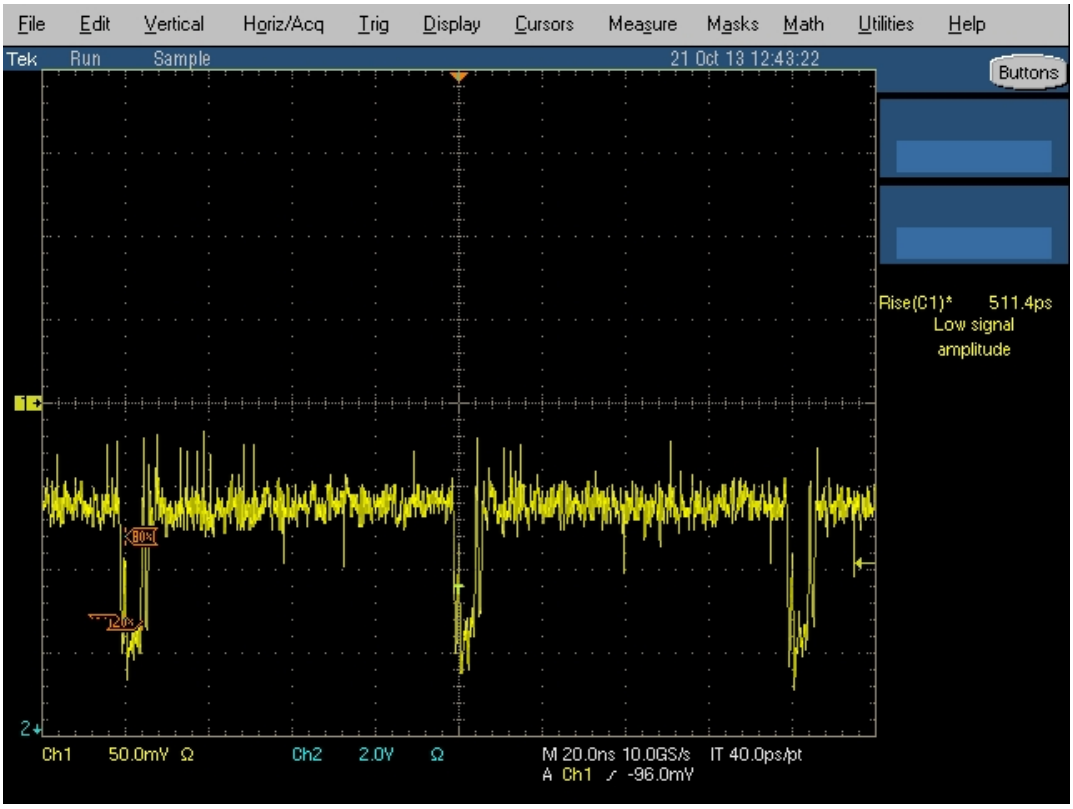

Figure 8: SLVS signal acquired at the receiving end of the cable, with a 1.5GHz differential probe P6248 and the oscilloscope TDS7254.

This is the signal seen as an input of the DUT during irradiation and during the measurements; its rise time has been measured as on Table 1.

Measurements of the input signal rise-time [20%-80% in ps]	238	263	261	284	286		Average=	266.4

Table 1: Rise time of the SLVS signal at the receiving end of the cable)as seen by the FPGA inputs).

The results of the measurements on the DUT LVDS outputs are reported on Table 2.

Measures of rise time [20%-80% in ps] at the DUT outputs											
CHANNEL											AVERAGE
Orange	293	309	296	303	312	302	295	305	303	301	301.9
Green	309	317	317	309	306	317	312	318	316	319	314
Blue	309	295	307	317	295	324	318	310	310	305	309
Brown	307	303	295	296	308	289	294	307	290	306	299.5

Table 2: rise time of the LVDS signals sent out by the DUT, when the DUT is fed with the SLVS signal shown above.

4. Conclusions

The tests performed show that the ProASIC3L FPGAs are capable to receive SLVS signals of a reduced swing of 100 mV after a Total Ionizing Dose of at least 201 Gy. The degradation in the rise time is modest if at all existing, the slowest rise time after irradiation is 324 ps.

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