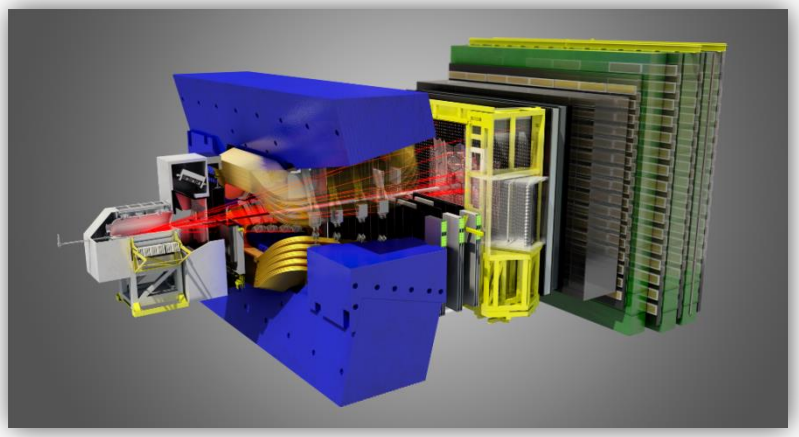
Technological Aspect of the Trigger-Less Readout Architecture for the LHCb Upgrade at CERN

Topical Workshop on Electronics for Particle Physics (IEEE 2013)
2013 October 27 - November 2
Seoul, Korea

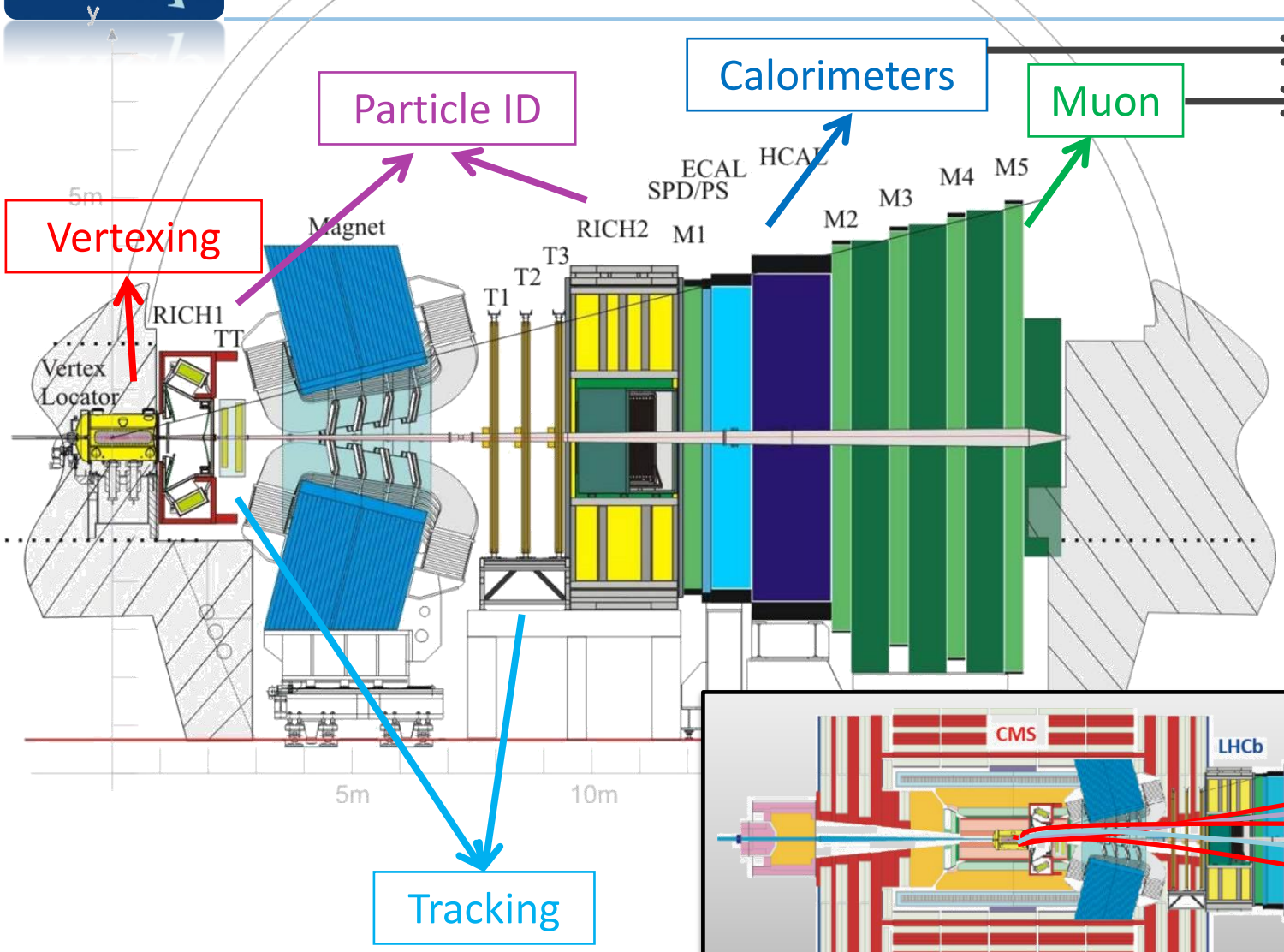
Guillaume Vouters
LAPP - Annecy - France
on behalf of the LHCb Collaboration

Outline

- Introduction to LHCb and current performance
- Motivations for an upgrade of the LHCb detector
  - Current limitations
- Detector Upgrade
- Readout Architecture Upgrade
  - FE Trigger-less electronics
  - DAQ technologies
  - Firmware architecture
- Outlook on plans and future running conditions



Current LHCb detector



Upgrading LHCb

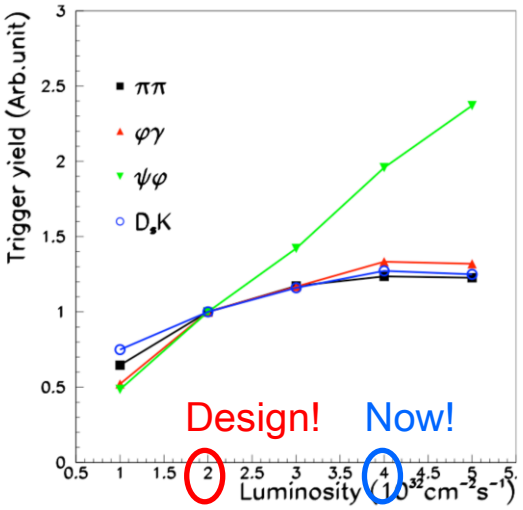
The amount of data and the physics yield from data recorded by the current LHCb experiment is limited by its detector, readout technologies and hardware trigger.

While LHC accelerator will keep steadily increasing …

- energy / beam (3.5 → 4 → 6.5 TeV → …)
- luminosity (peak 8×10^{33} → 2×10^{34} $cm^{-2}s^{-1}$ → …)

… LHCb will stay limited in terms of

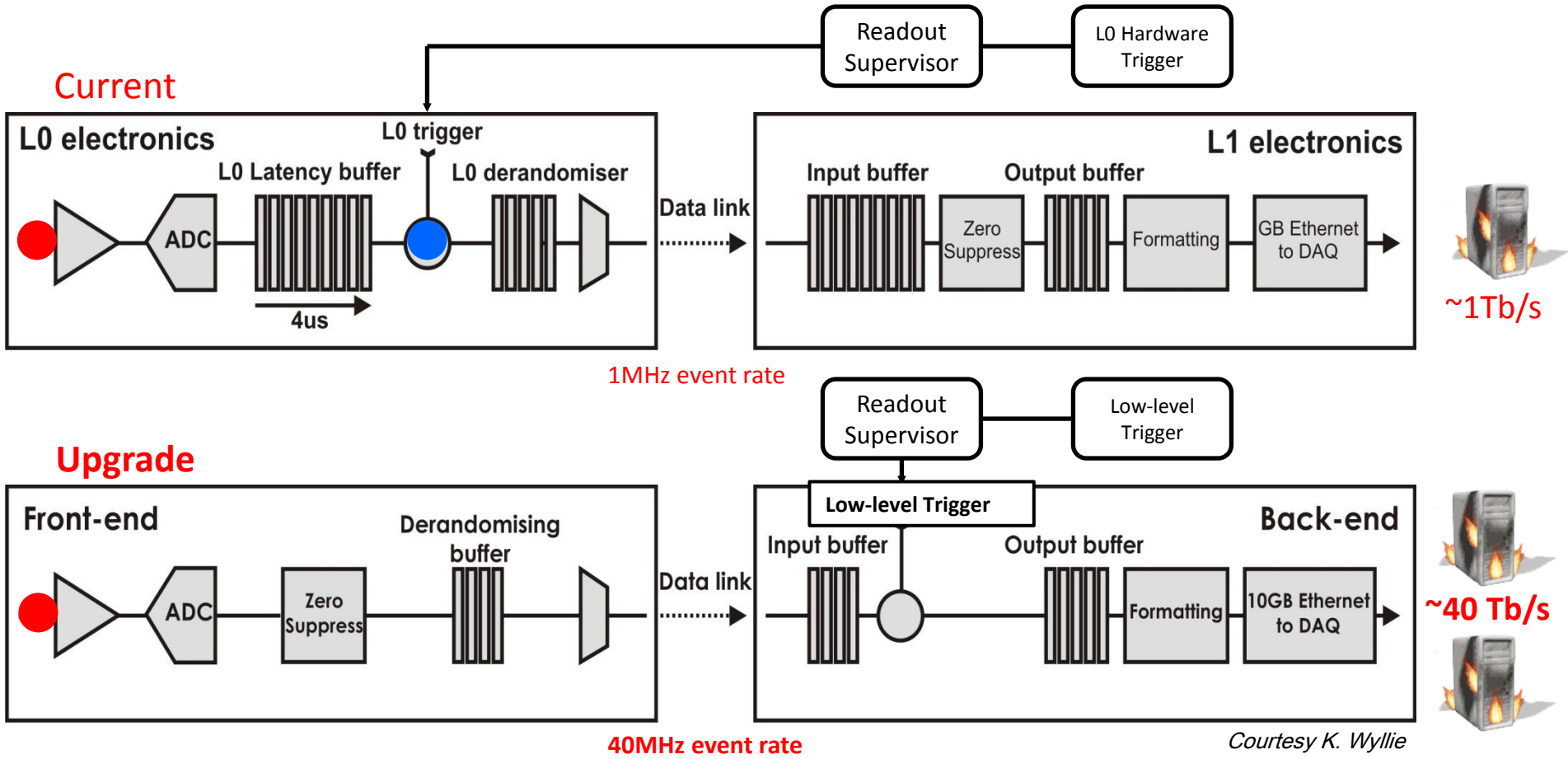
- data bandwidth: limited to 1.1 MHz / 40 MHz max
- physics yields for hadronic channels at the hardware trigger
- detectors degradation at higher luminosities



Upgrade Strategy

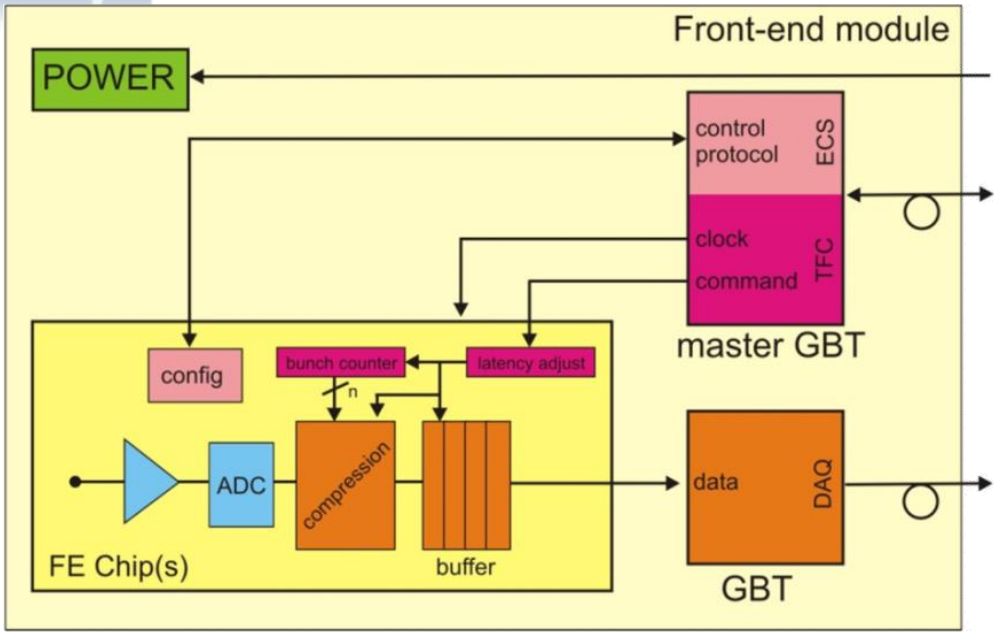
Remove first-level hardware trigger!

→ accept all LHC bunch crossing: trigger-less Front-End electronics



Courtesy K. Wyllie

Trigger-less FE



NO TRIGGER to FE!
→ Only commands, clock and slow control

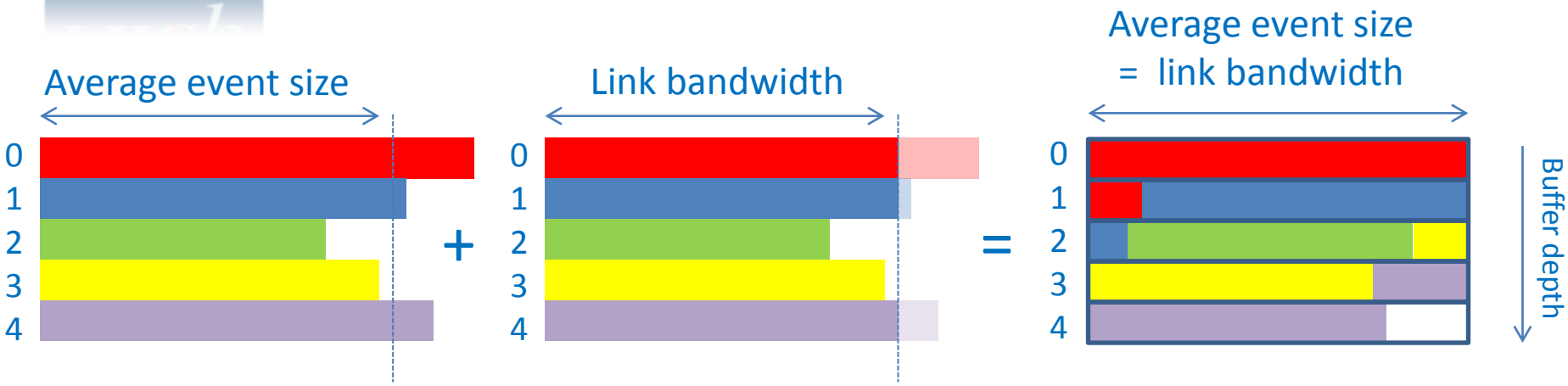
Compress (zero-suppress) data already at the FE

- reduce # of links from ~80000 to ~12500 (~20 MCHF to ~3.1 MCHF)
- data driven readout (asynchronous) + variable latencies!

Efficiently usage of link bandwidth for data

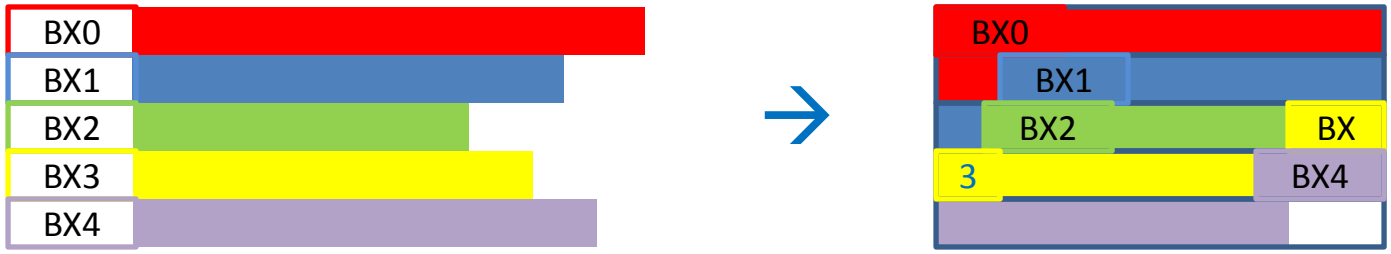
- pack data on data link continuously with elastic buffer
- extensive use of CERN GBT (robust FEC or WideBus mode)
  - ✓ evaluate choices based on complexity vs robustness

Efficient Data Packing Mechanism

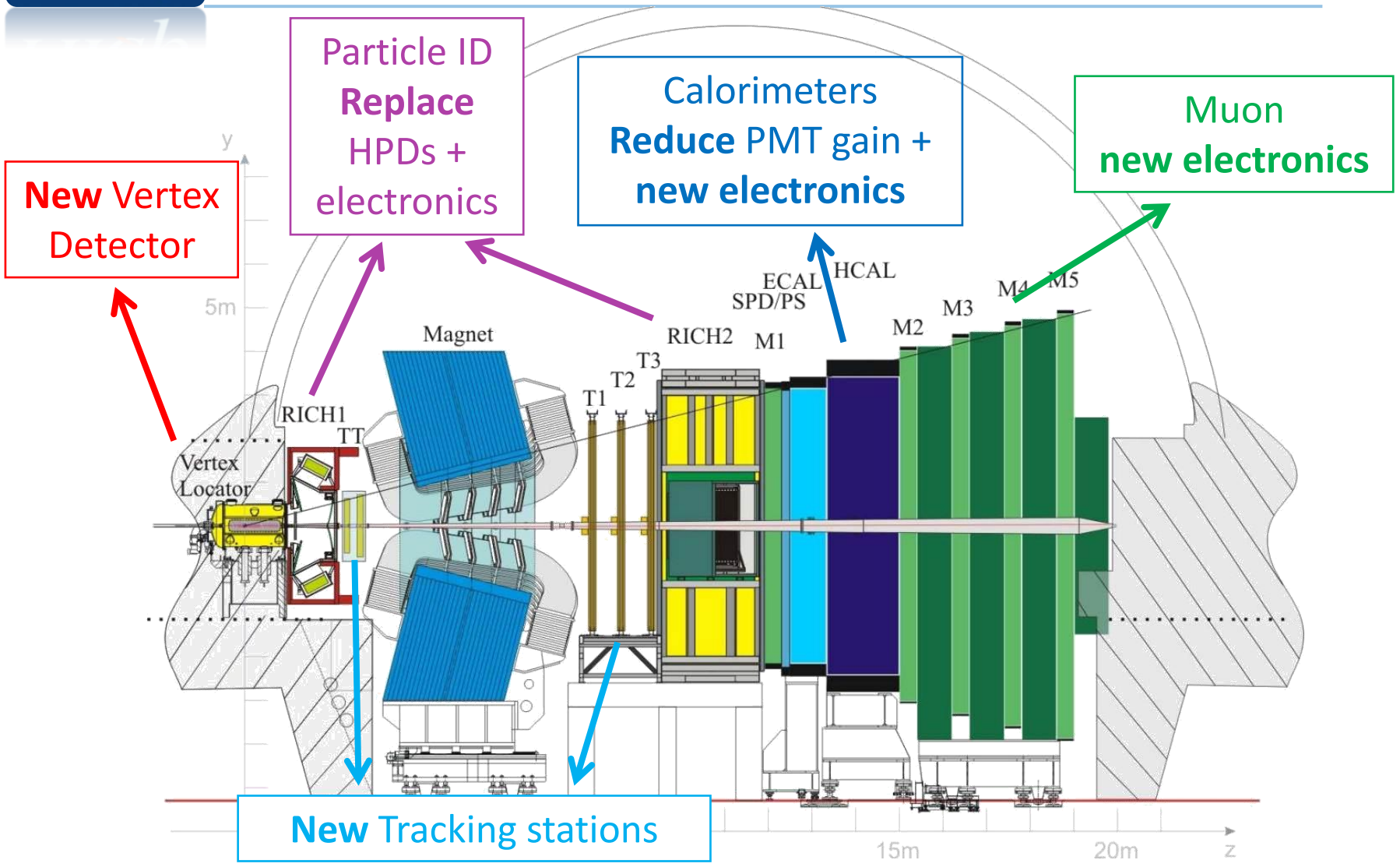


Header is the unique identifier for each event in frame

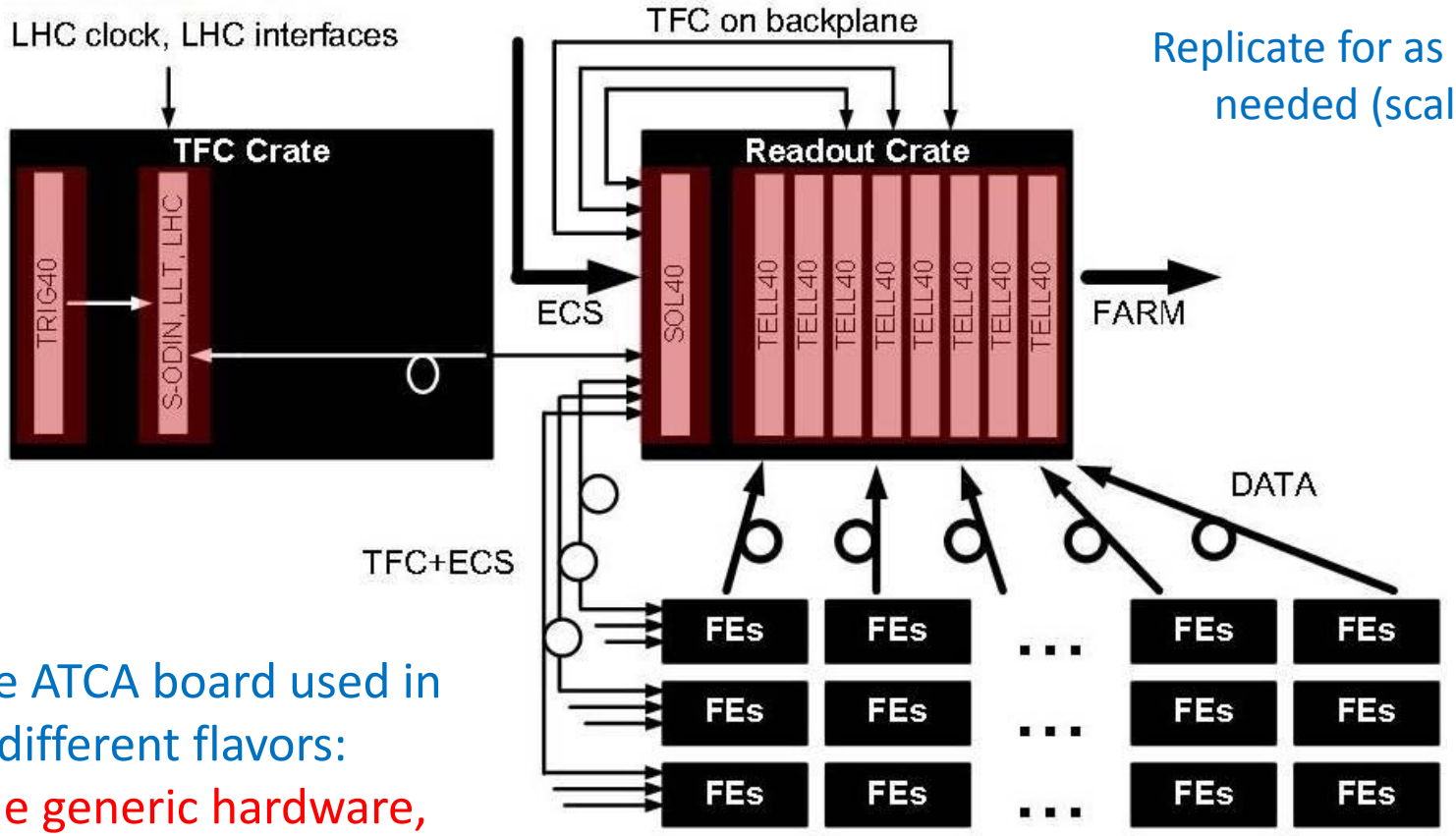
- ✓ Compulsory (tag for each LHC crossing)
- ✓ Programmable in its content (must contain length of frame and BXID)
- ✓ Used by readout board to decode and separate frames



Upgraded LHCb Detector



LHCb Upgrade Readout Architecture

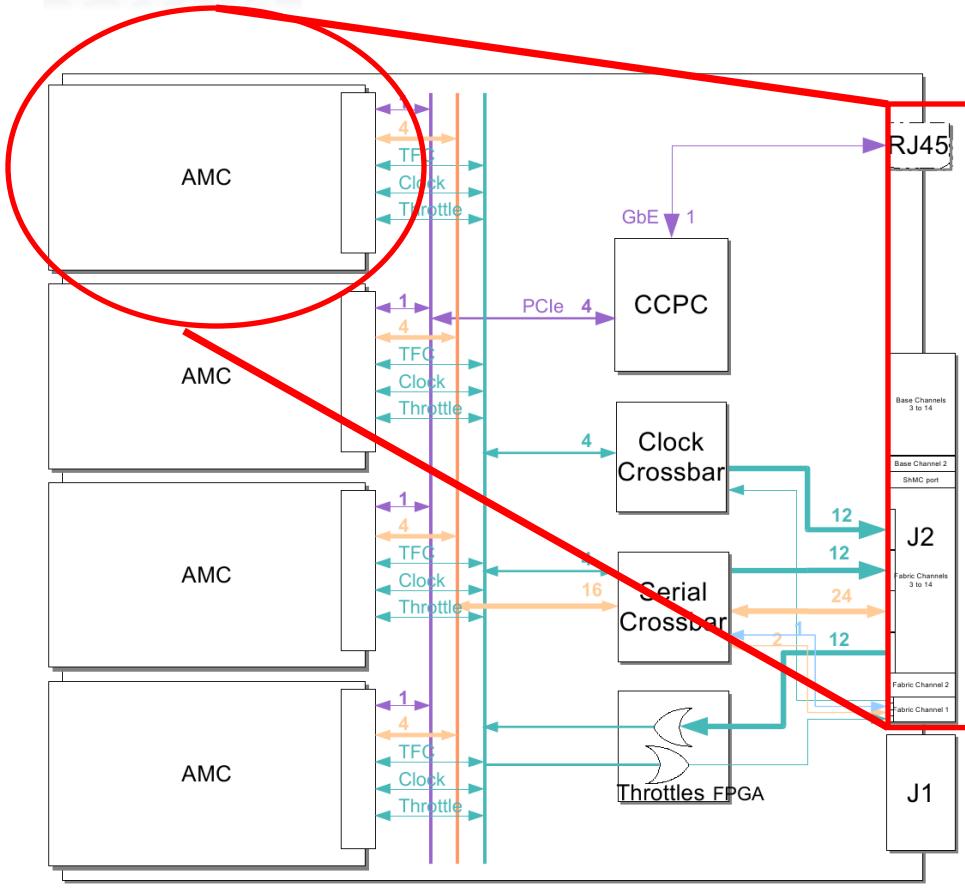


Replicate for as much as needed (scalable)

Same ATCA board used in different flavors:
same generic hardware, different firmware

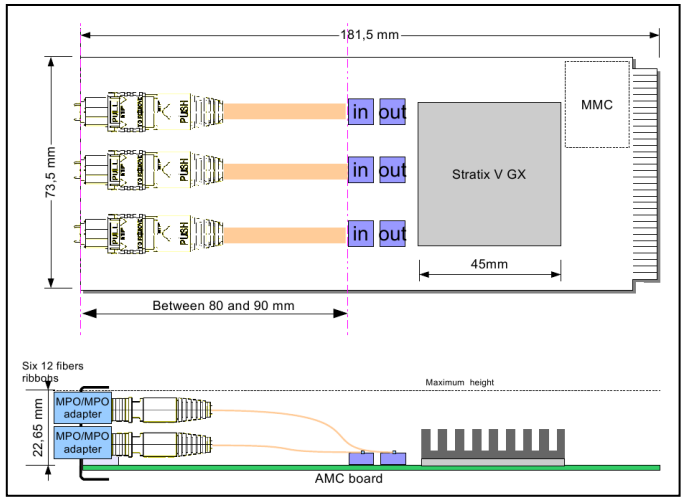
Back-End: New LHCb readout board

Classical approach: ~0.5 Tb/s data aggregator board with 10 GbE to FARM



24 inputs @ 4.8 Gb GBT format

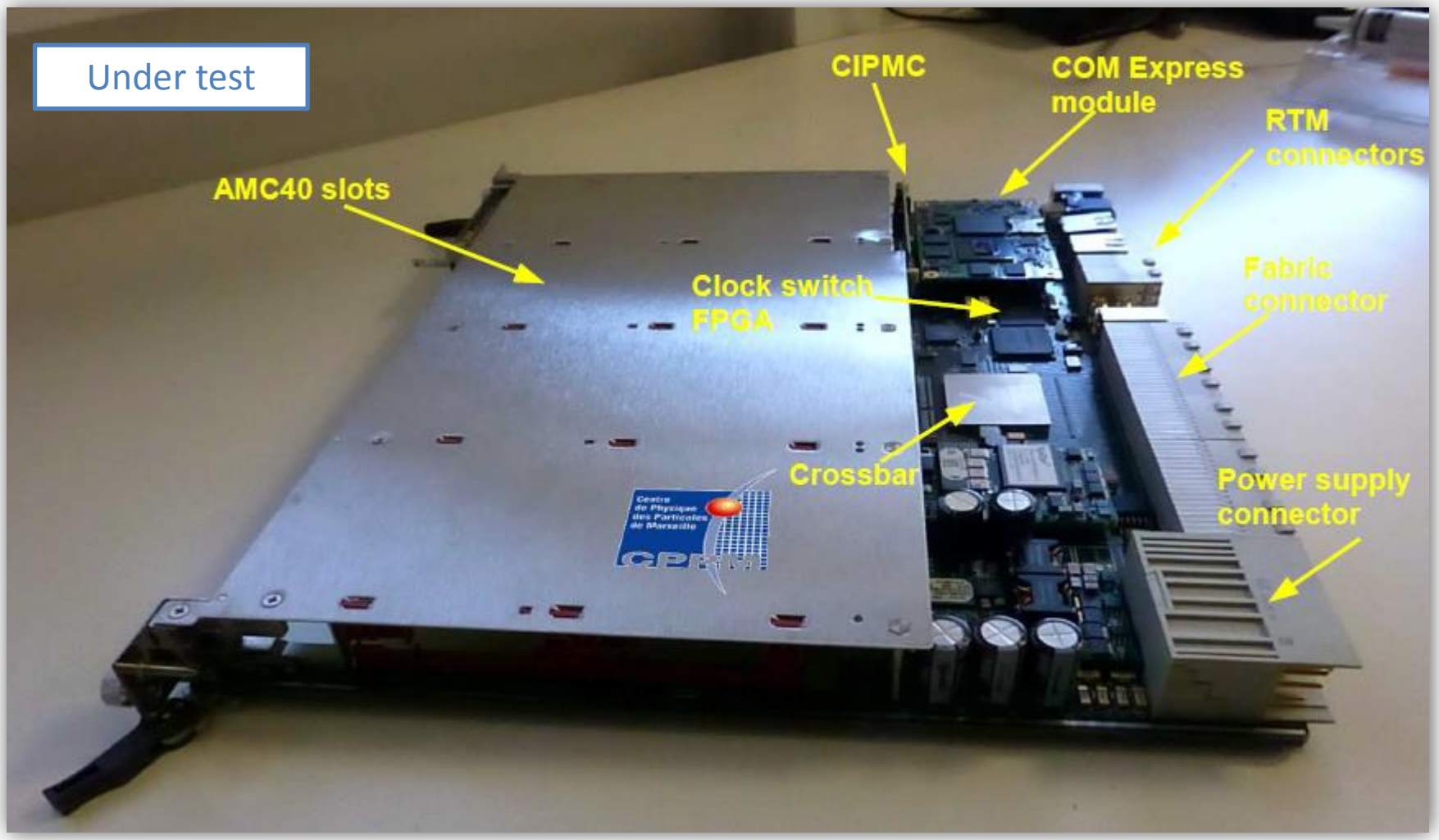
12 outputs/ inputs @ 10Gb ethernet



AMC

96 inputs @ 4.8 Gb → processing in FPGA → 48 x 10G ethernet ports

ATCA40

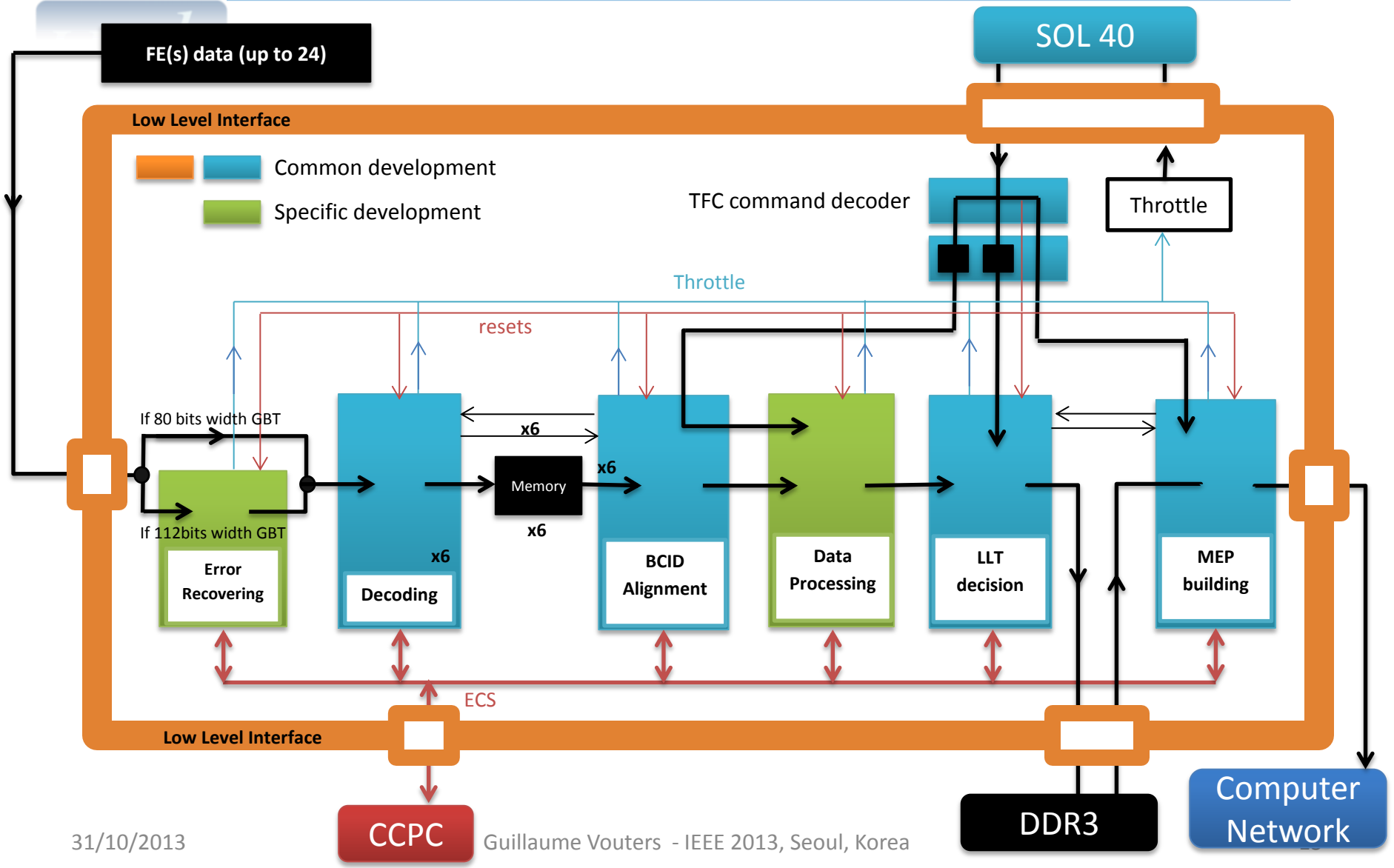

Under test
CIPMC
COM Express module
RTM connectors
AMC40 slots
Clock switch FPGA
Fabric connector
Crossbar
Power supply connector

AMC40

→TELL40 = ATCA40 + 4xAMC40
+ specific TELL40 firmware in AMC40

Now ready and being tested!

Common Firmware Development

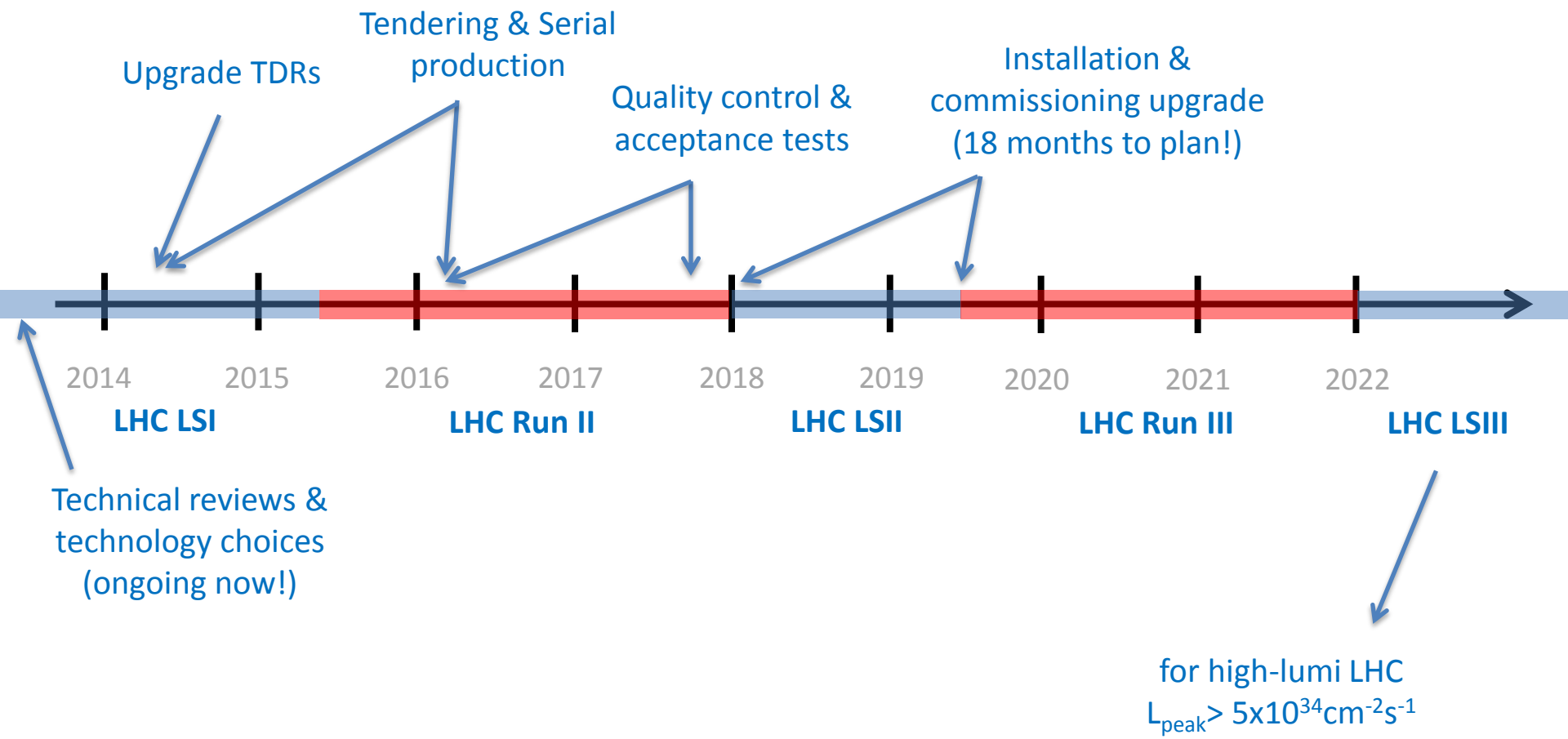


AMC40 test setup (MiniDAQ)

The MiniDAQ is the first step to the LHCb DAQ upgrade in order to check :

- ✓ Hardware functionalities
- ✓ Firmware developments
- ✓ Software developments

LHCb data taking plan



Conclusion

An upgrade plan of the LHCb experiment has been laid out

- Aim at collecting 10x more data and 20x more hadronic events

LHCb upgrade is technologically challenging and time wise tight

- Trigger-less, ~40 Tb/s network, minimize number of components
- Optimize costs and manpower: be smarter …
- R&D, specs, evaluation, validation are ongoing.

CERN endorsed the LHCb Upgrade by fully approving it!

We have exciting times ahead in 2014 and beyond!