Computing challenges in the certification of ATLAS Tile Calorimeter front-end electronics during maintenance periods

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Abstract. After two years of operation of the LHC, the ATLAS Tile calorimeter is undergoing a consolidation process of its front-end electronics. The certification is performed in the experimental area with a portable test-bench which is capable of controlling and reading out one front-end module through dedicated cables. This test-bench has been redesigned to improve the tests of the electronics functionality quality assessment of the data until the end of Phase I.

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1. Introduction

The hadronic Tile calorimeter [1] is one of the sub-detectors of the ATLAS experiment [2] at the LHC at CERN. It is a sampling calorimeter that uses plastic scintillating tiles as active medium and steel plates as absorber covering the central rapidity range of $|\eta| < 1.7$. The light produced in the tiles is grouped by cell and guided on each side of the module to the outer-most region of the barrel where photomultiplier tubes (PMTs) and the front-end electronics are mounted on so-called super-drawers. Each cell is read-out on each side by a different PMT. Digital data and analogue trigger signals are provided by each super-drawer.

During the first Long Shutdown (LS1) of the LHC the front-end electronics of the Tile calorimeter [3] are extracted for the required consolidation in view of the forthcoming operation at design conditions. The complete set of electronics is checked following a certification procedure based on specific tests that verify the correct functionality of the different front-end elements. Any under-performing component is replaced and complementary reinforcements are made on the connectors. The certification is assessed twice, first before any manipulation but after the super-drawer is extracted, and finally once the super-drawer is back into its final position. This first iteration is important because it allows the cross check of the problems identified during data

taking before any hardware manipulation is made. The certification of the repairs is assessed through the Mobile Data Integrity Check (MobiDICK) system.

2. Computing challenges

Recently, the ten year old MobiDICK system [4] was re-designed in order to extend its lifetime and simplify the long term support. The previous version of the system was based on a VME crate with custom and commercial electronics, a server running on the VME controller and a GUI running on a laptop. The laptop also provided the operating system kernel and libraries for the controller.

MobiDICK-4 [5] is the new generation of the test-bench, for which the requirements of the system were re-evaluated leading to a completely new design of the system, in half of the volume and almost a tenth of the weight.

2.1. Embedded design

The MobiDICK-4 system hardware is based on a FPGA embedded system core that controls different devices and mezzanine boards through dedicated firmware modules as shown in Figure 1. The core of the system is a commercial XILINX Virtex 5 FPGA evaluation board, model ML507, that contains an embedded 440 MHz PowerPC, 256 MB of RAM, a Compact Flash drive and GPIO ports to interface with the mezzanines and other auxiliary boards. An SFP module (Infineon V23818-M305-B57) connects to the TTC and ROD optical links, two serial-to-CANbus dongles (produced by Laciwel) interface the motherboard with Integrator and High Voltage (HV) control and monitoring CAN bus networks. A custom made ADC board with 12-bit precision and a sampling clock of 40 MHz, is used to measure analogue trigger outputs. Two additional custom made boards provide the HV level to operate the PMTs (HV board) and a fast light-pulse of known amplitude and phase that can be used for calibration purposes (LED board).

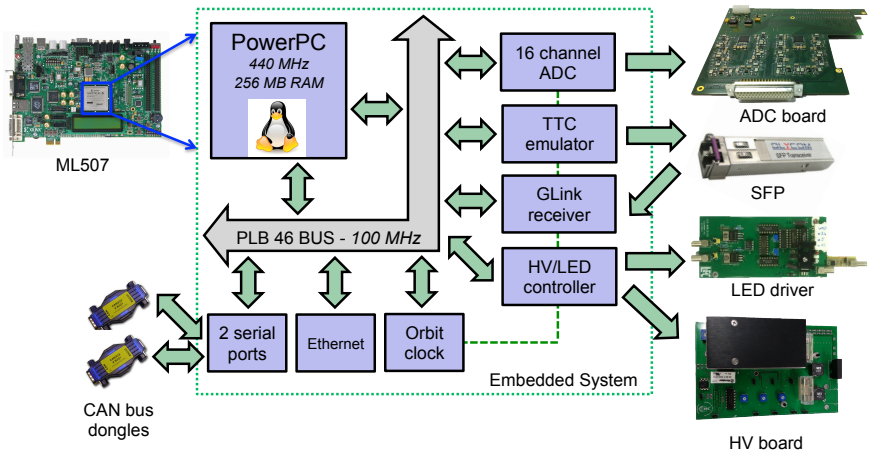

Figure 1. Sketch of the embedded system of the MobiDICK-4 test-bench.

At power on, the firmware is loaded from the Compact Flash, and the modules are initialized. Following, an image of Linux [6] that runs on the PowerPC, is uncompressed and booted. The core application that allows the user to perform all the front-end specific tests from the GUI is implemented in C++ and cross-compiled for the PowerPC using Xilinx ELDK. C++ language is the natural choice for this application, which can be started from the GUI. A full description of the system core can be found in Ref. [7].

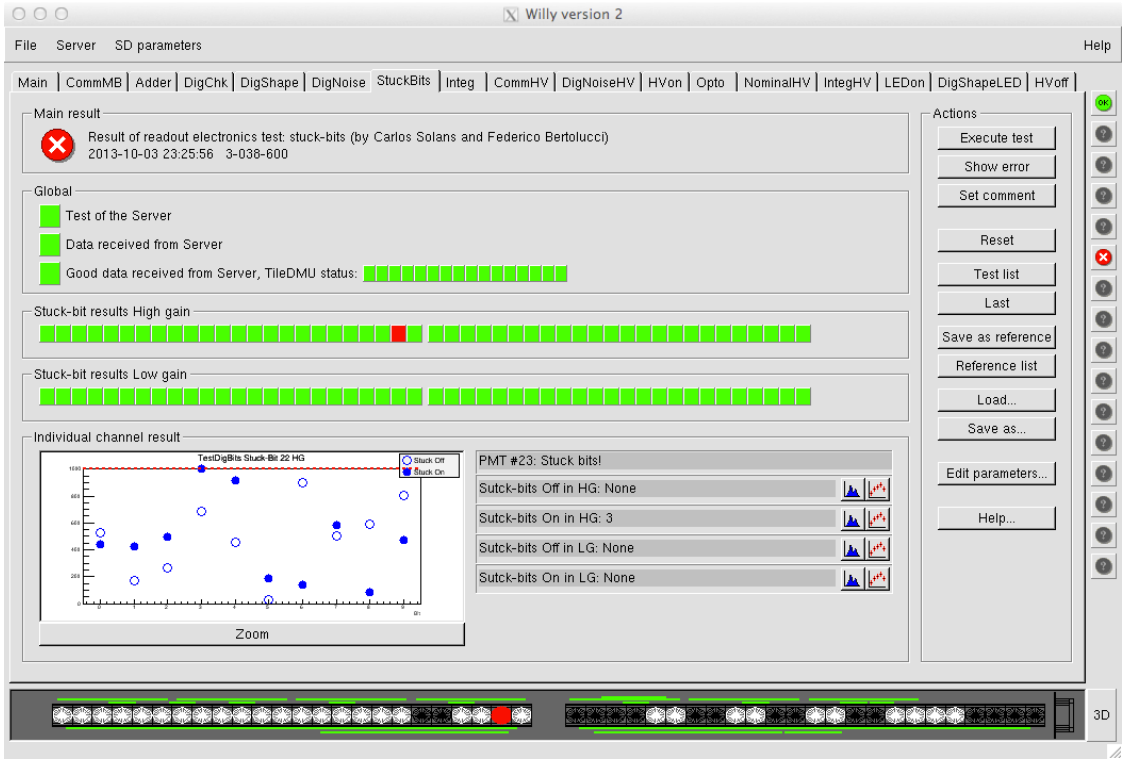

Figure 2. GUI panel for the specific test on stuck bits.

The embedded design of MobiDICK-4 makes it an integral tool for the certification of the super-drawers because it is completely encapsulated inside a box and doesn't depend on external resources. As opposed to previous versions, where the operating system was mounted from the laptop, the new version is completely stand-alone. One advantage of the system is therefore the independence from the device that runs the GUI.

2.2. Dependable evolution

MobiDICK-4 provides new functionalities in addition to enhanced and reliable measurements that meet the initial requirements. A newly implemented test, detects malfunctioning (ADC stuck bits) in the digital read-out that originated in the front-end electronics. In this test, a set of pulses that vary the 3 parameters of the pulse (amplitude, time and pedestal) are used in order to scan over all the 10 bits of the ADC. A certain bit is flagged as stuck on a channel when all of the events of that channel have the bit set to the same value, either on or off. Stuck bits can affect the automatic gain switching between the two available gains for each channel which is threshold based. Although the occurrence is very low, the effects on data quality are severe and thus it required a specific test to be implemented. Figure 2 shows the user interface panel for this test.

The chosen serial-to-CANbus adapter limits the speed of the communication with the CAN bus super-drawer interfaces to 125 kbps. In order to keep the speed of the test, the number of used points was decreased accordingly with no appreciable deterioration of the results.

Existing software has been used as much as possible and simplicity favoured in the design. A guideline has been the preservation of the aspect of the GUI to comfort operators. However, poorly performing pieces of code have been re-written, like the low level server interface class, that now implements fast time-out in hostname lookup and socket communication. The analogue

trigger signals are reconstructed using the sum of the ADC samples (Flat Filtering). These results are compatible with those obtained with more sophisticated algorithms like the Optimal Filtering [8] which was disfavoured because of its unnecessary complexity. Linearity of both algorithms is shown in Figure 3.

Furthermore, the code has been improved so that it compiles in other Unix-like systems like OSX, which is possible because it relies on ROOT [9] for the user interface.

2.3. Real-time processing

The motherboard provides all the computing power required by the system in a synergy between VHDL modules and C++ algorithms. Due to the system's flexibility to implement real-time processing tasks, it has been possible to deploy a test for format and CRC errors in all data fragments at the nominal Level 1 Trigger rate (100 kHz). A VHDL module checks every event and discards the data, while C++ reads the error counters available. The corresponding display has been updated to display the counters every 300 ms. This gives the user human scale updates of the real-time processing. C++ is used at lower rates and when more complex algorithms are required for every event.

2.4. Precision measurements

The custom made ADC board in MobiDICK-4 digitizes the analogue trigger outputs of the super-drawer at a sampling rate of 40 Msps using sixteen 12-bit ADCs. These outputs are used by the first level of trigger and are of two types, tower and muon. The first one is the signal that results from the sum of the three radial samplings, and the second one corresponds to the signal of the last layer cell. Figure 4 shows a diagram of the Tile cells and their grouping per trigger towers. The dynamic range of the ADC boards extend up to charges of 300 pC, which is approximately the full range of the trigger signal. At each read-out, up to 128 samples that are synchronized with the TTC clock, are stored in the memory of the system. This allows to perform characterization measurements of the pulse shape and noise levels.

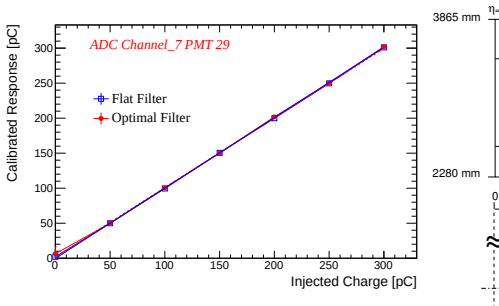

Figure 3. Example of calibrated response as a function of injected charge reconstructed by the ADC board.

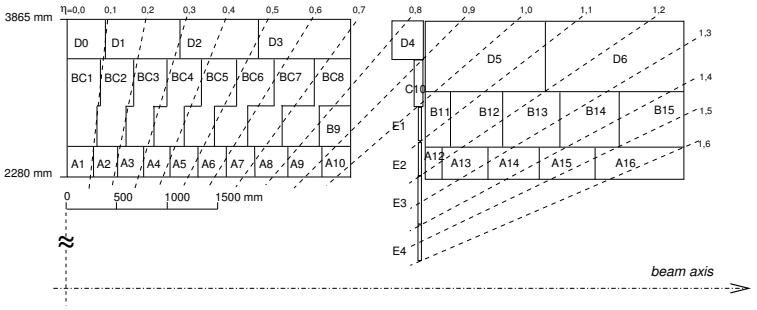

Figure 4. Segmentation in depth and in η of the Tile calorimeter modules in the central (left) and extended (right) barrels. The tile calorimeter is symmetric about the interaction point at the origin.

The pulse shape of the tower and muon outputs are shown in Figure 5, which is obtained by sampling the pulse with known charge at different injection times. These shapes are compatible with previous measurements and give an estimation of the precision of the system. Furthermore, Figure 6 shows that the RMS of the pedestal distribution for the muon output of the D6 cell is not symmetric across PMTs. This measurement revealed a noise pick-up in the propagation of analogue signals in the super-drawer and the cabling of D6-R has been better shielded accordingly, which ultimately proves the precision capabilities of the MobiDICK-4 system.

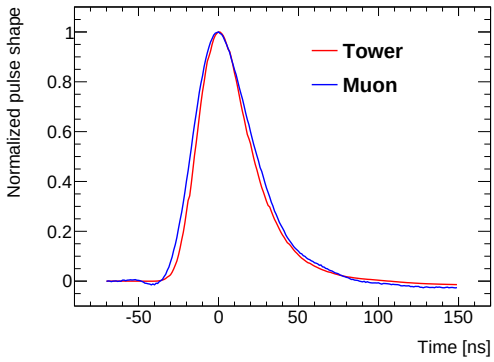

Figure 5. Charge injection pulse shape for tower trigger and muon signal outputs.

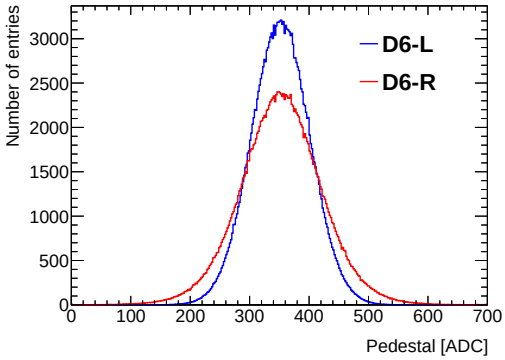

Figure 6. Pedestal distribution for both PMTs of the D6 cell.

3. Conclusions

The certification of the Tile front-end electronics poses several computing challenges that were overcome with the upgraded version of MobiDICK. It is based on an embedded system which as opposed to other general purpose solutions, focuses on the specific needs of the certification process. MobiDICK-4 increases the test-bench portability and reliability and provides a quicker turn around. On one side, the lifetime of the system has been extended, and maintenance costs have been reduced. Commercial off-the-shelf components are used whenever possible and dedicated test-bench laptop is not needed any more. On the other side, it is a fully equipped slice of the Tile back-end electronics that can perform high precision measurements on the front-end electronics.

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