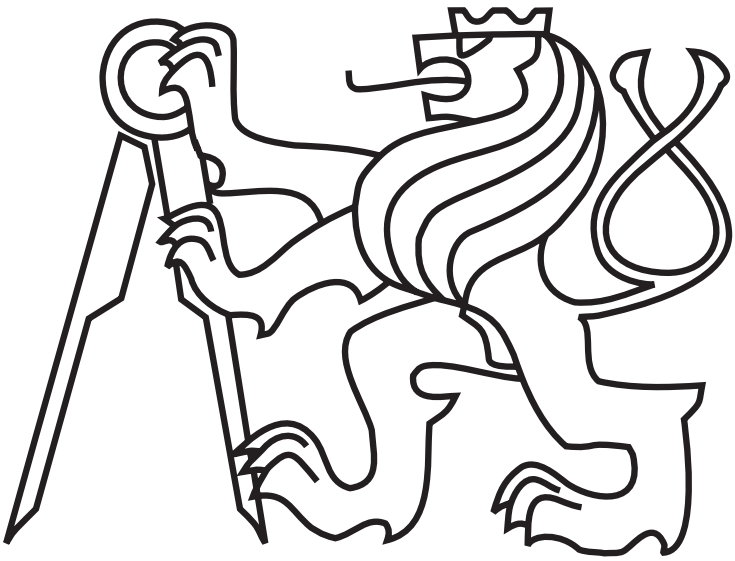
CZECH TECHNICAL UNIVERSITY IN PRAGUE

Faculty of Electrical Engineering

MASTER THESIS



Bc. Michal Eliáš

Digital Measurement System for the HIE-Isolde Superconducting Accelerating Cavities

Department of Cybernetics

Thesis supervisor: **Ing. Daniel Valúch, PhD**

Czech Technical University in Prague
Faculty of Electrical Engineering

Department of Cybernetics

DIPLOMA THESIS ASSIGNMENT

Student: Bc. Michal E l i á š

Study programme: Cybernetics and Robotics

Specialisation: Robotics

Title of Diploma Thesis: Digital Measurement System for the HIE-Isolde Superconducting Accelerating Cavities

Guidelines:

1. Study requirements for the superconducting cavity test bench in the SM18 hall. With help of your supervisor define the measurement system architecture and its relevant technical parameters (e.g. required bandwidth, noise properties, measurement accuracy etc.). Study methods to extract the cavity tune state, RF losses, quality factors and cavity field from the measured cavity forward, cavity reflected and antenna RF signals.
2. Implement the measurement system profiting from the existing low-level RF modules (VME boards with fast ADCs, DACs and FPGAs) and design any additional boards necessary e.g. clock generators). Design the FPGA firmware in VHDL language. With help of the Controls section design the user interfaces and integrate the measurement system into the CERN controls infrastructure.
3. Present the measurement results.

Bibliography/Sources:

[1] Wilson, E.: An introduction to particle accelerators. Oxford University Press, 2001, ISBN 0-19-850829-8
[2] Wangler, T.: RF Linear Accelerators. John Wiley & Sons, 2008, ISBN 978-3527-40680-7

Diploma Thesis Supervisor: Ing. Daniel Valuch, Ph.D.

Valid until: the end of the summer semester of academic year 2013/2014

L.S.

prof. Ing. Vladimír Mařík, DrSc.
Head of Department

prof. Ing. Pavel Ripka, CSc.
Dean

Prague, January 10, 2013

České vysoké učení technické v Praze
Fakulta elektrotechnická

Katedra kybernetiky

ZADÁNÍ DIPLOMOVÉ PRÁCE

Student: Bc. Michal E l i á š

Studijní program: Kybernetika a robotika (magisterský)

Obor: Robotika

Název tématu: Digitální měřicí systém pro supravodivé rezonanční dutiny HIE-Isolde

Pokyny pro vypracování:

1. Nastudujte požadavky na testovací systém supravodivých rezonančních dutin v hale SM18. S pomocí vedoucího práce definujte strukturu měřícího systému a jeho technické parametry (např. požadovanou šířku pásma, šum, přesnost měření). Nastudujte metody pro měření stavu odladění rezonanční dutiny, VF ztrát, činitele jakosti a vektoru elektrického pole z přímého, odraženého a anténního signálu.
2. Zkonstruujte měřící systém využívající již existující „Low-level RF" moduly (VME desky s FPGA, rychlými AČ a ČA převodníky). Pokud to bude nutné, navrhněte chybějící moduly (např. generátory hodin). Vytvořte zdrojové kódy pro FPGA v jazyce VHDL. S pomocí sekce řidicích systémů navrhněte uživatelské rozhraní a zakomponujte tento měřící systém do provozní technické infastruktury CERN.
3. Prezentujte výsledky měření.

Seznam odborné literatury:

[1] Wilson, E.: An introduction to particle accelerators. Oxford University Press, 2001, ISBN 0-19-850829-8
[2] Wangler, T.: RF Linear Accelerators. John Wiley & Sons, 2008, ISBN 978-3527-40680-7

Vedoucí diplomové práce: Ing. Daniel Valuch, Ph.D.

Platnost zadání: do konce letního semestru 2013/2014

L.S.

prof. Ing. Vladimír Mařík, DrSc.
vedoucí katedry

prof. Ing. Pavel Ripka, CSc.
děkan

V Praze dne 10. 1. 2013

Prohlášení autora práce

Prohlašuji, že jsem předloženou práci vypracoval samostatně a že jsem uvedl veškeré použité informační zdroje v souladu s Metodickým pokynem o dodržování etických principů při přípravě vysokoškolských závěrečných prací.

V Ženevě dne 03.05.2013 .....

Podpis autora práce

Acknowledgements

I would like to thank my supervisor Ing. Daniel Valúch, PhD, for his advices and support, to Gregoire Hagmann for providing us with a module that made the development much faster, to rest of my colleagues at CERN for doing a great job and answering all my questions. And most importantly to my family, always being there for me.

Abstrakt

Supravodivé rezonanční dutiny pro urychlovač HIE-Isolde jsou v současnou chvíli stále ve vývoji. Značné množství energie i zdrojů Evropské organizace pro jaderný výzkum (CERN) je investováno do výzkumu vedení vysokofrekvenčního pole uvnitř supravodičů, vývoji rezonančních dutin a naprašování a nanášení supravodivých materiálů. Pro usnadnění vývoje je důležité mít k dispozici systém, s jehož pomocí se dají rychle a přesně měřit vysokofrekvenční vlastnosti nově vyvinutých dutin. Současný systém založený na analogovém měření fáze a sledovacích VF generátorech není pro testy optimální. Pokud nejsou předem známy přesné parametry dutiny, tradiční zpětnovazební systém nebude schopný nalézt rezonanci, popřípadě její nalezení potrvá příliš dlouho. Toto je způsobeno velkým činitelem jakosti Q, kterého tyto dutiny dosahují (pásmo rezonance je široké jen zlomek Hz na frekvenci 100 MHz). Pokud je dutina rozladěna jen o několik šířek pásma, intenzita pole uvnitř dutiny při ladění frekvence bude téměř neměřitelná. Navíc má vysokofrekvenční pole uvnitř dutiny značnou setrvačnost, rychlost ladění je tudíž velmi omezená. Proto je nutné navrhnout nový, plně digitální, systém založený na stávajícím hardware vyvinutém pro LHC a SPS urychlovače. Dále uvážit nové způsoby pro rychlejší nalezení a sledování rezonance, které budou fungovat i v prostředí s vibracemi a výkyvy tlaku hélia.

Abstract

At the time of writing, the superconducting cavities for the HIE Isolde accelerator are still under development. Extensive R&D efforts are being invested at CERN into the fundamental science of the RF superconductivity, cavity design, niobium sputtering, coating and RF properties of superconducting cavities. Fast and precise characterisation and measurements of RF parameters of the newly produced cavities is essential for advances with the cavity production. The currently deployed analogue measurement system based on an analogue phase discriminators and tracking RF generators is not optimal for efficient work at the SM18 superconducting cavity test stand. If exact properties of the cavity under test are not known a traditional feedback loop will not be able to find resonant frequency in a reasonable time or even at all. This is mainly due to a very high Q factor. The resonance peak is very narrow (fraction of a Hz at 100 MHz). If the resonant frequency is off by several bandwidths, small changes of the cavity field during the tuning will not be measureable. Also cavity field will react only very slowly to any change of the drive signal. A new techniques to find and track the cavity resonance faster, as well as to keep the cavity field constant under strong microphonics and helium pressure variations must be found to meet the deadlines for the HIE Isolde machine. Therefore a new fully digital measurement and conditioning system based on the available existing hardware from the LHC and SPS must be designed and built.

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1 Introduction

Particle accelerator is a device that uses electromagnetic fields to propel charged particles to high speeds and to contain them in a form of spatially well-defined beams [7]. A very simple particle accelerators based on a DC acceleration were used by scientists already in the 19^{th} century. The final energy obtainable by the DC acceleration technique is however limited so a new generation of radio frequency powered accelerators was developed in the 1920s.

Two principal classes exist - the linear accelerators (linac) and the circular accelerators. In case of linacs the particles are accelerated and pass through the whole machine exactly once. The linac is typically constructed in one straight line, but machines with bends also exist. The beam is either extracted to the next machine, shot to a fixed target or collided with beam from another accelerator. In contrary the circular accelerators feature a closed beam trajectory. The beam is injected and circulates in the machine for many turns. Depends on type, the beam trajectory is either fixed (synchrotrons) or it is function of a beam energy (cyclotrons). The beam could be either accelerated and extracted to the next user, or could be simply stored for a long periods of time.

Both accelerator types have characteristic properties determining their function. The linear accelerators are typically very well suited for acceleration of a low energy beams when the speed of particles still significantly increases ($\beta << 1$). The linacs are also an accelerator of choice for the future very high energy lepton machines as they do not suffer of the synchrotron radiation problems. As the whole particle energy must be gained during the single particle passage the linacs are dominated by radio frequency (RF) accelerating structures what makes them difficult and expensive for high energies. On contrary, the circular accelerators feature a repetitive orbit (closed or not) and "re-use" the accelerator many times (revolutions). The required accelerating structures are then smaller and less powerful. In order to bend (and close) the particle trajectory it is necessary to cover a large fraction of the machine by bending magnets. The higher the particle energy is the stronger magnets need to be used resulting in a several Tesla dipoles in the highest energy accelerators. Charged particles interact with the bending magnetic field and emit so called synchrotron light making it difficult to accelerate light particles to a very high energies. Circular machines have a large variety of applications ranging from small cyclotrons in hospitals to a large scientific research accelerators.

From the RF system point of view both accelerator types are the same. Electromagnetic acceleration field inside of accelerating structures, often referenced as "accelerating cavities" or simply "cavities" must be kept at a very precise amplitude, phase and frequency required by the concrete machine and a momentary state of the system. This work focuses on a design of measurement and conditioning system for superconducting quarter wave resonators used as accelerating structures for the HIE-Isolde post-accelerator at CERN.

There is a large variety of particle accelerator applications, including fundamental and applied research, ion implantation, medical and industrial imaging, cancer therapy, biomed-

ical research, material sciences and many other. Main function of the European Organization for Nuclear Research (CERN) is fundamental research in the field of high energy physics. CERN develops, builds and operates particle accelerators for a large community of particle physicists from all around the world. Currently six accelerators, one decelerator, four collider and many fixed target experiments are running at CERN. All machines are interconnected in an accelerator chain, providing beams of hadrons, leptons and heavy ions at energy levels up to 7+7 TeV. A map of CERN accelerator chain is shown in Figure 1.

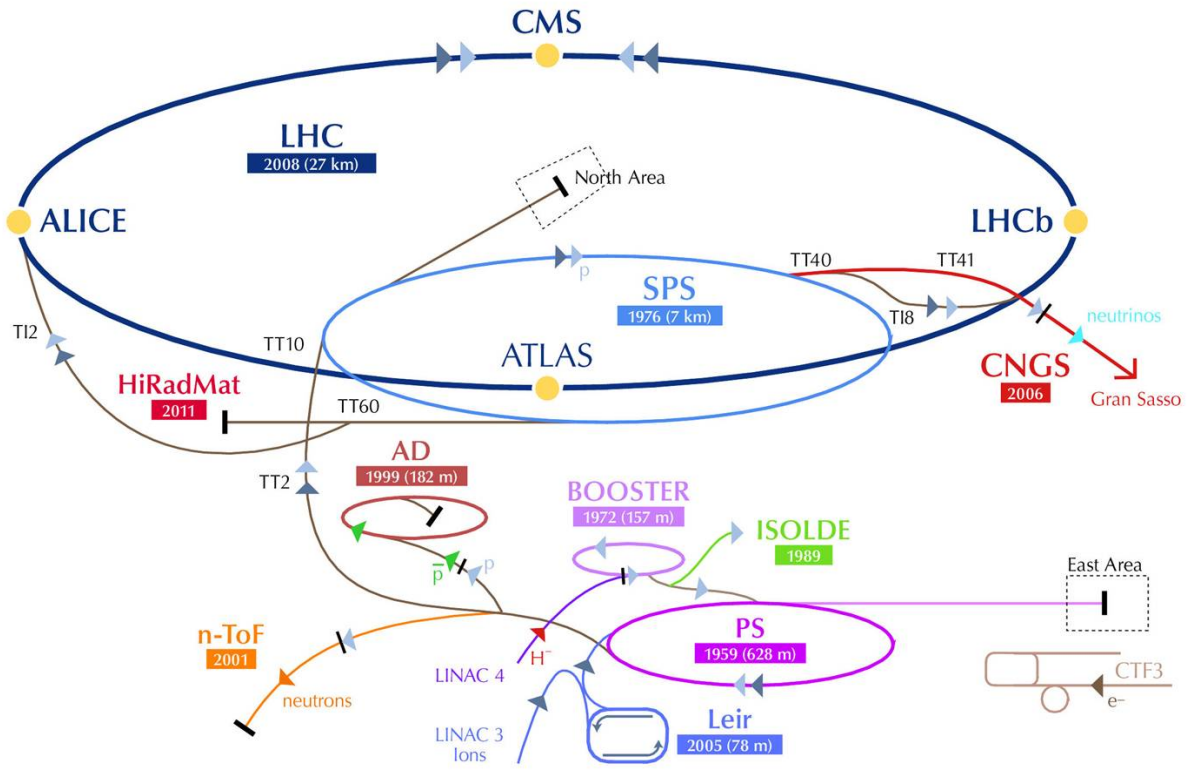

Figure 1: CERN accelerator complex (taken from [1])

2 HIE Isolde

The High Intensity and Energy (HIE) [8] project represents a major upgrade of the ISOLDE (On-Line Isotope Mass Separator) nuclear facility at CERN with a mandate to significantly increase the energy, intensity and quality of the radioactive nuclear beams provided to the European nuclear physics community for research at the forefront of topics such as nuclear structure physics and nuclear astrophysics. The HIE-ISOLDE project focuses on the upgrade of the existing Radioactive ion beam EXperiment (REX) post-accelerator with the addition of a 40 MV superconducting linac comprising 32 niobium sputter-coated copper quarter-wave cavities operating at 101.28 MHz and at an accelerating gradient close to 6 MV/m. The energy of post-accelerated radioactive nuclear beams will be increased from the present ceiling of 3 MeV/u to over 10 MeV/u, with full variability in energy, and will permit, amongst others, Coulomb interaction and few-nucleon transfer reactions to be carried out on the full inventory of radionuclides available at ISOLDE. The High Intensity and Energy ISOLDE project focuses on the energy upgrade of the present ISOLDE radioactive beams. Goal is to post-accelerate radionuclide beams from 3 MeV/u up to 10 MeV/u.

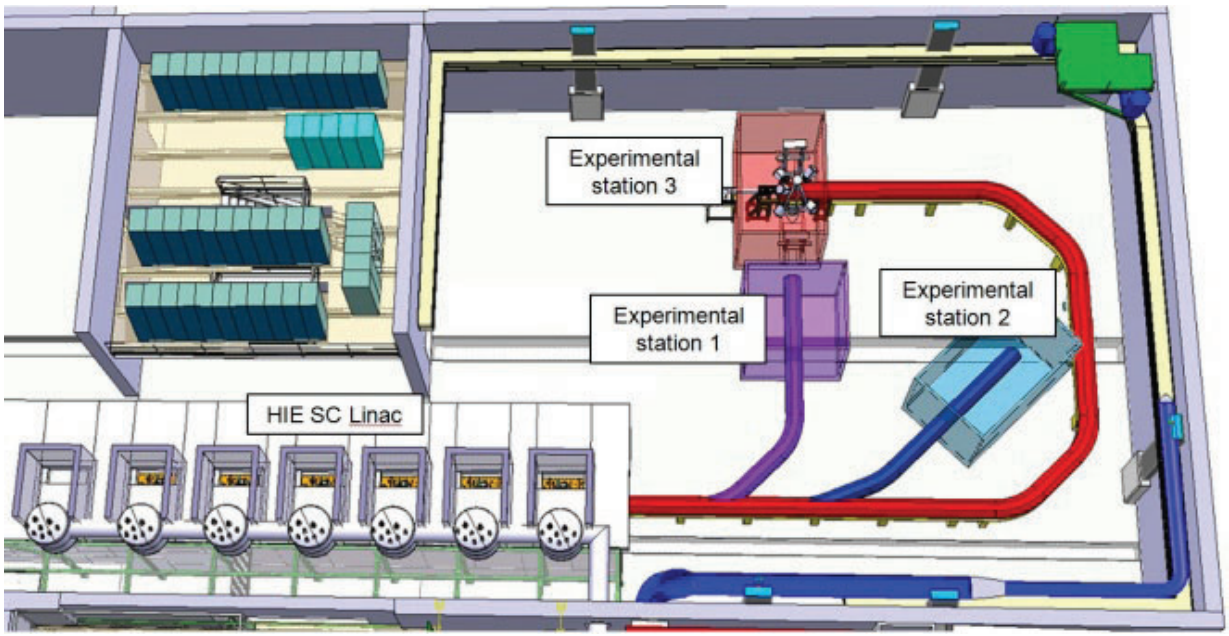

Figure 2: Isolde hall after upgrade

3 RF Systems

Radio frequency (RF) system is a vital part of any particle accelerator. It generates the accelerating electromagnetic fields inside the accelerating structures, often referenced as "accelerating cavities" or simply "cavities". The principal function of the RF system is to keep the circulating beam bunched, accelerate or decelerate and keep the circulating beam stable in the longitudinal and the transverse plane. The RF system usually generates also the time synchronization for the whole accelerator complex as many processes (e.g. beam transfer from one ring to the other) must be rigorously synchronous with the beam movement.

In general RF system of a particle accelerator typically consist of the following building blocks:

- Accelerating structures (RF cavities) providing the accelerating field to the beam,
- RF power amplifiers and transmission line systems supplying the cavities with RF power,
- Feedback and control loops (Low Level RF system, LLRF) precisely controlling the cavity field.

Depending on beam type and energy, different RF objects could be used as accelerating structures. For low energy rings with large frequency swing, lumped element resonators are typically used (Figures 3 and 4). They provide gap voltage in order of kilovolts with a tunable bandwidth in order of 1-2 octaves. In the medium energy accelerators where the beams are already relativistic (beam velocity is close to the speed of light), but increase of velocity is still noticeable, traveling wave structures (TWCs) are typically used (Figures 5 and 6). Such cavities typically offer a bandwidth of few per-cent and when fed by a megawatt amplifiers an accelerating voltage in order of MV could be achieved. For highly relativistic beams where bandwidth is not an issue standing wave resonators are typically used. Normal (Figures 9 and 10) or super-conducting (Figures 7 and 8), such resonators provide accelerating voltages in order of ones to tens of MV at a bandwidth of per-mill and lower.

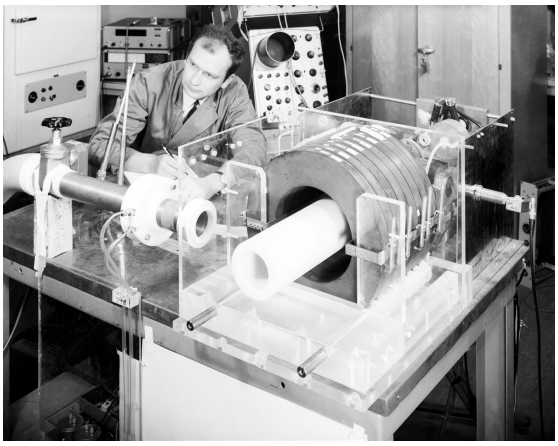

Figure 3: Model of a ferrite resonator [2]

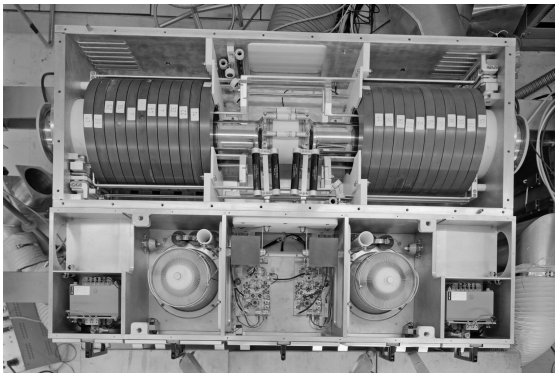

Figure 4: Booster RF ferrite cavity [2]

Figure 5: SPS 200 MHz travelling wave structure [2]

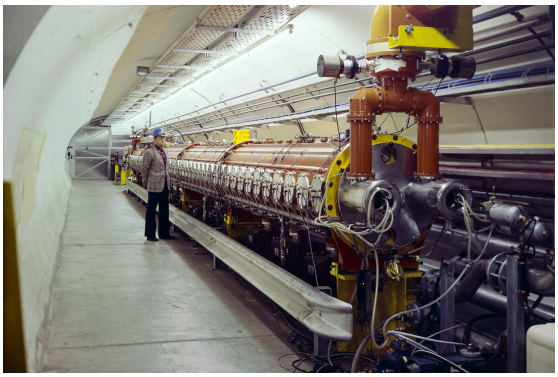

Figure 6: 200 MHz TWC in the SPS tunnel (circa 1975) [2]

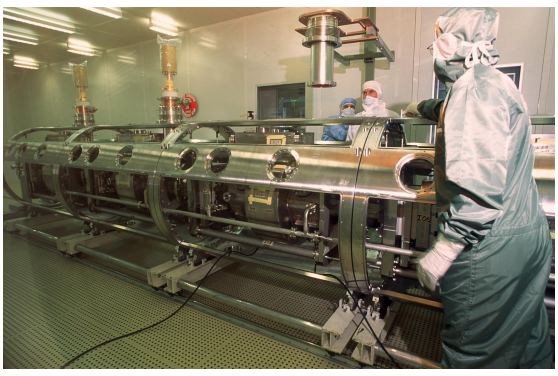

Figure 7: LHC 400 MHz superconducting cavity (production in the clean room) [2]

Figure 8: LHC superconducting cavities (in the machine tunnel) [2]

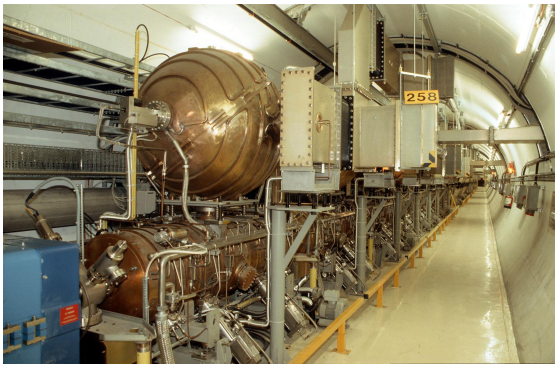

Figure 9: LEP 352 MHz normal conducting cavities [2]

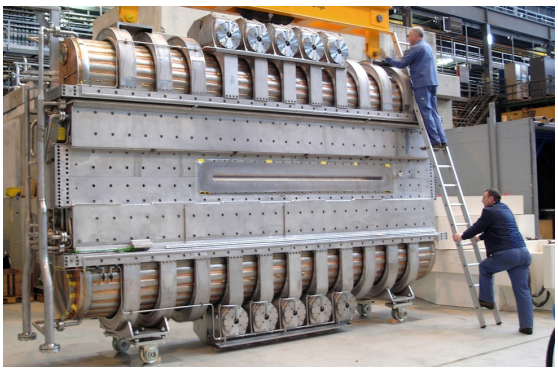

Figure 10: PSI 50 MHz normal conducting cavity [2]

Accelerating cavities are fed by RF power amplifiers. Typical accelerator amplifiers cover frequencies from ones of MHz to GHz and power levels from several kW to hundreds of MW depending on the accelerator. Lower frequency amplifiers ($<$ 200 - 400 MHz) are powered by tetrodes, higher frequency by diacrodes, inductive output tubes (IOT) or klystrons (Figures 11 and 11). Recent advances in the solid state technology allow to replace some tube powered amplifiers by a full solid state solutions, covering power levels up to hundreds of kilowatts CW in the VHF/UHF bands [9]. Smaller amplifiers ($<$ 1 kW) at frequencies below 100 MHz are already dominated by the solid state devices.

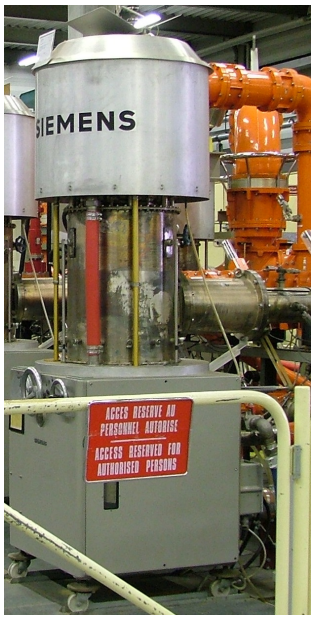

Figure 11: SPS RF amplifier [3]

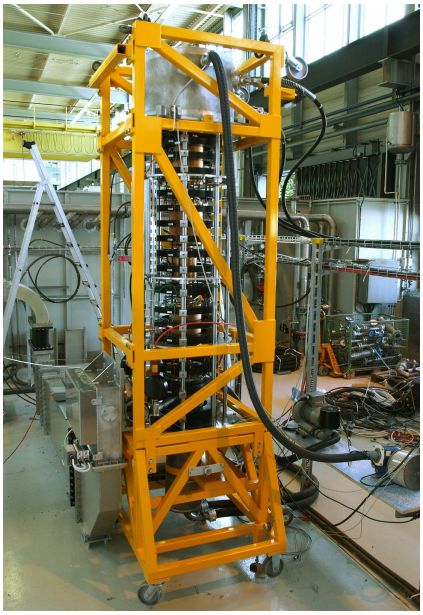

Figure 12: 300 kW klystron for LHC

Low Level RF system (LLRF) is a common name for set of all feedback and control loops maintaining the magnitude and phase of the accelerating field in the cavities within

the required limits. The low-level system typically generates the reference signals, measures the field in the cavity (cavities) and compensates for any deviations from the requested setpoints, caused for example by external perturbations or the beam loading. As field quality in the accelerating cavities is crucial for successful operation of the accelerator, these systems are typically very complex. The low level loops have to deal with accuracy, long and short term stability, low noise, response time etc.

Already for several years, the feedback loops and most of the signal processing is implemented in a digital domain. Signals are sampled using fast analogue to digital converters, then processed by digital signal processors (DSP), programmable logic devices (FPGA) or a combination of both. The resulting signals are then converted back into the analogue domain by means of fast digital to analogue converters, direct digital synthesis or digital up-conversion.

At CERN, the RF Feedbacks and Beam Control (FB) section deals with the Low Level RF systems for all CERN accelerators and projects. The FB section is part of the Radio Frequency group (RF) of the Beams Department (BE).

3.1 Quarter wave resonator for the HIE-Isolde machine

In order to make the new LINAC as short in length as possible, high-beta Niobium sputtered copper superconducting cavities will be used. Due to a relatively low frequency (101.28 MHz) and a low β the suitable accelerating structure type is the Quarter wave resonator (QWR). It can be described as a coaxial resonator [10], with length designed to be exactly $\lambda/4$ (one quarter of the wavelength at the desired resonant frequency). In order to fulfil the boundary conditions one end of the structure is shorted and the inner conductor on the other side is not connected to the end-plate short. The accelerating voltage develops between the outer and inner conductor at the end with gap. This configuration acts like a parallel LC circuit. Sketch of such structure can be seen in Figure 13. When used in an accelerator this configuration is called a quarter wave cavity.

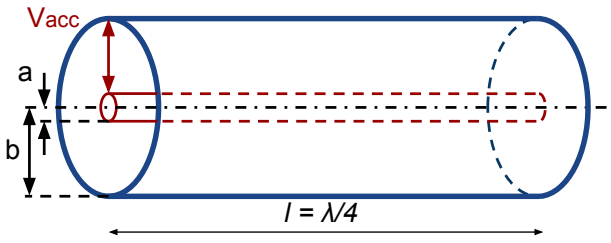

Figure 13: Coaxial quarter wave resonator

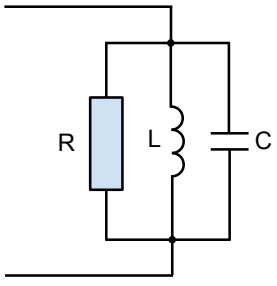

Figure 14: Cavity model

At the resonant frequency the cavity impedance seen by the generator is purely resistive. Its value is defined by the RF losses in the cavity body. RF losses in a resonator are

typically described by a quantity called the quality factor (Q, see the circuit theory for details). Normal conducting cavity could reach values of the intrinsic Q factor (Q_0) in order of 10^3 – 10^4, superconducting resonators easily 10^9 – 10^{11}. External loading of the resonators (e.g. by the coupling antennas) lowers the Q value, obtaining the so called the external Q, or the loaded Q value. The HIE-Isolde cavity is designed to dissipate 7 W in the walls for an accelerating field of 6 MV/m (resulting accelerating voltage 1.8 MV) at a $Q_0 = 6.6 \times 10^8$. The cavity will be fed by a moveable fundamental power coupler. Cavities in the machine are expected to be operated at a loaded Q between 1×10^8 (bandwidth 1 Hz) and 3.4×10^6 (bw. 30 Hz) requiring 20 to 500 W of forward RF power to reach the desired accelerating voltage [11].

3.2 LLRF system

3.2.1 Self excited loop

One possible mode of operation of an LLRF system is called the "self excited loop" shown in Figure 15. A self excited loop is a high gain, positive (unstable) feedback loop. RF power amplifier is feeding the cavity via the main (fundamental) power coupler. Sample of the electromagnetic field in the cavity is coupled out by a secondary coupler often called "antenna". There is no RF generator in the signal path, just a limiter and a phase shifter. By setting the phase shift, the feedback loop starts to oscillate. Frequency of those oscillations will be equal to the frequency where the resonance condition is fulfilled (note that is not necessarily at the exact cavity resonance frequency). Advantage of this excitation system is that it immediately finds "some" resonance and allows to inject energy into the cavity. The self excited loop is very popular for systems with not completely known parameters (e.g. a new cavity which arrived from the production, or a system which is restarted after a long stop period). However it allows only a very limited control over the generated field so it is not suitable for the linac operation and it has a limited use for the cavity conditioning.

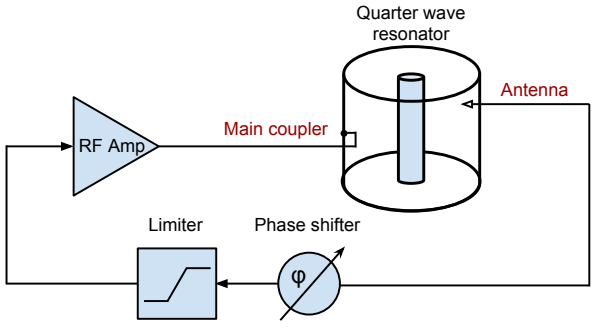

Figure 15: Self excited loop

3.2.2 Generator driven mode of operation

A different feedback loop configuration is the "generator driven mode", shown in Figure 16. An external generator injects the primary RF signal at the requested frequency but with no defined phase/amplitude relation to the controlled cavity field. The signal passes through a vector modulator and RF power amplifier feeding the cavity via the fundamental power coupler. Electromagnetic field in the cavity is again sampled by a secondary coupler. This antenna signal is then transformed either into an I-Q pair or a magnitude/phase pair. The respective quantity enters a traditional feedback loop. The error signal from the loop drives the vector modulator to keep the magnitude/phase at their desired values (set points). Provided sufficient power is available, this kind of loop is capable to lock the cavity to a given reference, compensate fast perturbations like cavity microphonics or beam loading. The cavity could also be perturbed mechanically by changing its resonant frequency, e.g. by variations in the helium pressure. Feedback loops need to constantly monitor the cavity tune state and eventually push it back to resonance by the tuning system. Operating cavity at or a very close to the resonant frequency assures optimal use of the RF power requested from the power amplifiers. This configuration is more complex to implement, but if designed properly it provides a full control over the field in the cavity. Generator driven mode also allows to do a sophisticated cavity conditioning.

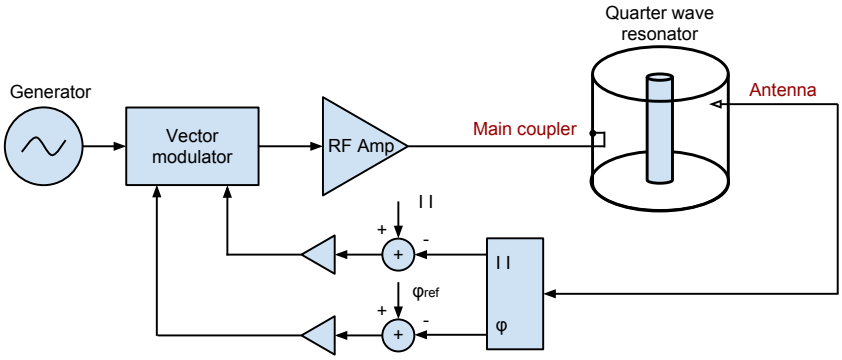

Figure 16: Generator driven system

For a high loaded Q cavity operation both types of feedback loops will need to be implemented. In the machine it is foreseen to start the cavity using the features of the self excited loop which will immediately find the resonant frequency. Note that the cavity bandwidth in the HIE Isolde will be only few Hz at an operating frequency of 101.28 MHz so finding the initial resonance is not a trivial task as finding it by measuring the cavity frequency response can be very time consuming. Once the cavity is powered the LLRF controller will tune it to the correct resonant frequency using the mechanical tuner. Then the feedback loop will be switched over to a generator driven mode locking it to the linac master RF reference. So the LLRF controller will profit from both configurations, using the best of each.

3.2.3 State of The Art

The Large Hadron Collider (LHC [12]) built at CERN during the years 2001 to 2008 is currently the world largest and the highest-energy particle accelerator. It is also considered to be the most complex machine the mankind ever built. Its purpose is to do fundamental research in the field of particle physics and structure of matter. The LHC are in fact two accelerators in one, accelerating two independent beams of protons and heavy ions up to the energy of 7 TeV (or equivalent for the heavy ions). Speaking of RF, each of the two rings is powered by 8 superconducting 400 MHz standing wave cavities.

Brief description of its LLRF system is provided in [4]. A diagram of this system is shown in Figure 18. The feedback system for each cavity is integrated on six very dense, mixed form factor VME cards, containing several sophisticated feedback and feed forward loops with a very different time constants ranging from 600 ns to few seconds. All loops need to "collaborate" together. Some of them are implemented purely in an analogue domain to obtain speed and short group delays, others in digital domain to obtain the precision and sophisticated functionality. The complete LHC LLRF system comprises of about 800 VME cards of about 25 different types, all developed, designed and built at CERN.

Each VME crate contains a front end control computer, one or several timing cards, space for RF specific VME cards and the clock distributor card. The crate is controlled remotely through the front end software. This is then implemented into the CERN control framework by means of FESA classes (Front End Software Architecture). A variety of high level applications (like the machine control system, data logging, the human interfaces, diagnostics etc.) talk to the FESA layer without need of explicit knowledge of the particular hardware behind.

The cavity controller is basically a multi channel vector RF receiver. For simplicity the LHC LLRF system uses a direct conversion architecture. Each RF signal relevant to the cavity operation is down-converted from the 400 MHz domain to an intermediate frequency of 20 MHz. Then it is digitized by 14 to 16 bit ADCs running at a sample rate of exactly four times the IF frequency (i.e. 80 Msps) providing the direct digital quadrature demodulation (this concept will be further explained in the later chapters). The I and Q components are digitally processed by programmable logic devices (FPGA) and digital signal processors (DSP). The corrective response is calculated and sent to a vector modulators. The signal is again up-converted to the RF domain and fed to the power amplifiers.

Recent advances in the digital technology allow to directly digitize the RF signals already in the GHz range omitting the analogue front-ends. For the HIE-Isolde project we have opted for a direct RF sampling and digital quadrature demodulation and a direct digital RF generation (see later chapters). It will be the first LLRF system at CERN using this concept (beyond the base band machines like the PS Booster and the PS).

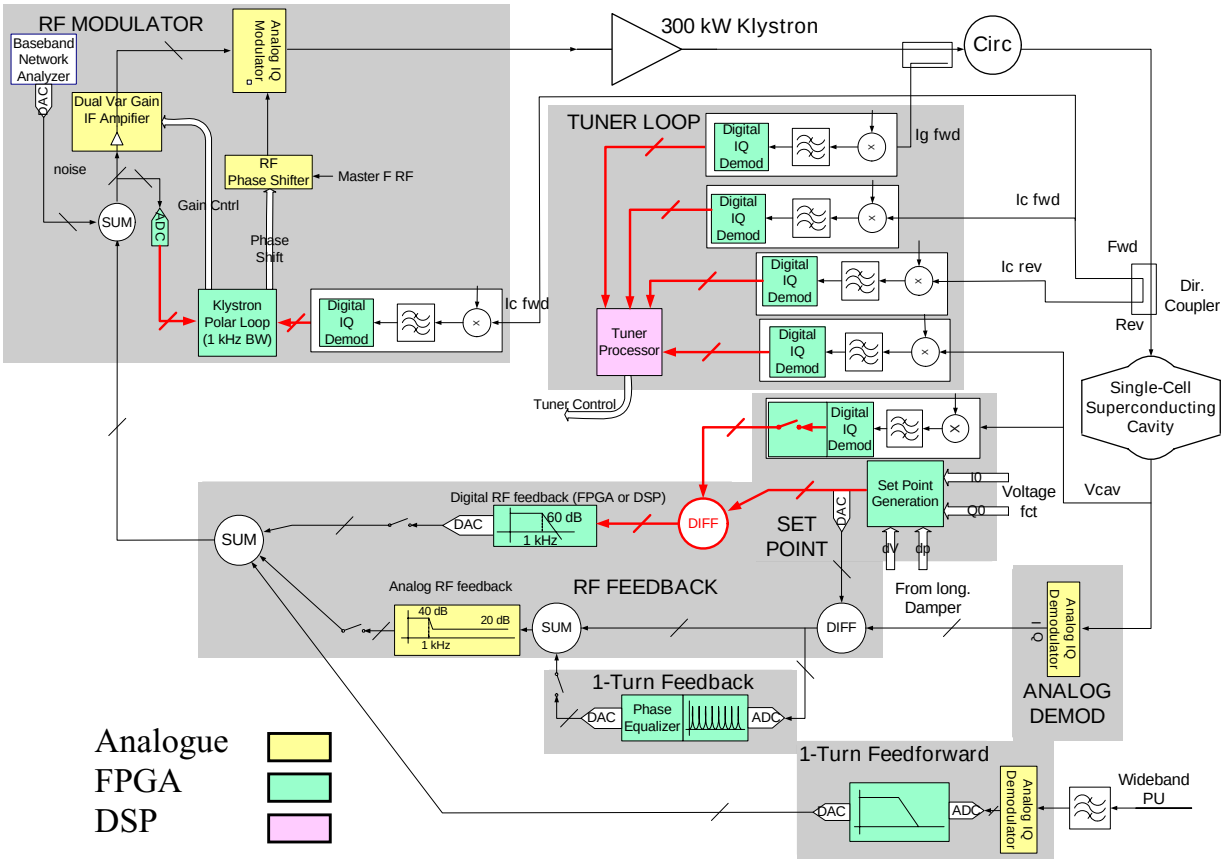

Figure 17: LHC cavity controller diagram [4]

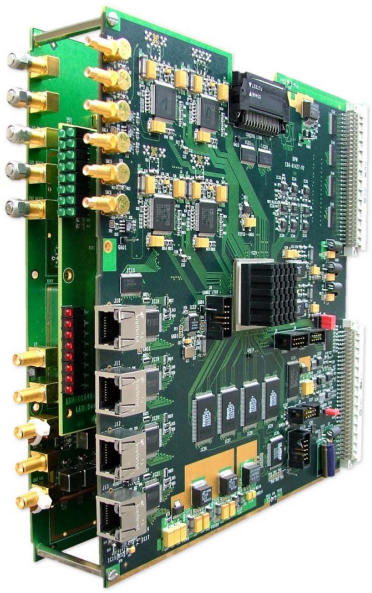

Figure 18: LHC beam phase module. An example of a mixed RF and digital VME board [3]

4 Warm cavity test setup

A full scale test setup was built in the building 864 to develop, validate and debug all hardware and software components for the HIE-Isolde LLRF system. A diagram of the test setup is shown in Figure 19. The test setup is equipped by a real HIE-Isolde quarter wave resonator cavity with striped niobium layer. It is actually one of the first cavity prototypes used to test the chemistry and the niobium sputtering process. The cavity is installed in a support frame and it is in a normal conducting state - therefore the "warm cavity setup". The Q_0 value of the normal conducting cavity is in order of 10 000 to 20 000, unlike 10^9 in the superconducting state. As it will be explained later, the Measurement card and the LLRF system as such however has a very good amplitude and phase measurement resolution and accuracy, so scaling of parameters between the superconducting and normal conducting state is possible.

The cavity is equipped by a real fundamental power coupler and a simulated antenna coupler. The cavity resonant frequency is controlled by a mockup of the final tuning mechanism. Couplers and tuner are controlled by a final version of the PLC controller.

A full scale LLRF system to control the cavity is being developed. The VME crate is located in the rack with other control systems. The LLRF system drives a 30 W RF power amplifier feeding the cavity.

A photo of the complete warm cavity setup is shown in Figure 20.

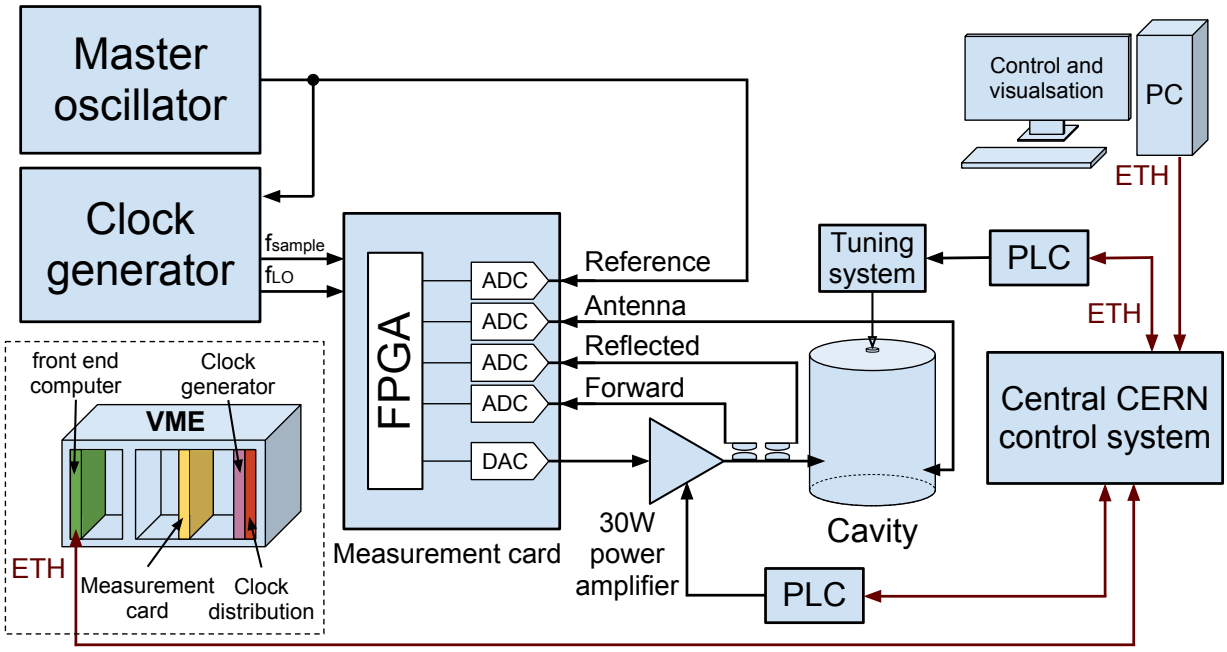

Figure 19: Schematic diagram of the warm cavity test setup

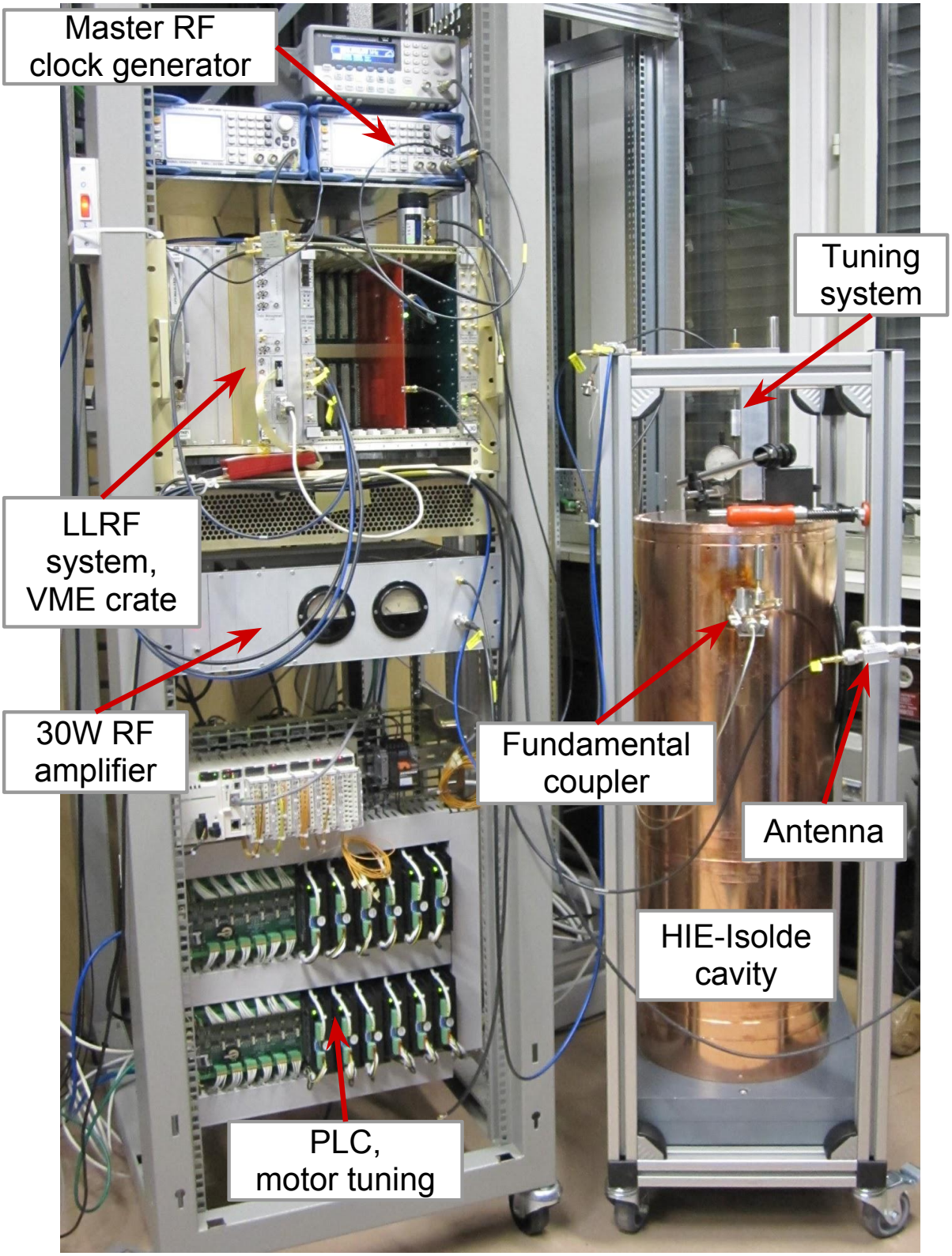

Figure 20: Warm cavity test setup in the building 864

5 Measurement card

5.1 Requirements

Field quality and stability is an essential parameter in an accelerator, which has a direct impact on the beam parameters. In order to obtain the desired beam quality in the HIE-Isolde, the accelerating field in each cavity needs to be controlled to better than 0.2° RMS in phase and 0.2 % RMS in amplitude with respect to the reference [13] [14]. The goal is to develop a module, which can precisely measure all four RF signals relevant to the cavity operation: the RF reference, cavity forward, cavity reflected and antenna signal. The four mentioned RF signals contain a full information about the cavity state and the accelerating voltage needed to control the cavity and stabilize the field. The measurement system discussed in this thesis is a preparatory work for the complete LLRF controller which will be built on the foundations of the measurement card.

The system should be fully digital. The RF signals will be sampled by a set of fast ADCs and processed by the FPGA. Calculation and generation of the RF signal should be done entirely in a digital domain inside the FPGA, to make the design simple, robust and open for potential future functionality upgrades. The digital output signal will be converted to an analogue domain using a high-speed digital to analogue converter (DAC).

As the system will be fully automatic and entirely remotely controlled several other features must be implemented. A fast and sufficiently large observation memory (to analyse measured and processed signals remotely), the so-called "post mortem" memory (to log last data in case of a critical system failure) an extensive diagnostic features. Configuration of the measurement card parameters will be done over the VME interface and the FPGA must be remotely programmable through the crate manager module. The HIE-Isolde LLRF system will be a part of the CERN infrastructure so all interfaces must be compliant with current CERN standards. Proposed block diagram for this card is shown in Figure 21.

5.2 VME modular system

VMEbus is a computer bus standard developed in 1981 for Motorola 68000 line of CPUs [15]. The VME crate consists of a power supply, backplane - providing data interconnections to all modules and an embedded control computer. The form factor is based on the Eurocard sizes [16]. The communication between cards is based on a parallel data and address bus with several bus arbitration lines (data transfer and interrupt lines). Several cards can be inserted into the VME crate making it a very versatile system. The VME specification evolved over the years - from a simple 16-bit, 32-bit to 64-bit versions today. Although not the most recent and powerful standard the RF group took a decision in the year 2000 to use the VME as the platform for the LLRF electronics at CERN. VME is a mature, proven and reliable technology providing the necessary infrastructure for systems where reliability and availability are the most critical parameters.

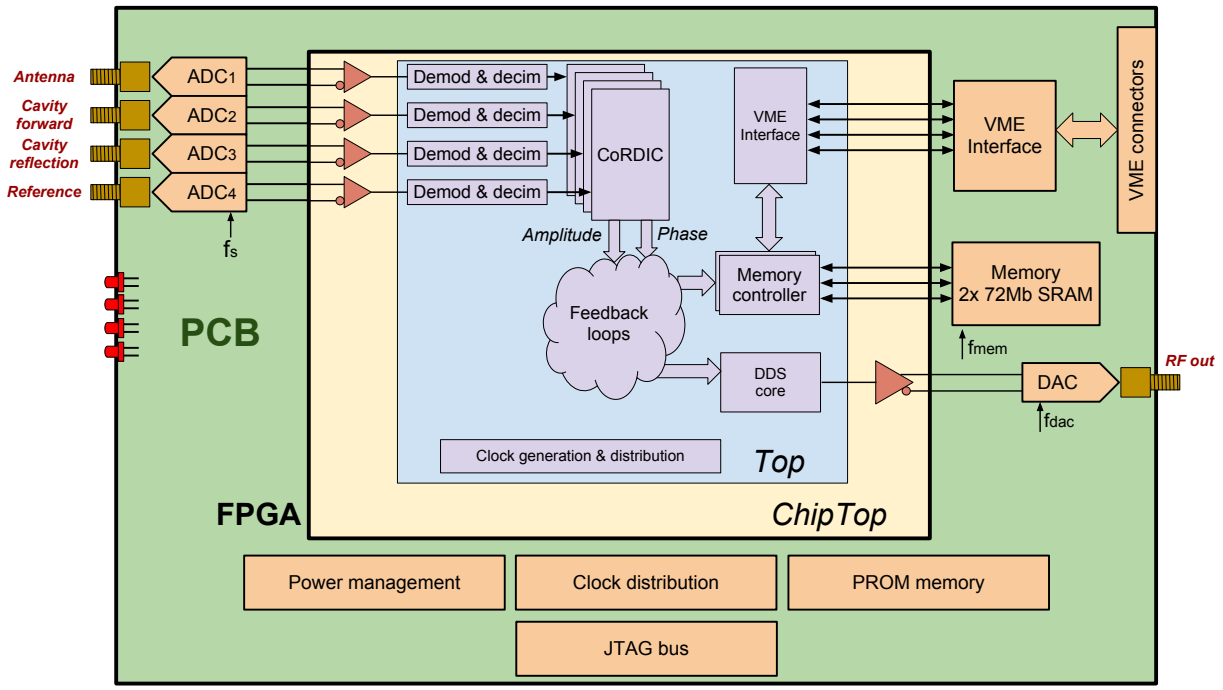

Figure 21: Measure card block diagram

The RF group at CERN introduced a modification to the VME standard, where the J2 connector (the bottom one) is not used for the VME communication but instead a custom backplane - called the LHC RF Low Level backplane is installed (see Figure 23) [17]. Main functions of the custom backplane are:

- Additional analogue supply rails distribution (±6 V, ±12 V)
- Digital +3.3 V distribution
- Clock distribution (4 ECL signals)
- Timing distribution (11 trigger lines)
- Function Generator Data distribution (slow serial links)
- Interlock lines
- Inter-module 1 Gbps LVDS digital data links
- Crate Centralized Reconfiguration JTAG chain
- Module Serial Number bus
- Automatic Slot Addressing

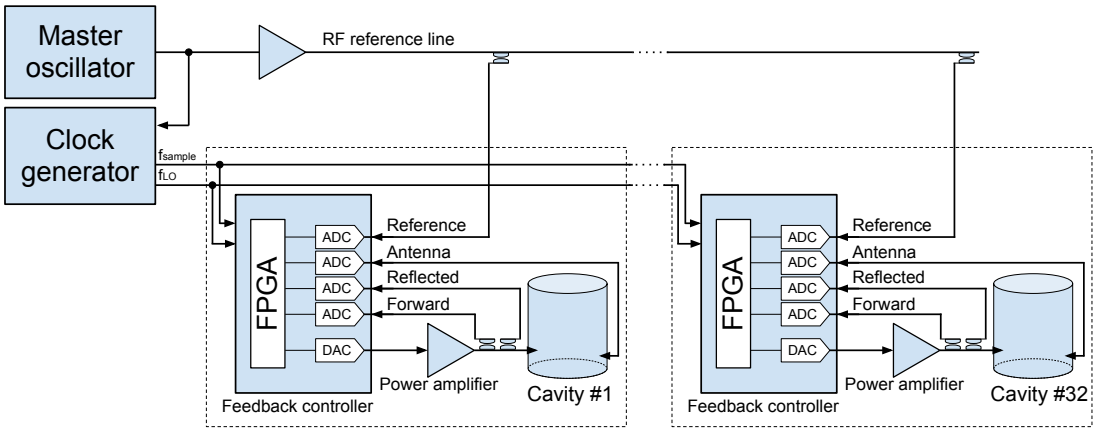

Figure 22: HIE-Isolde machine LLRF diagram

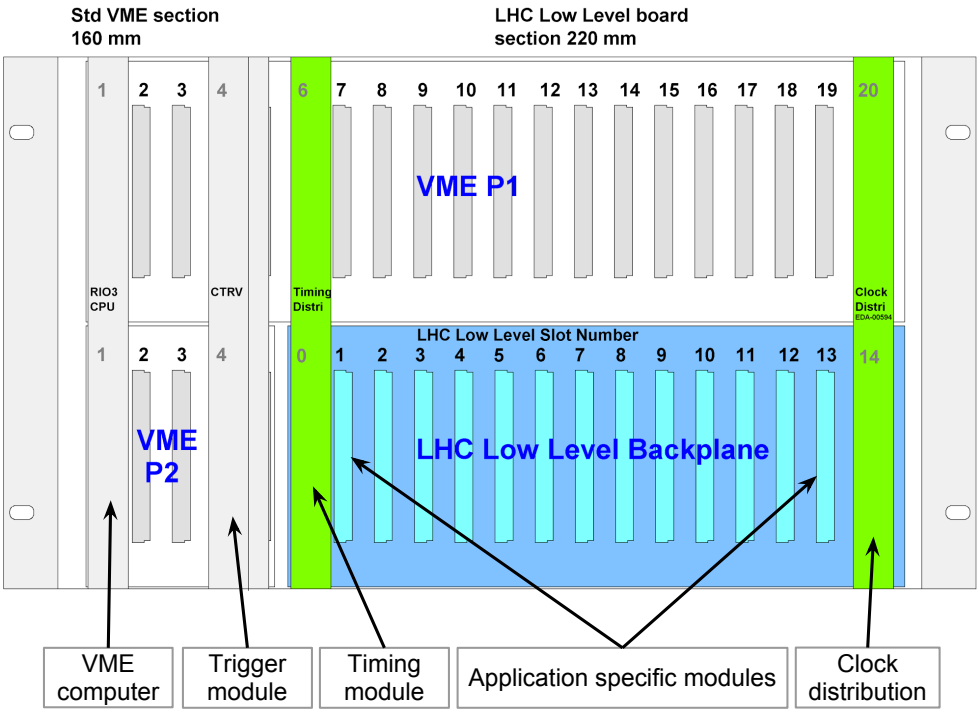

Figure 23: LHC RF Low Level chassis

VME is a register-based system, meaning that the embedded computer in the leftmost slot takes care of a bus arbitration, module addressing and configuration. From the user module (card) point of view the logic needed to implemented the VME communication is not very complex. Therefore no micro-controller on the custom boards or in the FPGA is needed simplifying the card design.

5.2.1 Direct RF sampling and direct digital quadrature demodulation

Since the cavity resonant frequency (f_0) of 101.28 MHz is well within the analogue bandwidth of modern AD converters, we can directly sample the RF signals without additional down conversion to an intermediate frequency. Loop dynamics of a system with very high Q cavity is a relatively slow process asking only for few hundred Hz bandwidth. Apart of direct RF sampling this also allows us to heavily undersample the RF signal.

For further processing the system must measure the input signals in a vector form. So it is convenient to choose the sampling frequency such that the AD conversion will immediately perform the direct digital quadrature demodulation, e.g. the sample stream will directly represent the I and Q components of the original RF signal. The direct digital demodulation is achieved by sampling the input signal at times corresponding to integer multiples of a 90° phase advance. The ADC then outputs a series of samples representing the I, Q, $-I$ and $-Q$ values. In order to fulfil this condition the sampling frequency f_s and the RF frequency f_0 must be locked in a relation defined as:

$$f_s = \frac{4f_0}{4k+1} \tag{1}$$

Where k is an integer number. This sampling scheme is illustrated in Figure 24 for $k = 0$. The Figure 25 illustrates the sampling at a lower rate ($k = 1$) with presence of a slow modulation.

5.2.2 ADCs

Quality of an input signal digitalization is the key parameter in the Measurement Card design. In case of a high noise, jitter or distortion, it would be almost impossible to develop a performing system. What we need is a high SNR (Signal to Noise Ratio), good resolution (at least 14-bit), high effective number of bits (ENOB) ideally close to the ADC resolution, differential signal and clock inputs and support for low sampling frequency. Several converters (14 and 16 bit resolution) from Analog Devices and Linear technology were evaluated. Finally the AD9255 was chosen.

The AD9255 is a 14-bit, 125 Msps ADC, with differential input and pipelined multi stage core. Its target applications are communications, instrumentation or medical imagining. It supports up to 300 MHz analogue signal bandwidth necessary for the direct RF sampling,

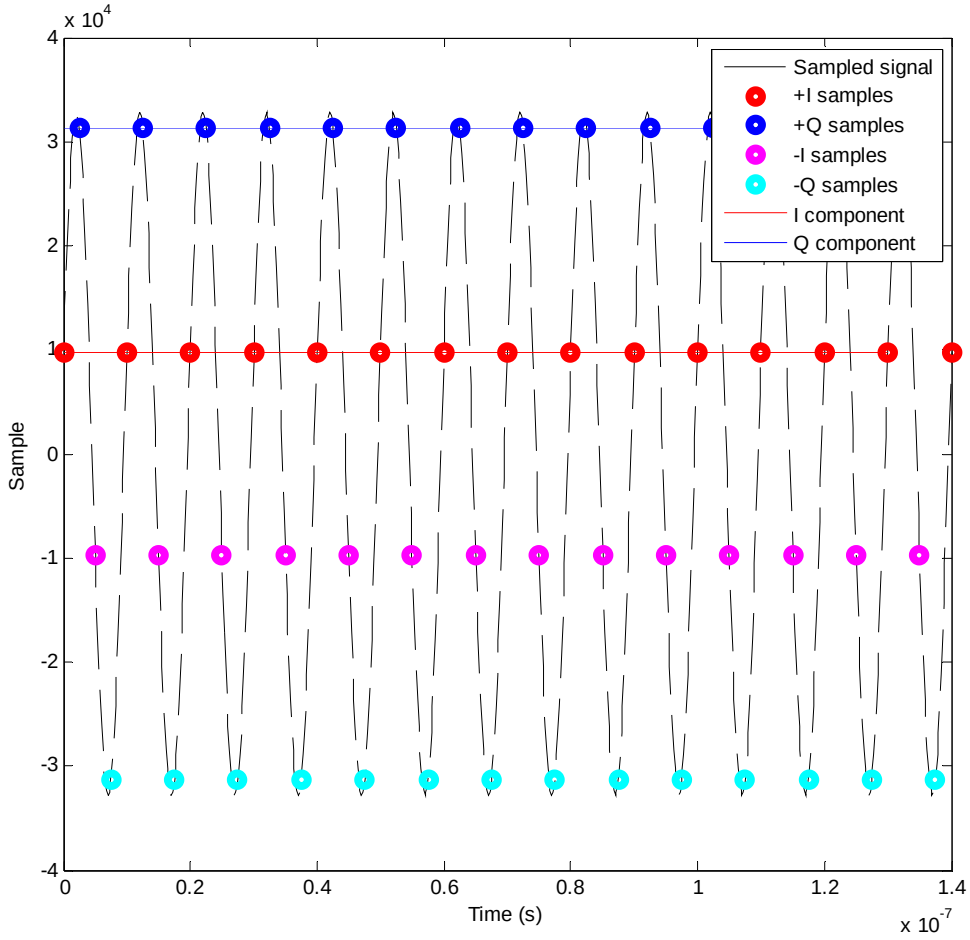

Figure 24: ADC sampling scheme, $k = 0$, locked frequencies

operates from a single 1.8 V power supply and offers a SNR of 78.3 dBfs. Functional diagram is shown in the Figure 26.

The input RF signal is directly fed into RF transformer to transform the single-ended inputs into differential with proper ADC bias voltage applied to the secondary winding centre. The ADC full scale voltage is configurable using the SPI (Serial Peripheral Interface). The AD9255 offers either 2 V internal voltage reference - so the input single ended signal should be at 10 dBm (into 50 Ω load) or 1.25 V corresponding to a 4 dBm input signal. Each ADC on the measurement board can be configured separately.

Due to practical limitations of real ADCs there is a minimal sampling frequency at which the converter can be operated. The AD9255 chip requires minimum f_{sample} of 10 MHz what has some consequences to the clocking scheme of the whole system.

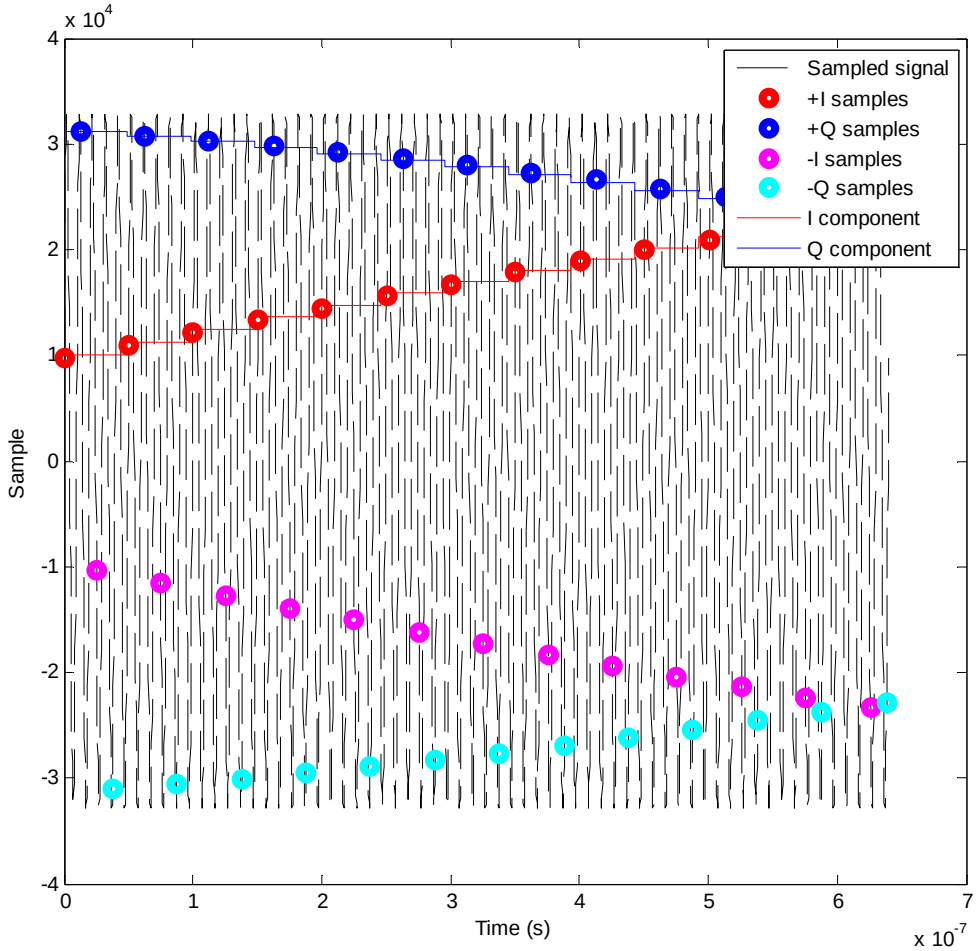

Figure 25: ADC sampling scheme, $k = 1$, variations in the RF signal

5.2.3 DAC

The measurement system is a preparatory work for the final LLRF controller. In order to close the feedback loop (and not only to measure the signals) it is necessary also to generate the RF signal. Following the same philosophy as for the input path it was decided to generate the RF directly, using an on-board digital to analog converter. A dual 16-bit TxDAC+ AD9122 with sample rate up to 1200 Msps was chosen [18]. It offers a multi-carrier generation up to the Nyquist frequency, interpolator/modulator, LVDS digital interface, two differential outputs (can be used as an I a Q channels). Functional diagram of the AD9122 can be seen in the Figure 27.

There are several options how to generate the output RF signal: a baseband generation by one DAC with up-conversion, a vectorial generation (I and Q DACs) with analogue up-conversion, a direct RF generation using up-sampling in the DAC, or a combination of these methods. The method is still to be evaluated but the AD9122 should support all of

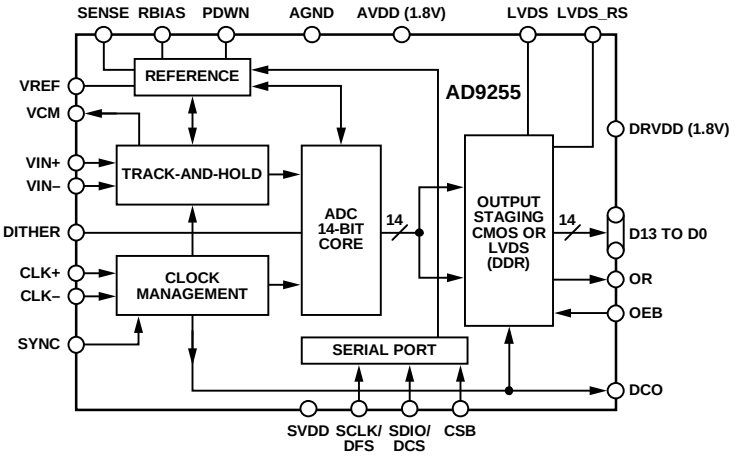

Figure 26: Functional block diagram of the ADC AD9255

these options.

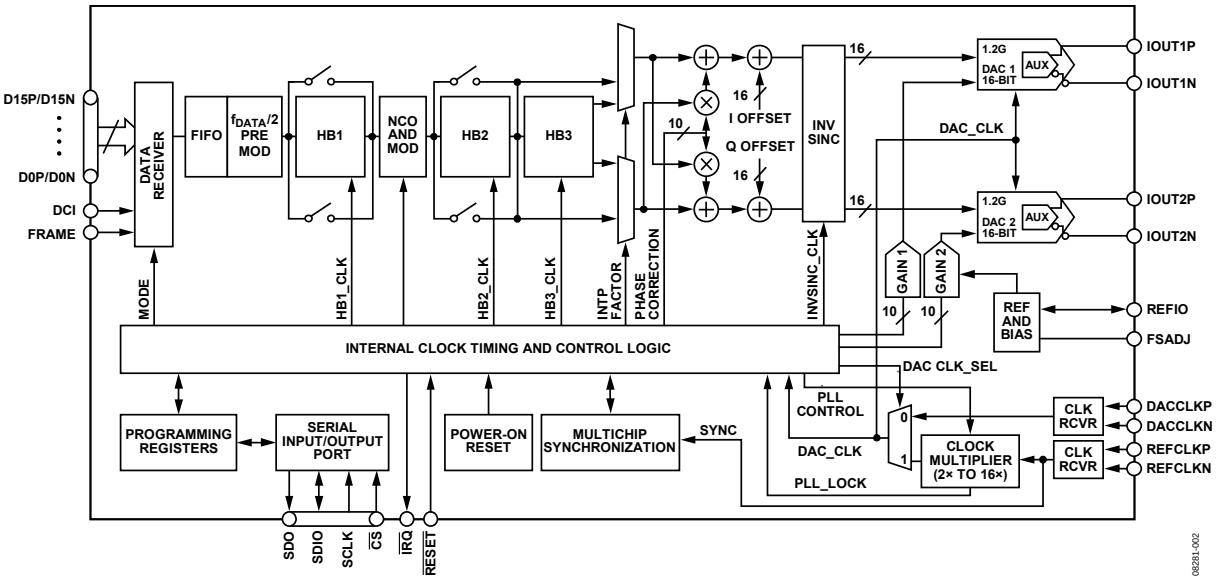

Figure 27: Functional block diagram of the DAC AD9122

5.2.4 Onboard clock distribution

Several clock signals are needed for operation of the measurement card. Some originating on the board itself (e.g. the 200 MHz crystal oscillator), some are received from the VME backplane. The clock signals are distributed using the AD9512 low noise clock distribution chip. Three low jitter output buffers are used, all of them connected directly into the

FPGA. The 200 MHz, 100 MHz and 50 MHz clocks are needed for the FPGA operation. All of them are distributed in the LVDS (low voltage differential signal) standard.

On top of the quartz oscillator, four differential clocks are received from the backplane P2 connector in a PECL (positive emitor coupled logic) standard. All of them are wired into the FPGA, but only one line is currently used - the ADC sampling clock with frequency about 10.9 MHz (see later) which is referenced to the master RF clock source frequency.

5.3 FPGA and the firmware

The measurement card is populated by the Xilinx Virtex 5 family FPGA [19], (type XC5VSX50T), designed for high-performance signal processing applications with advanced serial connectivity. This FPGA can work with 3.3 V logic, contains 8 160 Virtex-5 slices, 780 kb distributed RAM, 4 752 kb block RAM and 480 user I/Os. This FPGA is large and powerful enough to accommodate the measurement system functionality. As already mentioned, the measurement card is a preparatory work for the final LLRF controller. Complete functionality of the controller is not yet fully defined so the FPGA was chosen such that a larger pin-compatible model with more hardware resources could be soldered to the same printed board. The configuration memories are already prepared for the largest FPGA of this family.

There is a well established firmware design flow in the BE/RF/FB section. The firmware starts with a generic code created by a visual environment. A Mentor Graphics Visual Elite package is used for that. It allows to manage the whole project, supports VHDL and Verilog languages, hierarchical graphical blocks and many other features. It is possible to develop code both in a text form as well as in a graphical form - using logical blocks and macros, truth tables, state machines etc. Connection between the hierarchical blocks is done by a variety of signals, buses and taps. Every hierarchical symbol can contain as many underlying layers as required by the design. Internal design rules in the section dictate to use the block "Top" to accomodate the complete generic design (which could be compiled for any FPGA of any vendor). If specific hardware features of a specific FPGA are used (like DSP blocks, gigabit transceivers etc.) the "Top" block is inserted into a so called "ChipTop" block. All device specific primitives, defined as blackboxes are housed here. The I/O pins of the ChipTop block are considered to be the physical I/O pins of the FPGA. An example of this hierarchy is shown in Figure 28.

Control of the VME modules is done by a set of registers, called a memory map. In the design flow it has a fixed name "RegCtrl" (Register Control) assigned. The block contains a definition of all VME registers, way of accessing them, if they are persistent or not, default values as well as their folding or separation into individual VHDL signals used in the design. Generation of this block was fully automized using a tool called "Cheburashka" which was developed by the controls group in order to simplify the design process. The module developer prepares a list of all registers and memory interfaces in a simple tabular form. The tool then creates the VHDL block which is compiled into the design. It generates

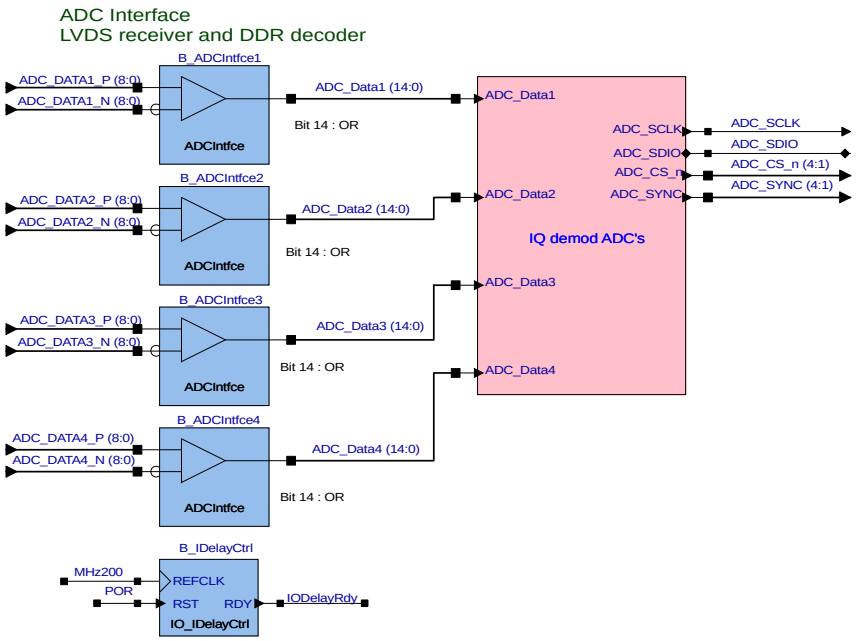

Figure 28: LVDS receiver and DDR decoder as a chip specific primitives defined on the ChipTop level

also all necessary XML files for automatic driver generation, skeleton for the FESA classes and integrates the design in the control system. The tool significantly shortens the design time and reduces chances of errors. Cheburashka user interface is shown in Figure 29.

Output of the Visual Elite is a single generic VHDL file. It is then loaded into the Synplify tool, which does all the optimizations and translations from the generic VHDL code into a device specific EDIF format (Electronic Data Interchange Format). It contains the design netlist with pre-mapped blocks in an industry standard form. This optimized netlist file is then loaded into the Xilinx ISE tool which does the place and route and timing analysis. The bitstream is than either directly loaded into the FPGA, or converted into a PROM file and flashed into the onboard PROM memory using the Xilinx iMPACT tool.

A complete firmware design flow used in the BE/RF/FB section is sketched in Figure 30.

5.3.1 Decimator and demodulator VHDL block

Relatively low required feedback loop bandwidth (hundreds of Hz) and a need of high sampling frequency due to the ADC limitations (> 10 MHz) allows us to heavily decimate the input data (by a factor of 2^{10}) lowering the noise while still fulfilling the Nyquist criterion. A decimator with simple rectangular window is suitable for our application. The

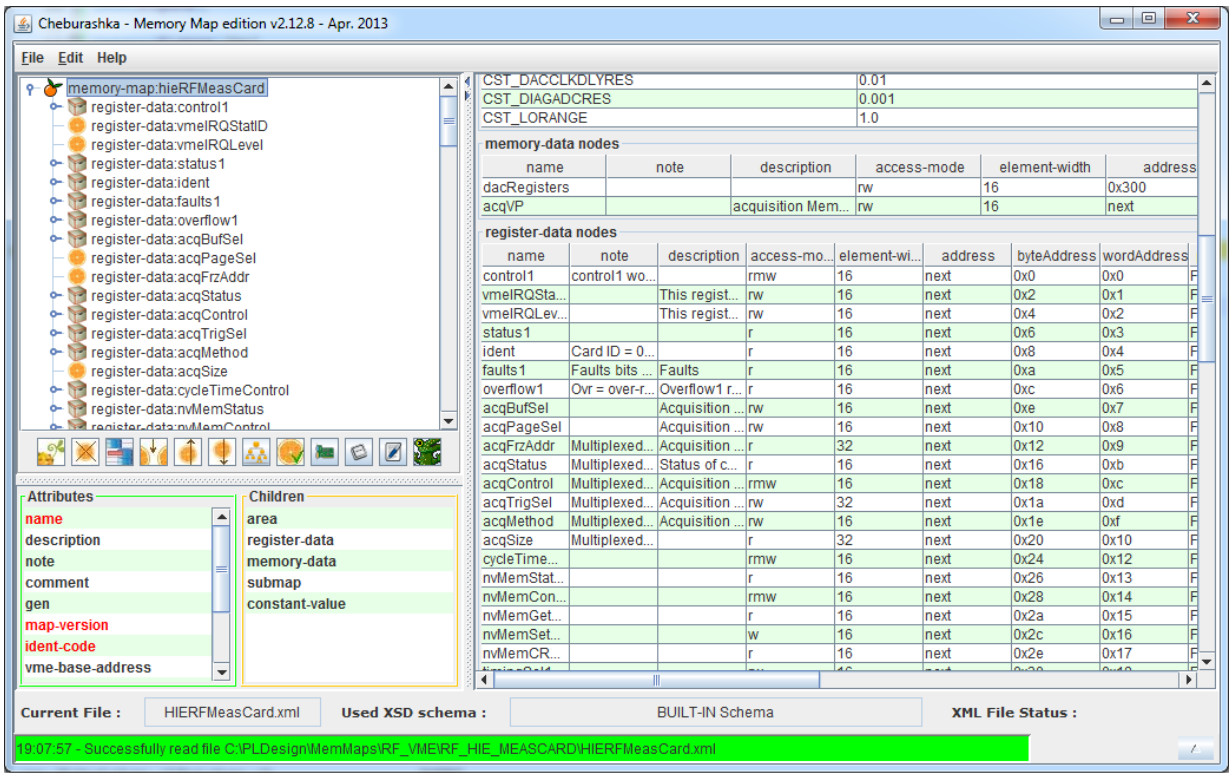

Figure 29: VME memory map in the Cheburashka software

transfer function of this decimator is described by (2) and (3).

$$I_{OUT} = \frac{1}{2^{DF+1}} \sum_{n=0}^{n=2^{DF}-1} [y(4n) - y(4n+2)] \tag{2}$$

$$Q_{OUT} = \frac{1}{2^{DF+1}} \sum_{n=0}^{n=2^{DF}-1} [y(4n+1) - y(4n+3)] \tag{3}$$

where $y(n)$ is the input data stream from the ADC, DF the decimation factor and I_{OUT}, Q_{OUT} the output data streams at a reduced data rate of $\frac{1}{2^{DF+2}}$.

This decimation algorithm was implemented in the VHDL language and synthesized into the Virtex 5 FPGA. Basic operational principle is the following - the data are sampled with ADC clock rising edge, modified to a proper bus format/size and enter decimation block. There, depending on the decimation factor, are sorted into I and Q samples, rescaled and stored into the accumulators. When defined number of I and Q samples is collected, value of those temporary registers is divided by a number of accumulated data samples, copied to the output port, and DecimMarker (Data_valid) strobe is asserted. This strobe is synchronous with the ADC clock, common for all ADCs and always lasts exactly one clock period. The strobe is used as a signal to inform the memory block that processed data

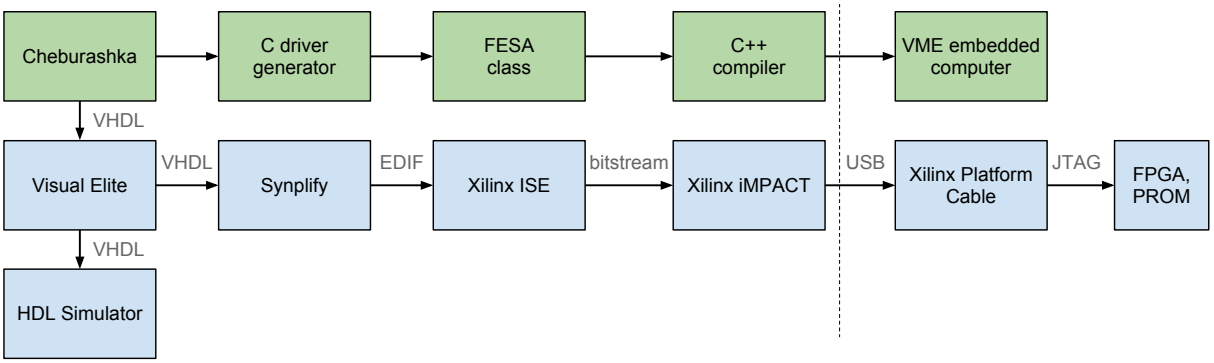

Figure 30: Firmware development design flow. Blue blocks show the hardware development, green blocks the software development

should be stored into the external SRAM memory using memory controller or a calculation on those data should be performed.

The decimated and demodulated I and Q data are converted from the cartesian to a polar format using VHDL implementation of a CoRDIC algorithm [20] (in our case pipelined core). The phase and magnitude of each channel is normalized using the reference channel. In the measurement card this is so far end of the signal processing, as we need only to observe the signals. In the future feedback controller these will be the error signals in a feedback loop to generate the accelerating voltage in the cavity. All those post processed signals can also be stored into the external (circular) memory buffers, and frozen at any time to readout any part of the buffers using VME bus.

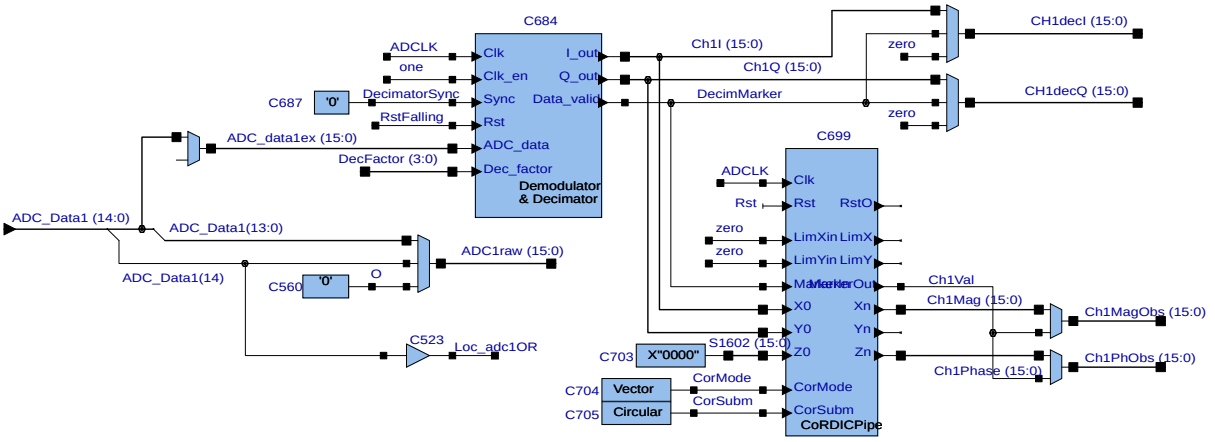

Figure 31: Decimation and CoRDIC blocks in the Visual Elite environment

```
architecture V1 of DemodDecimator is
  constant DecimInit : natural := 2**15-1;
  constant Zero : signed(28 downto 0) := (others => '0');
  signal Iacc, Qacc : signed(28 downto 0);
  signal IQstate : natural range 0 to 3;
  signal DecimCounter : natural range 0 to DecimInit;

begin
 process(Clk, Rst)
  begin
  if rising_edge(Clk) then
   if Rst = '1' or Sync = '1' then
    IQstate <= 0;
    Iacc <= (others => '0');
    Qacc <= (others => '0');
    I_out <= (others => '0');
    Q_out <= (others => '0');
    Data_valid <= '0';
    DecimCounter <= 2**To_Integer(Unsigned(Dec_factor))-1;
   elsif Clk_en = '1' then
    case IQstate is
     when 0 =>
      IQstate <= IQstate + 1;
      if DecimCounter = 0 then
       Data_valid <= '1';
       Iacc <= Zero + Signed(ADC_data);--(others => '0');
       Qacc <= (others => '0');
       I_out <= Std_logic_vector(Resize(shift_right(Iacc, To_Integer(
   Unsigned(Dec_factor))+1), 16));
       Q_out <= Std_logic_vector(Resize(shift_right(Qacc, To_Integer(
   Unsigned(Dec_factor))+1), 16));
       DecimCounter <= 2**To_Integer(Unsigned(Dec_factor))-1;
      else
       DecimCounter <= DecimCounter - 1;
       Iacc <= Iacc + Signed(ADC_data);
      end if;
      when 1 =>
       Data_valid <= '0';
       Qacc <= Qacc + Signed(ADC_data);
       IQstate <= IQstate + 1;
      when 2 =>
       Iacc <= Iacc - Signed(ADC_data);
```

```
       IQstate <= IQstate + 1;
      when 3 =>
       Qacc <= Qacc - Signed(ADC_data);
       IQstate <= 0;
     end case;
    end if;
   end if;
 end Process;
end;
```

Listing 1: Example of a VHDL code: implementation of the decimator and demodulator block

5.3.2 Memory controller

Two SRAM CY7C1480V33 72-Mbit pipelined sync SRAM operating up to 200 MHz are implemented on the card. The memory interface was designed using the switching waveforms (shown in Figure 32) in the Visual Elite environment. This controller can be seen in a graphical representation in Figure 33. To meet the memory access timing table the data are aligned with the address by means of the slice I/O flip flops. Tri-state buffer switches between the read and write data modes. Timing of the I/O block had to be carefully designed and properly simulated before synthesizing it into the FPGA as a bus conflict due to improper bus management can easily damage the FPGA I/O banks. To keep the clocking scheme as simple as possible the memory is currently clocked from the same clock source as the ADCs. This way the whole chain is synchronized and no buffer to change the clock domains is needed as this operation is always bit tedious. However read out of the full 4×1 M sample memory at the ADC clock frequency is rather lengthy, therefore a more sophisticated memory controller is foreseen. The memory will be written synchronously with the ADC clock, but the VME access (read out) will be carried out at much higher VME bus frequency (50 or 100 MHz). Memory controller was also designed in a way that it allows a single data write cycle - feature used for writing data only when the new decimated data are ready at a much slower rate than the ADC clock.

Two instances of this memory controller are used in the measurement card. This allows us to use the second physical memory as a post-mortem memory - operating in a different clock domain, storing data for later analysis in case of a machine fault. With the current memory configuration, each physical memory chip can simultaneously store two 18-bit channels, each containing 1 310 720 points. Depending on the decimation factor (decimal value from 0 to 15), the record length could be anything from 0.48 seconds (at a sampling frequency 2.723 MHz) for decimation factor of 0, to over 4 hours at factor of 15 (at a sampling frequency 83.3 Hz).

Since only four distinct input data streams can be simultaneously stored into the memory, various signals from the signal processing chain are multiplexed to allow observation

of any desired signal.

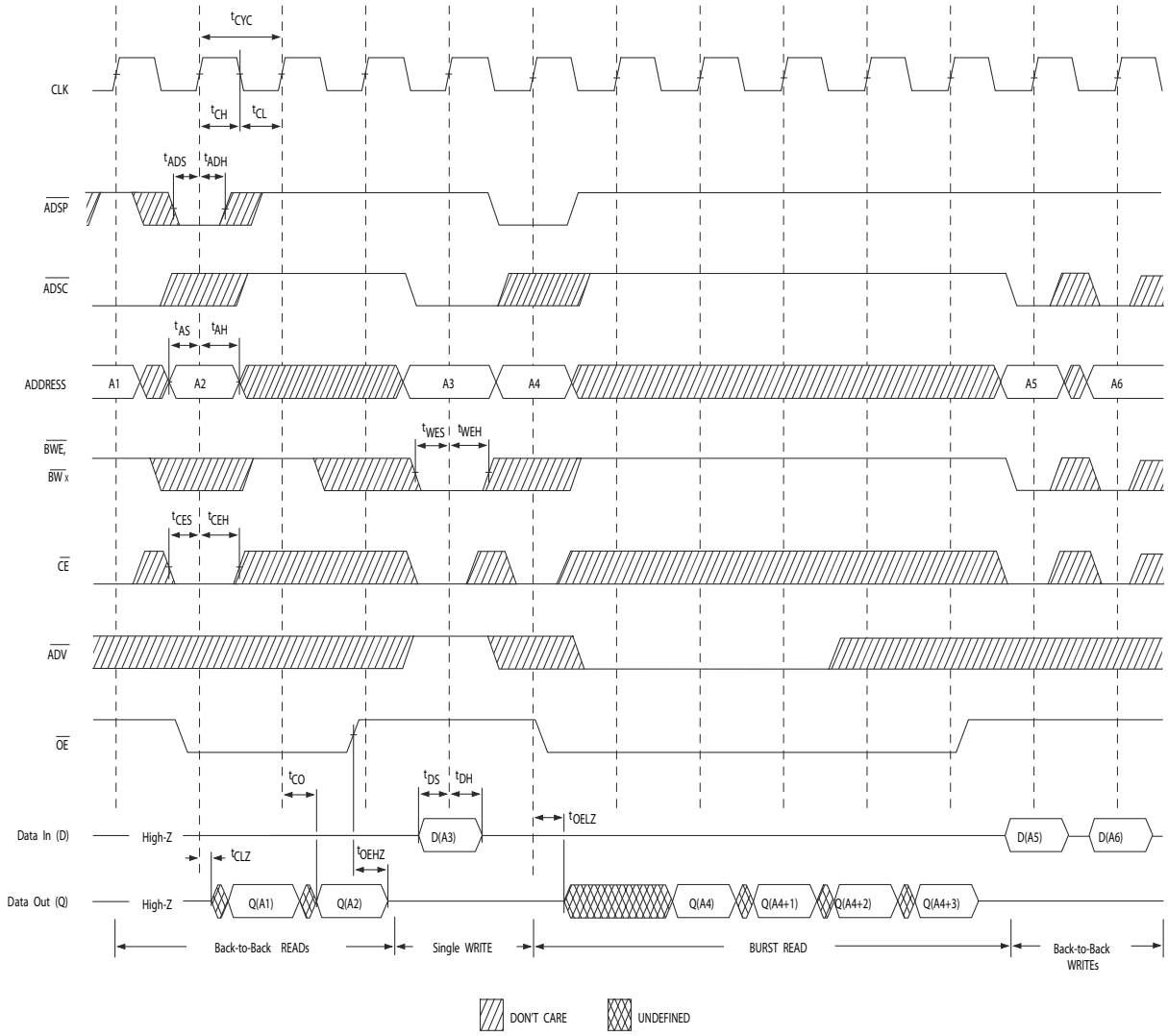

Figure 32: SRAM Read/Write cycle timing [5]

5.3.3 Module configuration

VME cards need to be initialized on start-up with their operational parameters. This is done automatically using the earlier mentioned drivers and the FESA classes running on the VME front end computer. Later, operators or the machine central control system can modify the parameters using either graphical user interfaces, or the databases and the control sequencers.

During development the VHDL code synthesis into a big FPGA is a time consuming process. Even on a modern eight core CPU it takes easily tens of minutes to compile even

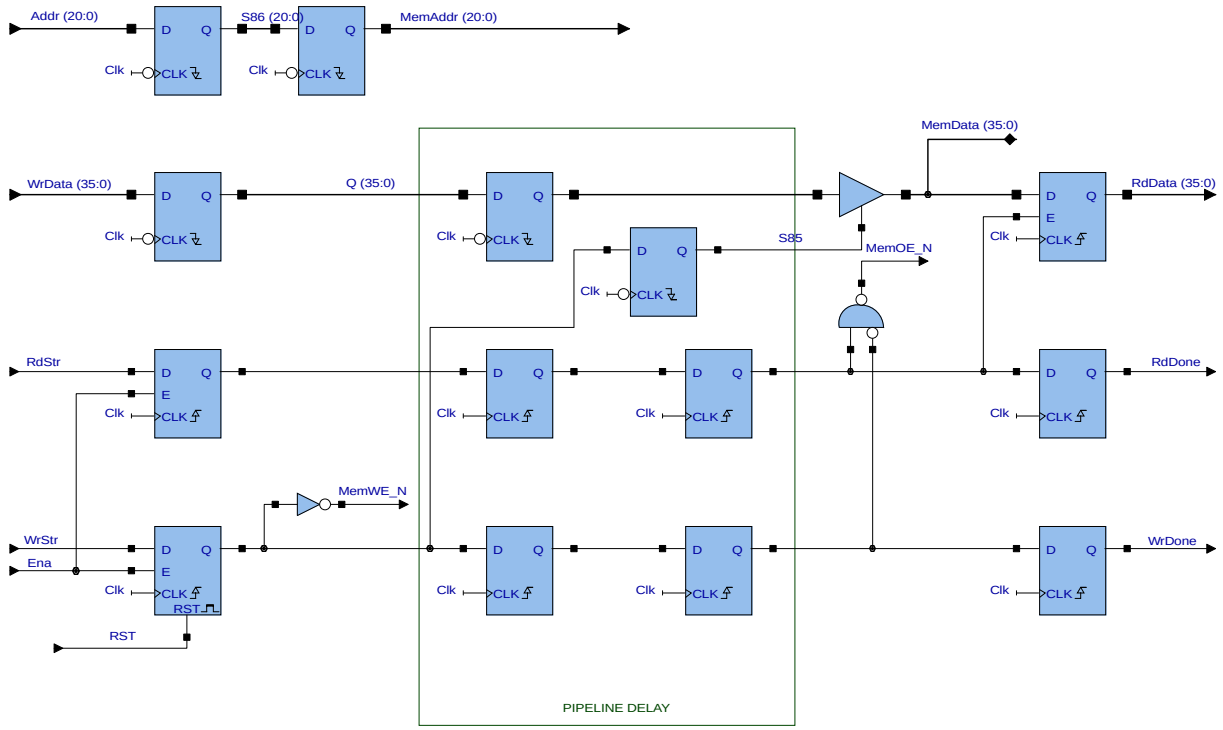

Figure 33: Lowest level of the memory controller in the Visual Elite environment

a simplest change in the code. Uploading bitstream into the PROM memory takes another ten minutes and the card must be rebooted to load the new firmware. For an operation in the particle accelerator with very limited access it is also advantageous to foresee a remote FPGA flashing. If there are more than few cards installed (in our case 32) a remote flashing is a must. Also many blocks within the Measurement card communicate over a SPI or I2C serial bus. In most of cases those blocks would not work without an initial configuration. So after the FPGA loads its bitstream from the PROM memory, it issues a controlled reset, configuring all onboard blocks with some sort of a default configuration hardwired in the VHDL code.

5.3.4 Configuration scripts

New VME boards are not immediately fully supported by the software section as the firmware and the memory interfaces are constantly changing. Therefore a low level direct register access must be available to configure the boards manually or to do a very sophisticated debugging in case all other attempts failed. For that, two functions have been implemented in the front end controller computer: readvme and writevme. The syntax is very simple and script-friendly.

readvme

Usage : readvme addr length
-c : continuous read operation
-e : full DMA error reporting
-n : non-legacy addressing
addr : starting address on VME
length : number of words to dump

writevme
Usage: writevme addr length [value1 value2 ...]
-e : full DMA error reporting
-n : non-legacy addressing
addr : starting address on VME
length : number of words to write
value1 : 4-character data values in hexadecimal

Using the programming language Python as well as some libraries to remotely access the VME front end computer it was possible to develop an all-in-one configuration script. Once it is run in a front-end command line the user is guided through the configuration process in an interactive mode (questions with list of possibilities are displayed, user picks from the list by writing a number). After all the input is collected, proper low level configuration commands are issued (writing into the VME registers, reading response values). This way the user does not have to care about the hexadecimal address of the registers, or how bits are masked in the commands to configure the multiplexers.

Second script that was prepared is a data acquisition script from Matlab. By running this script a Python interface is called to freeze the observation memory and reading all the data. Data are then loaded into Matlab variables and processed or displayed into any required form. Everything is done automatically.

5.4 Measurement card prototype

All the above blocks, selected components and design choices materialized in a Measurement card prototype board. As it is a rather complex card and the PCB design is very costly (approx. €12 000) the hardware development was done in synergy with the SPS Travelling Wave Cavity Loops module EDA-02490 [21] project. The TWC loops is a similar feedback module. It also features 4 RF inputs (at 800 MHz), one RF output (also 800 MHz), large FPGA for signal processing applications, gigabit communication links to other LLRF controller in the SPS Faraday cage. As the input/output signals are in the 800 MHz band a full analogue down/up converters to 25 MHz IF frequency have been implemented. The ADCs for the TWC project are intended to be running at 100 MSPS.

The board was designed in 2012 by Gregoire Hagmann from the BE/RF/FB section with input from Daniel Valuch. Several prototypes have been produced and one of them is used for the HIE-Isolde studies covered by this thesis. The EDA-02490 board is shown in Figure 34. The RF down converters have been bypassed and the ADCs are fed directly via a RF transformer. The RF output path required for the LLRF controller is being investigated these days. The FPGA code is not shared with the TWC project and it is developed specially for the HIE-Isolde project.

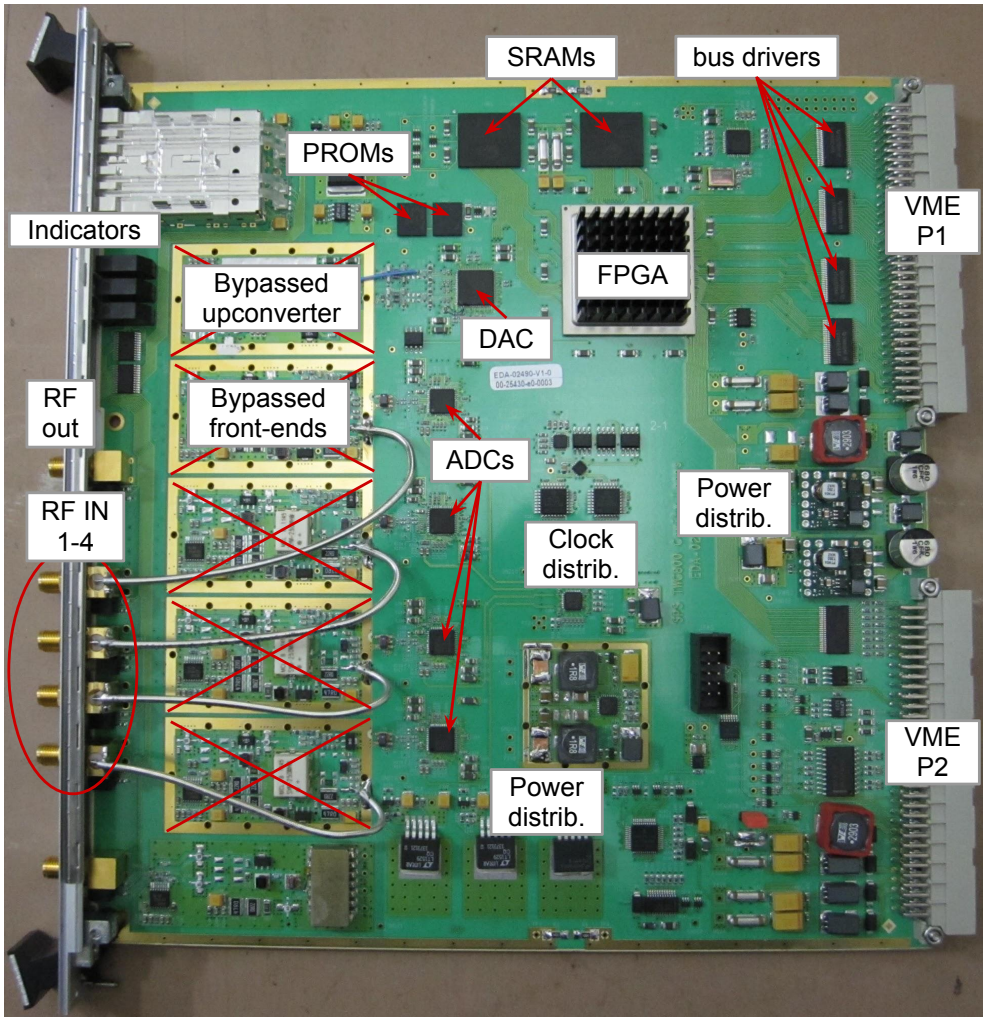

Figure 34: Modified SPS TWC800 Cavity Loops module

6 Clock Generator

Direct sampling of the RF signals significantly simplifies design of the feedback controller, however it comes at a price. In order to keep the sampling performance reasonable the sampling clock needs to have a very well controlled phase noise in order to minimize the sampling aperture jitter. The relation between the aperture jitter t_j and ADC SNR (or effective number of bits) when sampling a signal of frequency f_{RF} is defined by equation:

$$SNR = 20\log(\frac{1}{2\pi f_{RF} t_j}) \tag{4}$$

In case of HIE-Isolde, provided that the conversion noise comes only from the sampling clock jitter the t_j must be kept below 2.5 ps to achieve an ENOB of 9 bits. Then together with relatively high decimation factor we can aim at obtaining > 14 bit "noise free" data which will be sufficient performance for the measurement system and the later feedback controller. The equation (4) is shown in a graphical form in Figure 35. The red ellipse shows our desired operating region.

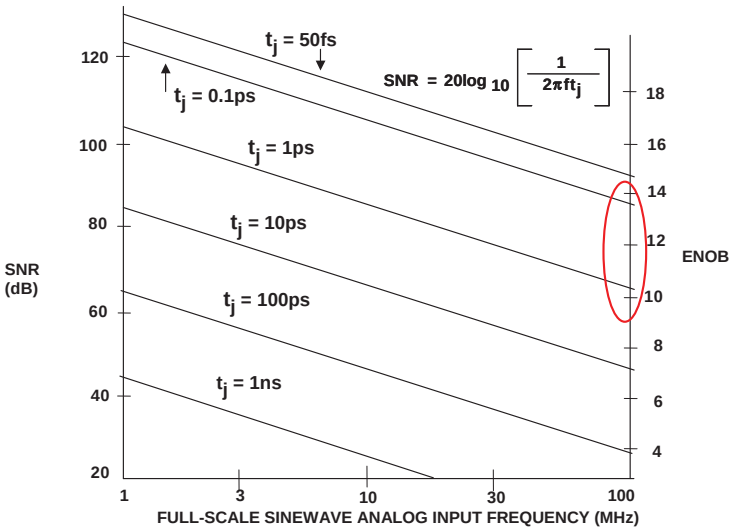

Figure 35: Effective number of bits as a function of the input signal frequency and the sampling clock jitter [6]

Modern ADCs require a 50 % duty cycle sampling clock so a practical issue arises with the clock generation circuitry. The denominator in the equation (1) is always an odd number what makes the output duty cycle control difficult. The whole fraction needs to be multiplied by two to allow insertion of a D flip-flop assuring the 50 % output clock duty cycle.

The proposed clock generator uses a direct frequency multiplication by means of a fast comparator instead of a PLL (phase locked loop). One input of the comparator is fed by the

reference clock (in this case the RF master clock with frequency of 101.28 MHz). The second input is connected to a voltage divider to introduce a threshold. The threshold is adjustable in order to find a proper duty cycle with enhanced content of the even harmonics. The eight harmonic is extracted from the comparator output signal of an 810 MHz bandpass filter ($f_{RF} \times 8 = 810.24$ MHz). This signal is relatively low amplitude to drive a digital logic, so it needs to be amplified by means of two stage monolithic amplifiers to reach a level of approximately 0 dBm. Finally it is converted into a differential form using an RF transformer. Now it is possible to use this multiplied signal to drive the clock input of the fast ECL divider realising the denominator division by a factor of 37. As already mentioned the odd ratio divider cannot provide the 50% duty factor required by the ADC so a final D flip flop with feedback is used to further divide this signal by a factor of two. Resulting clock signal has a frequency

$$f_s = \frac{8}{(2 \times 37)} f_0 = 10.9492 \text{ MHz} \tag{5}$$

locked to the input RF frequency of $f_0 = 101.28$ MHz.

A block diagram of the sampling clock generation scheme is shown in Figure 36.

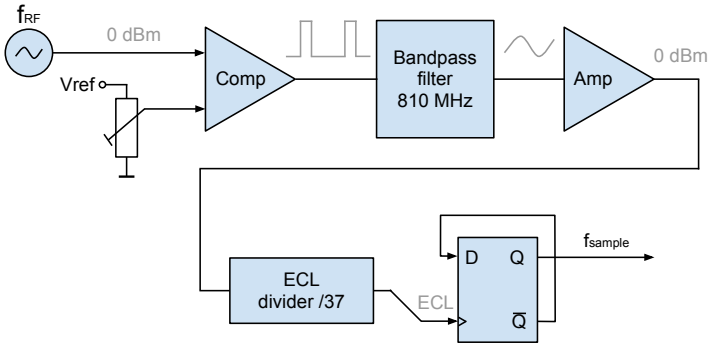

Figure 36: Clock generation scheme

6.1 Sampling clock generator prototype board

To test feasibility of this scheme and evaluate the clock quality a simple prototype circuit on a bread board was built (Figure 37). The RF input was AC coupled and fed into an ADCMP606 - fast, rail-to-rail CML comparator with 1.2 ns propagation delay. CML (current mode logic) output stage is differential, designed to drive 400mV directly into 50 Ω load. To interface it to the 810 MHz bandpass filter the differential output was transformed to single-ended using RF balun. Monolithic amplifier Mini-Circuits GVA-83, connected after the filter was used to amplify the filtered eight harmonic signal by 20 dB. This signal could then be fed directly into the divider - MC100E016 (ECL 8-Bit up synchronous binary counter). A D flip-flop MC100E031 divides the output frequency by two, providing the 50%

duty cycle. The results were encouraging. The frequency multiplication by a factor of 8 was performing as expected, but the division was working only at a lower than desired frequency (700 MHz maximum).

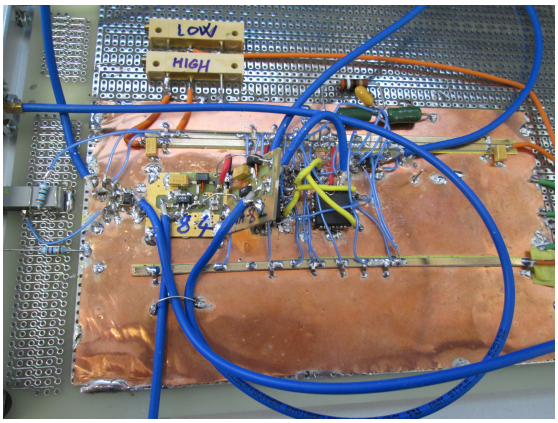

Figure 37: Prototype of the clock generator

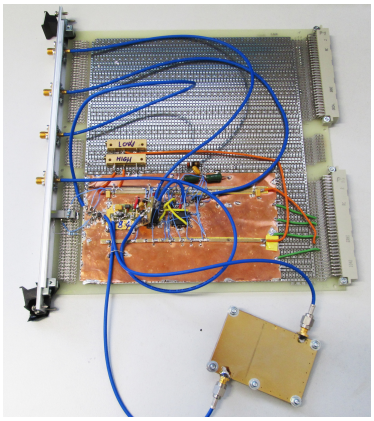

Figure 38: With bandpass filter connected

6.2 PCB version

After evaluation of the circuit prototype a proper 6-layer PCB was designed. A faster version of the MC100E016 divider as well as better bandpass filter (described in the following section) was implemented. High frequency design techniques and proper grounding significantly improved the divider performance. Assembled board is a standard form factor pluggable into the VME crate. RF signal input and clock output SMA connectors are mounted on the front panel. This board can be seen in Figure 39.

Only minor issues were discovered during testing of the PCB version of the clock generator (missing termination, need for a higher gain etc.). However one serious issue was found. A glitch in the synchronization pulses between the two divider stages making the circuit generate an incorrect frequency. This bug have had a very good pedagogical value. The glitch was so short that it could not be seen by a standard 500 MHz 1:10 oscilloscope probe. The new generation of the ECL gates used on the board is very fast and the glitch caused a mis-firing of the D flip flop. The problem was discovered only when using an active high frequency oscilloscope probe (the glitch pulse was less than 2 ns long). Detail of the glitch could be seen in the Figure 40. Yellow and blue traces are inputs to the ECL OR logic gate, green is output of the OR gate. Red trace is a logic error in the following circuitry due to the glitch. Solution of the problem was to de-interlace the two inputs by increasing the delay in one of the OR gate inputs (by inserting a longer wire).

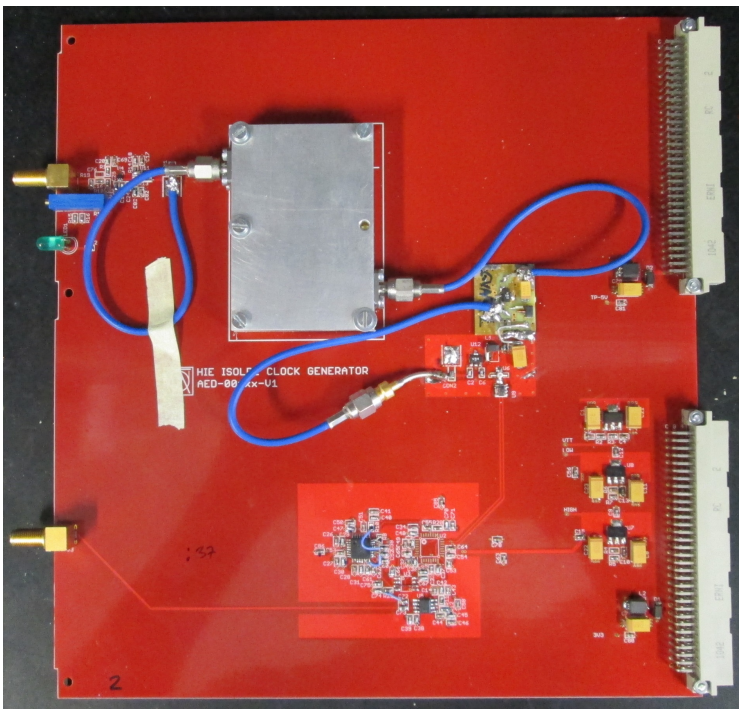

Figure 39: PCB version of the Clock generator

6.3 810 MHz band pass filter design

To select the eight harmonic from the comparator output a simple 810 MHz band pass filter was built for the first lab tests. Off the shelf low pass filter from Mini-Circuits followed by a home brew high pass using two SMA connectors soldered together, with SMD capacitors and pieces of copper foil to form the inductance (Figure 42). The filter was measured by Network Analyser E5071C (Figure 43). A proper band pass filter was later designed using the AWR Microwave office (see Figure 44).

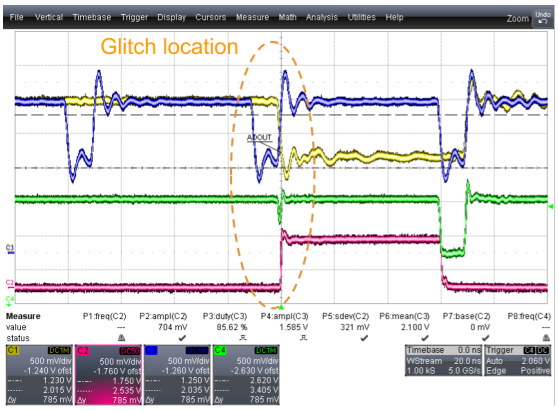

Figure 40: Glitch in the ECL circuit

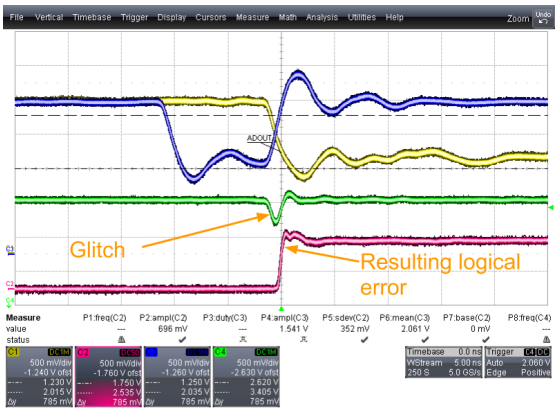

Figure 41: Glitch detail

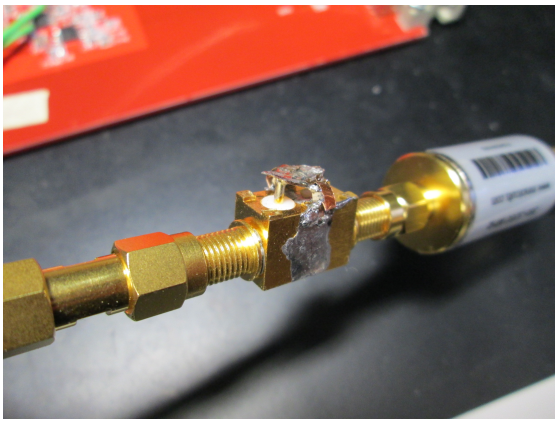

Figure 42: Filter prototype

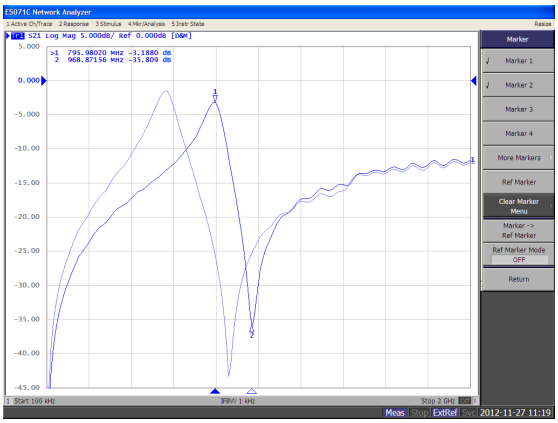

Figure 43: Tuning the resonant frequency

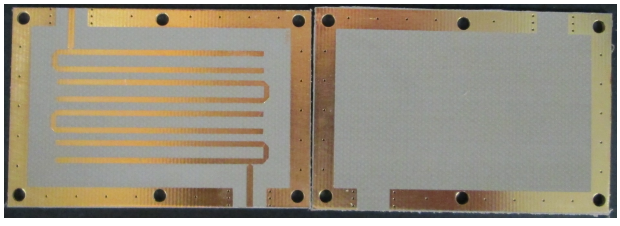

Figure 44: Stripline hairpin band pass filter

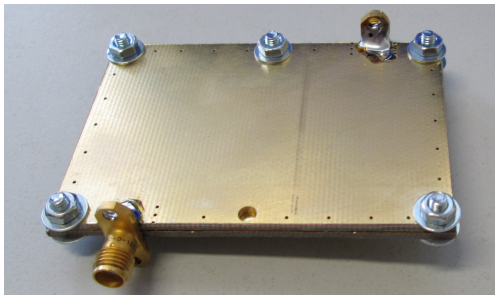

Figure 45: Assembled filter

7 RF amplifier

In order to obtain sufficient power levels at the Cavity forward, reflected and antenna returns, the cavity at the warm cavity test setup needs to be driven by few tens of Watts of RF power. A 30 W power stage for broadcasting applications was bought and modified for our needs. The amplifier stage was built into a 3U Europa chassis with its power supply, circulator and termination, RF switch and indicators of forward and reflected power.

In order to provide the complete and reliable RF amplifier as fast as possible, mostly off-the-shelf, proven components were used. Diagram of the proposed amplifier is shown in Figure 46. Mains input module Schaffner FN1393-10-05-11 contains filter, mains switch and a glass fuse. The amplifier is powered by a switched mode supply MeanWell S-100F-24, with an output rated on 28 V 4.5 A.

The RF input is routed via a fast RF switch SPST CDS0671 currently controlled by a mechanical switch on the front panel. For the full setup this switch will be piloted by the interlock system providing the RF veto function. First amplifier stage is equipped by a Mini-Circuits ZFL-1000VH, low noise, 20dB gain amplifier. The second (power) stage is a 100 MHz 30 W RF amplifier module, manufactured by Elektronika SRL. This module already provides temperature interlocks and forward and reflected power measurement. Output of the power stage is protected against the reflected power from the cavity by a RF circulator TECHNIWAVE type H100.5M03S01L. The return port of the circulator is terminated by a 300 W a 50 Ω dummy load from Diconex, mounted on a common heatsink. Specific voltages required by different components are taken from the second stage amplifier's internal circuits - 5 V and 15 V. The prototype amplifier can be seen in Figure 47

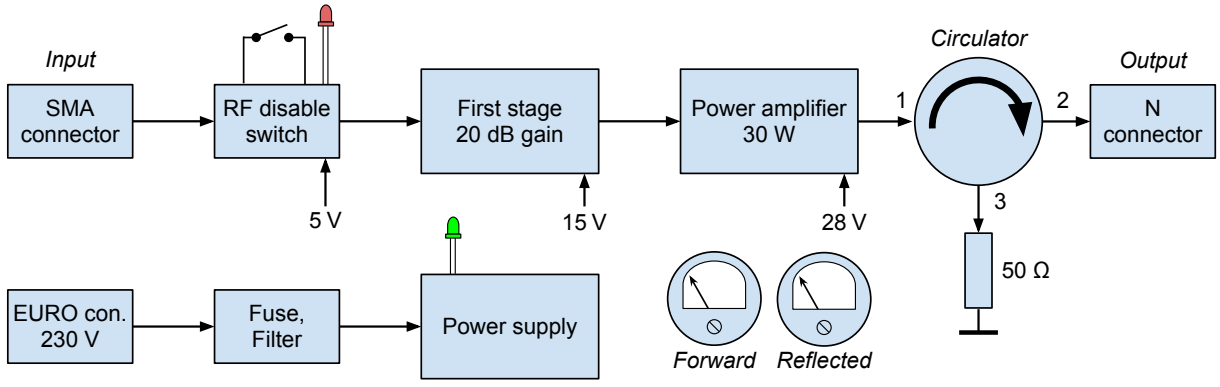

Figure 46: Block diagram of the 30 W RF amplifier

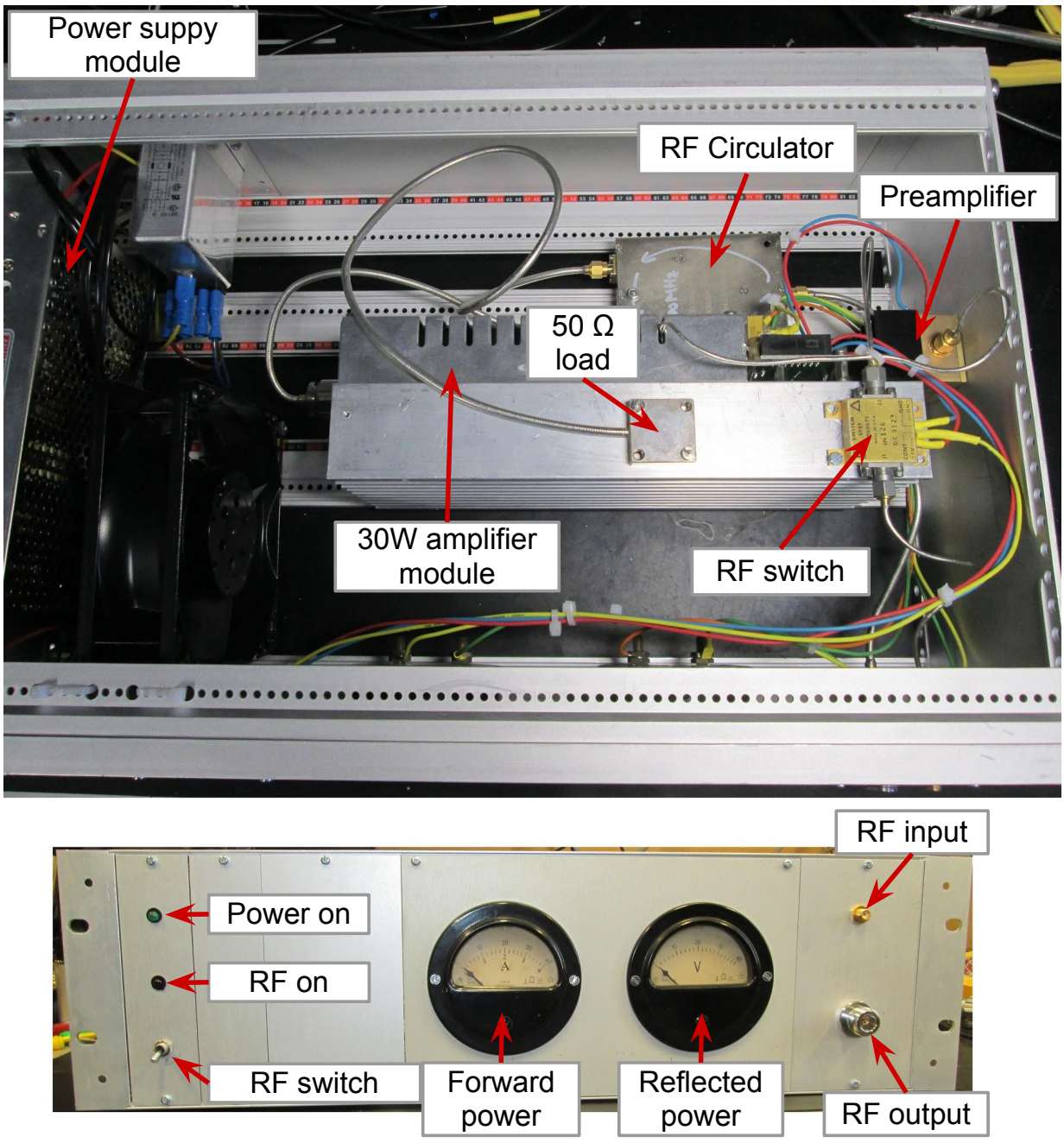

Figure 47: 30 W RF amplifier prototype. The analogue gauges are used for forward and reflected power indication. Full scale 30 W

8 Cavity tuning system

The cavity resonant frequency is a function of the cavity physical size and geometry. The geometry is fixed by design, however the manufacturing tolerances are finite and the thermal contraction when cooling to 4.5 K is not always perfectly reproducible. For the accelerator operation the cavity must be on resonance at a frequency which is the linac operating frequency. Without some form of an active compensation this would not be possible to achieve only by the cavity mechanical design.

The tuning system deforms slightly the cavity geometry in order to tune the resonant frequency to the desired value. The tuning could be done e.g. by squeezing or stretching the cavity, changing the cavity temperature, inserting tuning pistons and many more. In case of a quarter wave resonator the most convenient method is to deform the cavity bottom plate (underneath the open end of the inner conductor). The tuning range must be sufficient to cover the mechanical imperfections, what is in case of the HIE-Isolde first prototypes about 100 kHz. Thanks to an excellent repeatibility of the production process, the following cavity prototypes needed only a reduced tuning range of about 10 kHz. Note, that this range is still about 1 000 times the final cavity operating bandwidth. The tuning sensitivity calculated for the prototype cavities was in order of 50 nm/Hz, or in other words, a displacement of only 500 nm would detune the cavity by one bandwidth. A tuner this sensitive presents a risk of perturbing the cavity operation by bringing in a mechanical noise from the cryostat and making the operation very difficult. Therefore a tuning plate with reduced sensitivity is being developed.

To be able to experiment with a warm cavity in the lab, a simple preliminary tuning system was put in place. A non-corrugated copper sheet is installed instead of the final tuning plate. It is driven by a stepper motor with a tuning screw, to convert a rotational motion to a linear motion. The concept can be seen in Figure 48. The motor is driven by the slow control system based on a PLC with stepper motor drivers. The slow controls for the HIE-Isolde linac is responsibility of the BE/RF/CS section, namely Luca Arnaudon, David Landre and David Glenat. The control user interface is written in the LabVIEW software and allows setting of direction, motor speed, number of steps and automatic stepping sequences. The system will be later automated, collecting input about the cavity tune state from the LLRF controller and commands to keep the cavity on tune by a feedback loop.

At first, IP address for the PLC controller, port and other default values are set. Then TCP/IP connection is initialized using block "TCP open connection". Program then enters main loop, which is executed every n ms. In this loop, all parameters (direction, command, Steps to go, MotorSpeed, etc.) are read, composed into array of integers. It is then send using "TCP Write" followed by "TCP Read" to verify the status. Results from this block are processed in the second thread. Several indication values are determined from this response - including "Run state", "Direction" or "Limit switch reached". Data transfers and state is determined from "Data" and "Error" lights in the user interface.

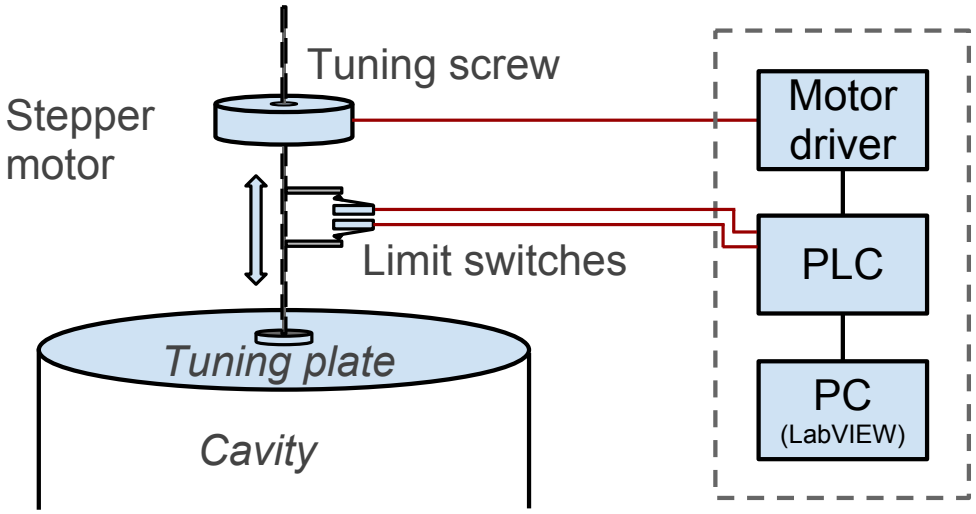

Figure 48: Cavity tuning system

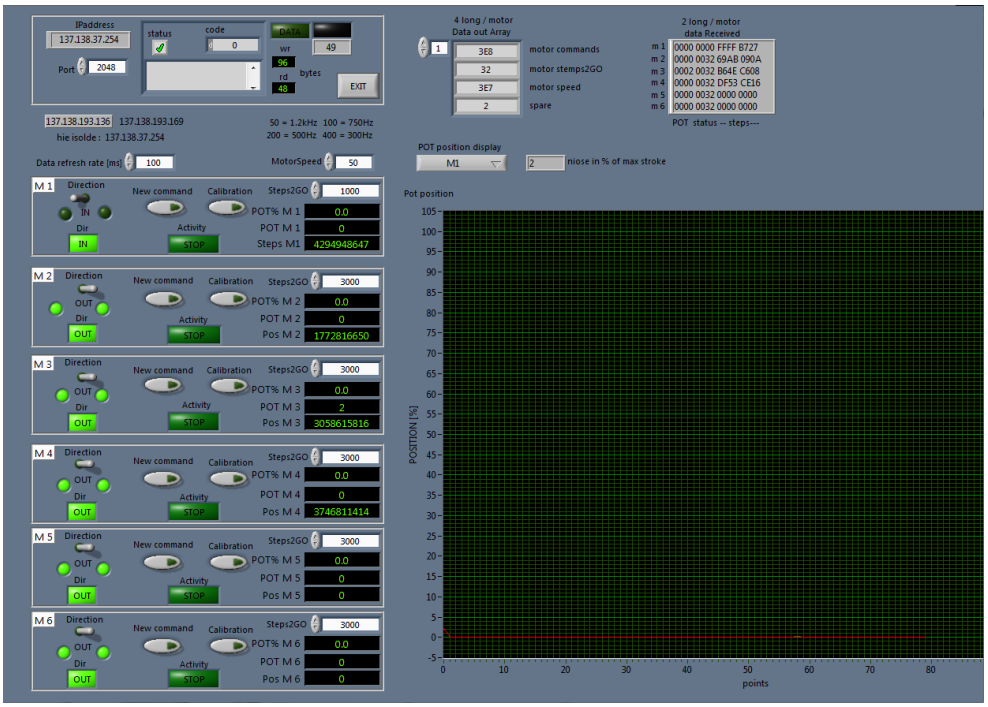

Figure 49: Tuning control user interface

9 Project status and the next steps

At the time of writing this thesis the measurement card project was very advanced. Feasibility of the sampling clock generation principle has been tested and phase noise performance measured. The selected ADCs have been evaluated in terms of compatibility with the RF signal and interfacing to the FPGA. Overall sampling performance of the ADCs together with the sampling clock generator qualified the direct RF sampling method as usable for the project. The FPGA to DAC interface is validated up to 200 MHz sampling frequency. The digital quadrature demodulation technique together with decimation has also been qualified to be used for the measurement card project.

A preliminary version of the firmware is already running in the FPGA allowing to do basic measurements on the four RF channels. The measurement card is fully integrated in the CERN control infrastructure and the drivers and the FESA class are being prepared.

The next step is to find and test a proper method to generate the RF signal directly from the FPGA+DAC. Once the RF generation is operational the firmware will evolve to implement the self excited loop algorithm to assist the cold cavity tests in the SM18 facility. All hardware modifications of the EDA-02490 board collected during the measurement card development process will be properly integrated to the PCB layout and ten pre-series LLRF boards should be manufactured before the fall 2013.

10 Measured results

Some essential results obtained during the development of the HIE-Isolde cavity measurement system are presented in this chapter.

10.1 Sampling clock generator

Feasibility and performance of the sampling clock generator is vital for qualification of the direct RF sampling technique. As presented in the chapter 6 (Clock Generator) it is essential to keep the sampling clock jitter below 2 - 2.5 ps in order to obtain $>$ 9 bits ENOB. As we are directly sampling the RF signal without any analogue down conversion and IF amplifiers, almost whole noise budget could be used for the sampling clock jitter. Figure 50 shows the measured sampling clock phase noise spectrum and the integrated jitter in the band 10 Hz to 5 MHz which is 1.93 ps, well within the specification. The sampling performance has been also independently verified by acquisition of sinusoidal signals and looking at the ADC noise floor and spurious free dynamic range, see Figure 51.

10.2 Direct RF sampling and digital quadrature demodulation

Figures 52 and 53 show histograms of all four sampled data channels (reference, cavity forward, cavity reflected, antenna signals) with real input signals from the warm cavity test setup. The signal levels are intentionally not at the ADC full scale to simulate performance of a real system.

Demodulated signals for all four channels normalized to the reference channel are shown in the Figure 54 for magnitude and in Figure 55 for phase. The residual noise on the magnitude measurement is about 2×10^{-4} peak to peak. The residual noise on the phase measurement is about 0.002° peak to peak.

The system was therefore qualified for the future feedback loop implementation where the residual regulation errors in the cavity voltage must be below 0.2% magnitude and 0.2° phase.

10.3 Cavity tuning transient

Storing the data into a relatively long observation memory allows us to capture the system response to various excitations. For example tuning the cavity using a stepper motor is relatively "noisy" operation. Even in a microstepping mode the motor performs discrete steps. When applied to an elastic tuning plate it causes vibrations in the mechanical structure of the cavity. For the feedback loop design it is essential to know the level of perturbation caused by the tuning process as well as mechanical resonant frequencies of the cavity itself. If external noise (e.g. helium pressure variations, cryocompressor vibrations, mechanical noises transferred through the cryostat) hits the mechanical resonance of the cavity, the disturbing effect could get amplified and the feedback loop may not be able to compensate for it.

Figure 56 shows the cavity resonant frequency (calculated by the Measurement card) during tuning. The cavity was about 15% bandwidth off resonance and the motor was commanded to perform few steps to tune it into the resonance. The motor steps could be clearly visible. The excited mechanical oscillations last for more than a second. FFT of the tuning transient presented in Figure 57 shows the dominant mechanical modes of the cavity and its tuner mechanism located at 54 Hz, 76.5 Hz, 86.6 Hz, 100.2 Hz, 175.7 Hz, 152.6 Hz, 181.6 Hz.

10.4 Other interesting results

A frequency response of the warm cavity was measured using the Measurement card prototype. The RF reference signal feeding the cavity was frequency modulated to cover several cavity bandwidths, while the sampling frequency was kept constant. The cavity response could be seen in Figure 58.

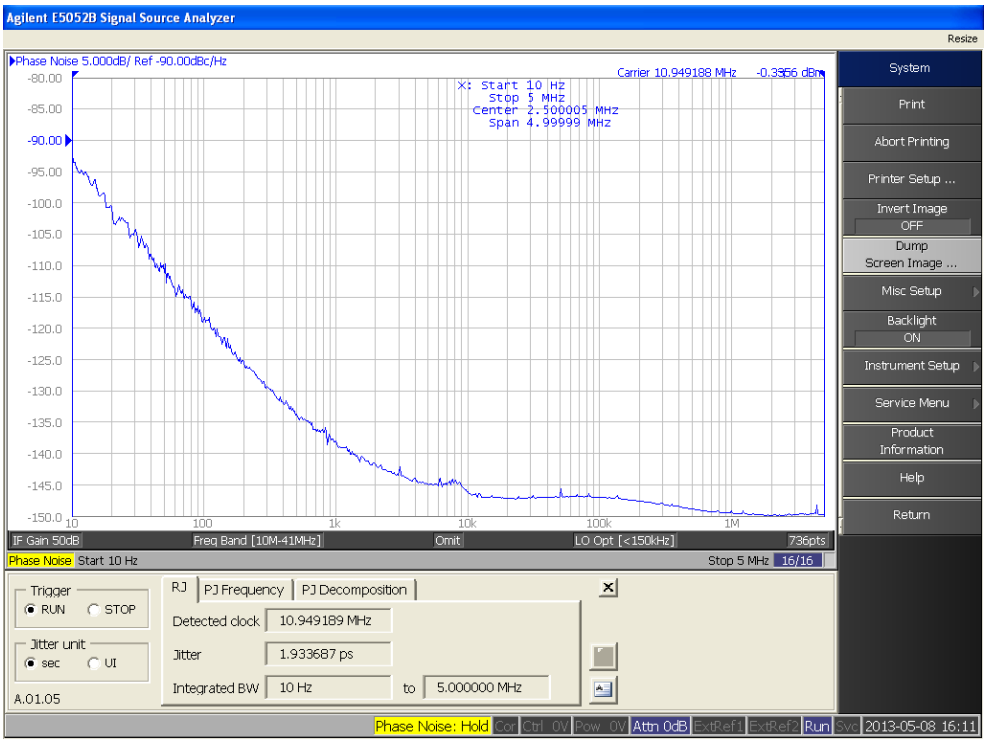

Figure 50: Sampling clock generator jitter measurement

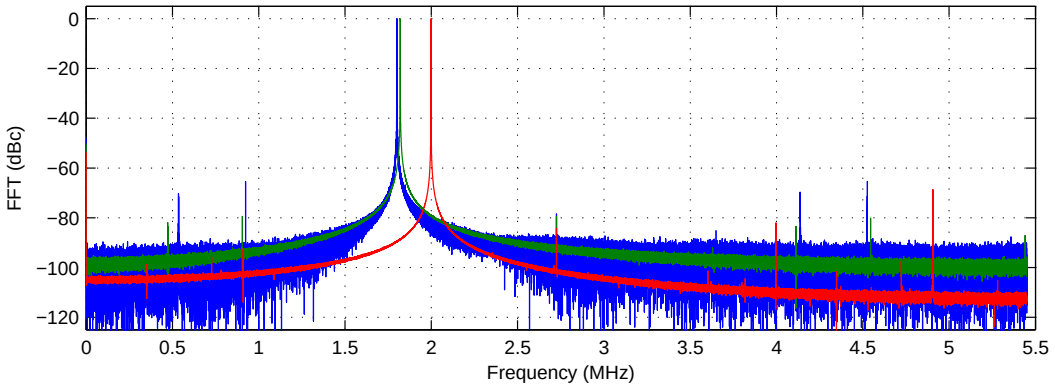

Figure 51: ADC noise floor for different values of the input signal frequency. Red trace $f_{RF} = 2$ MHz, green trace $f_{RF} = 20$ MHz, blue trace $f_{RF} = 100$ MHz. $f_{sample} = 10.949$ MHz

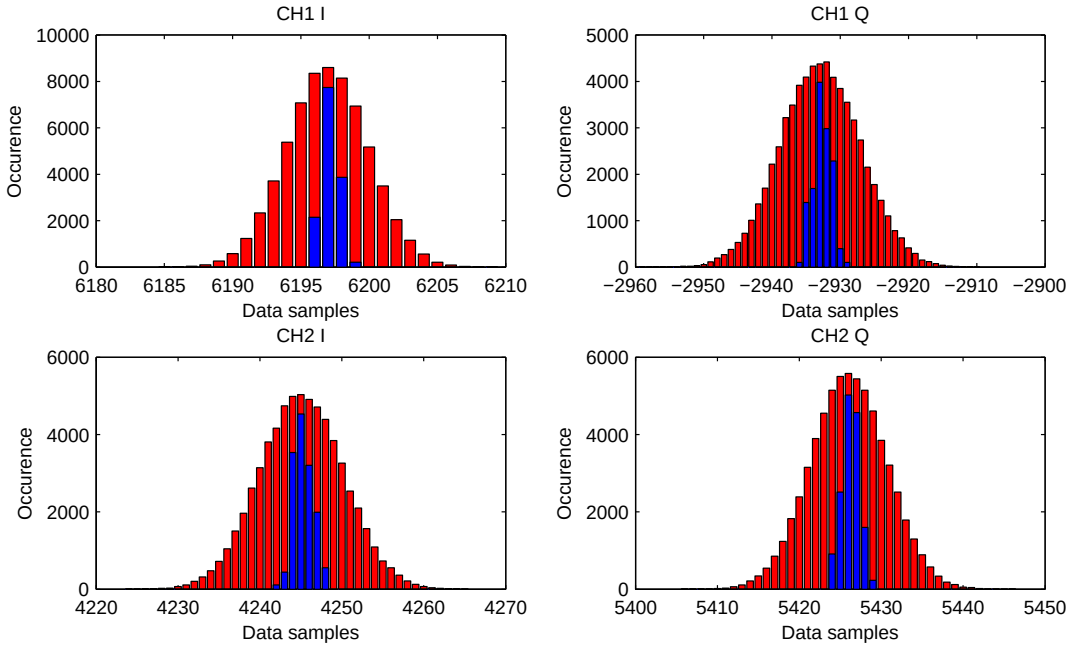

Figure 52: Sampled data, channel Reference (CH1) and Cavity Forward (CH2). Red bars are the raw undecimated data, blue bars after decimation by factor 8 192.

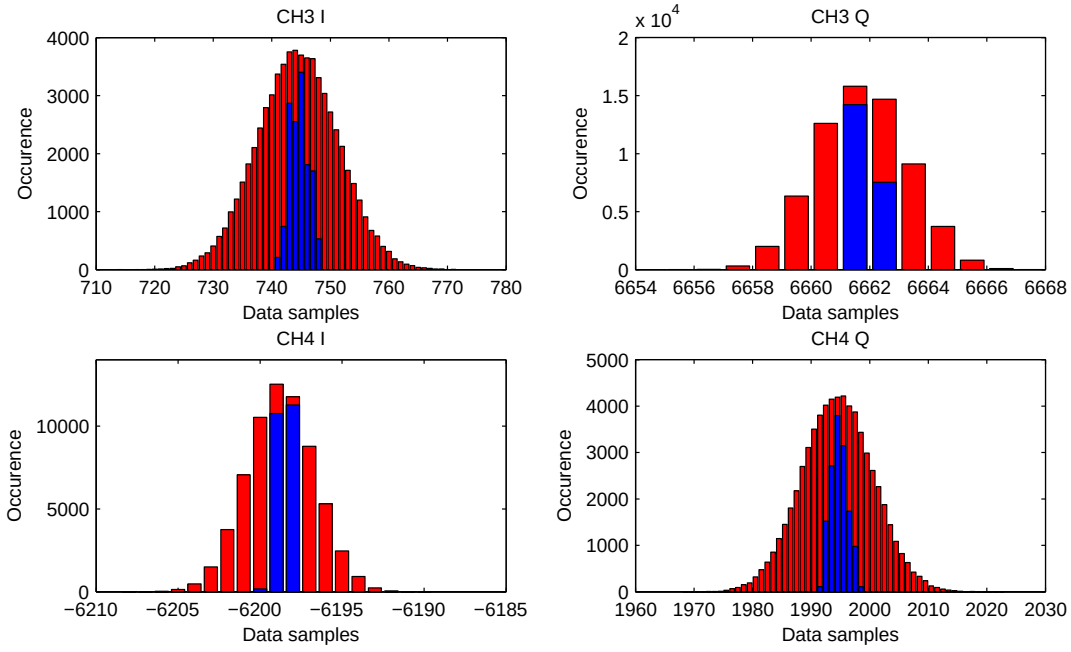

Figure 53: Sampled data, channel Cavity Reflected (CH3) and Antenna (CH4). Red bars are the raw undecimated data, blue bars after decimation by factor 8 192

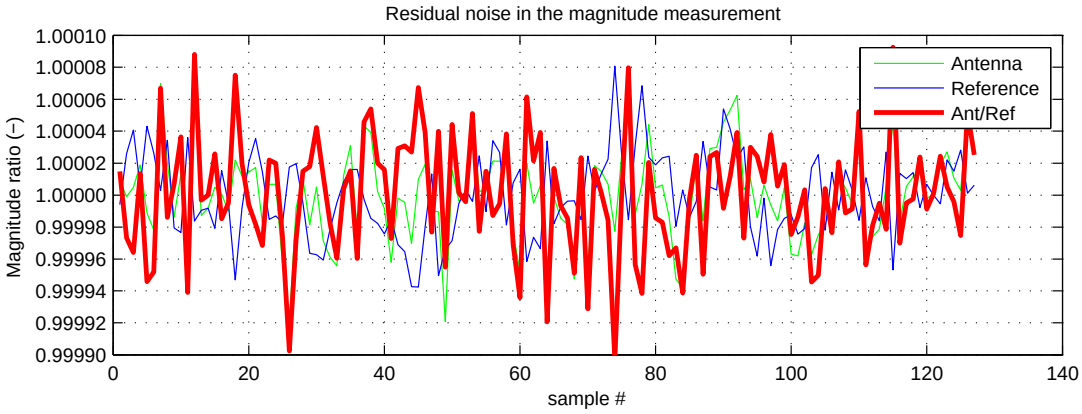

Figure 54: Residual noise on the magnitude measurement. f_{sample} = 10.949 MHz, decimation by 8 192.

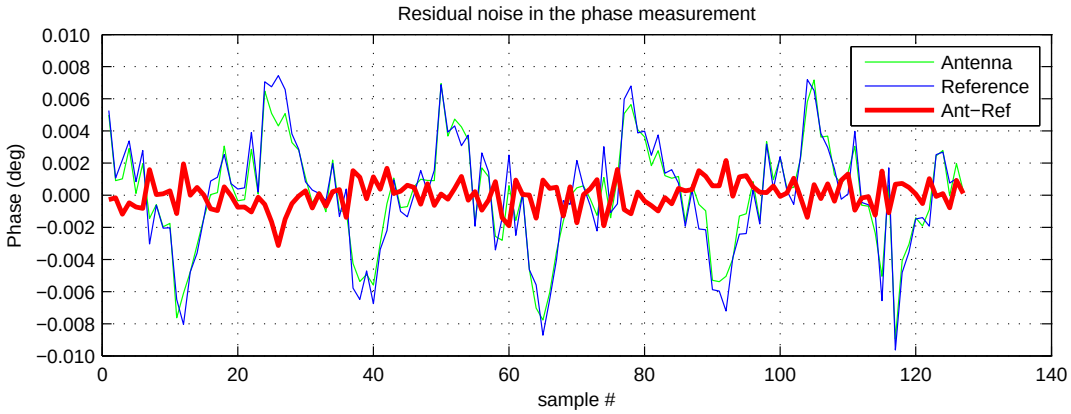

Figure 55: Residual noise on the magnitude measurement. f_{sample} = 10.949 MHz, decimation by 8 192.

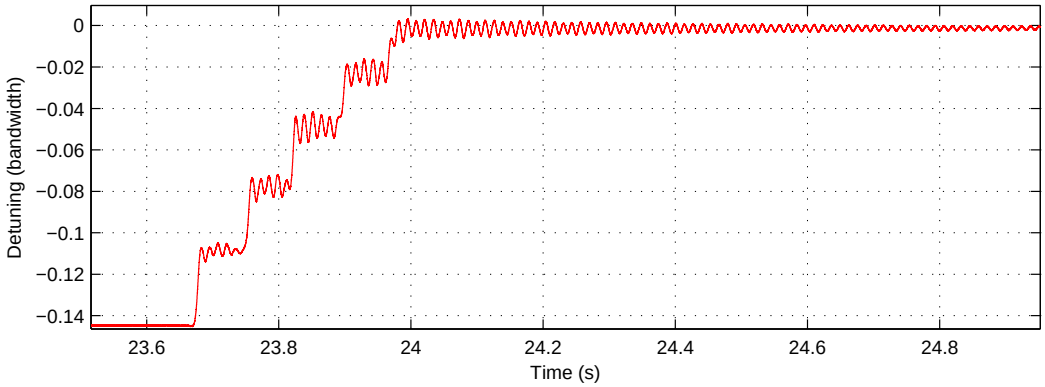

Figure 56: Cavity resonant frequency during the tuning transient as captured by the Measurement system

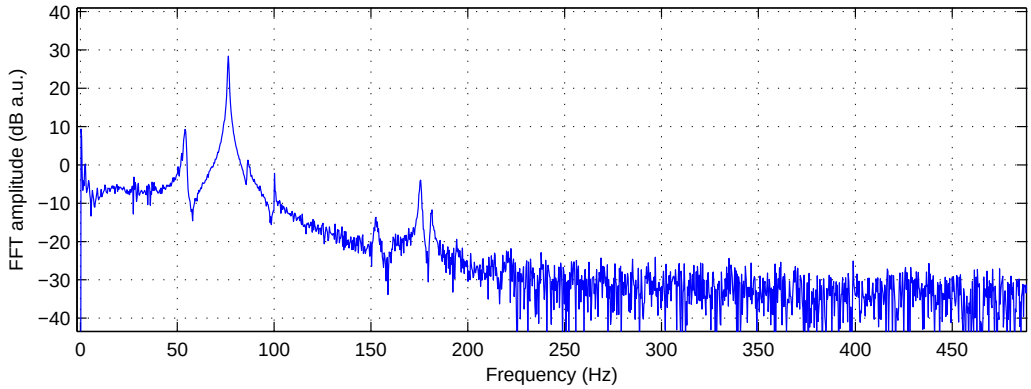

Figure 57: FFT of the tuning transient showing the mechanical modes of the cavity

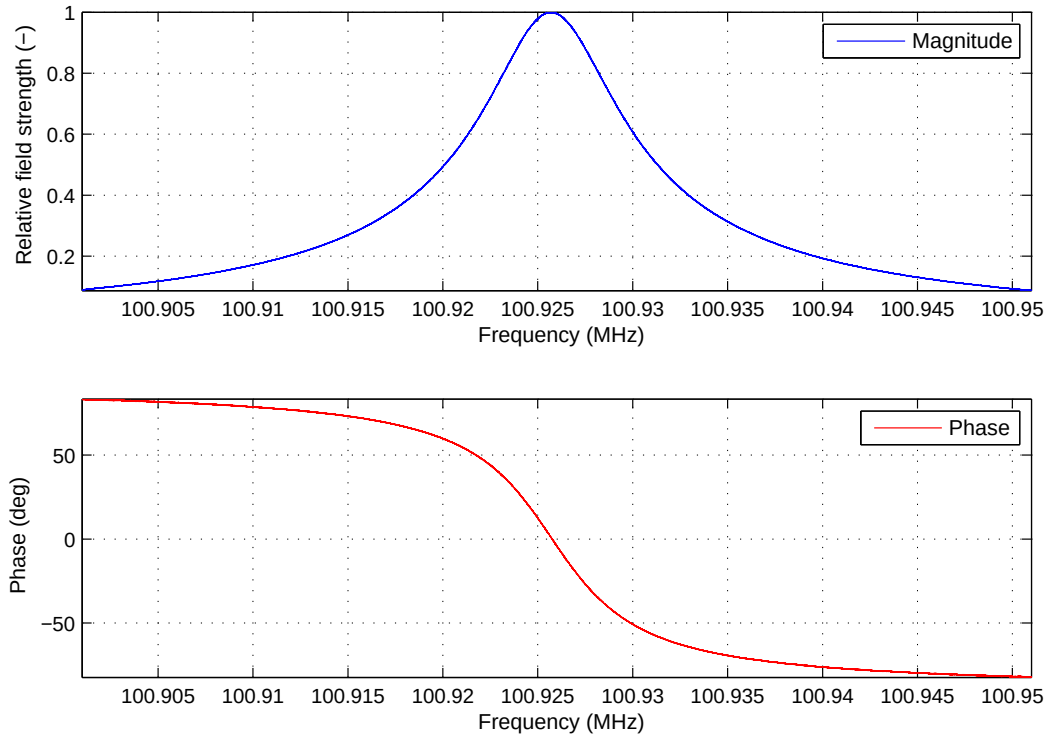

Figure 58: Frequency response of the warm HIE-Isolde cavity, measured by the developed Cavity measurement system

11 Conclusion

Purpose of this work was to design and develop a Digital Measurement System for the HIE-Isolde Superconducting Accelerating Cavities. In order to understand the problem a study of accelerator RF systems and corresponding feedback systems was done. Some examples are presented in this thesis. Two main modes of the LLRF system operation were described (self excited loop and generator driven mode). Operation of a very high Q cavities require combination of the both feedback techniques to be implemented. The self excited loop for fast start up of the cavity with switching over to the generator driven mode for the accelerator operation and conditioning. To allow testing of the LLRF system during the initial development a warm cavity test setup with standardized interfaces and tools used at CERN was proposed and built. VME modular system, master RF oscillator, PLCs for the cavity tuning system, newly developed HIE-Isolde cavity and proposed measurement system etc.

Based on the user requirement a structure of the measurement card was proposed, selection of the ADCs, sampling scheme, memory and DAC were discussed. For the prototype version, already developed SPS Travelling Wave Cavity Loops module was used. Various aspects of the firmware development written in the VHDL language (demodulator and decimator, memory controller, module configuration) are presented.

To achieve a direct digital quadrature demodulation of the RF signals, a clock generator module was developed. At first on the breadboard to test the concept feasibility, followed by a final prototype using 6-layer PCB afterwards.

In order to obtain sufficient power levels at the Cavity forward, reflected and antenna signal the cavity at the warm cavity test setup needed to be driven by few tens Watts of RF power. Therefore a 30 W RF amplifier stage was bought and modified to form a mockup RF amplifier simulating the final solid state RF amplifiers used in the machine.

To be able to experiment with a warm cavity in the lab and move the tuning plate, simple preliminary tuning system was put in place - using a stepper motor with a tuning screw, to convert rotational motion to linear motion.

Some essential results obtained during the development of the HIE-Isolde cavity measurement system were presented in the thesis, including ADC noise floor, cavity tuning transient and performance of the sampling clock generator, having only around 1.93 ps of jitter, allowing us to obtain > 9 bits ENOB before decimation.

The main goal, to design a superconducting cavity measurement system was fully achieved. The performance of the system was demonstrated on a warm cavity test stand, but the system will be moved to the superconducting test facility SM18 in a near future. As the next step a RF signal generation options must be further explored and implemented, new version of the measurement card developed and the final LLRF controller implemented. Still a lot of work needs to be done before the HIE-Isolde accelerator will be installed and commissioned (foreseen for 2014).

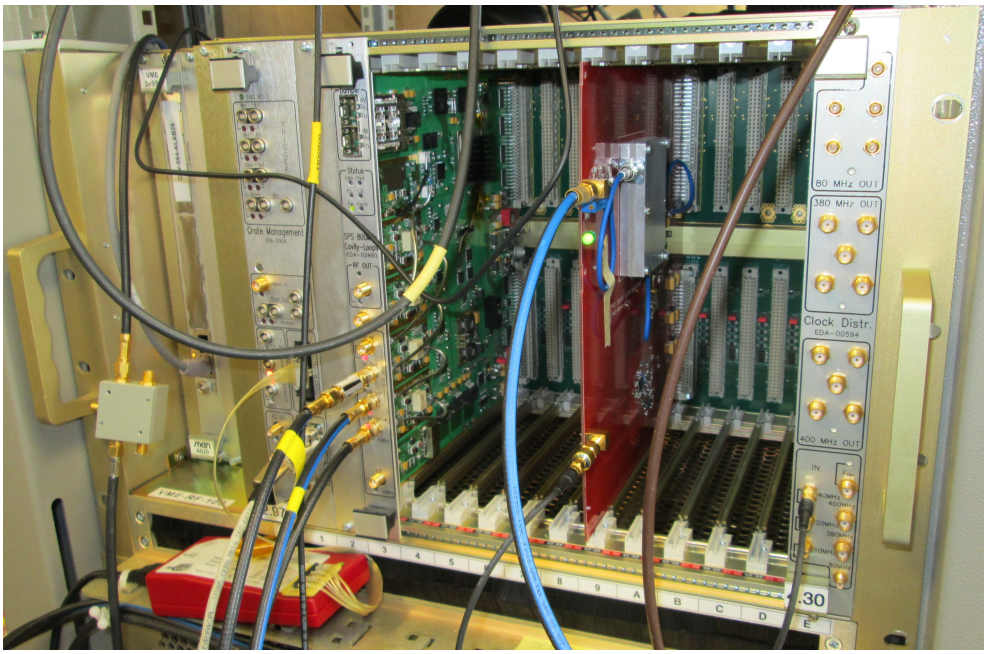

Figure 59: VME crate with all modules discussed and developed for this thesis

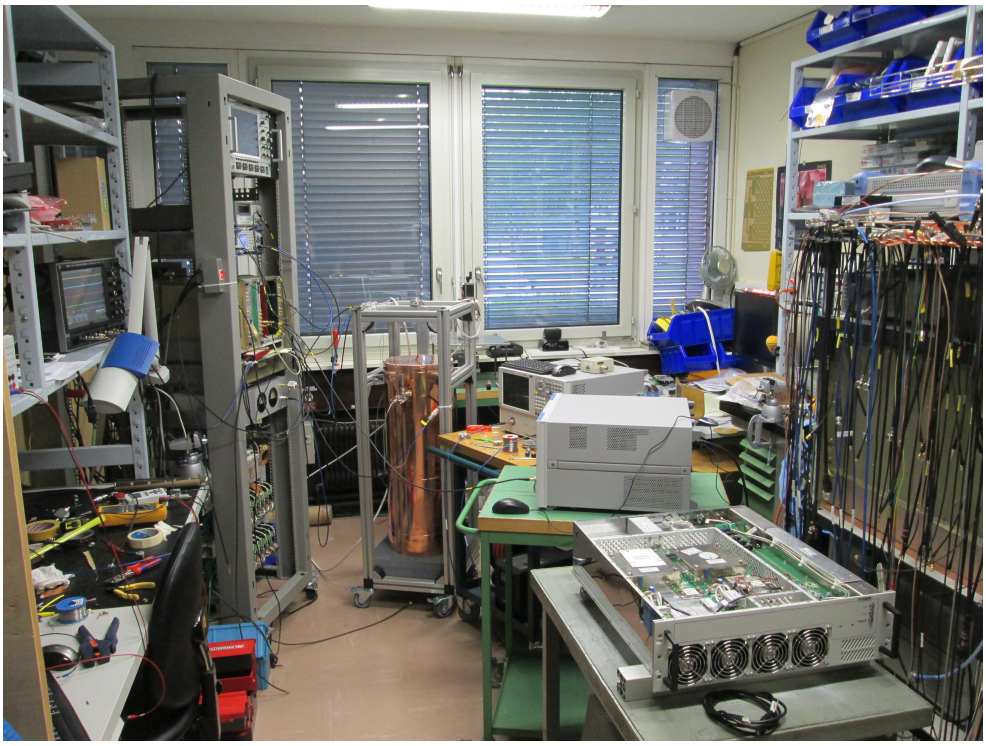

Figure 60: Warm cavity test stand the night before submitting this thesis

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Appendix

CD Content

In table 1 are listed names of all root directories on CD

Directory name	Description
mt.pdf	master thesis in pdf format.
sources	source codes
electronics	schematics, boards
photos	photos, drawings

Table 1: CD Content