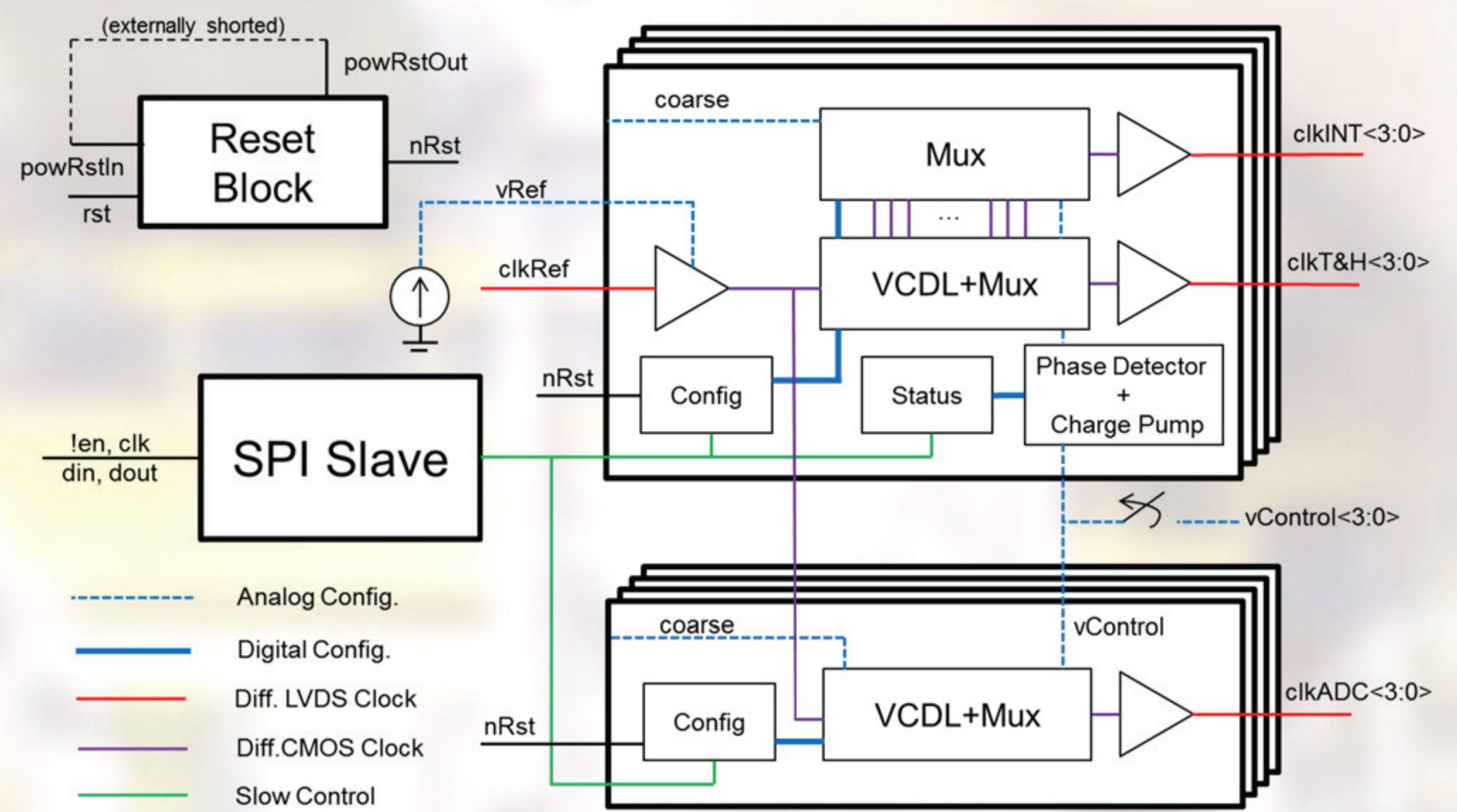
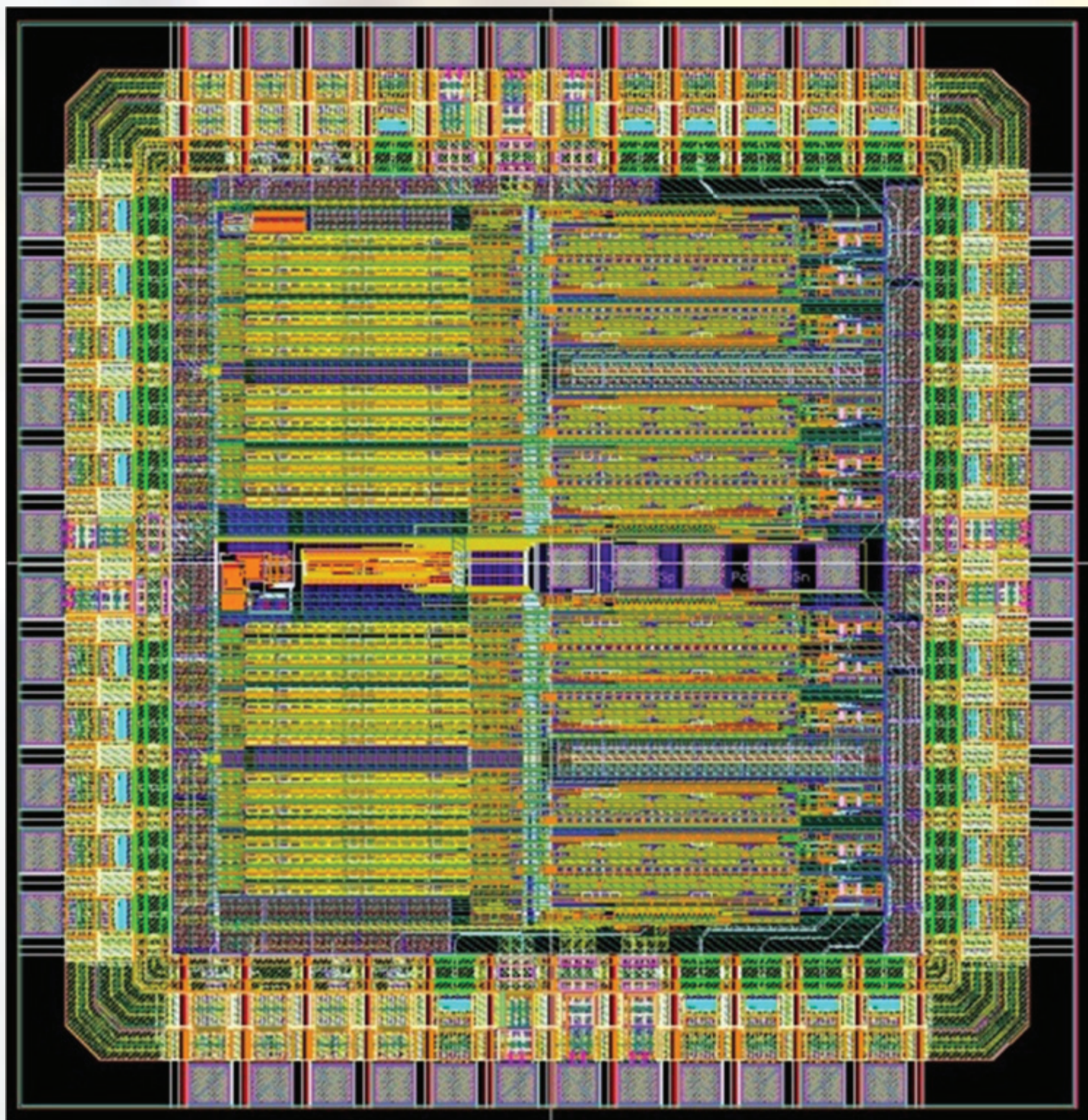


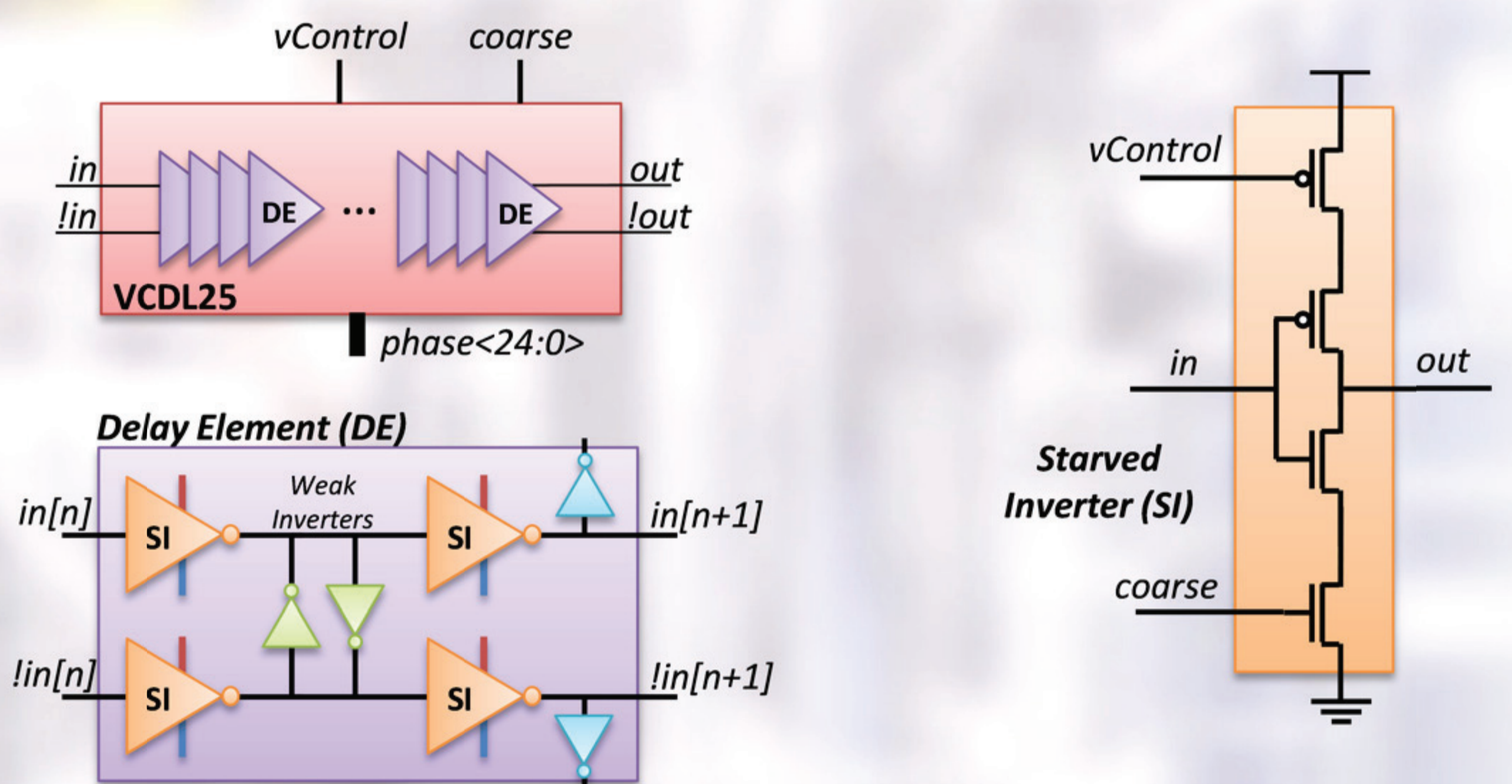
Radiation hard programmable delay line for LHCb Calorimeter Upgrade

J. Mauricio, D.Gascón, X. Vilasís, E. Picatoste, F. Machefer, J. Lefrancois, O. Duarte

Abstract - This poster describes the implementation of a SPI-programmable clock delay chip based on a Delay Locked Loop (DLL) in order to shift the phase of the LHC clock (25 ns) in steps of 1ns, with a 4ps jitter and 18ps of DNL. The delay lines will be integrated into ICECAL, the LHCb calorimeter front-end ASIC in the near future. The stringent noise requirements on the ASIC imply minimizing the noise contribution of digital components. This is accomplished by implementing the DLL in differential mode. To achieve the required radiation tolerance several techniques are applied: double guard rings between PMOS and NMOS transistors as well as glitch suppressors and TMR Registers. This 5.7 mm² chip has been implemented in CMOS 0.35um technology.



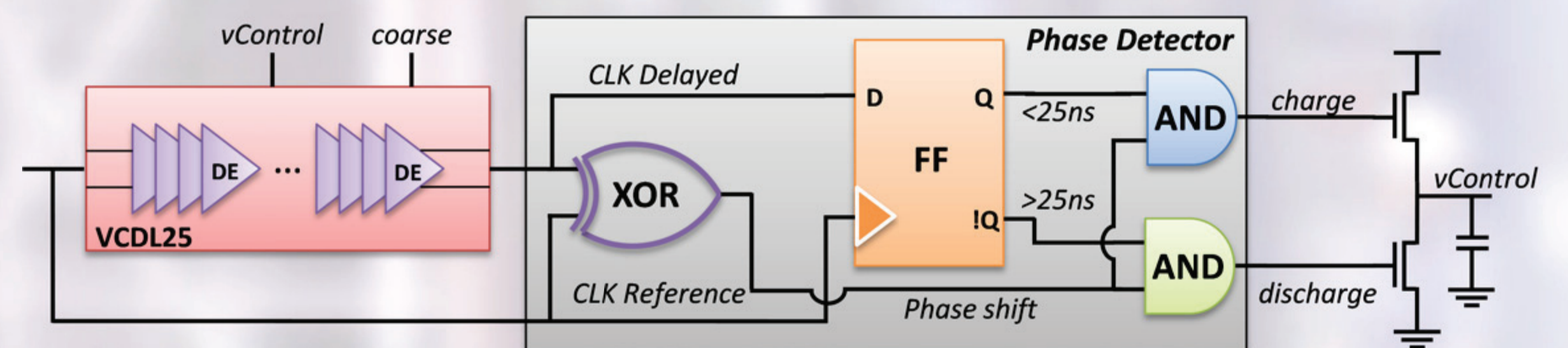
Voltage Controlled Delay Line (VCDL) design:



Features:

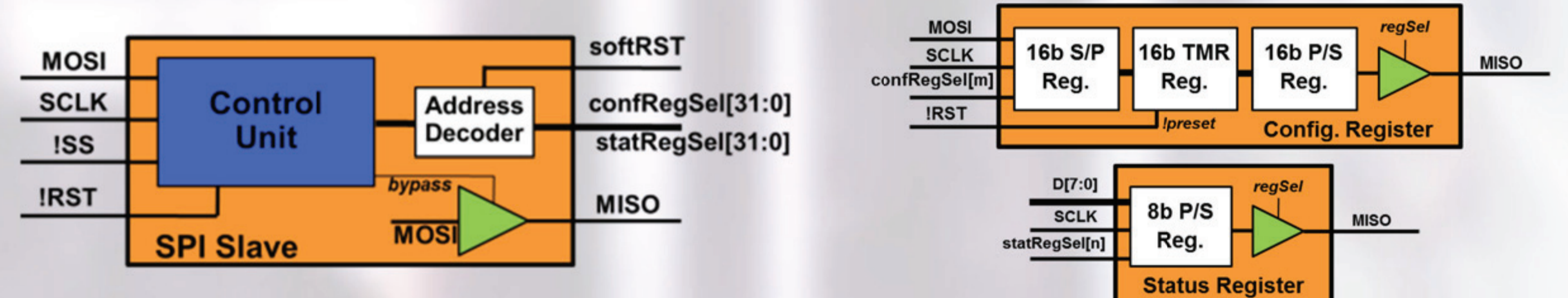
- Main features:**
 - 4 triple-channel DLL-based delay lines:
 - 12 LVDS output clocks.
 - Full custom design.
- Configurability:**
 - 25 configurable clock phases (1-ns steps).
 - Slow control via SPI.
- Noise:**
 - Peak-to-peak jitter: 3 ps.
 - DLL control voltage fluctuation ~ 1mV.
- Process, Voltage & Temperature variations:**
 - External voltage compensates DLL process variations.
 - Internal voltages compensate dynamic variations.
 - Operating range of 17.45 to 39.88ns.
 - Mismatch: Differential Non-Linearity (DNL): 18 ps.
 - Starved inverter.
- Radiation hardness:**
 - Single Event Upset tolerance: triple voting flip-flops.
 - Single Event Transient tolerance: glitch suppressors.
 - Single Event Latch-up avoidance: guard rings.

Phase detection:

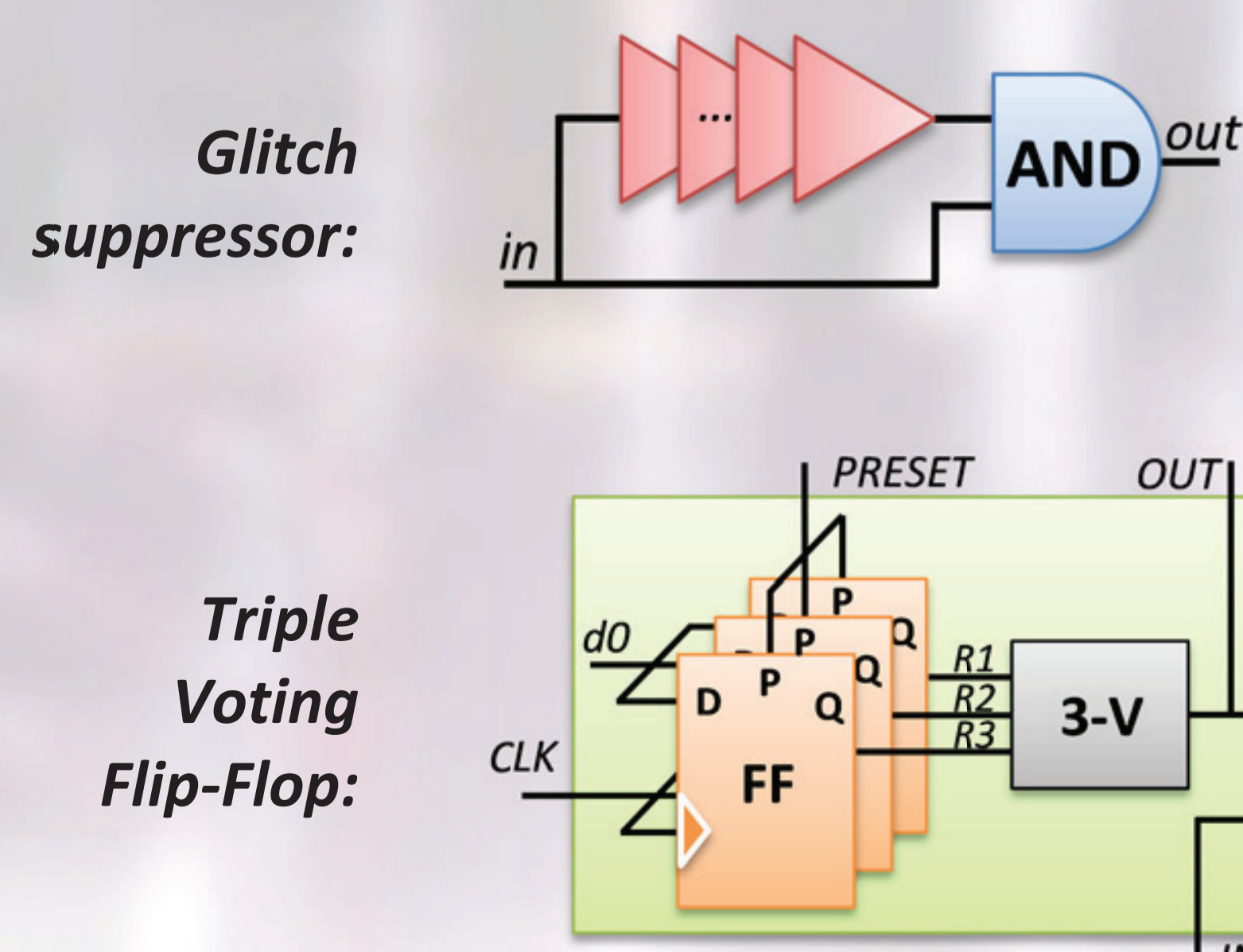


Phase detection is done in two steps: sign is detected by means of a flip-flop, while an XOR-2 detects the modulus. Combining them charge pump is charged or discharged.

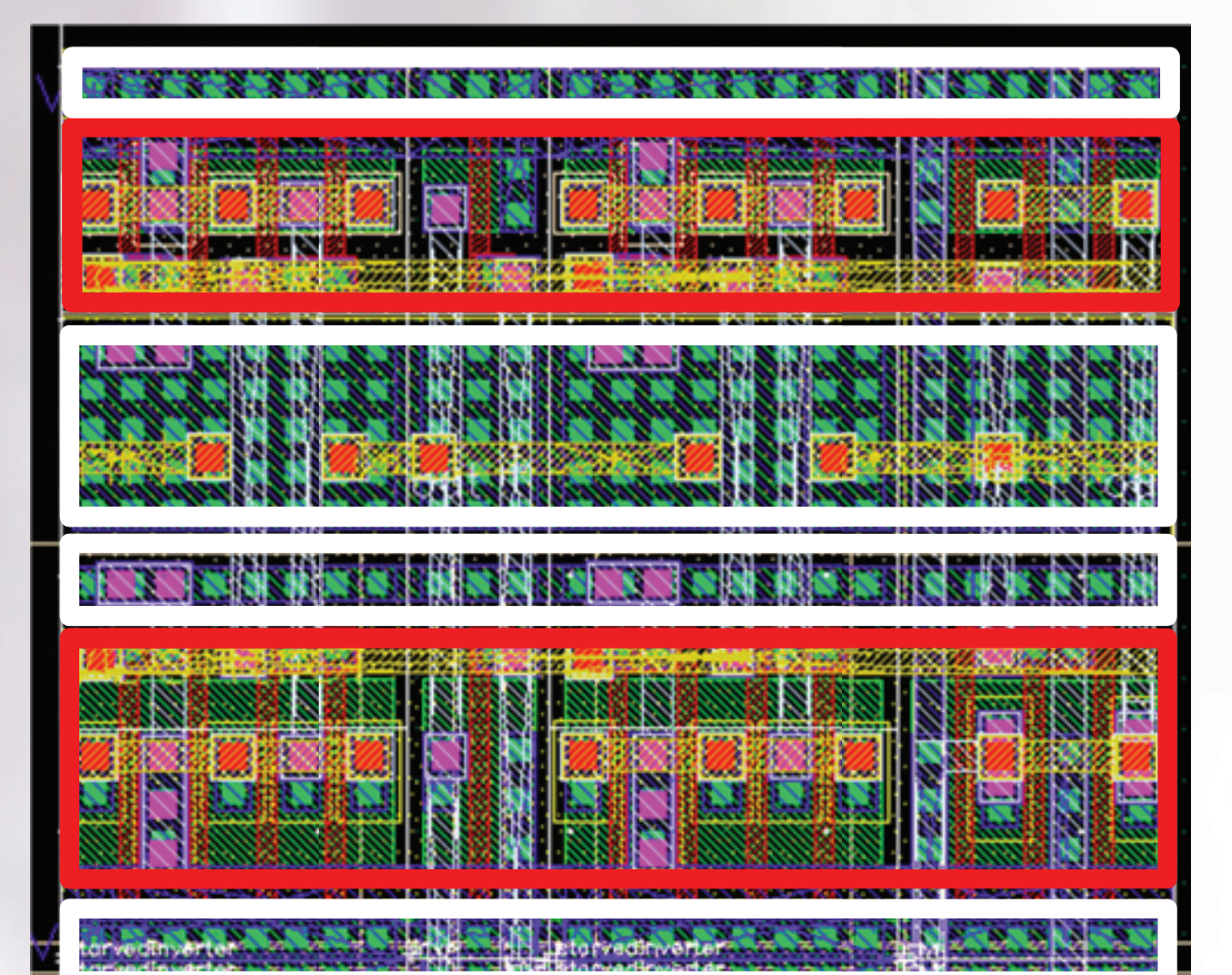
Slow control:



Reliability:



Guard rings:



	Simulated	Measured
Frequency range	25~57.3 MHz	35~70 MHz
σ Jitter	0.44 ps	5 ps
DLL vControl σ noise	0.53 mV	6 mV
σ DNL	6.37 ps	21.5 ps
SPI bitrate	20 Mbps	15 Mbps