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ATLAS

Liquid Argon Calorimeter

Phase-I Upgrade

Technical Design Report

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1 Overview of the Phase-I LAr upgrade project

This Technical Design Report details the scientific motivations and the technical implementation of the ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade project proposed to enhance the physics reach of the experiment in the high-luminosity environment foreseen in the next 10 years. The scope of the project is to design, build, and install new trigger readout electronics during the second long shutdown (LS2) of the Large Hadron Collider (LHC) in 2018.

The objective of this upgrade is to provide higher-granularity, higher-resolution and longitudinal shower information from the calorimeter to the Level-1 trigger processors. The 10-fold increase in granularity can be seen in Fig. 1, which compares the energy deposition of an electron in the existing trigger readout system to that of the proposed upgrade system. This upgrade improves the trigger energy resolution and efficiency for selecting electrons, photons, τ leptons, jets, and missing transverse momentum ($E_{\mathrm{T}}^{\mathrm{miss}}$), while enhancing discrimination against backgrounds and fakes in an environment with high instantaneous luminosity, i.e. with a large number of multiple interactions per LHC bunch crossing, or “pileup". As the LHC luminosity increases above the design value, the improved calorimeter trigger electronics will allow ATLAS to deploy more sophisticated algorithms, enhancing the ability to measure the properties of the newly discovered Higgs boson and the potential for discovering physics beyond the Standard Model.

The Phase-I upgrade project is an essential part of a broad upgrade program of the LAr calorimeters through the lifetime of the Large Hadron Collider and is fully compatible with the future Phase-II upgrade program of the ATLAS experiment planned for the third long shutdown (LS3) in 2022 - 2023, as briefly outlined in Secs. 1.1 and 1.4.

1.1 LHC baseline roadmap

Probing electroweak symmetry breaking (EWSB) will remain at the core of the physics program at the LHC over the course of the next two decades. This will include as complete an exploration as possible of the Higgs phenomenology with measurements of the couplings to both fermions and bosons and the observations of rare decay modes. Furthermore, the LHC will continue to exploit its unique access to the energy frontier in the search for new phenomena such as Supersymmetry (SUSY), extra dimensions, and other scenarios.

To support and extend the physics program and the discovery reach of the experiments, the LHC complex will be upgraded in three phases, as laid out in the mid- and long-term baseline plan [1] shown in Fig. 2:

- **Long Shutdown 1 (LS1):** $2013-2014$**.** The ongoing shutdown is used to consolidate machine elements (repairing the magnet splices and upgrading the collimation scheme) in order to achieve the design beam energy and luminosity.
- **Run 2:** $2015-2017$**.** The LHC will collide beams at $\sqrt{s} \simeq 13$ TeV in 2015, and is expected to reach and possibly exceed the design peak luminosity of $\mathcal{L}=10^{34}$ cm^{-2} s^{-1}. An integrated luminosity of $75-100\,\mathrm{fb}^{-1}$ is expected to be delivered to ATLAS and CMS during the 3 years of running in Run 2.
- **Long Shutdown 2 (LS2):** 2018**.** The Linac4 will be connected into the injector complex, and the injection beam energy of the Proton Synchrotron Booster will be upgraded in order to reduce the beam emittance. New cryogenics plants will be installed to separate the cooling of the superconducting radio frequency modules and the magnet cooling circuit.
- **Run 3:** $2019-2021$**.** The LHC design parameters should allow for an ultimate peak instantaneous luminosity of $\mathcal{L} \sim 2.2\times10^{34}$ cm^{-2} s^{-1} (Phase-I operation) and for delivering an integrated luminosity of $\sim 300\,\mathrm{fb}^{-1}$ during Run 3.

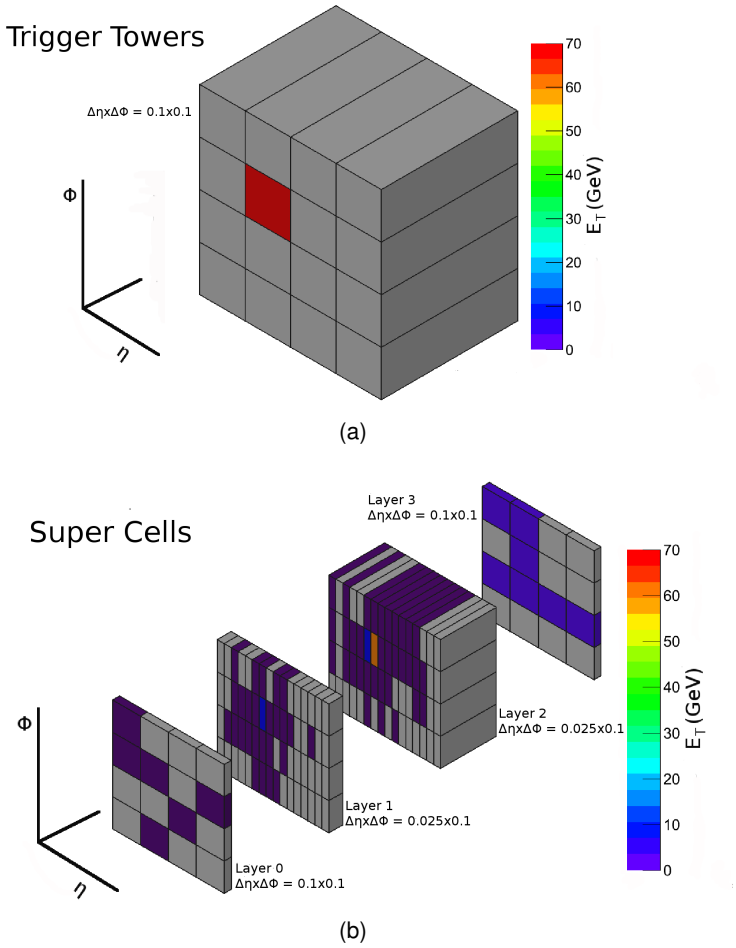


Figure 1. An electron (with 70 GeV of transverse energy) as seen by the existing Level-1 Calorimeter trigger electronics (a) and by the proposed upgraded trigger electronics (b).

- **Long Shutdown 3 (LS3):** $2022-2023$**.** The LHC will undergo a major upgrade of its components (e.g. low-β quadrupole triplets, crab cavities at the interaction regions).
- **High-Luminosity LHC (HL-LHC):** $2024-2030$ **and beyond.** The LHC complex will deliver levelled instantaneous luminosity $\mathcal{L} = 5{\times}10^{34}$ cm^{-2} s^{-1} (Phase-II operation) and an annual integrated luminosity of $250\,\text{fb}^{-1}$, i.e. up to $3\,\text{ab}^{-1}$ after 12 years of running.

1.2 ATLAS upgrade plans up to 2030 and beyond

To optimize the physics reach at each phase of the accelerator complex upgrades, ATLAS has devised a staged program in three phases, corresponding to the three long shutdowns.

The upgrades during LS1 consist of consolidation of the existing sub-detectors including the installation of a fourth (inner) layer for the pixel detector requiring a new, smaller radius central (Be) beam pipe, additional chambers in the muon spectrometer to improve the geometrical coverage, and more neutron shielding in the muon endcap toroids.

After LS2, instantaneous luminosities of $\mathcal{L} \sim 2.2{\times}10^{34}$ cm^{-2} s^{-1} are expected with 25 ns bunch spacing and the average number of interactions per crossing will be $\langle\mu\rangle \sim 60$. If ATLAS is to exploit this increase in luminosity and maintain a low-p_{T} lepton threshold (~ 25 GeV) in the Level-1 trigger

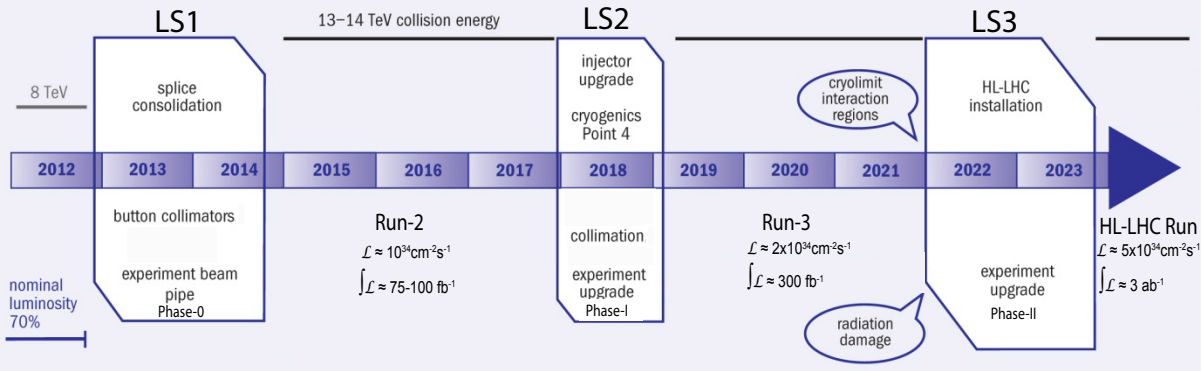


Figure 2. LHC baseline plan $2013-2030$. The first long shutdown (LS1) is scheduled for the consolidation of the machine elements to achieve design beam energy and luminosity. A second shutdown (LS2) is planned to upgrade the injector system and secure the ultimate LHC luminosity. The third shutdown (LS3) will allow for the installation of new focusing quadrupoles for the HL-LHC. The total integrated luminosity at the end of the HL-LHC lifetime will be approximately 10 times higher than the luminosity expected by the time of LS3. (from Ref. [1]).

while keeping the same trigger bandwidth (100kHz), the development of new detector and readout components are needed [2]. This is the primary motivation of the Phase-I detector upgrades, which include the additional chambers in the forward muon spectrometer, the upgrade of the calorimeter trigger electronics and the installation of new Level-1 trigger processors, a new Level-1 topological trigger processor, and a fast track trigger at the input of the Level-2 trigger system. The performance requirements and design specifications of each upgrade component are defined for $\mathcal{L} = 3\times10^{34}$ cm^{-2} s^{-1} and $\langle\mu\rangle = 80$ interactions per bunch crossing, to allow some margin in case of further improvements in the LHC peak instantaneous luminosity.

The Phase-II upgrades [3] for the HL-LHC run are motivated by the aging of the inner tracker (primarily because of radiation exposure), by the increased occupancy of the detector systems and data volumes that would saturate the readout links, by the obsolescence of some of the detector sub-system electronics, and by additional requirements that the trigger system will impose on the detector readout in order to cope with the expected luminosity during the HL-LHC era (5×10^{34} cm^{-2} s^{-1} with $\langle\mu\rangle = 140$ interactions per bunch crossing). Specifications of each upgrade component are then defined for up to $\langle\mu\rangle = 200$ interactions per bunch crossing.

1.3 Objectives of the Phase-I LAr upgrade project

The existing calorimeter trigger information is based on the concept of a “Trigger Tower" that sums the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta\times\Delta\phi = 0.1\times0.1$. The Trigger Tower is created through several stages of on-detector analog electronics, whose technical implementation is briefly outlined in Sec. 3.

The new finer granularity scheme is based on so-called “Super Cells", which provide information for each calorimeter layer for the full η range of the calorimeter, as well as finer segmentation ($\Delta\eta\times\Delta\phi = 0.025\times0.1$) in the front and middle layers of the EM barrel (EMB) and endcap (EMEC) for $|\eta| \leq 2.5$. This scheme is detailed for the EMB in Table 1 and is illustrated in Figs. 1 and 3. A full description of the geometrical representation of the Super Cells proposed for the entire calorimeter can be found in Appendix A.

The architecture of the upgraded calorimeter trigger electronics is depicted in Fig. 4, with the upgraded and new components outlined in red. The technical implementation of the upgraded front-

Table 1. Comparison of the current Trigger Tower granularity vs. the proposed Super Cell granularity in the LAr EM barrel calorimeter, in terms of both elementary cells and $\Delta\eta$ and $\Delta\phi$. The number of elementary cells grouped for the trigger readout in η and ϕ are indicated by n_η and n_ϕ, respectively.

Layer		Elementary Cell	Trigger Tower		Super Cell	
		$\Delta\eta\times\Delta\phi$	$n_\eta\times n_\phi$	$\Delta\eta\times\Delta\phi$	$n_\eta\times n_\phi$	$\Delta\eta\times\Delta\phi$
0	Presampler	0.025×0.1	4×1	0.1×0.1	4×1	0.1×0.1
1	Front	0.003125×0.1	32×1		8×1	0.025×0.1
2	Middle	0.025×0.025	4×4		1×4	0.025×0.1
3	Back	0.05×0.025	2×4		2×4	0.1×0.1

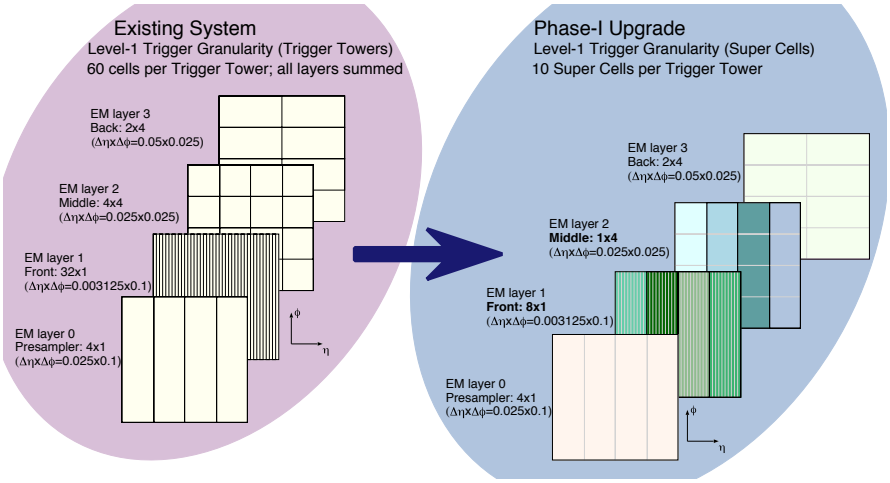


Figure 3. Geometrical representation in η,ϕ space of an EM Trigger Tower in the current system, where the transverse energy in all four layers are summed (left) and of the Super Cells proposed for the Phase-I upgrade, where the transverse energy in each layer is retained in addition to the finer granularity in the front and middle layers (right). Each square represents an area of size $\Delta\eta\times\Delta\phi = 0.1\times 0.1$.

end and back-end electronics is described in detail in Sec. 4 and 5 respectively.

To provide high-granularity and high-precision information to upgraded trigger processors called Feature EXtractors (FEXs) [4], new LAr Trigger Digitizer Boards (LTDB) are installed in the available spare slots of the Front-End crates. The upgrade of the layer sum boards and of the baseplanes allows the LTDBs to digitize information with granularity up to $\Delta\eta\times\Delta\phi = 0.025\times 0.1$ in the front and middle layers of the EM calorimeters. The LTDB also recreates the 0.1×0.1 analog sums and feeds them back to the Tower Builder Board (TBB) to maintain the "legacy" system as fully operational. The digitized signals are processed remotely by the LAr Digital Processing System (LDPS) modules, which convert the samples to calibrated energies in real-time and interface to the FEX processors.

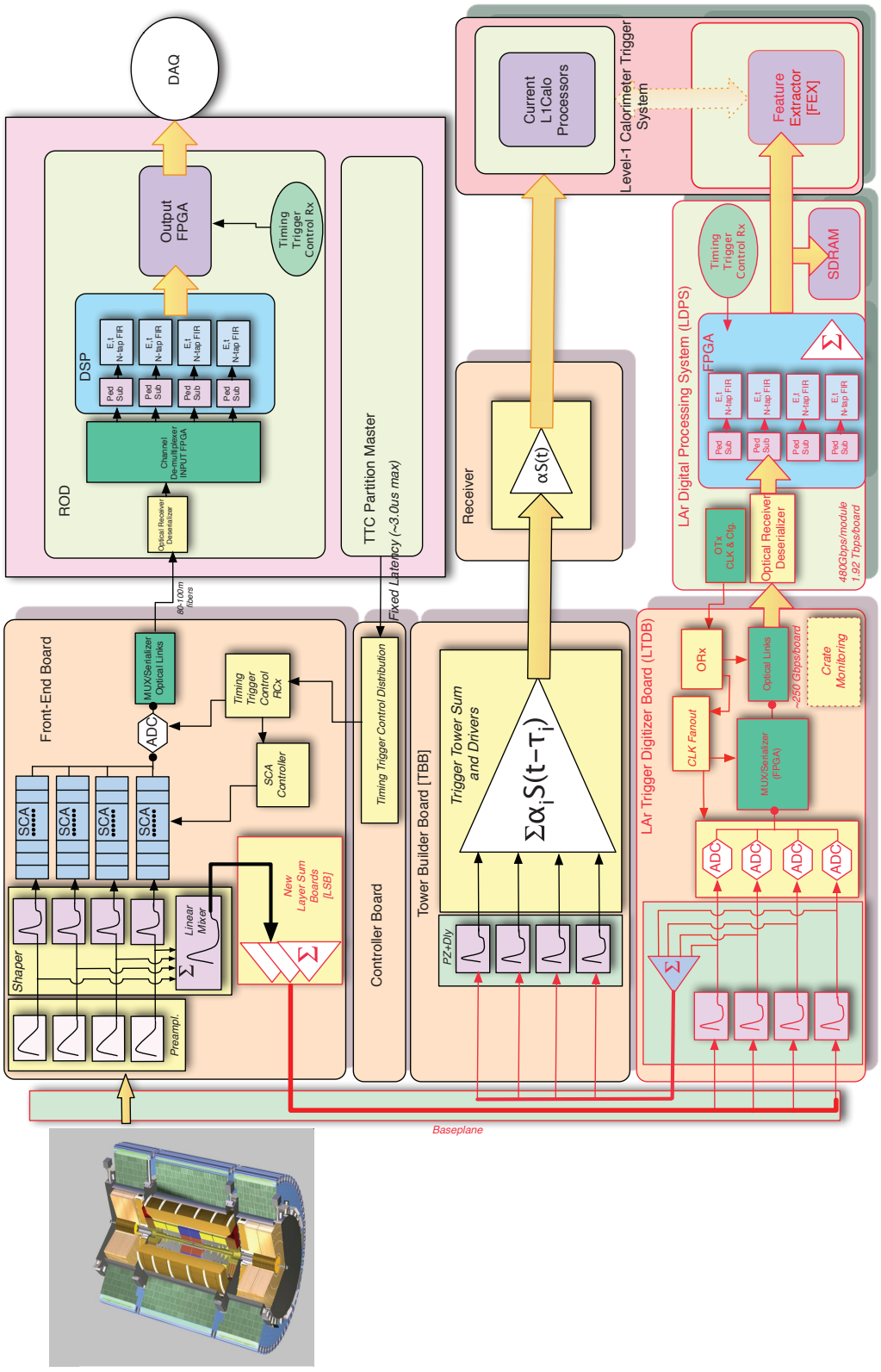


Figure 4. Schematic block diagram of the Phase-I upgrade LAr trigger readout architecture. The new components are indicated by the red outlines and arrows.

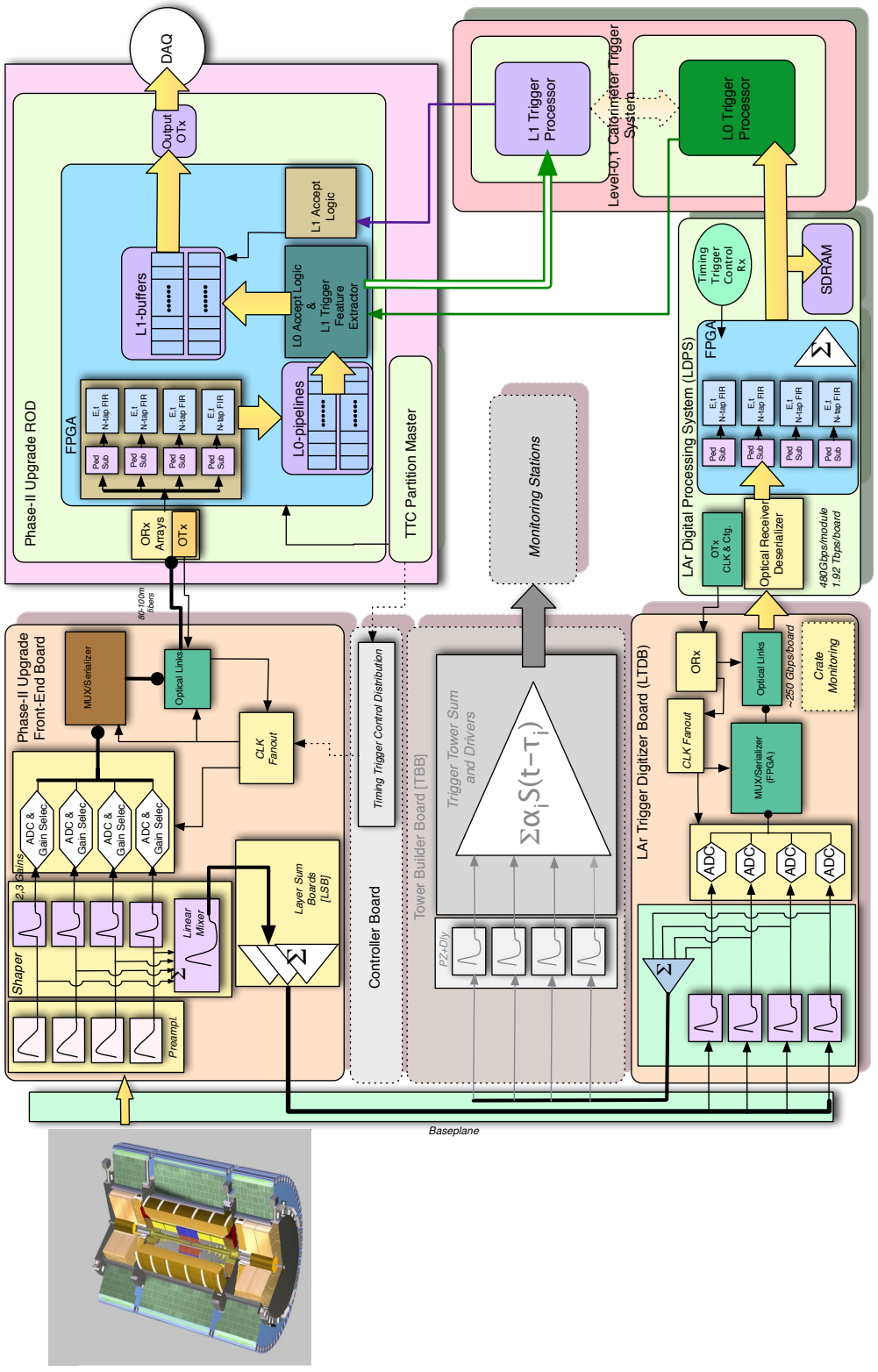


Figure 5. Schematic block diagram of the Phase-II upgrade LAr readout architecture. The "legacy" trigger electronics (grayed out in the figure) will be decommissioned during LS3.

The scope of the ATLAS Phase-I upgrades is limited to a few sub-detectors only. The readout of most of the systems will remain unchanged, limiting the capability of extending some of the parameters of the Level-1 trigger system, like the maximum rate and maximum latency. Reference [5] documents the latency budget assigned to each sub-system. Table 2 details the estimated latency of the components of the proposed LAr Phase-I upgrades. The total latency amounts to 44.2 bunch crossings (BCs). In addition, the Feature Extractor processors require 14 BCs to extract the trigger primitives and transmit them to the Topological processors. The overall 58.2 BC latency of the calorimeter trigger system is consistent with the maximum (65 BCs) value allowed in [5] at the input of the Topological Trigger processors where data from both the calorimeter and the muon trigger modules are combined.

Table 2. Latency budget for the Phase-I upgrade of the LAr trigger readout electronics

	Latency		Sub-total [BCs]	Total [BCs]
	[ns]	[BCs]		
Time-of-flight at $\eta = 2$	15	0.6		
Cable to pulse preamplifier	30	1.2		
Preamplifier and shaper	10	0.4		
			2.2	**2.2**
Digitization on LTDB	200	8.0		
Multiplexing on LTDB	25	1.0		
Serializer on LTDB	50	2.0		
Optical Cable (70 m) from LTDB to LDPS	349	14.0		
			25.0	**27.2**
Deserializer on LDPS	50	2.0		
Channel Demultiplexing on LDPS	25	1.0		
Pedestal Subtraction	25	1.0		
E_{T} with forward correction	125	5.0		
Digital summation	50	2.0		
Multiplexing $40-320$ MHz on LDPS	25	1.0		
Serializer on LDPS	50	2.0		
Optical cable (15 m) from LDPS to FEX	75	3.0		
			17.0	**44.2**

The upgrades aim to better control the trigger rates by improving the selectivity of EM and τ objects, the resolution of jets and $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger signatures, and the discrimination power against background emerging from both the out-of-time and in-time pileup. Performance studies and impact on physics analyses are outlined in Sec. 2 of this report and in the complementary TDAQ TDR [4]. Ultimately the project targets are:

1. Reduce jet backgrounds in the Level-1 EM trigger by deploying shower shape algorithms and high-precision isolation criteria for electron and photon identification.
2. Deploy algorithms currently used in the high-level trigger to improve τ identification in the Level-1 trigger.
3. Improve the Level-1 jet and $E_{\mathrm{T}}^{\mathrm{miss}}$ resolutions and efficiencies to effectively reduce the rates while retaining the same physics acceptance in the offline analyses.

These improvements will be achieved by taking advantage of the higher η-granularity of the Super

Cells compared to Trigger Towers, the layer segmentation, providing longitudinal shower information for the Level-1 trigger, and the higher precision of the energy in the Super Cells due to a smaller quantization scale. Ultimately the goal is to maintain the thresholds of single and multi-object Level-1 calorimeter triggers at values comparable to those used in Run 1 despite the increased centre-of-mass energy, potential instantaneous luminosity up to $\mathcal{L} = 3{\times}10^{34}$ cm^{-2} s^{-1}, and pileup up to $\langle\mu\rangle = 80$.

To demonstrate the expected performance, an “in-situ Demonstrator" is planned to be installed on a partition ($\Delta\eta \times \Delta\phi = 1.4 \times 0.4$) of the ATLAS LAr EM barrel calorimeter at the end of LS1 (see App. D for more details).

1.4 Compatibility with Phase-II upgrades

The long-term plan of the ATLAS LAr calorimeters foresees installation of upgraded trigger electronics in LS2 and replacement of the main readout electronics during LS3 to be able to continue to operate the LAr calorimeter system at its full potential during the HL-LHC era. The radiation levels measured in ATLAS after Run 1 [6] show that the on-detector electronics will be able to survive the integrated luminosity before LS3.

Figure 5 shows the readout architecture planned for the Phase-II upgrades: the Phase-I upgrade components will be maintained during the HL-LHC run, the “legacy” trigger electronics (grayed out in the figure) will be decommissioned, and the main readout electronics will be completely replaced by new front-end boards, which will digitize the signals at each bunch crossing and send them over fast optical links to pre-processor readout modules which will apply full precision calibration and fill trigger pipelines.

This architecture fits naturally in the ATLAS plans described in [3]. The hardware-based first level trigger will be divided into two (Level-0 and Level-1) sub-systems: in the Level-0 trigger the calorimeter trigger “core” is made out of the LTDB, LDPS, and FEX systems installed in LS2 for the Phase-I upgrades, while a Level-1 trigger will access the full granularity detector information to further enhance discrimination against backgrounds.

For these reasons, the Phase-I upgrade project is fully compatible with the overall ATLAS upgrade long-term plans and can be considered the first step of a single, staged upgrade path.

2 Physics Requirements and Expected Performance

Probing the details of the electroweak symmetry breaking is among the highest priorities for the LHC experiments after the summer 2012 discovery of a 125 GeV Higgs boson. The Phase-I upgrade of ATLAS will provide an excellent laboratory to make precision measurements of this new particle, in particular its couplings to fermions and electroweak gauge bosons. Additionally, ATLAS will continue to explore the energy frontier in order to address outstanding questions by looking for new physics including supersymmetry (SUSY) and extra dimensions.

The Super Cell trigger readout of the LAr Calorimeter upgrade provides additional information and more powerful tools to the Level-1 trigger feature extraction. These improvements will be essential to maximize the physics potential at the higher instantaneous luminosities and more severe pileup conditions expected after the Phase-I and Phase-II upgrades of the LHC. The motivation and ultimate goal of the upgrade is to improve the performance of the Level-1 single object triggers based on the calorimeter information by (i) enabling the use of shower-shape variables for a more effective identification of electrons, photons and τ leptons; (ii) sharpening the EM, jet, and $E_{\mathrm{T}}^{\mathrm{miss}}$ efficiency turn-on curves using more advanced reconstruction algorithms at Level-1 and utilizing pileup subtraction techniques on an event-by-event basis (as currently implemented in the offline analyses).

These performance improvements are possible thanks to the following upgrades:

- The calorimeter segmentation available in the Level-1 trigger is made finer using Super Cells as described in Sec. 1.3: groups of calorimeter cells are summed together in the front-end electronics to form areas as narrow as $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$ in the front and middle layers of the EM calorimeters. Information on the longitudinal shower development — the Super Cells provide the transverse energy for each layer in the electromagnetic calorimeter — will also become available for the Level-1 trigger decision.

- The digitization precision of the Super Cell signals is improved by at least a factor of 4 compared to the existing Level-1 system: the quantization scale and the dynamic range of the digitizers are optimized in each η-region and for each layer of the calorimeter to achieve sensitivities at the level of the Super Cell electronic noise or better.

- The transverse energy deposited in the Super Cells is calculated at each bunch crossing through optimized algorithms; techniques similar to the optimal filtering currently implemented in the LAr Readout Drivers [7] provide results close to the energy resolution obtained from the offline reconstruction.

In the performance studies presented here, the transverse energy reconstruction in each Super Cell is assumed to be implemented through optimal filtering on the digitized signals of the individual calorimeter cells forming the Super Cell as explained in Sec. 2.1. A detailed comparison of the different signal processing techniques with merit and issues related to the implementation of the algorithms in FPGAs is summarized in Sec. 5.6.

This chapter is structured in three sections. After a brief summary of the transverse energy reconstruction in the Super Cells (Sec. 2.1), Sec. 2.2 summarizes the expected performance for Level-1 trigger objects: electrons and photons, τ leptons, jets, and $E_{\mathrm{T}}^{\mathrm{miss}}$. Section 2.3 shows the impact of this upgrade on the event selection and background rejection for a few relevant examples from the LHC physics program.

2.1 Super Cell Energy Reconstruction and Resolution

Energy reconstruction in the calorimeter Super Cells aims to extract the energy deposited by particle showers with high precision and assign it to the correct bunch crossing with high efficiency and a low

misidentification rate. To achieve this goal, the pulse shape in the LAr calorimeter must be known to high accuracy. The extensive experience gained in Run 1 with respect to the energy reconstruction and calibration at the level of the elementary calorimeter cells can be directly applied to the Super Cells.

2.1.1 Energy reconstruction

The energy deposited in the elementary LAr calorimeter cells is reconstructed through an optimal filtering [7] algorithm based on a linear combination of the signal samples with coefficients that minimize the contribution of electronics and pileup noise (see also Sec. 5.6). This minimization relies on the precise knowledge of the pulse shape and, in particular, of its autocorrelation function, which is attainable with detailed calibration procedures.

As the luminosity increases, pileup becomes the dominant contribution to the total noise in many regions of the calorimeter. Figure 6 shows the predicted total noise of the cells of the ATLAS calorimeters (LAr and Tile) for the conditions expected during Phase-I (a) and Phase-II (b) operations.

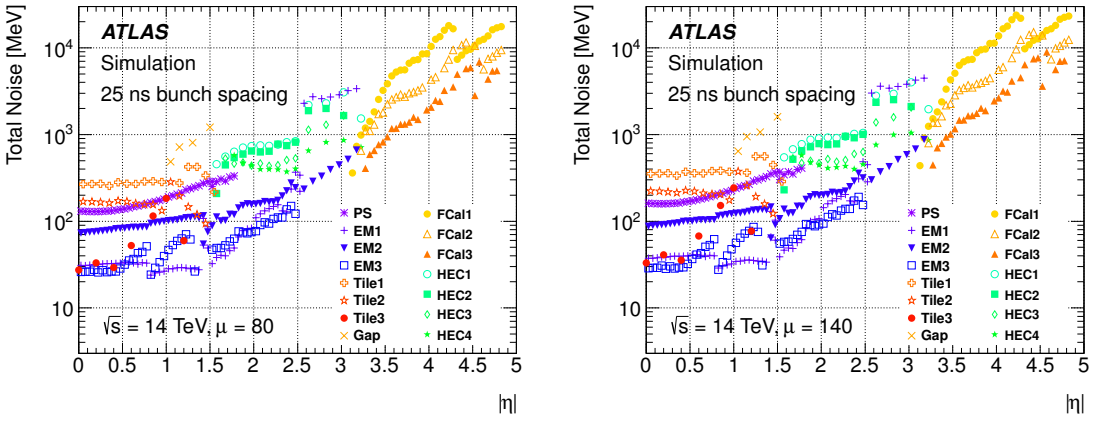


Figure 6. Simulated noise (transverse energy per cell) in the various layers of the Liquid Argon and Tile calorimeters as a function of $|\eta|$ for proton-proton collisions at $\sqrt{s} = 14$ TeV and a bunch spacing of 25 ns. The average numbers of interactions per bunch crossing (pileup events) are $\langle\mu\rangle = 80$ (a) and $\langle\mu\rangle = 140$ (b), corresponding to the nominal Phase-I and Phase-II pileup conditions, respectively.

It is important to emphasize that in all the performance studies described in Secs. 2.2.1–2.2.5, the Super Cell energy is reconstructed by summing the energies of the individual cells belonging to it. This procedure is a good approximation considering that the optimal filtering techniques are a linear estimation of the input deposited energy, the cross-correlation of the electronics noise among cells in a Super Cell is negligible[1], and the effective pulse shape of the Super Cell signal is similar to the shapes of the individual calorimeter cells. Furthermore, the correlations of the pileup contribution are handled by the simulation. However, this procedure does not take into account any other coherent contribution to the noise fluctuations, or any second-stage noise sources in the readout processing of the Super Cell pulses. For a full and detailed analysis of the performance of the analog signal filtering, the digitization and the digital signal processing will be implemented directly in the Geant4

[1] The coherent noise contributes less than 10% of the total electronics noise.

simulations. This is an ongoing effort that will be completed after this Technical Design Report is submitted.

2.1.2 Energy Resolution

The high-granularity and high-resolution data provided by the Super Cells will enable the upgraded Level-1 trigger system to reconstruct electromagnetic clusters with improved precision.

The transverse energy (E_{T}) in each Super Cell is obtained through an optimal filtering algorithm on the raw input data with a quantization scale of 125 MeV in the middle EM layer and 32 MeV elsewhere. EM clusters are then formed from the Super Cells over an area of size $\Delta\eta \times \Delta\phi = 0.075 \times 0.2$; the optimal size and shape of the clusters will continue to be studied beyond this report. Corrections are applied to each layer[2] and as a function of η to account for the material in front of the calorimeter: a strategy that is only possible with the Phase-I upgrade.

The excellent correlation between the resulting Super Cell cluster E_{T} ($E_{\mathrm{T}}^{\mathrm{SC(3\times2)}}$) and the transverse energy of the offline reconstructed electrons ($E_{\mathrm{T}}^{\mathrm{off}}$) is shown in Fig. 7 (a). Preliminary studies, shown in Fig. 7 (b), demonstrate the significant improvement in the energy resolution using the layer-weighted 3×2 Super Cell cluster E_{T} compared to the existing Level-1 E_{T} ($E_{\mathrm{T}}^{\mathrm{L1}}$). This resolution improvement translates into an improved efficiency for EM objects in the trigger for a given offline E_{T}, sharpening the turn-on curve and thus making it possible to lower the offline E_{T} threshold by several GeV for the same trigger rate.

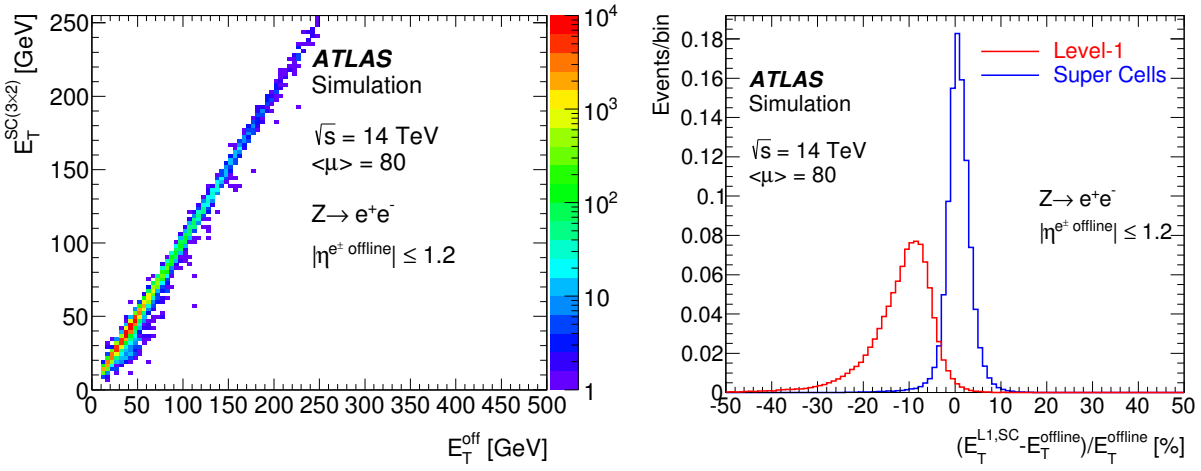


Figure 7. (a) Distribution of $E_{\mathrm{T}}^{\mathrm{SC(3\times2)}}$ vs. $E_{\mathrm{T}}^{\mathrm{off}}$, and (b) the percent difference between $E_{\mathrm{T}}^{\mathrm{L1}}$ and $E_{\mathrm{T}}^{\mathrm{off}}$ (red) compared to that between $E_{\mathrm{T}}^{\mathrm{SC(3\times2)}}$ and $E_{\mathrm{T}}^{\mathrm{off}}$ (blue) for simulated $Z \rightarrow e^{+}e^{-}$ events in the LAr EM barrel calorimeter. The electron candidates are required to be within $|\eta| \leq 1.2$

The dynamic range of the digitized pulses will be optimized for the overall performance by taking into account the impact of noise due to the least significant bit and second stage noise in the amplifiers, and the expected saturation energy. Current studies assume a least significant bit of transverse energy equal to 32 MeV and 125 MeV in the front and middle layer, respectively. This choice of least significant bit has a negligible effect on the resolution while optimizing the dynamic

[2]The technical implementation of the layer correction in the FPGA would be through look-up tables and will need to be evaluated to fully assess the impact on the system latency.

range. With a 12-bit range, E_{T} values up to 102 GeV and 400 GeV in the corresponding calorimeter layers will be properly processed without loss of precision. Very energetic electrons, which have a more concentrated shower than taus or jets, may exceed these values. Additional details of the energy reconstruction using various filtering techniques, as well as a discussion of saturation and bunch crossing identification, can be found in Sec. 5.6.

2.2 Level-1 trigger performance studies

The results presented in this section are based on full simulation studies of the ATLAS detector [8] made with Geant4 [9]. The trigger efficiency for the various physics objects (e, τ, etc.) is evaluated using samples of signal (e.g. $Z \to e^+e^-$ and $Z \to \tau^+\tau^-$) events overlaid with an average of 80 (unless otherwise stated) minimum-bias events generated with PYTHIA [10], to reproduce the pileup conditions expected in Run 3. Rejection of background and trigger rates are obtained from a sample of overlapping minimum-bias events with $\langle\mu\rangle = 80$. The improved resolution provided by the upgraded electronics is included in the studies presented here.

2.2.1 EM trigger performance

The trigger rates at the LHC design energy and instantaneous luminosity expected in Run 3 will be unaffordable for the relatively low-p_{T} thresholds required by many crucial physics studies unless additional discriminating criteria are introduced to separate electrons and photons from jets. EM showers due to electrons and photons can be effectively distinguished from the background of QCD jets through the use of additional shower shape variables which will become accessible at the upgraded Level-1 trigger thanks to the higher Super Cells granularity, the calorimeter longitudinal layer information and the finer quantization scale. The studies presented below demonstrate a substantial reduction in trigger rates when using these variables, which translates into a possible reduction of the Level-1 trigger threshold by 7 GeV compared to Run 2.

2.2.1.1 Shower shape analysis The finer granularity of the Super Cells enables a more sophisticated rejection of jet backgrounds than in the current system through the use of shower shape variables. The performance of the following three discriminating variables (chosen for their importance to offline electron identification) is investigated:

R_η Given a 3×2 group of Super Cells in $\eta\times\phi$ centered on the highest-energy Super Cell in the middle layer (2), R_η is defined as the transverse energy measured in the 3×2 group divided by the transverse energy measured in a 7×2 group:

$$R_\eta = \frac{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}}{E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.175\times0.2}} \tag{1}$$

f_3 The ratio of the transverse energy measured in the back EM layer (3) in an area of size $\Delta\eta\times\Delta\phi = 0.2\times0.2$ to that deposited in all three layers for an EM cluster; the energies in the front (1) and middle (2) EM layers are reconstructed in the area $\Delta\eta\times\Delta\phi = 0.075\times0.2$:

$$f_3 = \frac{E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}{E^{(1)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(2)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2} + E^{(3)}_{\mathrm{T},\Delta\eta\times\Delta\phi=0.2\times0.2}}. \tag{2}$$

$w_{\eta,2}$ The spread of the shower in the middle EM layer (2) in a 3×2 Super Cell region, defined as:

$$w_{\eta,2} = \sqrt{\frac{\Sigma\left(E_{\mathrm{T}}^{(2)}\times\eta^2\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}^{(2)}} - \left(\frac{\Sigma\left(E_{\mathrm{T}}^{(2)}\times\eta\right)_{\Delta\eta\times\Delta\phi=0.075\times0.2}}{E_{\mathrm{T},\Delta\eta\times\Delta\phi=0.075\times0.2}^{(2)}}\right)^2}, \tag{3}$$

where the sums run over the Super Cells.

The separation power of these variables is illustrated in Fig. 8 for electrons from $Z\rightarrow e^+e^-$ events and background jets. As expected, R_η has a narrow distribution for electrons, close to unity. In comparison, the distribution for jets is much broader. Similarly, the distributions of $w_{\eta,2}$ and f_3 are typically narrower for EM showers than for hadronic showers.

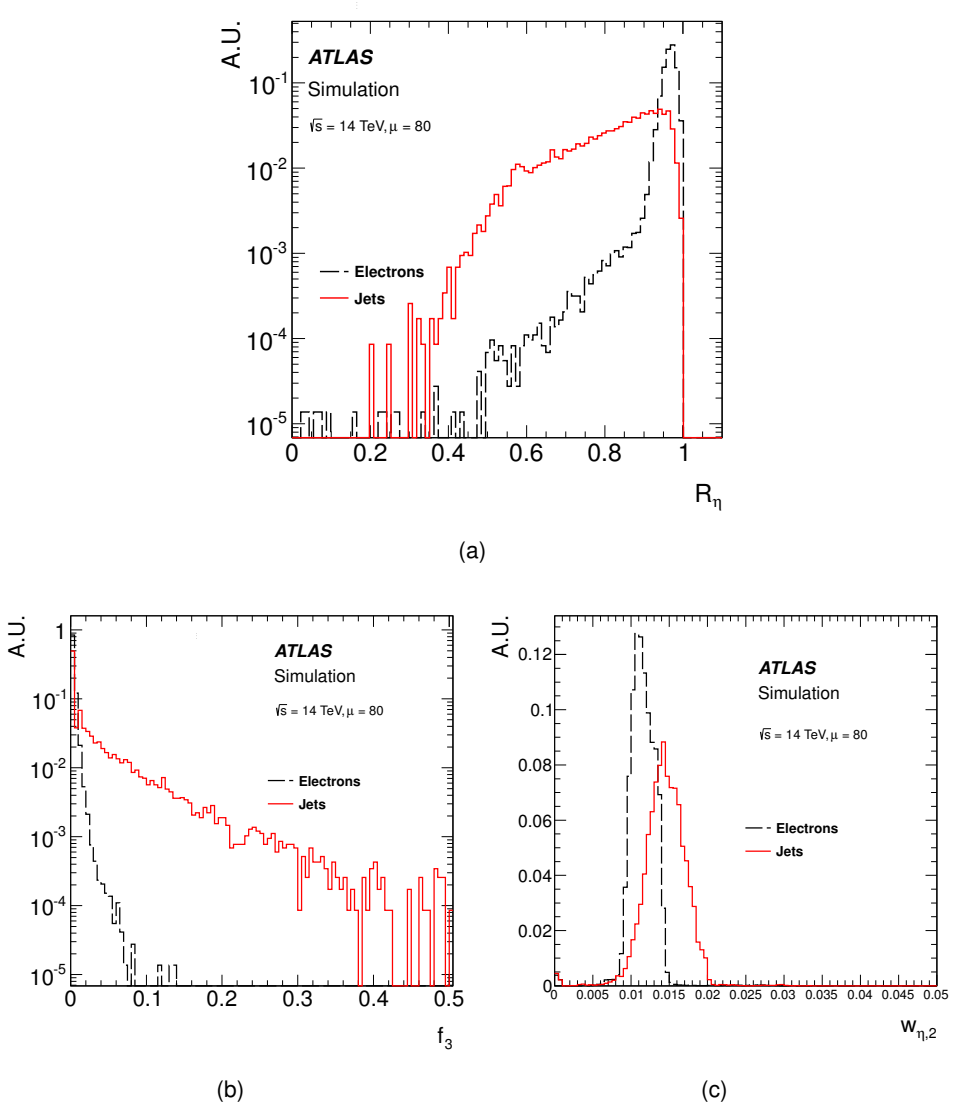


Figure 8. Distributions of variables allowing to distinguish between electrons (black) and jets (red) with $p_{\mathrm{T}} > 20$ GeV and with the upgraded Level-1 trigger: R_η (a), f_3 (b), and $w_{\eta,2}$ (c), as defined in the text. Each distribution is normalized to unit area.

2.2.1.2 Multi-dimensional optimization of shower shape variables A multi-dimensional optimization is performed to minimize the trigger rate while keeping a high signal efficiency. This optimization explores the parameter space covered by the discriminating variables R_η, $w_{\eta,2}$, and f_3 in minimum bias events. In addition, hadronic isolation (*HadCore* ≤ 1 GeV) is required for each electron candidate, where *HadCore* is defined as the transverse energy deposited in a $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ region of the hadronic calorimeter behind the EM shower. The trigger efficiencies quoted in this section are derived from simulated $Z \to e^+e^-$ signal events. All efficiencies are computed as the fraction of offline electrons with $p_{\mathrm{T}} > 20$ GeV in the signal sample reconstructed with tight identification requirements [11] that pass the trigger selection. Using this definition of efficiency leads to slightly lower values than obtained with a higher p_{T} selection: e.g., requiring $p_{\mathrm{T}} > 30$ GeV would lead to an approximately 2 % higher efficiency.

The dependence of the signal efficiency on the parameter R_η is shown in Fig. 9 (a) with the *HadCore* requirement and with successive cuts on optimized values of $w_{\eta,2}$ and f_3. Figure 9 (b) shows the corresponding trigger rates as measured from simulated $\langle\mu\rangle = 80$ minimum bias events. The curves labeled *HadCore* ≤ 1 GeV correspond to the present Level-1 trigger without EM isolation.

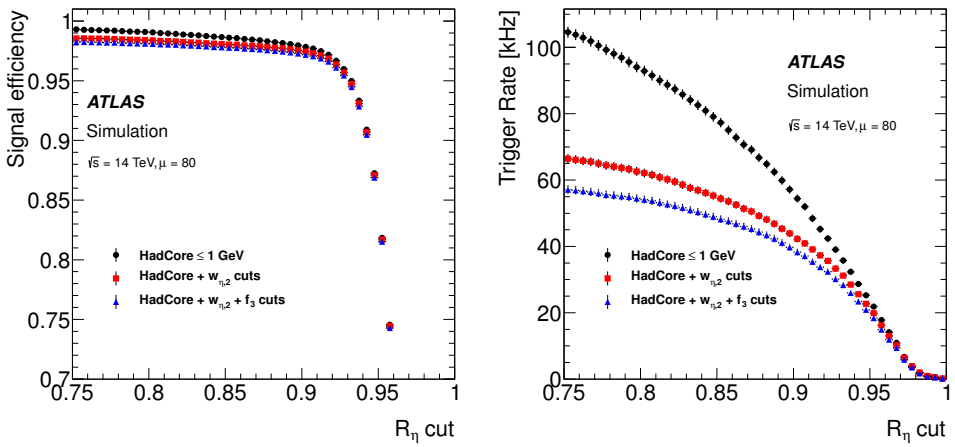


Figure 9. (a) Trigger efficiency as a function of the requirement on the R_η variable for a p_{T} threshold of 20 GeV from $Z \to e^+e^-$ events. The curves refer to the present Level-1 trigger (black points) and upgraded Level-1 trigger with various requirements on the R_η, $w_{\eta,2}$ and f_3 variables. (b) Trigger rate evolution for $\mathcal{L} = 3 \times 10^{34}$ cm^{-2} s^{-1} with requirements on R_η for electrons with $p_{\mathrm{T}} > 20$ GeV.

Figure 10 displays the dependence of the trigger rate on E_{T} threshold for successive selection criteria: *HadCore*, $w_{\eta,2}$, R_η, and f_3. The individual criteria were optimized in all three shower-shape variables. The use of these three new variables to reject jet backgrounds provides a decrease (by up to a factor of 4 for $p_{\mathrm{T}} \sim 20$ GeV) in the trigger rate for the same electron efficiency. The correlations among the three variables clearly do not allow the total gain in trigger rates to be a sum of the individual improvements.

As a result of these studies, the optimized parameters were chosen to be $R_\eta \geq 0.93$ (0.94), $w_{\eta,2} < 0.0146$ (0.014), and $f_3 \leq 0.02$ (0.02), yielding a trigger efficiency of 95 % (90 %) and a 20 kHz rate for an E_{T} threshold of 21.5 (20.5) GeV, respectively. The trigger rates can be further reduced to 15 kHz and 11 kHz by raising the E_{T} threshold to 24 (22) GeV and 25.5 (24) GeV, respectively. Figure 11 provides a comparison of the Run 2 Level-1 trigger performance to that of the upgraded Level-1 trigger for a 95 % electron efficiency in both cases. It shows that for a given bandwidth of

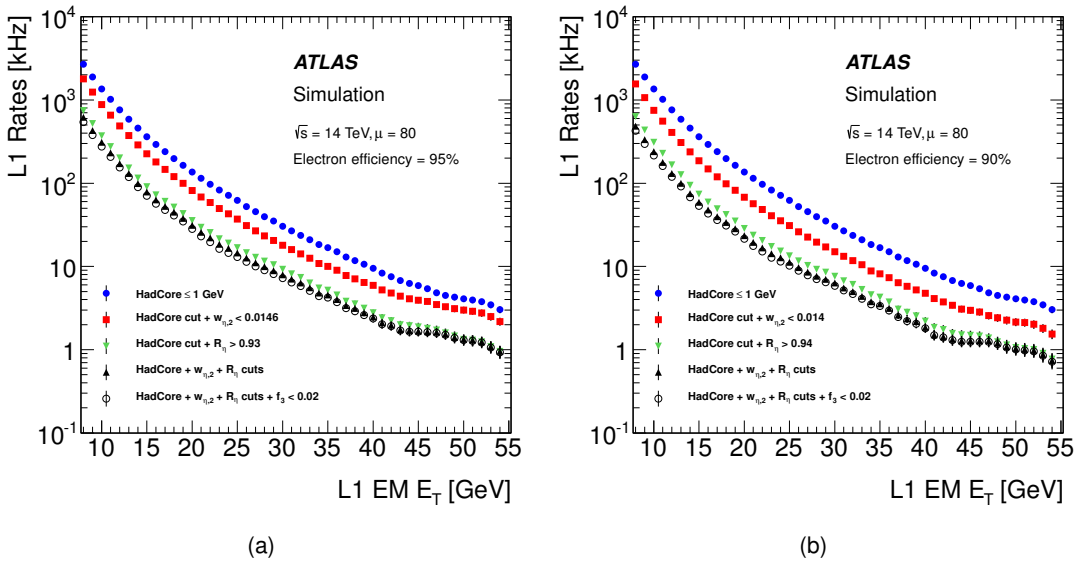


Figure 10. Trigger rates for $\mathcal{L} = 3 \times 10^{34}$ cm^{-2} s^{-1} as a function of E_{T} thresholds with optimized requirements on *HadCore*, $w_{\eta,2}$, R_{η}, and f_3. Subfigures (a) and (b) correspond to trigger efficiencies of 95 % and 90 %, respectively, for electrons from simulated $Z \to e^+e^-$ decays.

e.g. 20 kHz, the Level-1 threshold, which would need to be 28.5 GeV assuming Run 2 conditions, could be lowered by 7 GeV to 21.5 GeV with the proposed upgrade. On top of this improvement, the better Level-1 EM resolution due to the possible application of layer weights, as shown in Sec. 2.1.2, will substantially sharpen the trigger turn-on curves, resulting in an additional reduction of the offline threshold by several GeV. This translates into a considerable improvement of the signal acceptance for many physics channels, as discussed with a few examples in Sec. 2.3.

It should be noted that the exact values of the parameters R_{η}, $w_{\eta,2}$ and f_3 will have to be re-optimized using data to correct for small differences between the simulated shower shapes and those observed in data. The same had to be done for the offline selection criteria for electrons and photons after the first data were recorded in 2010.

2.2.1.3 Photon performance A verification of the photon trigger efficiency with the optimized EM shower shape requirements derived in the previous section is needed, given the importance of high-sensitivity measurements of the Higgs boson in the $\gamma\gamma$ decay mode. Simulated $H \to \gamma\gamma$ events with leading photon $p_{\mathrm{T}} > 40$ GeV (as used in the standard ATLAS analysis) have therefore been studied. Table 3 shows the resulting photon efficiencies for the working points derived from the $Z \to e^+e^-$ sample. It should be noted that the requirements for R_{η}, $w_{\eta,2}$ and f_3 were chosen so as to yield the same electron efficiencies as during Run 1 conditions. This implies that the single photon and di-photon efficiencies will also be very similar.

2.2.1.4 Clustering algorithms The studies shown in this document are performed using the present ATLAS clustering algorithms to define EM showers. Similar results are expected with algorithms based on Super Cells, where an initial seed is any Super Cell above 3 GeV in the EM calorimeter with $|\eta| < 2.5$. The electron energy is then computed by adding the energy from all EM layers in a 3×2 region for $|\eta| < 1.4$ and a 5×2 region beyond. The electron η and ϕ are determined by an energy-weighted average of the Super Cell position.

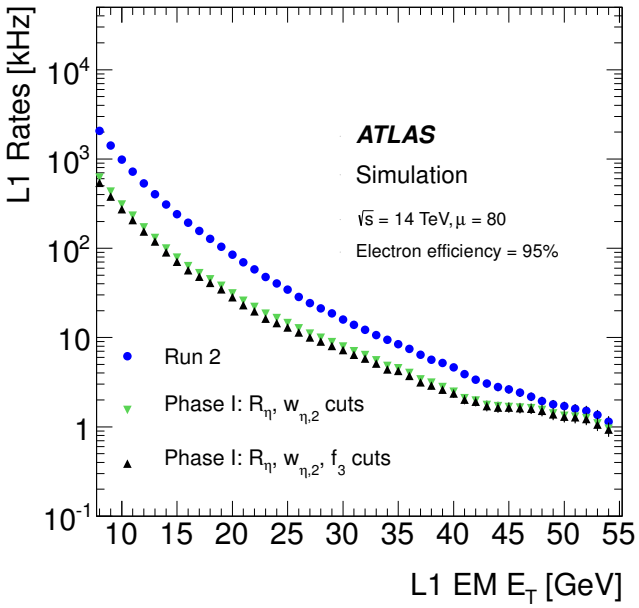


Figure 11. Level-1 trigger rates for a 95% electron efficiency as a function of the EM E_{T} threshold assuming Run 2 conditions (blue points) and for Run 3 conditions ($\mathcal{L} = 3 \times 10^{34}$ cm^{-2} s^{-1}) for two sets of variables (green and black triangles), as measured from a sample of simulated minimum bias events with $\langle\mu\rangle = 80$.

2.2.1.5 Dependence on quantization scale With the electronics upgrade, the least significant bit for the front and middle EM layer trigger readouts are lowered to 32 MeV and 125 MeV, respectively, as compared to 1 GeV in Run 2. This increased precision results in improved resolutions and sharper trigger turn-on curves: approximately 1 GeV is gained in the rise from 5 % to 98 % efficiency.

2.2.2 Tau trigger performance

The ATLAS physics program with τ leptons includes Higgs boson studies in the di-τ channel, several electroweak measurements, searches for Supersymmetric particles and other new physics processes. Approximately $65\,\%$ of τ decays are hadronic, indicated here as τ_{had}, with one neutrino and one or more hadrons. The challenge at the trigger level, especially at the low-p_{T} values required by

Table 3. Photon efficiencies and corresponding electron efficiencies for various sets of (optimized) requirements on the parameters R_η, $w_{\eta,2}$, and f_3. The photon (electron) efficiencies are calculated for photons (electrons) with $p_{\mathrm{T}} > 40$ GeV ($p_{\mathrm{T}} > 20$ GeV).

Variables	Optimized Values	Single Photon efficiency	Di-Photon efficiency	Electron efficiency
R_η, $w_{\eta,2}$	$R_\eta > 0.93$, $w_{\eta,2} < 0.0146$	97.5%	94.9%	95%
R_η, $w_{\eta,2}$	$R_\eta > 0.94$, $w_{\eta,2} < 0.014$	94.5%	88.6%	90%
R_η, $w_{\eta,2}$, f_3	$R_\eta > 0.93$, $w_{\eta,2} < 0.0146$, $f_3 < 0.02$	95.8%	91.9%	95%
R_η, $w_{\eta,2}$, f_3	$R_\eta > 0.94$, $w_{\eta,2} < 0.014$, $f_3 < 0.02$	92.8%	85.8%	90%

Higgs boson studies, is to distinguish hadronic tau decays from QCD jets.

In the offline analysis, τ_{had} reconstruction and identification is based on both tracking and calorimeter information. The track multiplicity is a powerful handle as τ_{had} decays mostly give rise to one or three tracks. The calorimeter uses the shape of the energy deposit in both the transverse and longitudinal directions to distinguish the narrow τ clusters from the broader jets. Furthermore, the transition radiation information from the TRT provides discrimination between electrons and pions and thus rejection of the electron background.

For the ATLAS Level-1 trigger system, where there is no tracking information available, the entire burden is on the calorimeter system. Given the importance of the longitudinal and transverse shower profiles to discriminate between taus and jets, the increased granularity available with the Super Cells over the present Level-1 trigger towers is expected to be crucial to keep low thresholds on τ_{had} decays in the increased luminosity and pileup environment after LS2, hence achieving high sensitivity on Higgs boson couplings measurements and other physics studies involving low-p_{T} taus.

The following studies are based on a simulated $Z \rightarrow \tau\tau$ sample with $\langle\mu\rangle = 60$. The signal efficiency is calculated by matching the Level-1 trigger object to the true τ_{had} from the simulation. The background rejection is determined using minimum bias events simulated at $\sqrt{s} = 14$ TeV, with $\langle\mu\rangle = 80$, and 50 ns bunch-spacing. Slight variations in the simulation conditions are not expected to have a large impact on the results.

The variables described below are studied at three operating points that correspond to 80 %, 90 % and 95 % efficiency, respectively. Only the middle layer (2) of the EM calorimeter is used in these studies, with additional rejection power expected from including additional layers.

f_{core} This variable is designed to take advantage of the narrowness of the τ_{had} cluster compared to the background jets. The variable builds a numerator and denominator based on the transverse energies deposited within a region up to $\Delta\eta \times \Delta\phi = 0.4 \times 0.4$. The numerator is a set of Super Cells that form a subset of the denominator Super Cells:

$$f_{\text{core}} = \frac{E^{(2)}_{\text{T,small area}}}{E^{(2)}_{\text{T,large area}}}\,, \tag{4}$$

where the sizes of the small and large areas were optimized to achieve maximum rejection power. Typical values used are: $\Delta\eta \times \Delta\phi = 0.175 \times 0.1$ for the small area and $\Delta\eta \times \Delta\phi = 0.275 \times 0.3$ for the large area.

EM Radius The EM radius variable R_{EM} takes advantage of the distribution of the Super Cells in the cluster, weighted as a function of their energy:

$$R_{\text{EM}} = \frac{\sum\limits_{\text{area}} E^{(2)}_{\text{T}} \times \sqrt{(\eta_{\text{SuperCell}} - \eta_{\text{cluster}})^2 + (\phi_{\text{SuperCell}} - \phi_{\text{cluster}})^2}}{\sum\limits_{\text{area}} E^{(2)}_{\text{T}}}\,, \tag{5}$$

where — similar to the variable f_{core} — the size of the area was optimized to achieve maximum rejection power within an area of $\Delta\eta \times \Delta\phi = 0.4 \times 0.4$.

The minimum Super Cell transverse energy entering these variable definitions was also optimized, and the optimal value was found to be 1 GeV. The background rejection for each of these variables is shown in Fig. 12.

The current Level-1 trigger system employs an EM isolation variable, which uses an isolation ring in the middle layer of the EM calorimeter to reject events with significant energy outside the tau

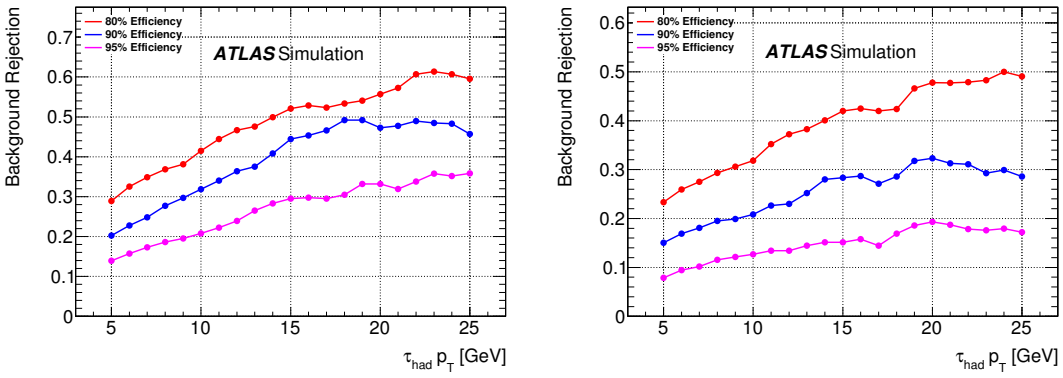


Figure 12. The background rejection corresponding to 80%, 90% and 95% τ_{had} efficiencies for the f_{core} (a) and EM radius (b) variables, optimized as a function of the τ p_{T}.

cluster core. However, the background rejection using this variable was only 12% for 15 GeV τ_{had} candidates in Run 1, and a similar performance is expected in Run 2.

The increased granularity provided by the Super Cells gives a significant additional rejection of the background even with only one additional variable. Using the variable f_{core} alone, a rejection of nearly 50 % can be achieved with a 90 % efficiency for 25 GeV τ_{had} objects. Studies are ongoing to optimize the performance combining several variables and using the most important physics channels as benchmarks.

2.2.3 Jet trigger performance

The high-luminosity environment in Run 3 and beyond will pose new challenges to jet reconstruction and identification at the trigger level.

Offline jets in ATLAS are reconstructed from three-dimensional locally calibrated (LCW) clusters [12] of calorimeter cells using the anti-k_{t} recombination algorithm [13]. The noise used in the clustering algorithm is the sum in quadrature of the electronics noise and pileup noise ($\sigma_{\text{noise}}^{\text{pile-up}}$). For these studies, $\sigma_{\text{noise}}^{\text{pile-up}}$ is recomputed for each $\langle\mu\rangle$ value. The median p_{T} density in an area corresponding to the jet size is used in ATLAS [14] to subtract the pileup contribution to each offline jet p_{T}, as proposed originally in Ref. [15].

Significantly increased in-time and out-of-time pileup collisions will lead to a dramatically larger event activity than in Run 1, as shown in Fig. 13 (a) for the event-by-event median p_{T} density ($\langle\rho\rangle$) as a function of the mean number of interactions per bunch crossing. Without a pileup subtraction procedure applied to jet reconstruction, this increased energy per event would result in a linear growth of the multiplicity of jets produced from pileup collisions as a function of the number of vertices (N_{vtx}), as shown in Fig. 13 (b). A direct consequence of the increased jet multiplicity from pileup is the increase in overall jet trigger rates, which would reduce the efficiency for high-p_{T} jets of interest from hard scattering due to the limited trigger bandwidth, unless pileup is already subtracted in the Level-1 trigger. In the following, jet reconstruction algorithms expected to be robust against pileup and which can be implemented in the upgraded ATLAS trigger system are discussed.

The jet simulation studies presented in this section use Trigger Towers reconstructed from Super Cells (cells) in the LAr (Tile) calorimeters as the input to jet reconstruction algorithms within $|\eta| < 2.5$. The current Level-1 jet trigger is simulated by forming jet elements of the size $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$

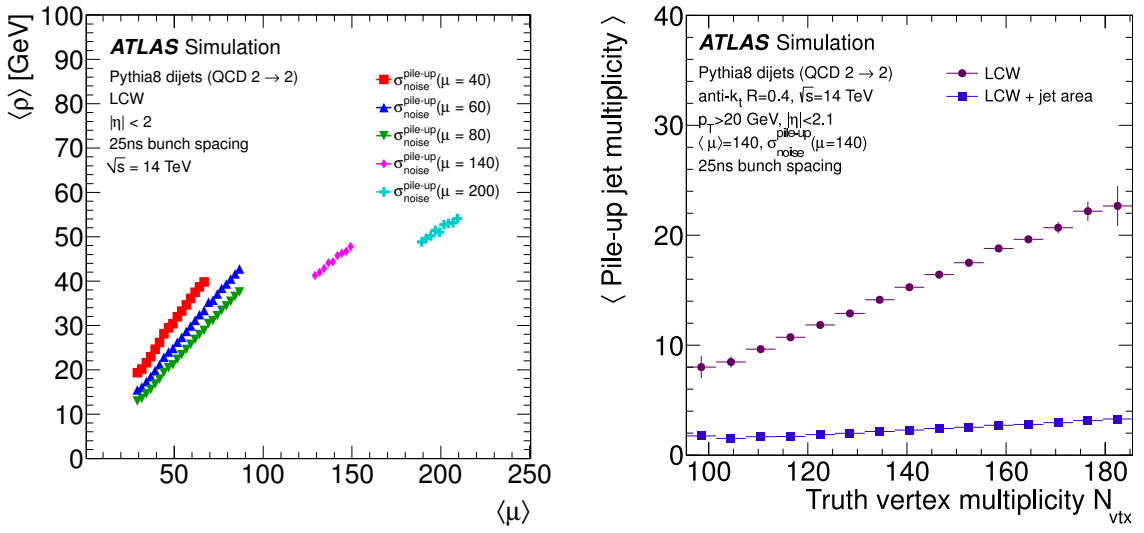


Figure 13. (a) Event-by-event median p_{T} density as a function of the mean number of interactions per bunch crossing in simulated dijet events for $R = 0.4$ jets. For each choice of pileup noise ($\sigma_{\mathrm{noise}}^{\text{pile-up}}$), the dependence is approximately linear. (b) Average number of jets ($p_{\mathrm{T}} > 20$ GeV and $|\eta| < 2.1$) reconstructed as a function of the number of true (i.e. from the Monte Carlo generator record) vertices in a simulated dijet sample with $\langle\mu\rangle = 140$. The upper (lower) curve corresponds to the distribution before and after pileup subtraction using an event-by-event p_{T} density.

from the Trigger Towers and running a sliding window algorithm. The sliding window comprises 4×4 jet elements, covering an area of $\Delta\eta\times\Delta\phi = 0.8\times0.8$. The studies presented in the following profit from the finer quantization of the Super Cell energies and make use of global event quantities for pileup suppression which could be calculated in the proposed L1Calo global FEX [4] and applied in the Level-1 topological processor planned for Run 2. The exact implementation of the algorithms presented will need to be worked out in detail. The expected performance results will depend on this technical implementation. The studies here are based on reasonable assumptions which will be verified once the full design is complete.

2.2.3.1 Inclusive Jet and Multijet Trigger Performance The improved energy resolution of the LAr calorimeter upgraded trigger electronics allows for an improvement in the energy resolution of jets reconstructed in the Level-1 trigger system. Figure 14 compares the trigger efficiency as a function of the highest p_{T} jet in QCD dijet events between the current and the upgraded systems for a Level-1 jet threshold of 20 GeV. The performance of the Super Cell-based algorithm is comparable to that of the current system in a low pileup environment ($\langle\mu\rangle = 20$), but a clear improvement in the steepness of the turn-on curves is seen in a high pileup environment ($\langle\mu\rangle = 80$) when an algorithm based on Super Cells is used.

The upgraded electronics can also improve the efficiency for triggering on events with many jets (multijet events). This study investigates a particular jet clustering algorithm, called a Gaussian filter

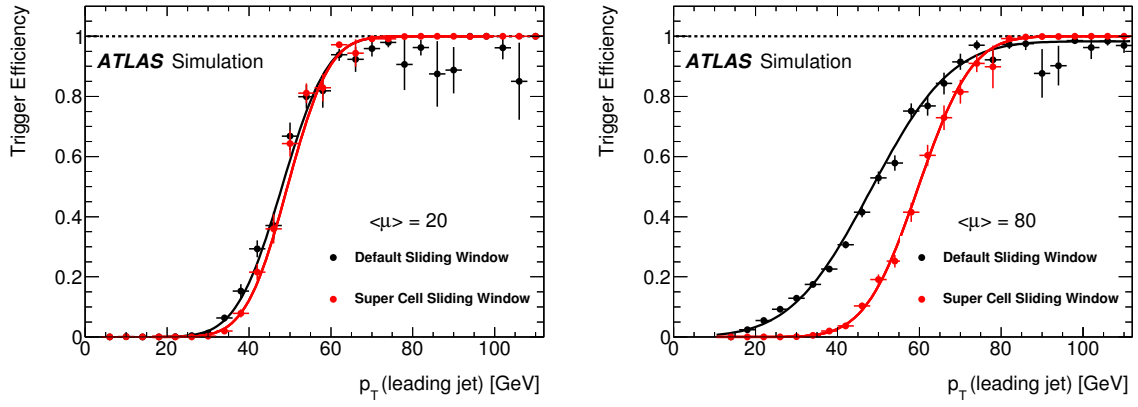


Figure 14. The trigger efficiency as a function of the highest p_{T} offline jet for $\langle\mu\rangle = 20$ (a) and $\langle\mu\rangle = 80$ (b) in simulated QCD dijet events. The performance of the default sliding window algorithm (black points) is compared to that of the sliding window algorithm based on Super Cells (red points) for jets within $|\eta| < 2.5$.

algorithm, that has been used to reconstruct heavy ion collision events in the PHENIX experiment at RHIC [16]. As shown in Fig. 15, the present Level-1 jet trigger system based on the sliding window algorithm displays an inefficiency for multijet triggers at the plateau region, mainly caused by a limited capability to separate jets produced in close proximity to one another. This effect is especially illustrated in $Z' \rightarrow t\bar{t}$, where the top quarks are Lorentz-boosted and their decay products are close together. The default algorithm is compared to the anti-k_{t} algorithm with a distance parameter of $R = 0.4$ that is used in ATLAS for offline jet reconstruction. Results are also shown for a Gaussian filter algorithm where the value of the standard deviation ($\sigma = 0.1$) is chosen to optimize the jet separation. In contrast to the default sliding window algorithm, the jets reconstructed with the Gaussian filter reach full efficiency in the plateau region and therefore will help to recover current inefficiencies of multijet triggers. Such an algorithm can only be applied to a Level-1 jet trigger based on Super Cells.

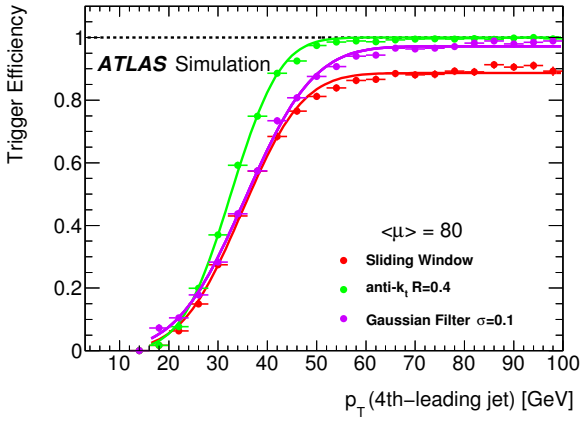
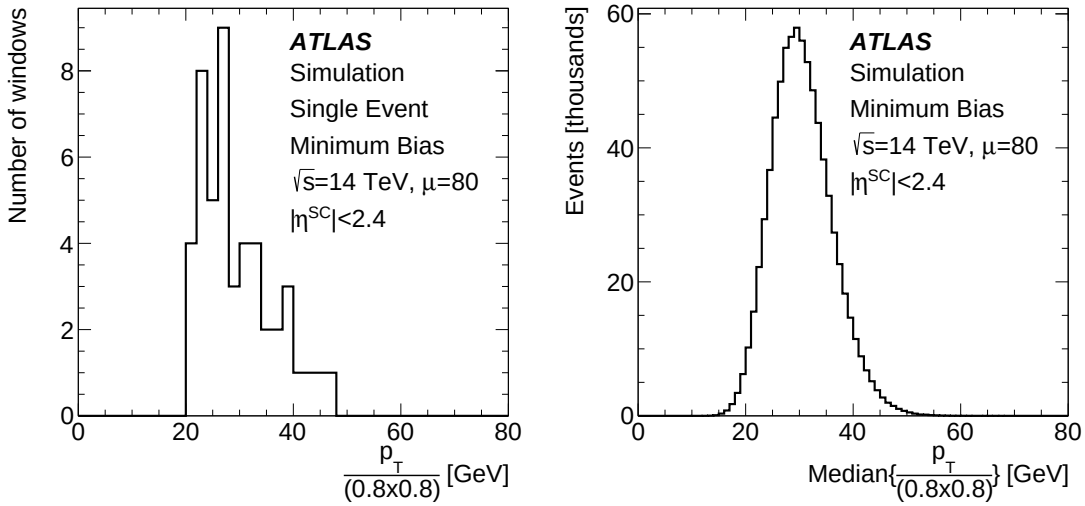


Figure 15. The trigger efficiency as a function of the fourth-highest p_{T} offline jet for $\langle\mu\rangle = 80$ in simulated $Z' \rightarrow t\bar{t}$ events. The Level-1 jet thresholds require four jets with $p_{\mathrm{T}} > 20$ GeV. The default sliding window algorithm (red points) is compared to a Gaussian filter algorithm (purple points) and the anti-k_{t} algorithm (green points) for jets within $|\eta| < 2.5$.

2.2.3.2 Pileup subtraction The effects of event-by-event energy fluctuations due to pileup can be mitigated by estimating the median p_{T} density at the trigger level. The pileup subtraction method discussed in this section is inspired by the offline p_{T} density, ρ. The initial step of the method divides the detector into large 0.8×0.8 windows in the $\eta \times \phi$ plane. Subsequently, the p_{T}'s of all Super Cells contained in these windows are summed across η, ϕ, and layer. The resulting summed p_{T} distribution for one event is shown in Fig. 16(a). It is expected that pileup interactions cause an overall increase in energy deposition across windows while high p_{T} objects would only appear in a few windows. To estimate the pileup contribution excluding high p_{T} objects, the median of the window p_{T} distribution is computed for each event.

As a cross-check, the median $\left\{\frac{p_{\mathrm{T}}}{0.8\times0.8}\right\}$ is compared to the ρ variable used in the offline pileup corrections in Fig. 17. A linear correlation between these two quantities is observed. To quantify the effectiveness of this procedure in suppressing fake jets from pileup, the method is tested using offline jets with $p_{\mathrm{T}} > 20$ GeV from a simulated minimum bias sample with $\langle\mu\rangle = 80$. The p_{T}s of the jets are corrected by subtracting the median$\left\{\frac{p_{\mathrm{T}}}{0.8\times0.8}\right\} \times \pi R^2$, where R is the anti-k_{t} radius. The corrected jet multiplicity is then taken as the number of jets with $p_{\mathrm{T}} > 20$ GeV after subtraction. Figure 18 shows that the jet multiplicity is stable as a function of the number of reconstructed vertices (N_{PV}) for $R = 0.4$ and $R = 1.0$ anti-k_{t} jets after the described pileup subtraction procedure is applied. These are studied in simulated minimum bias events, for which ~ 1 (~ 0) anti-k_{t} jets with $R = 0.4$ ($R = 1.0$) and $p_{\mathrm{T}} > 20$ GeV are expected from the mean number of ρ-corrected offline jets. This pileup suppression has the potential to reduce the jet rates in the Level-1 trigger by a large fraction, freeing bandwidth for other triggers or lower thresholds.



(a) $\frac{p_{\mathrm{T}}}{0.8\times0.8}$ for a single event

(b) Median of $\frac{p_{\mathrm{T}}}{0.8\times0.8}$

Figure 16. (a) Distribution of the transverse energy density in calorimeter windows of size 0.8×0.8, $\frac{p_{\mathrm{T}}}{0.8\times0.8}$, for a single event in the simulated $\langle\mu\rangle = 80$ minimum bias sample. (b) Median$\left\{\frac{p_{\mathrm{T}}}{0.8\times0.8}\right\}$ distribution for a sample of minimum bias events with $\langle\mu\rangle = 80$.

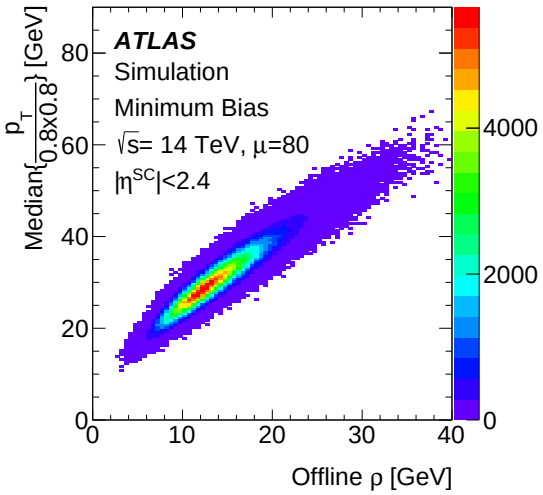


Figure 17. The correlation between the offline energy density variable ρ and the median$\left\{\frac{p_{\mathrm{T}}}{0.8\times0.8}\right\}$ variable to be used in the upgraded Level-1 trigger system.

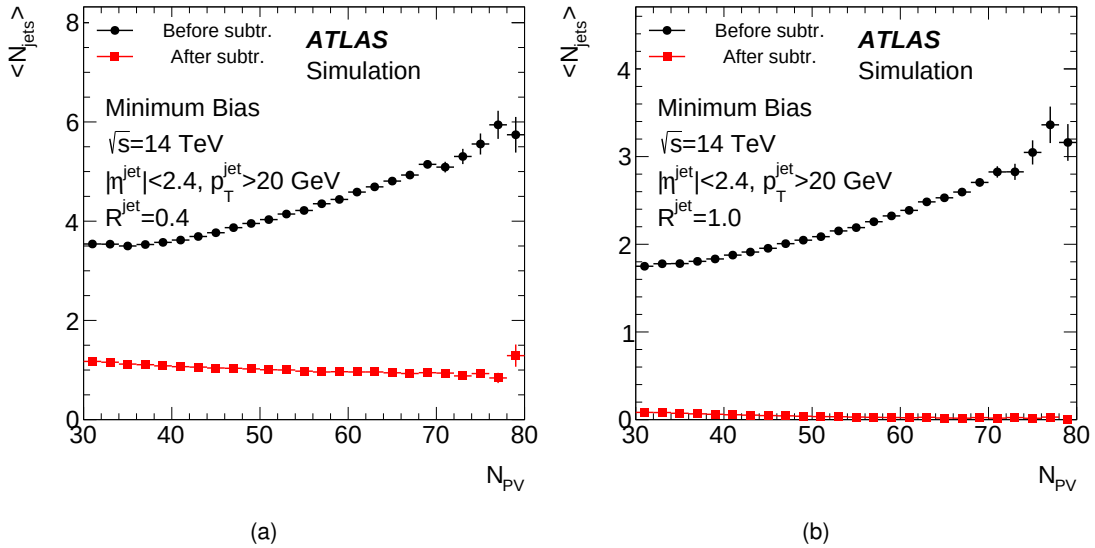


Figure 18. The average number of anti-k_{t} jets with $R = 0.4$ (a) and $R = 1.0$ (b) before and after pileup subtraction, as a function of the number of reconstructed vertices.

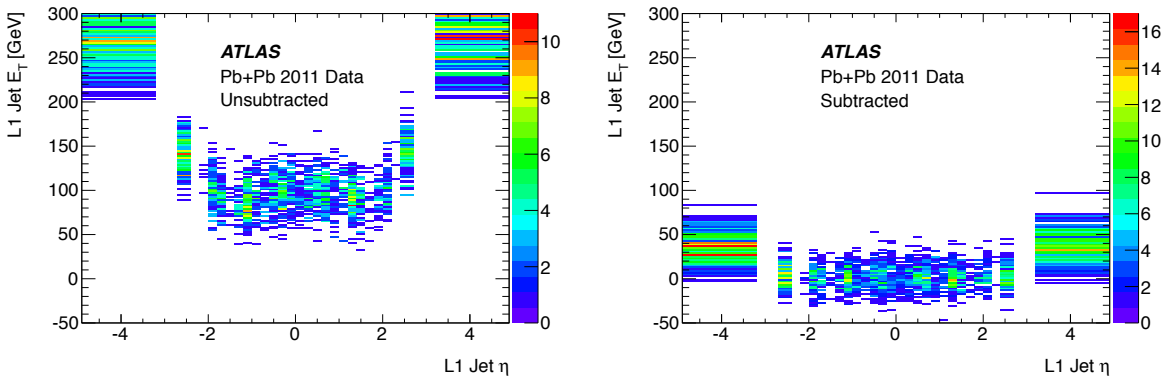


Figure 19. Level-1 transverse energy of jet elements measured in the minimum-bias Pb-Pb data, as a function of the Level-1 jet η: (a) before subtraction (where the underlying event pedestal is clearly observed) and (b) after subtraction using the unbiased average transverse energy in each $\Delta\eta = 0.2$ slice.

2.2.4 Trigger performance in heavy ion events

One important application of the L1Calo global feature extractor is to allow a baseline subtraction in heavy ion collisions which minimizes the impact of the underlying event on jet triggers. In general, the underlying event fluctuations are quite large from event to event, due to the selection of a random impact parameter between the two lead (Pb) nuclei. In the 10% most central events, a typical jet cone of size $R = 0.4$ in an event without a jet can contain between 60 and 100 GeV. Thus, at high luminosity, the fluctuation tails can lead to a substantial rate of spurious Level-1 jet triggers, which would far exceed the high-level trigger input rate. Furthermore, heavy ion collisions with high centrality are very similar to extremely high pileup events of p-p collisions and provide an opportunity to test algorithms that the Level-1 trigger system can benefit from during p-p running. Figure 19 (a) shows the distribution of transverse energies as a function of Level-1 jet η for the $0-10\%$ most central events from ATLAS Pb-Pb data recorded in 2011. Nearly every Level-1 jet is above 50 GeV.

In the standard heavy ion reconstruction, a sophisticated iterative procedure has been established that subtracts out both the average pedestal and the elliptic modulation which is generally understood to be the effect of collective expansion of the hot, dense system. This modulation is especially large in more peripheral events where the initial geometry of the colliding nucleons is well known to be highly anisotropic. While this entire procedure has been implemented in the high-level trigger and was used successfully in the 2011 HI run, the high-level trigger bandwidth limited the Level-1 input rate to 3 kHz. In Run 3, rates on the order of $25-50$ kHz are expected.

Studies are underway on the possible implementation and performance of less-sophisticated algorithms at Level-1, which could remove the spurious rate from underlying event fluctuations without substantially impacting real jets. The most natural first attempt involves simply calculating, in each event, the unbiased average of the jet element transverse energies in slices of size $\Delta\eta = 0.2$ and then subtracting these energies from each Level-1 jet. This procedure is straightforward for Level-1 jets in $|\eta| < 2.4$ where the jet elements are a uniform grid. Progress on handling the forward jets is currently underway and will continue after the submission of this report. The Level-1 jet triggers are simulated by determining whether any of the subtracted Level-1 jets satisfies the nominal threshold after the pedestal subtraction. This is done assuming the improved energy resolution of the Level-1 system.The results are illustrated in Fig. 19 (b), which shows the Level-1 jet transverse energies as a

function of η for the 10% most central minimum-bias events. In the central region the large pedestal and η structure of the jet energies has been removed. Typical rate reductions are a factor of 1.7 for jets with $p_{\mathrm{T}} > 20$, a factor of 3.7 for jets with $p_{\mathrm{T}} > 30$ and a factor of about 60 for jets with $p_{\mathrm{T}} > 50$.

2.2.5 $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger performance

The missing transverse momentum ($E_{\mathrm{T}}^{\mathrm{miss}}$) trigger is designed to select events with weakly interacting particles, such as neutrinos or predicted new particles like the lightest supersymmetric particles (LSP). The $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger is crucial, for example, for Higgs boson studies in the $ZH \to \nu\bar{\nu}b\bar{b}$ channel, and R-parity conserving supersymmetry searches. The total transverse energy (ΣE_{T}) trigger is designed to select events with significant transverse energy due to hard scattering processes.

In order to cope with the severe pileup conditions expected after the Phase-I upgrade, two event-by-event approaches to suppressing the impact of pileup on the $E_{\mathrm{T}}^{\mathrm{miss}}$ triggers are investigated. Both rely on the better energy resolution provided by the LAr electronics upgrade. In addition, the η-slice-based pileup subtraction can be computed in the proposed L1Calo global FEX [4] and the layer-based pileup subtraction method takes advantage of the additional layer information provided by the Super Cells.

The first 12 bunch crossings in each LHC bunch train are excluded from these studies since they are disproportionately sensitive to pileup effects and, left untreated, would dominate the trigger rate.

2.2.5.1 η slice-based pileup subtraction The concept of η slice-based pileup subtraction was initially developed in the context of jet reconstruction in ATLAS heavy-ion studies [17], as presented in Sec. 2.2.4, where the energy density is determined as described above in η-slice bins, event-by-event, and subtracted from each jet. This strategy is investigated here for the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger in order to suppress the in-time pileup and possibly some contributions from the out-of-time pileup.

For this event-by-event determination of the pileup contribution, the Super Cells are formed into $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ Super Cell Towers up to $|\eta| < 3.2$ and $\Delta\eta \times \Delta\phi = 0.4 \times 0.4$ for $3.2 < |\eta| < 4.9$. The proposed granularity of the global FEX is $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$. Slices in η (with size $\Delta\eta = 0.2$ or 0.4) are formed, and the median E_{T} in each slice is computed. The median of the E_{T} distribution in each slice is considered instead of the mean, since the latter could shift due to large energy deposits from particles produced in the hard scattering process. Figure 20 shows the mean and RMS of the EM and hadronic E_{T} in each η-slice before and after this subtraction. The $E_{\mathrm{T}}^{\mathrm{miss}}$ is computed for all summed Super Cell Towers within $|\eta| < 4.9$.

Figure 21 (a) shows the impact of the event-by-event pileup subtraction on the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ distributions in simulated minimum bias events. This simulated sample is also used to determine the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger rate shown in Fig. 21 (b). A cross-check was performed by applying this method to simulated $ZH \to \nu\bar{\nu}b\bar{b}$ events (with intrinsic $E_{\mathrm{T}}^{\mathrm{miss}}$); the resolution of the η-slice-subtracted $E_{\mathrm{T}}^{\mathrm{miss}}$ was found to be comparable with the current Level-1 trigger $E_{\mathrm{T}}^{\mathrm{miss}}$ performance.

This method shows a dramatic suppression of the trigger rate (by a factor of 10) that would not be possible without the LAr Phase-I upgrade. Much of the gain is in the forward region of the calorimeter, where the E_{T} deposition due to pileup is the largest.

2.2.5.2 Layer-based pileup suppression An important feature of the Super Cells is the layer information that is transmitted to the Level-1 FEXs. The following study exploits this information by examining the energy deposition in the middle layer of the EM calorimeter and comparing this energy to the expected noise:

$$E_{\mathrm{thr}} = 3 \times \left(\sigma_{\text{electronics noise}} \oplus \sigma_{\text{pileup noise}} \right), \tag{6}$$

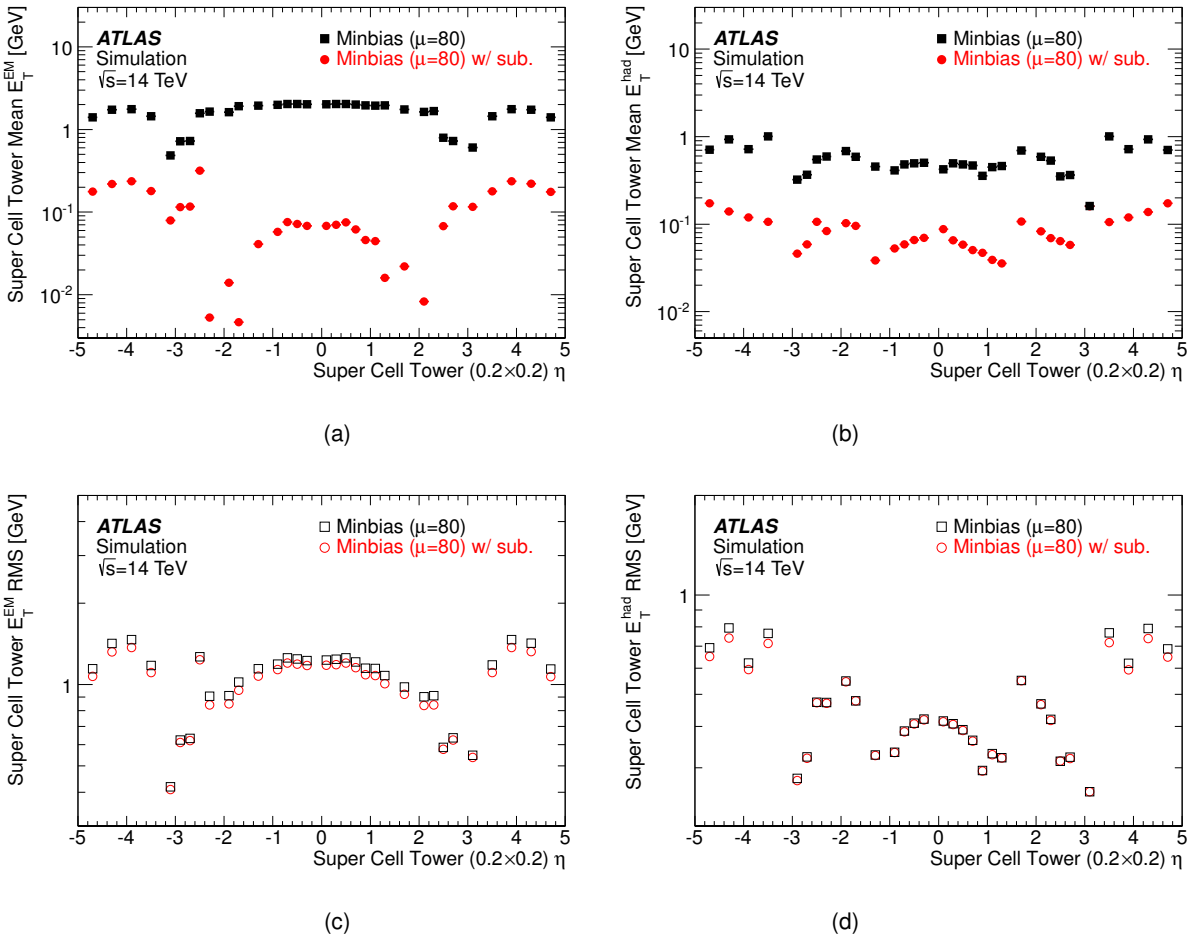
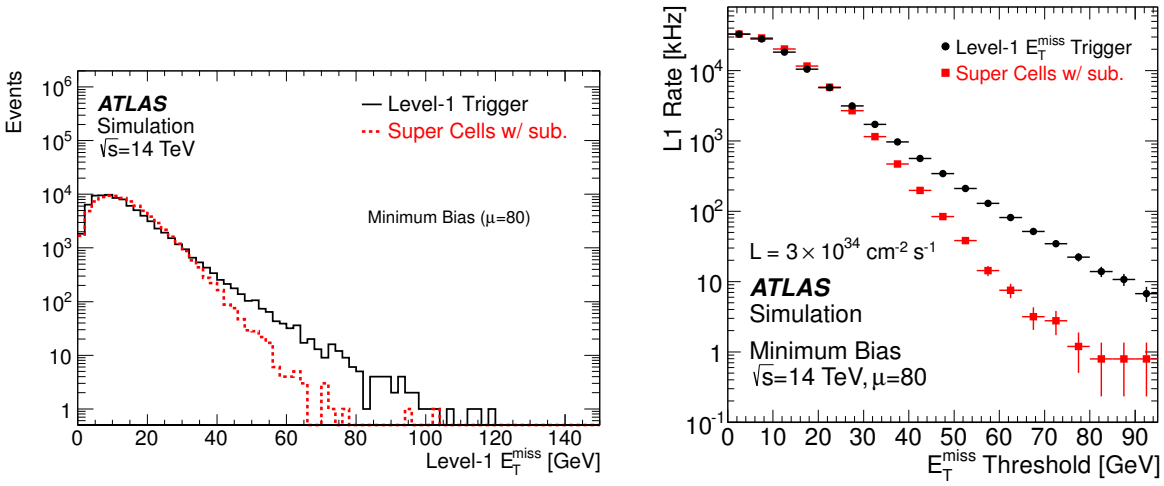


Figure 20. The mean (a) and RMS (c) EM E_{T}, and the mean (b) and RMS (d) hadronic E_{T} deposited in η-slices of size 0.2 before (black points) and after (red points) event-by-event pileup subtraction. Events are from a simulated sample with $\langle\mu\rangle = 80$, and the first 12 bunch crossings in each LHC bunch train are excluded.



(a) (b)

Figure 21. (a) Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ distribution with (red lines) and without (black lines) the 0.2 η-slice-based pileup subtraction. (b) The Level-1 trigger rate for the current $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger (black points) compared to the trigger rate after the η-slice subtraction (red points). The $E_{\mathrm{T}}^{\mathrm{miss}}$ is determined within $|\eta| < 4.9$, and the first 12 bunch crossings in each LHC bunch train are excluded.

Table 4. Noise values $\left(\sigma_{\text{electronics noise}} \oplus \sigma_{\text{pileup noise}}\right)$ for $\langle\mu\rangle = 80$ used to compute the threshold for the middle layer of each Super Cell as described in Eqn. 6. The Super Cell granularity changes in the regions $2.5 < |\eta| < 3.0$ and $|\eta| > 4.0$ (see Appendix A).

$\lvert\eta\rvert$	$0-0.5$	$0.5-1.5$	$1.5-2$	$2-2.5$	$2.5-3$
Noise [GeV]	0.36	0.40	0.60	1.00	0.50
$\lvert\eta\rvert$	$3-3.2$	$3.2-3.3$	$3.3-3.4$	$3.4-3.5$	$3.5-3.8$
Noise [GeV]	0.8	1.0	2.0	3.5	5.0
$\lvert\eta\rvert$	$3.8-4.0$	$4.00-4.15$	$4.15-4.30$	$4.3-4.6$	$4.6-4.9$
Noise [GeV]	8	10	20	10	15

where $\sigma_{\text{electronics noise}}$ is the electronics noise. Typical total noise values are shown in Fig. 6 for $\langle\mu\rangle = 80$ and $\langle\mu\rangle = 140$.

Figure 22 illustrates the impact of a simple layer-based pileup suppression scheme. If the middle layer (2) of each Super Cell passes the criteria $E > E_{\text{thr}}$, then the energy from the entire Trigger Tower is added to the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ sum. The noise values used for each Super Cell as a function of η are shown in Table 4. These values were derived from the linear sum of the noise for each cell in Fig. 6 (a).

This strategy was also tested on a $ZH \rightarrow \nu\bar{\nu}b\bar{b}$ sample with true $E_{\mathrm{T}}^{\mathrm{miss}}$ due to the neutrinos in the final state, and good agreement was found between the $E_{\mathrm{T}}^{\mathrm{miss}}$ computed at Level-1 with the layer-based pileup subtraction and the true $E_{\mathrm{T}}^{\mathrm{miss}}$. The Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger rate with the layer-based pileup subtraction as a function of $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold is plotted in Fig. 22 (b).

The results from these studies indicate that the $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold could be lowered to at least 70 GeV in Run 3 while keeping the same bandwidth as the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold of 90 GeV in Run 2. This substantial decrease of the $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold translates into an increase of acceptance for

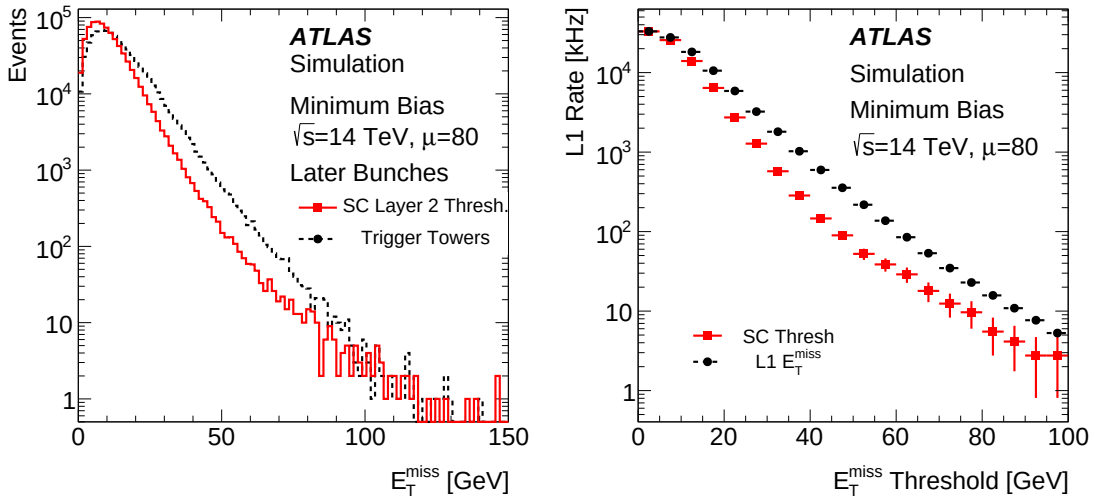


Figure 22. (a) Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ distribution for the Trigger Towers with no pileup subtraction (black, dashed) and for the Super Cell layer-based pileup subtraction scheme (red, solid). (b) The Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger rate obtained by using the Super Cell layer-based pileup subtraction as a function of the online $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold. For both subfigures, the Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ is determined within $|\eta| < 4.9$, and the first 12 bunch crossings of the train are excluded.

SUSY searches and Higgs physics, as discussed in Sec. 2.3 with a few examples.

2.2.6 Expected trigger rates

The expected trigger rates are summarized in Table 5, which is adapted from the concurrent ATLAS TDAQ Phase-I Upgrade Technical Design Report [4]. The third column of the table shows a possible trigger menu for Run 3 assuming the full ATLAS Phase-I upgrade program is realized. The decrease of trigger thresholds of EM, τ, jet, and $E_{\mathrm{T}}^{\mathrm{miss}}$ objects between the second (Run 2) and third (Run 3) column is the result of the performance improvements of the LAr Level-1 trigger due to the upgrade proposed in this TDR.

It should be noted that not all possible performance improvements discussed in the previous sections have been taken into account; there are therefore good reasons to believe that the final thresholds could be lower than those listed in the table. The final trigger menu for LHC Run 3 will be developed in the future, based on the experience gained in Run 2 and on the understanding of the physics requirements at the time of LS2; it can therefore differ substantially from the one given here for illustration. The menu in Table 5 is nevertheless used in Sec. 2.3 as a guideline to demonstrate, with a few examples, the impact of the LAr Phase-I upgrade on the ATLAS physics potential in Run 3.

Run 1	Offline p_{T} Threshold [GeV]	Rate [kHz]	Run 2	Offline p_{T} Threshold [GeV]	Rate [kHz]	Run 3	Offline p_{T} Threshold [GeV]	Rate [kHz]
EM18VH	25	130	EM30VHI	38	14	EM25VHR	32	14
EM30	37	61	EM80	100	2.5	EM80	100	2.5
2EM10	2x17	168	2EM15VH I	2x22	2.9	2EM12VHR	2x19	5.0
EM total		**270**			**18**			**20**
MU15	25	150	MU20	25	28	MU20	25	15
2MU10	2x12	14	2MU11	2x12	4.0	2MU11	2x12	4.0
Muon total		**164**			**32**			**19**
EM10VH_MU6	17,6	22	EM15VH_MU10	22,12	3.0	EM10VHR_MU10	17,12	3.0
			EM10H_2MU6	17,2x6	2.5	EM10HR_2MU6	17,2x6	1.0
TAU40	100	52	TAU80V	180	4.7	TAU80VR	180	3.2
			2TAU50V	2x110	3.8	2TAU40VR	2x100	3.9
2TAU11I_TAU15	30,40	147	2TAU20VI_3J20	2x50,60	5.2	2TAU15VR_3J15	2x40,50	8.1
2TAU11I_EM14VH	30,21	60	2TAU20VI_ EM18VHI_3J18	50,25,60	2.8	2TAU15VR_ EM13HR_3J13	40,20,50	3.3
			TAU15VI_MU15	40,20	3.8	TAU11VR_MU11	35,12	6.4
TAU15_XE35	40,80	63	TAU20VI_ XE40_3J20	50,90,60	4.4	TAU15VR_ XE40_3J15	40,90,50	5.0
Tau total		**238**			**20**			**25**
J75	200	34	J100	200	7.0	J100	200	7.0
4J15	4x55	87	4J25	4x60	3.3	4J25	4x60	3.3
			J75_XE40	150,150	8.3	J75_XE40	150,150	8.3
XE40	120	157	XE90	250	10	XE70	200	13
Jet/$E_{\mathrm{T}}^{\mathrm{miss}}$ total		**306**			**25**			**25**
Topological triggers		**-**			**~5**			**~20**
Total		**~800**			**~100**			**~100**

Table 5. Examples of Level-1 trigger menus for various running configurations for a luminosity of 3×10^{34} cm^{-2} s^{-1} (adapted from Ref. [4]). The column labeled Run 1 corresponds to the menu used at the end of 2012 at $\sqrt{s} = 8$ TeV (scaled to a luminosity of 3×10^{34} cm^{-2} s^{-1}). The columns labeled Run 2 give the expected menu for $\sqrt{s} \sim 14$ TeV after LS1. The columns labeled Run 3 illustrate a possible menu for $\sqrt{s} \sim 14$ TeV after the Phase-I upgrade is completed at the end of LS2. The first letters indicate the object type (EM for electrons and photons, MU for muons, TAU for τ leptons, J for jets, and XE for $E_{\mathrm{T}}^{\mathrm{miss}}$), the following numbers the transverse energy threshold, numbers preceding the object letters give the object multiplicity, and the final letters indicate the isolation requirements. The letter R indicates the R_η and f_{core} variables made possible by the upgrade. The offline thresholds typically correspond to the point at which the trigger turn-on curve reaches $90-95\%$ of its plateau value. The items listed in the table assume no overlap removal. For example, in the item 2TAU20I_3J20, it is assumed that both τ candidates will also cause jet triggers if they pass the 20 GeV τ p_{T} requirement and, additionally, the 20 GeV jet p_{T} requirement. The topological triggers are described in Ref. [4].

2.3 Impact on physics

The Level-1 ATLAS trigger system must be extremely robust to fulfill the mission of a broad ATLAS physics program at luminosities up to 3×10^{34} cm^{-2} s^{-1}. The proposed Phase-I upgrade is essential to allow flexibility in the system despite the high pileup environment.

The trigger performance results shown in the previous section are applied here to a crucial component of the physics program at the upgraded LHC, namely studies of the Higgs boson. Given that the Higgs boson is light, maintaining low trigger thresholds on the physics objects into which it decays is mandatory in order to measure as many of its properties as possible with the highest precision. In addition, the ability to trigger on low-p_{T} single leptons provides a very effective trigger for a wide range of possible new physics signatures.

2.3.1 Higgs physics

2.3.1.1 $H \to \tau\tau$ For Higgs boson decays to τ leptons, vector boson fusion (VBF) production provides a distinct experimental signature due to the additional forward jets present in the final state. This study examines the case where one τ lepton decays leptonically (in particular to an electron) and the other decays hadronically. Signal events consist of one isolated electron, one τ_{had} candidate, two jets, and $E_{\mathrm{T}}^{\mathrm{miss}}$. The trigger that can record these events is either a single electron trigger or a multi-object trigger such as an electron + τ_{had} or an electron + τ_{had} + jet trigger. Since the electron is a decay product of the τ lepton, its p_{T} tends to be soft. The p_{T} distributions of both the electrons and τ leptons are shown in Fig. 23. The offline selection criteria from Table 5 achievable with the proposed LAr Phase-I upgrade (electron $p_{\mathrm{T}} > 20$ GeV and τ_{had} $p_{\mathrm{T}} > 40$ GeV) as well as those assuming Run 2 conditions (electron $p_{\mathrm{T}} > 25$ GeV and τ_{had} $p_{\mathrm{T}} > 50$ GeV) are indicated with dashed lines on the plots.

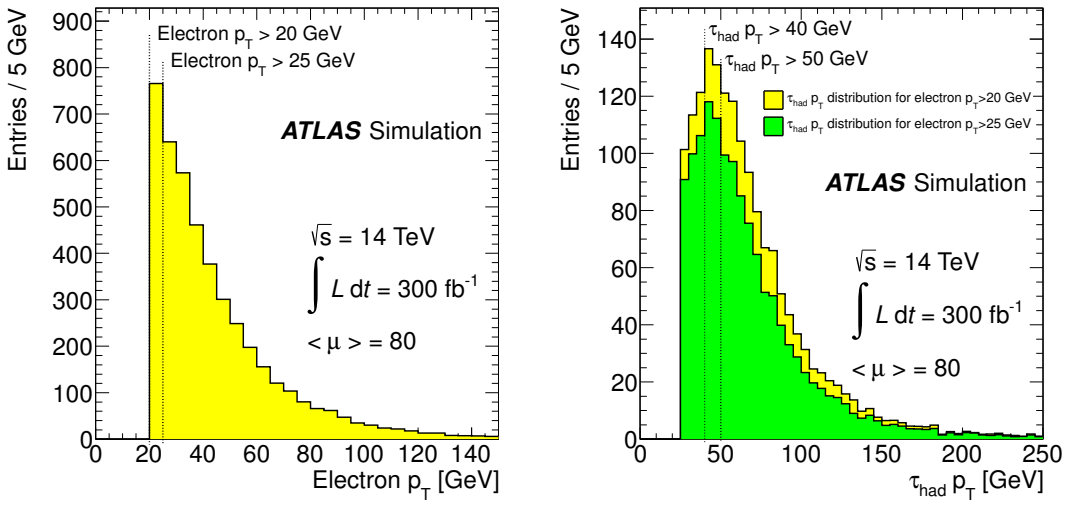


Figure 23. The electron p_{T} distribution (a) and τ p_{T} distribution after applying the requirement electron $p_{\mathrm{T}} > 20$ GeV (yellow) and electron $p_{\mathrm{T}} > 25$ GeV (green) (b) for simulated $H \to \tau\tau$ events where one τ decays to an electron plus neutrinos, while the other τ decays hadronically. The distributions are normalized to the expected numbers of events for $300\,\mathrm{fb}^{-1}$.

This study assumes $\sqrt{s} = 14$ TeV p-p collisions at the LHC with $300\,\mathrm{fb}^{-1}$ of integrated luminosity

and $\langle\mu\rangle = 80$. Generator-level Monte Carlo events are used with parameterized efficiencies and smearing applied to model the expected detector performance under high pileup conditions.

Table 6 illustrates the impact of various trigger selection criteria. It can be seen that raising the p_{T} requirement for the electron candidate (from 20 GeV to 25 GeV) and for the τ_{had} candidate (from 40 GeV to 50 GeV) translates into a decrease of the signal acceptance by 37%. The loss of acceptance observed when applying all other selection criteria that are used in the analysis of the Run 1 data but with the above higher thresholds for the electron and τ p_{T} is very similar. For this channel, which requires the identification of a relatively low-p_{T} τ_{had} candidate, the impact of the proposed LAr Phase-I upgrade is significant.

Trigger Requirement	$p_{\mathrm{T}}(e) > 20$ GeV $p_{\mathrm{T}}(\tau) > 40$ GeV	$p_{\mathrm{T}}(e) > 25$ GeV $p_{\mathrm{T}}(\tau) > 50$ GeV
Electron selection efficiency	$(25.4 \pm 0.2)\,\%$	$(21.0 \pm 0.2)\,\%$
Electron and tau selection efficiency	$(7.5 \pm 0.1)\,\%$	$(4.7 \pm 0.1)\,\%$
Relative acceptance	1	0.631 ± 0.015

Table 6. Efficiency of electron p_{T} and τ p_{T} selections for VBF $H \to \tau\tau$ events in which one τ decays into an electron and neutrino and the other τ decays hadronically. The last row shows the acceptance loss when raising the electron p_{T} selection from 20 to 25 GeV and the τ p_{T} selection from 40 to 50 GeV.

2.3.1.2 $H \to b\bar{b}$ in associated $(W/Z)H$ production In the Standard Model, the $H \to b\bar{b}$ decay mode is predicted to have the largest branching fraction (58 %) for $m_H = 125$ GeV [18]. An inclusive search for $H \to b\bar{b}$ is not feasible at hadron colliders because of the overwhelming background from multijet production. Associated production of a Higgs boson with a vector boson, W or Z, offers a viable alternative because leptonic decays of the vector boson, $W \to \ell\nu$, $Z \to \ell^+\ell^-$ ($\ell = e,\mu$), and $Z \to \nu\nu$, can be efficiently used for triggering and background reduction purposes. The Monte Carlo simulated samples produced for the analysis of 2012 ATLAS data [19] have been used to estimate the signal significance for different lepton and $E_{\mathrm{T}}^{\mathrm{miss}}$ selection criteria. Even though this study uses pileup conditions experienced during the 2012 data taking period, the results yield an indication of the loss in signal acceptance and significance when raising the selection thresholds without including the impact of systematic uncertainties. In [19], the samples are split into three categories: 0-lepton, 1-lepton and 2-lepton. In this section, the impact of higher $E_{\mathrm{T}}^{\mathrm{miss}}$ and electron p_{T} thresholds for the 0-lepton category is briefly discussed.

The signal for the 0-lepton category is dominated by $ZH \to \nu\nu b\bar{b}$ decays and relies on the $E_{\mathrm{T}}^{\mathrm{miss}}$ trigger. For the 2012 data, the offline event selection includes the requirement $E_{\mathrm{T}}^{\mathrm{miss}} > 120$ GeV, corresponding to $\sim 85-90\%$ trigger efficiency. The higher Level-1 $E_{\mathrm{T}}^{\mathrm{miss}}$ thresholds outlined in Table 5 will require raising the offline requirement to $E_{\mathrm{T}}^{\mathrm{miss}} > 200$ GeV assuming Run 2 conditions[3]. With the proposed LAr Phase-I upgrade, however, an offline requirement of $E_{\mathrm{T}}^{\mathrm{miss}} > 160$ GeV can be achieved. This increase will reduce the signal acceptance, compared to the present analysis, by 47 % (for $E_{\mathrm{T}}^{\mathrm{miss}} > 160$ GeV) and 72 % (for $E_{\mathrm{T}}^{\mathrm{miss}} > 200$ GeV), respectively. The background is dominated by $t\bar{t}$ and $Zb\bar{b}$, and is also reduced by higher $E_{\mathrm{T}}^{\mathrm{miss}}$ thresholds. The loss of sensitivity can therefore be mitigated with the proposed LAr Phase-I upgrade compared to Run 2 conditions.

[3] The actual offline thresholds will need to be optimized at the analysis level. The proposed upgrade will not only make it possible to lower the $E_{\mathrm{T}}^{\mathrm{miss}}$ threshold compared to Run 2, but the smaller least significant bit will also help to sharpen the $E_{\mathrm{T}}^{\mathrm{miss}}$ turn-on curve and hence allow lower offline thresholds.

2.3.1.3 $H \rightarrow WW^*$ Evidence of the SM Higgs boson in the $H \rightarrow WW^* \rightarrow \ell\nu\ell\nu$ channel using the full 2011 and 2012 ATLAS data set has been presented in [20]. This decay mode is of great interest since it directly accesses the W boson coupling which is central to the Higgs mechanism.

The simulated samples produced for the analysis of the 2012 ATLAS data have been used to estimate the signal acceptance and significance for different offline selection criteria applied to the leptons compatible with the trigger thresholds listed in Table 5. It is assumed that di-lepton triggers are used (with a 80 % efficiency), complemented by single-lepton triggers (with 90 % efficiency), to include events with the lowest possible p_{T} of the sub-leading lepton. In the following, the two final state categories with leading electrons are used to demonstrate the impact of the LAr Phase-I upgrade.

The present offline selection requirements for the $e\nu e\nu$ channel are $p_{\mathrm{T}} > 25$ GeV ($p_{\mathrm{T}} > 15$ GeV) for the leading (sub-leading) electron and the requirements for the $e\nu\mu\nu$ channel are $p_{\mathrm{T}} > 25$ GeV ($p_{\mathrm{T}} > 15$ GeV) for the leading electron (sub-leading muon). The offline cuts compatible with Run 2 trigger thresholds become $p_{\mathrm{T}} > 22$ GeV ($p_{\mathrm{T}} > 22$ GeV) for the leading (sub-leading) electron in the $e\nu e\nu$ channel and $p_{\mathrm{T}} > 22$ GeV ($p_{\mathrm{T}} > 14$ GeV) for the leading electron (sub-leading muon) in the $e\nu\mu\nu$ channel complemented by a single-electron threshold of $p_{\mathrm{T}} > 38$ GeV. Without the Phase-I upgrade, these more stringent requirements would translate into a considerable signal acceptance loss of 24 % (12 %) in the $e\nu e\nu$ ($e\nu\mu\nu$) channel in the 0-jet category and a loss of significance of 12 % (6 %) with respect to the current selection criteria.

The proposed LAr Phase-I upgrade will allow to recover this loss of acceptance and significance almost entirely. Using the proposed offline selection criteria from the third column of Table 5, $p_{\mathrm{T}} > 19$ GeV for both electrons in the $e\nu e\nu$ channel and $p_{\mathrm{T}} > 17$ GeV ($p_{\mathrm{T}} > 14$ GeV) for the leading electron (sub-leading muon) in the $e\nu\mu\nu$ channel, complemented by a single-electron threshold of $p_{\mathrm{T}} > 32$ GeV, would result in an acceptance loss of only 3 % (7 %) in the $e\nu e\nu$ ($e\nu\mu\nu$) channel in the 0-jet category and only a 1 % (3 %) loss in significance. Similar results are obtained for the 1-jet and 2-jet categories. Using an asymmetric di-electron trigger with offline requirements $p_{\mathrm{T}} > 26$ GeV for the leading electron and $p_{\mathrm{T}} > 16$ GeV for the sub-leading electron would further improve the signal acceptance by 3 %.

2.3.2 Impact on other physics channels

The improvements in the single and multi-lepton, τ, jets and $E_{\mathrm{T}}^{\mathrm{miss}}$ triggers are expected to have an impact on many other measurements and searches for new physics.

Searches for rare decays of the top quark or new resonances decaying to top quarks will benefit from the lower single-lepton trigger threshold. While in the SM the top quark decays nearly 100% of the time to Wb, in many models of new physics sizable rates of flavor changing decays to Hq, Zq or γq with $q = u$ or c are predicted. These searches are typically performed requiring one top quark to decay via Wb (with $W \rightarrow \ell\nu$) while the other top quark may decay to a u or c quark (e.g. for the Hc decay the signature is a lepton, $E_{\mathrm{T}}^{\mathrm{miss}}$, 3 b-jets and one c-jet). The $E_{\mathrm{T}}^{\mathrm{miss}}$ and the jets are all too low p_{T} to pass any Level-1 trigger with high efficiency, and thus a single-lepton trigger at Level-1 is the most promising avenue.

Measurements of diboson and triboson production will benefit from the lower dilepton and trilepton trigger thresholds. In particular $W\gamma$, $Z\gamma$, $W^{\pm}W^{\mp}$, WZ and ZZ production have all been studied in detail in Run 1, and interpreted in the context of trilinear gauge couplings. In all cases the most promising trigger signatures are either single leptons paired with a photon or dilepton or multilepton triggers. Another class of processes which are intimately linked with the mechanism of electroweak symmetry breaking are those involving quartic couplings. They are either probed in vector boson scattering processes (e.g. $W^{\pm}W^{\pm}$, WZ and ZZ with additional forward jets) or in triboson production (e.g. $W\gamma\gamma$, $W\gamma\gamma$ etc.). These processes have not yet been observed in Run 1 and represent a major

goal of the future LHC physics program. The average p_{T} of leptons involved in these processes is $\approx 30-40$ GeV.

The lepton triggers are also critical for searches for electroweak production of supersymmetric particles, i.e. the pair production of neutralinos, charginos or sleptons. An important process is the associated production of a chargino and a neutralino, $pp \rightarrow \tilde{\chi}_1^+\tilde{\chi}_2^0$. Depending on the SUSY realization, the decays can proceed via sleptons, gauge or Higgs bosons, or mixtures of these. For instance, if the χ^+ decays to a W and a $\tilde{\chi}_1^0$ and the $\tilde{\chi}_2^0$ decays via a Z boson, the final state contains three leptons. If the masses of the involved SUSY particles are near-degenerate, which represents an important and not unlikely scenario in Natural SUSY, the leptons can be soft. These events will typically be triggered by the multi-lepton triggers and lower thresholds will increase the sensitivity. Alternatively the $\tilde{\chi}_2^0$ could decay via a Higgs boson and a $\tilde{\chi}_1^0$, resulting in a final state of $\ell + b\bar{b} + E_{\mathrm{T}}^{\mathrm{miss}}$, $\ell + \tau\tau + E_{\mathrm{T}}^{\mathrm{miss}}$ or $\ell + W^+W^- + E_{\mathrm{T}}^{\mathrm{miss}}$. These will benefit from the lower lepton threshold in the single lepton, τ+lepton and multi-lepton triggers. Another important search is that for top squark production. It relies mostly on the single and dilepton triggers and again the leptons may be soft depending on the masses of the top squark and the $\tilde{\chi}_1^0$.

Searches for strong production of SUSY particles without leptons, for SUSY with degenerate mass spectra, and for graviton emission or pair production of dark matter particles rely mostly on the capability of triggering on $E_{\mathrm{T}}^{\mathrm{miss}}$ in association with jets. For example, pair production of dark matter particles can only be searched for by exploiting the presence of jets from initial state radiation. The production rate is low and the designed searches currently require $E_{\mathrm{T}}^{\mathrm{miss}} > 150$ GeV [21], corresponding to a Level-1 threshold of 70 GeV that may be achieved with the LAr upgrade as shown in Figs. 21 (b) and 22 (b). Similarly, in SUSY the primary benefit of a lower $E_{\mathrm{T}}^{\mathrm{miss}}$ requirement is for scenarios where the squarks, gluinos, sleptons, charginos and next-to-lightest neutralinos are not much heavier than the LSP.

3 Overview of the Existing Readout and Trigger System

3.1 Readout electronics

The current LAr readout electronics system is designed to record energies in a range from ~ 50 MeV to ~ 3 TeV for a total of $182,468$ channels and with a required energy resolution of $\sigma_E/E = 10\%/\sqrt{E} \oplus 0.7\%$ out to $|\eta| < 3.2$. The system samples the triangular-shaped current signals at 40 MHz and sends digitized samples for each bunch crossing upon a Level-1 trigger accept, up to a maximum Level-1 trigger rate of 75 kHz in Run 1 of LHC data-taking. In Run 2, it is expected that the system will operate up to a Level-1 trigger rate of 100 kHz.

An overview of the readout architecture is depicted in Fig. 24. It is composed of two main components: Front End (FE) electronics placed close to the detector and Back End (BE) electronics located off the detector in the USA-15 counting room. The system has been in operation almost continuously and extremely reliably since its installation in 2008. Maintenance operations have taken place during end-of-year shutdowns when access to the FE electronics was possible.

3.1.1 On-detector front-end electronics

Due to the stringent performance requirements of the LAr electronics, the FE electronics are mounted directly on the LAr cryostats, both in the gap between the barrel and endcap calorimeters and on the outer face of the end cap cryostats. This area has limited access and requires radiation tolerant electronics components. The on-detector electronics have been qualified in terms of radiation tolerance for up to 10 years of operation at the LHC, i.e. equivalent to an integrated luminosity in the range of $700 - 1000$ fb^{-1} [22].

The FE electronics are housed in 58 FE crates. As shown in Fig. 24, each FE crate contains:

Front End Boards (FEBs) : These are the main elements in the FE electronics and are designed to read out and digitize the LAr calorimeter signals without degrading the energy resolution. Analog signals are summed on Layer Sum Boards (LSBs). Each FEB is a large (~ 0.5m$\times 0.5$m), dense, 10-layer printed circuit board (PCB) that processes the signals from 128 channels in a specific layer of the calorimeter.

Tower Builder Boards (TBBs) : Analog signal sums[4] are sent over a dedicated backplane in the FE crate to the TBB, which forms trigger towers with a granularity of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The corresponding signals are sent over analog cables to the Level-1 calorimeter trigger system.

Calibration Boards : The calibration boards deliver a calibration pulse whose shape is close to the calorimeter ionization signal. The readout electronics are calibrated to better than 0.25%.

Controller Boards : The controller boards receive and distribute the 40 MHz LHC clock as well as other configuration and control signals.

On the FEB, the detector signals are first subject to several stages of analog processing. Preamplifier hybrids amplify the raw signals; three versions match the subdetector capacitances and dynamic ranges. Although 97% of the preamplifiers are on the FEBs, the HEC has cryogenic preamplifier summing boards mounted on the detector inside the cryostat. For the HEC, the preamplifiers on the FEBs are replaced by reshapers that invert, amplify, and shape the signal. The signals are then split and further amplified by shaper chips to produce three overlapping linear gain scales, with

[4] In the HEC and FCal, no further summation of signals is required, so Tower Driver Boards (TDBs) are used in place of TBBs.

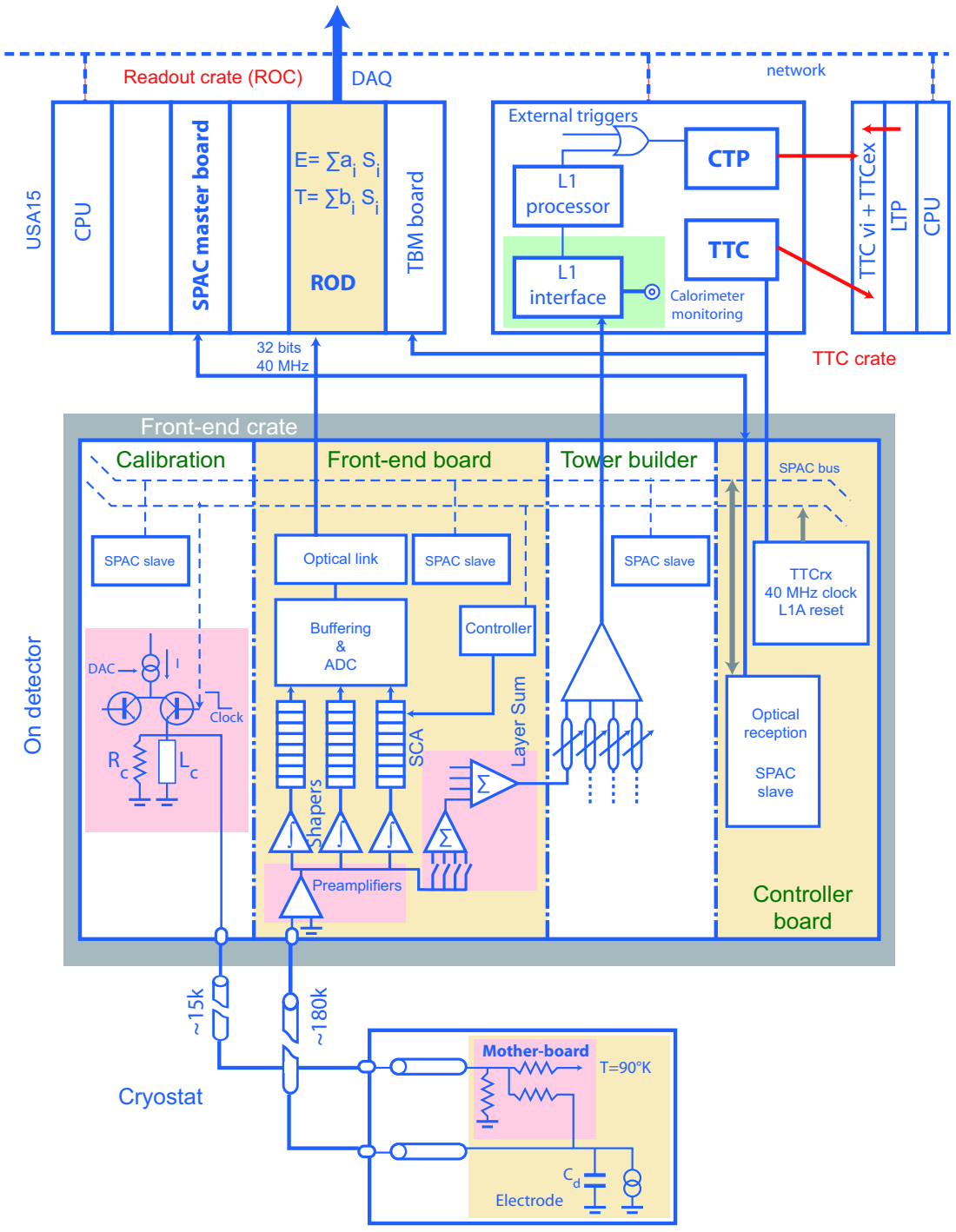


Figure 24. Schematic block diagram of the current LAr readout electronics architecture. The LAr ionization signal proceeds upwards, through the FE crates mounted on the detector to the BE electronics in the USA15 counting room. This diagram is valid for the EM calorimeters; slight changes would be needed to describe the HEC and FCal.

gain ratios of ~ 10. Gain selector chips choose the gain for each channel based on the peak sampled value of each signal. Fast bipolar shaping is performed with a time constant $\tau = RC = 13$ ns. The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz by switched capacitor array analog pipeline chips. Figure 25 shows the triangular pulse shape from the detector along with the shaped and sampled signal pulse shape. For events accepted by the Level-1 trigger, typically five samples per channel are read out from the switched capacitor array using the optimal gain scale, and digitized using a 12-bit analog-to-digital converter (ADC). The digitized data are formatted, multiplexed, serialized, and then transmitted optically via a 1.6 Gbps fiber optic link off the detector to the BE electronics.

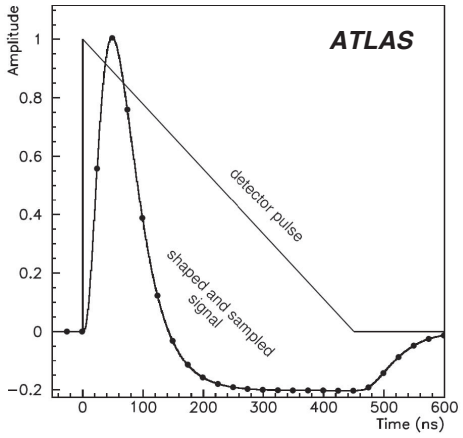


Figure 25. The amplitude vs. time for the triangular pulse shape from the LAr calorimeter, overlaid with the bipolar-shaped and sampled pulse shape.

3.1.2 Off-detector readout

The BE electronics perform digital filtering, formatting, and monitoring of the calorimeter signals. Each FE crate is associated to a VME-based Readout Driver (ROD) crate, which contains:

Read Out Drivers (RODs) : The RODs synchronize the output of the FEBs with the Level-1 trigger and compute physical quantities such as the energy, time phase, and quality of the signal.

CPU Board : The CPU board is a VME processor that controls the ROD crate.

SPAC Master Board : A communication module to configure or load parameters into the various boards of the FE crate or to read back registers; configuration and monitoring take place using the Serial Protocol for ATLAS Calorimeters (SPAC).

Trigger Busy Module (TBM) : The TBM receives the trigger, timing, and control (TTC) signals that include the 40 MHz LHC clock and other synchronous commands.

Each ROD receives raw data (typically five digitized samples) from eight FEBs. Four input field programmable gate arrays (FPGAs) parallelize the incoming data and verify its integrity. The memory is separated into two banks: one for writing incoming data, the other for the data that is read by the digital signal processor (DSP). A ROD holds four Processing Units (PUs), each with two DSPs. Each DSP can perform 5.7×10^9 instructions per second, and the calculations have been optimized to

accommodate the Level-1 trigger rate (for a rate of 75 kHz, the calculations must be performed within 13μs). An optimal filtering algorithm is used to calculate the energy deposited in the calorimeter from the digitized samples. Above a given (programmable) energy threshold, the time of the energy deposition and the quality of the pulse are also calculated. The quality factor quantifies whether a pulse matches the expected shape or whether it may be mismeasured. A second energy threshold is defined, above which the values of the raw samples are written out in addition to the results of the optimal filtering algorithm. These resulting quantities are then sent via optical fibers to the data acquisition (DAQ) system.

3.2 Level-1 trigger readout

The current Level-1 calorimeter (L1Calo) system receives analog, summed Trigger Tower signals from the LAr Tower Builder Boards described in Sec. 3.1.1, as well as equivalent signals from the Tile Calorimeter system. The architecture of the L1Calo system is illustrated in Fig. 26.

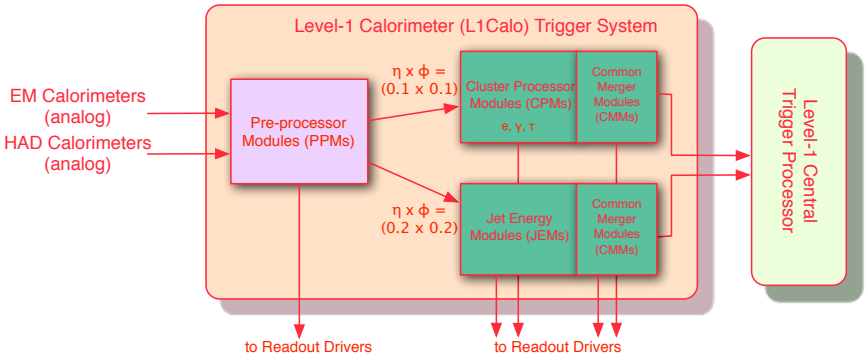


Figure 26. Schematic block diagram of the Level-1 Calorimeter (L1Calo) Trigger System.

Pre-processor Module (PPM) : The PPMs sample the analog Trigger Tower signals at 40 MHz, identify the bunch crossing using the pulse shape, and use a look-up table to compute the transverse energy. The digital data is then transmitted to the Cluster Processor Modules and Jet Energy Modules.

Cluster Processor Module (CPM) : Each CPM identifies isolated electron, photon and τ lepton candidates from the $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ granularity energy deposits in a given calorimeter region. A Region of Interest (ROI) is defined using a sliding window algorithm, and electromagnetic and hadronic isolation quantities are computed from the surrounding clusters.

Jet Energy Module (JEM) : Each JEM identifies energetic jet candidates from $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ jet elements in a given calorimeter region. Similar to in the CPM, a ROI is defined using a sliding window algorithm. The sum of the total transverse energy and the missing transverse energy are also computed.

Common Merger Module (CMM) : The results from the CPMs and JEMs (e.g., the number of candidates passing a given threshold) are transmitted over crate backplanes and summed in CMMs before being sent to the Central Trigger Processor (CTP).

After receiving a Level-1 Accept, the L1Calo modules provide readout data and ROIs to the High-Level Trigger (HLT) system via readout drivers.

4 Front End electronics

The upgrade to the trigger branch of the LAr system begins with the signal which is produced by the linear mixer in the FE electronics, as shown in the block diagram in Fig. 4. This signal is sent over the baseplane to the new LAr Trigger Digitizer Board (LTDB), where it undergoes digitization. A feature of the Level-1 trigger system is that the thresholds are in units of transverse energy, whereas the signals from the calorimeters are proportional to energy. In the existing system, the conversion factor of $\sin\theta$ is applied to signals in the trigger chain in several steps: through the choice of preamplifier and the gain of the linear mixer in the FEB for all calorimeters, and through the η-dependent gains that are applied in the TBB for the EM calorimeters in LSBs and in the receiver for the HEC and FCal. In the upgraded system, the choice of preamplifiers and gains in the FEB will remain unchanged. How the η-dependent gains will be applied is not yet decided; they may be included in the analog section of the LTDB or as a factor in the calibration constant which is applied in the BE electronics.

Detailed block diagrams of the analog and digital treatment of signals in the FE trigger chain are given below, and these diagrams show in more detail the logic illustrated in the block labelled LTDB in Fig. 4. A brief discussion of the elements in the current system ("legacy" electronics) that will also be part of the Phase-I system can be found in Appendix B.

The upgrade to the FE electronics is described in two different sections: in Sec. 4.1 components of the system which are new or modified versions of the current system are introduced; and in Sec. 4.2 we discuss how these components are utilized in the different regions and types of calorimeters comprising the LAr system.

4.1 Upgraded front end electronics components

Although the current LAr Calorimeter readout architecture remains basically intact, the proposed modifications in the Phase-I upgrade extend this system and require the following changes to the front end electronics:

- New Layer Sum Board (LSB): The current LSB is a personality card plugged on the FEB to produce 0.1×0.1 analog sum signals in $\Delta\eta \times \Delta\phi$ in a given layer of the calorimeter. In the Phase-I upgrade, the new LSB produces finer granularity Super Cell signals in the Front and Middle layers.

- New Base Plane: The new base planes will allocate new slot(s) for the LTDBs (either by utilizing empty slots or by eliminating the CMB module), while keeping the other front end electronics boards slots intact. In addition, a much larger number of signals are transferred from the FEBs to the LTDB than are currently used in the trigger chain. It also routes the legacy trigger signals to the TBB or TDB, as is done by the current baseplane.

- New LAr Trigger Digitizer Boards (LTDB): The LTDB will receive and digitize Super Cell signals and transmit digital Super Cell signals to the back end digital processors. It also forms layer sum signals and sends them to the TBB to keep the current analog trigger chain unaffected.

These elements are described in detail in the following subsections.

4.1.1 LSBs for the upgraded system

The function of the LSB is to provide either a second level of summing in the trigger summing tree or, in the case that only one level of summing is needed, to act as a driver to transmit the analog signals to the processing boards on the baseplane (TBB, TDB, and the LTDB).

Table 7. Number of LSBs to be installed in the FEBs, listed by type. Suffixes serve to indicate various configuration options, as discussed in the text. The number of boards that are removed from FEBs and can be reused in the upgraded system are given in the second column. The third column contains the difference between the two, the number of new boards that must be produced. The LSBs for the FCal, designated by the suffix "F", are of a special design and are discussed in Sections 4.1.1.3 and 4.2.4.2.

LSB type	Installed	Reused	New
S1x16H	200	200	0
S1x16M	32	32	0
S1x16L	896	96	800
S2x8	1216	160	1056
S2x8D	288	0	288
S1x16F	24	0	24
S2x4+S1x8F	32	0	32
S2x6D+S1x4	128	0	128
S1x6+S6x1	128	0	128
Totals	2944	488	2456

In the existing system, there are basically four types of LSBs, which vary in the number of circuits on the board and the number of elements in the sum. The types are S1x16, S2x8, S4x4, and S8x2, where the first digit indicates the multiplicity of the sum and the second digit the number of summing (or driver) circuits on the board. Suffixes, discussed in detail below, are used to indicate various configuration options for the circuits, such as gain options or numbers of outputs. Although there is not a 1:1 relationship between LSB type and layer or region of the calorimeters, in the current system, the S1x16H is used primarily for the presampler, and the S8x2, S4x4, and S2x8 are used primarily for the front, middle, and back layers, respectively, of the EM calorimeters. FEBs for the HEC use several types of S1x16 boards. Special boards of type S4x4, S2x8, and S1x16 were built for the FCal region, where the large bins in η required weighted sums to be used.

For the new system, in addition to the standard summing configurations, there are some special purpose boards which handle trigger sums in special regions of the calorimeters, including areas where cabling anomalies were found to exist. A set of new boards with weighted sums will also need to be built to achieve higher granularity in the FCal trigger signals.

In the new system, the bulk of the LSBs are limited to two types, the S1x16 and S2x8, each of which exist in different types as indicated by suffix letters. The number of LSBs required for the upgrade are listed by type in Table 7. The S2x8 and S1x16 boards are used in the upgraded system to provide higher granularity for the front and middle layers, respectively. It is for this reason that the bulk of the new LSBs to be built are of these two types. The distribution of boards for the EM calorimeters are summarized according to the type of baseplane in Tables 15, 17, and 18. The HEC requires no new LSBs; the FCal LSBs are discussed in Sec. 4.2.4.2.

4.1.1.1 LSB type S1x16 The S1x16 LSB is the only one of the layer sum boards which does not have a summing function; it serves only as a line driver for the linear mixer output signal. This circuit requires only one stage, which must be non-inverting. In some cases (*e.g.*, the presampler) the signals which this board handles are rather small, and it is advantageous for noise reduction to introduce an extra factor of gain at this stage. Thus there are two gain options on the board. The high-gain board (S1x16H) has a gain of 2, and the low-gain one (S1x16L) has a gain of unity. In

the upgraded system, the S1x16L will be used in the middle layer in both the barrel and endcap calorimeters.

The circuit diagrams for both gain configurations are shown in Fig. 27. Since the amplifier is in the non-inverting configuration, the signal at the input cannot exceed the common mode limit for the opamp, which has a minimum value of 1.8 V for the HFA1135 (an operational amplifier with a voltage limiting feature, used in all types of LSB). For the high gain case (gain=2), this does not present a problem, since output limiting at 3.4 V limits the input in the linear region to 1.7 V. For the low gain case, the input signal is attenuated by a factor of two, giving an overall gain of unity. Thus the maximum voltage seen at the input node is the same as for the high gain case.

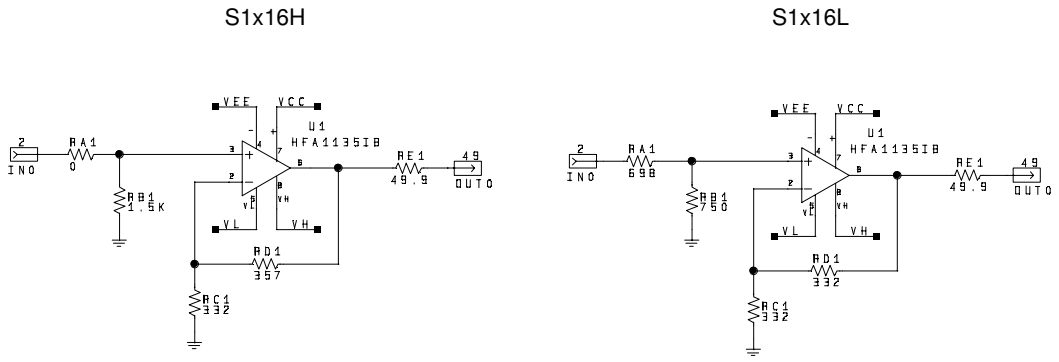


Figure 27. Schematic diagram of S1x16 layer sum board. The high gain version (S1x16H) is shown on the left, whereas the unity gain version is shown on the right. Any of the 16 channels on the board can be configured for either gain value.

The LSB is designed in such a way that either option can be chosen for any channel on the board. The advantage of this solution is that it permits both high-gain and low-gain channels to be mixed on the same LSB (called S1x16M), a feature that is required for the HEC.

4.1.1.2 LSB type S2X8 The S2x8 LSB will be used in the front layer of the EM calorimeters to produce Super Cell signals with $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$. This board requires only one output, since the signals are sent only to the LTDB, where the legacy sums are generated.

The S2x8 configuration will also be used, as it is currently, in the back layer of EM calorimeters (see Table 14). It will be required to produce only a signal summed over the trigger tower. However, this sum is to be sent to two destinations: the LTDB, where it is treated as an Super Cell signal, and the TBB, where it is treated as a legacy LSB signal. The new LSB is called S2x8D, where the "D" signifies dual output. If the required gain is the same for both signals, a simple splitter may be used as indicated in Fig. 28. Another option would be to provide a dual buffer at the output to give greater flexibility and better isolation. Both options will be prototyped by the end of 2013, at which time the design choice will be made. The S2x8D can also be used in the front layer, since an unused second output does not pose a problem. For this reason, all new LSBs of the S2x8 configuration will be of the type S2x8D.

4.1.1.3 LSBs with η-dependent weights In general, the LSB is used to form an unweighted sum of cells in a narrow region of η lying within the area in a given layer bounded by the trigger tower. In the case of the FCal, each layer corresponds to a module. An LSB performs a sum over a relatively wide range in pseudorapidity and azimuth to form a pseudo “trigger tower”. Over this wide

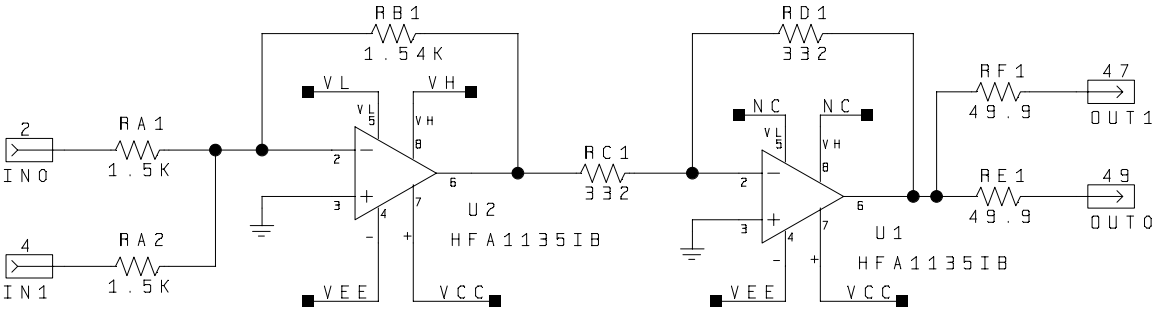


Figure 28. Schematic diagram of a possible layout for the S2x8D layer sum board.

range in η the conversion factor from energy to transverse energy changes markedly. For this reason the inputs to be summed on the FCal LSBs are weighted by $\sin\theta$, where θ is the angle relative to the beam line of the geometric center of each of the cells at the LSB input. This weighting converts energy to transverse energy before summing. The calculation of these weights is tedious because of the inherent x-y organization of the FCal readout cells. With an irregular azimuthal symmetry, cells in each of the 16 phi slices have disparate geometric centers. This leads to a large variety of LSBs, which, within a given FCal module, differ only by the weighting resistor values. These boards are designated with the suffix “F” in Table 7, and their usage is detailed in Table 20.

4.1.1.4 LSBs with special requirements

There are certain irregular sections of the calorimeters that require LSBs with special configurations. These needs are met in some instances by exercising certain jumper options on the boards, but in other cases a special design must be fabricated. One such case occurs in the end of the EM Barrel, where the elements of the front section for $|\eta| > 1.4$ are 12 elements of $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$, and the middle section contains 4 elements of $\Delta\eta \times \Delta\phi = 0.075 \times 0.025$. These elements are routed to the FEB servicing the back layer. There the linear mixer forms sums over 4 channels in azimuth as usual, and the LSB is required to send each sum to the LTDB, along with six normal twofold sums from the back layer, which are sent to both the LTDB and the TBB. Thus a special hybrid LSB with the configuration S2x6D+S1x4 is required.

A similar situation occurs in the Standard EMEC crate in the region $1.8 < |\eta| < 2.0$, where the trigger tower contains 24 elements (“strips") in the front section. These are summed in groups of four by the shapers, and we therefore have six sums of size $\Delta\eta \times \Delta\phi = 0.0167 \times 0.1$. To maintain high granularity, it is desirable to send these signals individually to the LTDB. However, a sum of six is required to fabricate the legacy signal for the TBB, whereas the summing circuit in the LTDB has only 4 inputs. This could be done in a special LSB configured as S1x6 + S6x1, where the sixfold sum would be sent only to the TBB and the six individual sums would be sent to the LTDB. A decision on how this problem will be handled has not yet been reached.

It is possible that in the detailed design of the other baseplanes other such situations will arise and additional special purpose LSBs will be needed.

4.1.2 Modifications to the Front End Crate

After a careful examination of all LAr detector regions, it was concluded that new LTDBs could be introduced to FECs with minimum interference with the current system. The following is the summary of the design considerations of the new baseplanes; these considerations are intimately related to the interface to the warm cables and signal routing.

Ribbon cables (the so-called “warm cables") form the connection between the cryostat feedthrough

and the baseplane. Therefore to replace the baseplane, it will first be necessary to unplug these cables from the baseplane end and reposition them to their new slot positions before reconnecting them to the replacement baseplane.

New high density connectors on the LTDB raise concerns about the insertion and extraction forces on this module which may require additional crate modifications, as discussed below.

4.1.2.1 Baseplane design New baseplanes for the front-end electronics crates have been or are being designed and are similar to the existing baselines. The differences are: the presence of three high-density Hard Metric connectors, ERNI part number 104735, for each of the LTDB slots, as well as higher density baseplane interconnects between the analog signal outputs of the FEB, the LTDB, and the legacy TBB inputs. The number of controlled-impedance stripline signal layers on the baseplane has been increased from four to five (at least for the EM baseplanes). Total PCB thickness remains unchanged, 2.4mm, for compatibility with the existing card cage and front-end boards. Use of the Hard Metric connectors imposes a constraint on the slot assignments in the baseplane since the dimensions of this connector preclude the mounting of a FEB, with shielding springs on its 96-pin DIN connector, next to the LTDB.

Routing of signals on the new baseplane is more complex than for the current baseplane. Signals from Super Cells which have higher granularity than a trigger tower (called summed channels) are transmitted to the LTDB, where the sum is performed, and this sum is transmitted over the baseplane to the Tower Builder Board (TBB). For the cases where the Super Cell is identical to the trigger tower (called spectator channels), the signal goes directly from the FEB to both the LTDB and the TBB or TDB.

The ERNI p/n 104735 connectors feature a self-aligning post which can tolerate up to +/- 2.5mm initial misalignment of the LTDB. In addition, each LTDB slot will have two guide pins, Tyco p/n 2000676, requiring a compatible guide module (p/n 2000677 or 2000713) to be installed on the LTDB. This allows an initial misalignment up to +/- 3.5mm, virtually eliminating the risk of improper card insertion.

Electrical connectivity on various types of baseplanes (three EM types, one Hadronic type, one FCal type) aims to be compatible with a common LTDB pinout. The LTDB pinout currently implemented on the new EM baseplane has 64 groups of four inputs with summing, 64 inputs with no summing (for a total of 320 input signals and 64 output signals), 276 designated ground contacts corresponding to LTDB designated ground contacts, and 264 ground contacts on the two connector rows which correspond to the LTDB connector GND shields.

Some signal groups may only be partially used, or not used at all, depending on the type of baseline. Signals designated as LTDB inputs are grounded on the baseplane when not used. Signals designated as LTDB outputs are left unconnected on the baseplane when not used.

The designs of baseplanes for the different calorimeters are discussed in Sec. 4.2.

4.1.2.2 Crate and baseplane mechanics The high density LTDB connectors will be equipped with a mix of three possible pin heights, so as to minimize the LTDB insertion force. The exact configuration has not yet been defined.

Higher card insertion force is expected for the LTDB. There will be tests and possibly structural calculations performed to determine whether the longitudinal baseplane support bars, mounted on the crate pedestal, need to be redesigned (reinforced) in order to keep the deflection to an acceptable value.

The card cage provides for two front panel mounted thumbscrews, which can also be driven with a wrench, as an aid for card insertion and extraction. This feature was not intended to cope with the

insertion forces that are expected for the LTDB. A custom card insertion-extraction mechanism may be required for the LTDB slot.

4.1.3 LAr Trigger Digitizer Board (LTDB)

4.1.3.1 Introduction The LTDB (see Fig. 29) is the key electronics board to be built for the Phase-I upgrade. It will be responsible for the formation of the legacy layer sum signals (i.e. signals currently formed in the LSBs) as well as the digitization of Super Cell signals. The baseline design of the LTDB will have the following features :

- Each LTDB will process up to 320 Super Cell signals for the granularity scheme of the Super Cells designated "1-4-4-1", which means (per trigger tower of size $\Delta\eta\times\Delta\phi = 0.1\times0.1$): 1 Super Cell in the presampler, 4 in the front layer, 4 in the middle layer, and 1 in the back layer).
- The flavor of the LTDB is distinguished either by the configuration of its sub-sections or by the treatment of analog signals within its sub-sections.
- Since the LTDBs will need to operate beyond the Phase-II upgrade, the powering section of an LTDB will use a modular design to provide forward compatibility.
- The power budget of the LTDB is specified as 160 W; therefore the new cooling plates will use two (as opposed to one for boards in the current system) water circulation channels.
- The LTDB will include the functionalities of the current Crate Monitoring Board (CMB) for monitoring of front end low voltages. See Sec. 4.1.3.4 for details on the cooling system.

There is one LTDB per baseplane in each EMB, HEC, and EMEC Standard Crate, but in the EMEC Special and FCal crate, two are required (labelled "0" and "1"). The number of channels to be treated in each type of LTDB, along with the number of units required, is detailed in Table 8. A total of 124 LTDB modules will be installed in the system.

Table 8. Number of channels to be treated in each type of LTDB and the number of boards required. The EMB, EMEC Standard, and HEC crates require only one LTDB per baseplane but in the EMEC Special and FCal crates two LTDBs per baseplane are required. Suffixes "0" and "1" are used to distinguish the LTDB modules in these two crates.

LTDB Type	Channels	LTDB per region
EMB	290	64
EMEC Std	312	32
EMEC Spc 0	240	8
EMEC Spc 1	160	8
HEC	192	8
FCAL 0	192	2
FCAL 1	192	2
Total		124

4.1.3.2 Analog signal treatment The primary purpose of the analog section of the LTDB is to provide the appropriate gain, shaping, offset and common mode such that the full 12-bit dynamic range of the ADC (see Sec. 4.1.3.2.4) is utilized without meaningful sacrifice to the signal to noise ratio. This implies that the quantization error should not exceed the intrinsic electronic noise arising from the preamplifiers and the noise from the linear mixer and the summing amplifiers.

The Phase-I upgrade must also maintain the current functionality of the trigger chain (Tower Builder Board/Tower Driver Board plus Receiver) for three different situations. The first two cases occur in layers where the size of the Super Cell is the same as that of the legacy trigger tower: in these cases signals are sent directly to both the TBB/TDB and the LTDB. To obtain maximal signal fidelity the use of separately terminated lines for this transmission is preferred. This is possible when the LSB is of the S2x8 type (i.e. either the S2x8 or the S2x8D). Due to the limited number of connections between the FEB and the baseplane, only one line per channel is available when the LSB is of the S1x16 type. In this case the LTDB will receive these baseplane signals with a high impedance tap. The line is terminated in 50 Ω at the TDB/TBB and with a much higher impedance (i.e., several hundred ohms) at the LTDB. This circuitry is required to not distort the signal shape, which places a strong requirement on the parasitics of the LTDB connection to the baseplane. The third case occurs when the baseplane signals from the LSB have a finer granularity in η than a single trigger tower. These signals must be received from the baseplane with a low-impedance termination. They are used both for the generation of ADC signals and summed in groups of four to provide the TBB with signals corresponding to the trigger tower, preserving shape, polarity, and timing for re-transmission onto the baseplane and termination on the TBB as in the original system.

To perform these functions the LTDB must have three different analog signal processing configurations. These may be realized as circuits with different layouts or simply as the placement of different sets of components, including jumpers, onto a common PCB. To summarize the cases:

- Spectator signals. The TBB/TDB signal is unchanged from the one used in the current system and the LTDB utilizes it to create digitized representations. This can occur two ways:
  - Low-impedance mode: the signal from the LSB is terminated in 50 Ω at the LTDB.
  - High-impedance mode: the signal from the LSB is terminated in 50 Ω at the TBB or TDB, and the LTDB receives it using a high impedance tap.
- Summed signals. The LTDB terminates a set of four signals from the baseplane and sums them together, the summed output being transmitted to the TBB.

A block diagram illustrating these treatments is shown in Fig. 30.

4.1.3.2.1 Spectator signals in high impedance mode In high-impedance mode, the parasitics must be small enough that the signal to the TBB is undisturbed. This appears fairly daunting, but the long rise time (typically greater than 30 ns) and a low driving impedance make it possible to consider sending the signal onto the LTDB and tens of centimeters, perhaps even through an additional connector for an analog mezzanine board, with very little impact on the signal shape. Fig. 31 compares simulations of the signal monitored at the termination on the TBB board both with and without connection onto an LTDB board. The LTDB board was modeled with a transmission line followed by an additional connector of the type needed for an analog mezzanine board. Although this result is reassuring, it will be necessary to fabricate a test board before qualifying this particular approach. Signals received in this manner are sent directly to the ADC driver and shaping circuit discussed in Sec. 4.1.3.2.3.

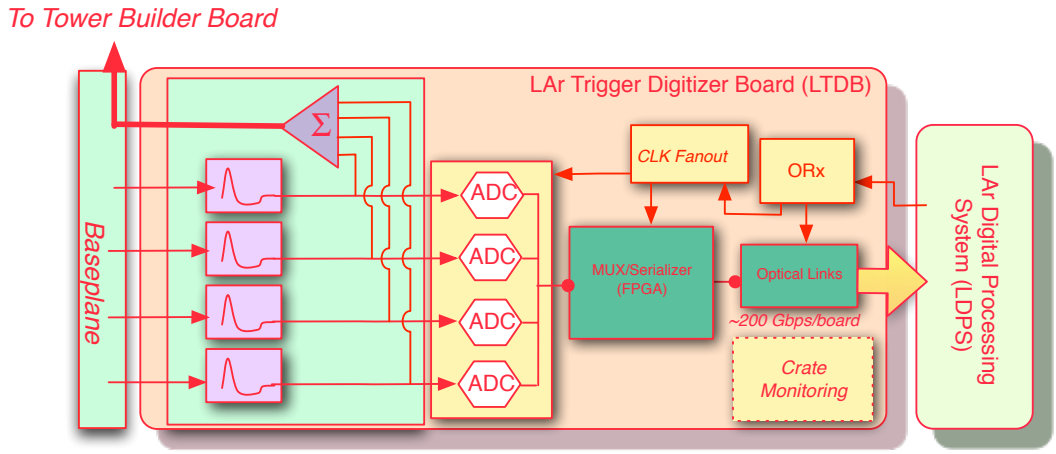


Figure 29. Schematic block diagram of the proposed LAr Trigger Digitizer Board (LTDB).

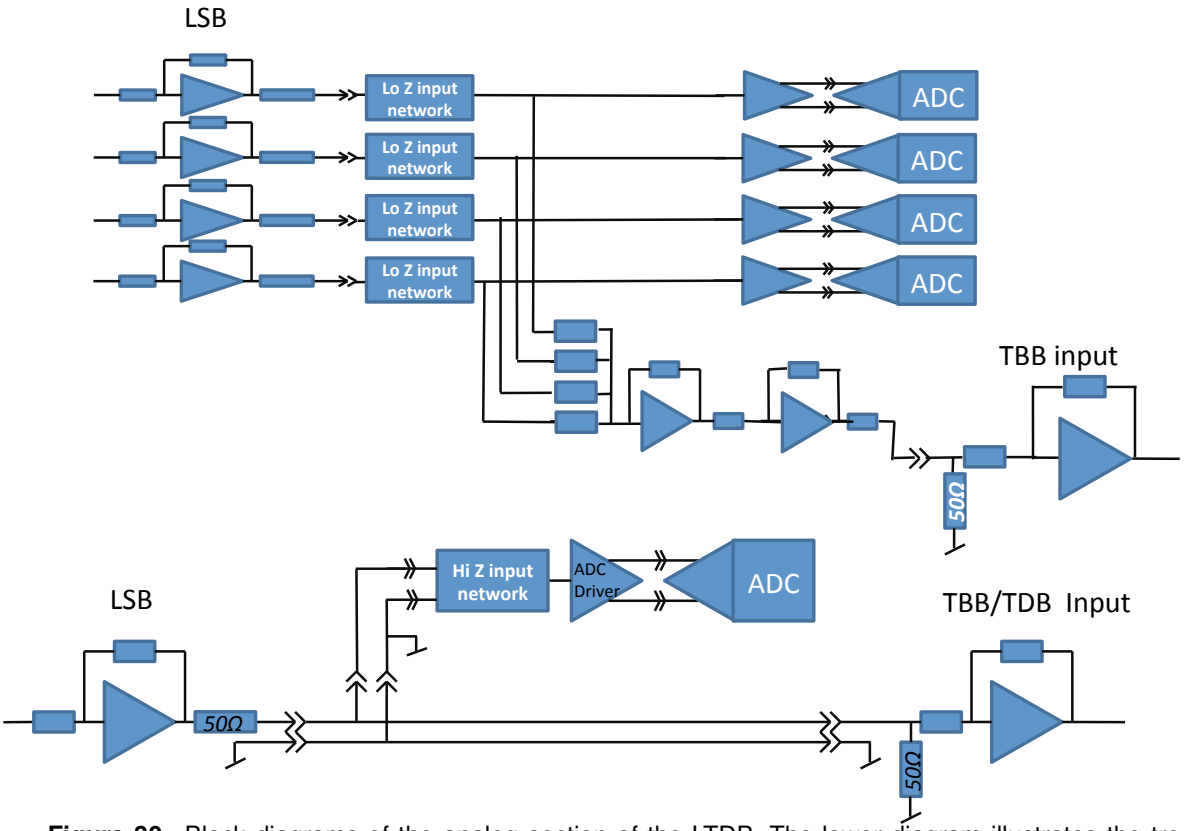


Figure 30. Block diagrams of the analog section of the LTDB. The lower diagram illustrates the treatment of a spectator channel in high-impedance mode, where the signal is received from the baseplane using a high-impedance tap. The upper diagram shows the treatment for summed channels, with the sum transmitted to the Tower Builder Board. A third type of treatment (not shown) is used for spectator channels in low-impedance mode which, like the summed channels, are terminated in 50 Ω at the LTDB. The only difference between the diagram for these channels and the (lower) one shown is that the label "Hi Z input network" is replaced by "Lo Z input network". The blocks labelled “network” may or may not contain active elements.

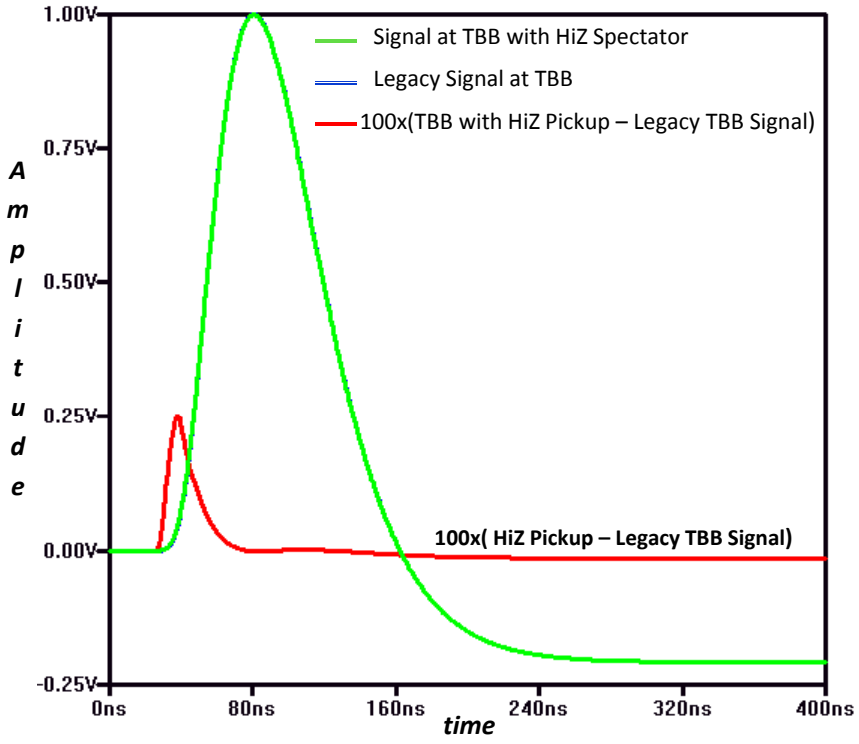


Figure 31. Results of a study of the effects of the high-impedance tap on the shape of a simulated waveform. This plot shows a comparison of a reference signal at the LSB output as measured at the TBB input(blue line) with the same signal at the TBB but with a high-impedance spectator input to the LTDB (green line). The parasitics associated with this latter case are two extra connectors and an additional trace of 20 cm length that takes the spectator signal to the high impedance voltage follower on an analog mezzanine board. The line in red is the point-by-point difference between the two signals, multiplied by 100, after multiplying the reference waveform by 1.0007 and delaying it by 1.25 ns. The two waveforms (one slightly adjusted as noted above) are virtually indistinguishable as shown by the red curve. This indicates that signal amplitude distortions at the TBB input due to parasitics associated with the LTDB will be $\sim 0.1\%$ and the signal will have a very slight additional delay.

4.1.3.2.2 Summing circuit and baseplane driver In order to maintain the legacy granularity for the TBBs, these signals must be reconstituted by performing an analog sum of the four signals and driven from the LTDB to the TBB with the same type of 50Ω series termination as used in the LSB. Because this signal is terminated on the TBB, the summing amplifier will need to have a gain of 2. One concern will be to retain as closely as possible both the shape and time of arrival of the signal at the TBB.

Once Super Cell signals arrive at the LTDB, they are received by a low-impedance input stage. Beyond that, there are two signal paths. The first path is to the ADC driver and shaping circuit discussed in Sec. 4.1.3.2.3, The second path is to a summing circuit that performs an inversion, followed by a stage that again inverts the signal and drives a line onto the baseplane which is terminated at the TBB.

Since the TBB performs analog sums over the layer sum signals to obtain the final trigger tower sum, it includes a set of programmable delay lines to permit adjustment of the timing of the four input signals. This time adjustment system has a range of 17.5 ns (see Sec. B.3), which is intended to cover the range of cable and rise time delays for signals from various paths. In the case of summed signals from the LTDB, the time of arrival is delayed, relative to their timing in the current system, by the transit times associated with the traces and the propagation delay due to two stages of amplification. This latter quantity, for the amplifier used in the LSB (HFA1135) is measured for signals of our type to be close to 3 ns per stage, creating an insertion delay for the LTDB of at least 6 ns, a sizable fraction of the range of the TBB timing adjustment. We have examined the delay settings currently in use for most of the EM channels, and it is clear that the delay lines can be used to correct for the insertion delay in all cases for the EMB. For the EMEC standard crates, the insertion delays for the middle layer can be compensated for all trigger towers, but for the front layer, there is a problem with the trigger towers at lowest eta (TT3 and TT4). There are a total of 139 channels where the timing will be incorrect if an insertion delay is added. The EMEC special crate is still under study, as of the time of this writing (July 2013). We are considering possible solutions to this problem. One possibility would be to use single-stage LSBs, which send inverted signals to the LTDB, 3 ns earlier than normal LSBs. Since the sum on the LTDB is also an inverting stage, its output could be sent directly to the TBB, restoring the timing to its current value except for timing differences caused by additional traces. This could be done either for all channels summed in the LTDB or only those whose TBB delay settings are problematic. For the channels where this is done, existing LSBs cannot be used, and the analog chain in the LTDB will need to be able to handle signals of both polarities (the polarity of spectator channels cannot be changed).

4.1.3.2.3 ADC driver and shaping circuit As discussed in Sections B.1.2.1 and B.1.2.2, the shaping for the main readout and the trigger chain differ by one stage of integration, because the final integration stage for the trigger chain should be placed after the summing amplifiers to perform bandwidth limiting of the noise. For this reason, the driver for the ADC must contain a final pole. In addition, depending on the choice for the dynamic range of the ADC (see Sec.4.1.3.2.4) it may be necessary to introduce η-dependent gains, which would also be done in the driving circuit. Since the signal is bipolar, a differential driver circuit will be used to convert each of the signals to differential form with appropriate common mode offset to take full advantage of the dynamic range of the ADC.

4.1.3.2.4 Dynamic range of Super Cell transverse energy There are two issues to be considered when choosing the dynamic range of the digitization of the signal. The first issue is the required precision for calculating the isolation variables or the parameter R_η (see Sec. 2.2.1), and the second is the need for determining the timing of the signal, in order to associate it with the correct bunch crossing using a digital filtering algorithm (for non-saturated signals). For the former, one

Table 9. Proposed least significant bit (lsb) and maximum amplitude for the front and middle layers of the EMB if the ADC digitizes with a fixed lsb over the entire range of pseudorapidity. Here the baseline is assumed to be set at 20% of the full scale of the ADC.

Layer	lsb (MeV)	Maximum E_{T} (GeV)
Front	32	102
Middle	125	400

would like to optimize the ADC lsb value to achieve the maximum precision, whereas for the latter, one would like to extend the reach of the ADC to signal amplitudes up to the saturation level of the analog circuitry. Determination of the timing for signals above the saturation level of the analog chain is a separate topic and is not considered in this section.

Simulations have shown that least significant bit (lsb) values of $65\ \mathrm{MeV}$ in E_{T} in the front layer and $250\ \mathrm{MeV}$ in the middle layer provide acceptable performance in the new trigger scheme. A 12-bit ADC has a full range of 4096, which should cover both the positive and negative lobes of the pulse, the latter having an amplitude of about 20% of the former. Another requirement is that the performance should not suffer too much in the event that the detector would need to be operated at a reduced high voltage. For example, a reduction of the high voltage by a factor of 2 decreases the pulse height by 25%. If a high voltage channel is missing altogether (due to a short), the pulse height is decreased by 50%, due to the interleaving of the electrodes across two HV channels. In summary, choosing the lsb values to be half of those mentioned above addresses both issues.

With this choice, the dynamic range will be $32\ \mathrm{MeV}$ to $102\ \mathrm{GeV}$ in the front layer and $125\ \mathrm{MeV}$ to $400\ \mathrm{GeV}$ in the middle layer (at nominal voltage). These values are summarized in Table 9, where both the full range of the ADC and the maximum amplitude (assuming that the baseline is set at 20% of full range) is given. Note that the analog part of the middle layer saturates at values of E_{T} from $350\ \mathrm{GeV}$ to $1\ \mathrm{TeV}$, depending on pseudorapidity. The above procedure would require a gain stage in the analog section which completes the conversion from E to E_{T}, so that all ADCs of a given layer function at the same lsb (in units of transverse energy). A consequence of this procedure is that the timing is determined through digital filtering only for pulses up to the maximum amplitude given in Table 9. A different approach would be to use a gain uniform in η in the analog chain and hence an lsb which varies with pseudorapidity. In this case the ADC digitizes the signal over the full dynamic range of the analog chain, and permits digital filtering to be performed for all amplitudes below the saturation level of the analog signal. Such an approach would permit bunch crossing identification to be made for all pulse heights below the saturation level of the analog circuitry. Monte Carlo studies are currently under way to evaluate the effect of this approach on the calculation of R_{η}.

4.1.3.3 Digital signal treatment A block diagram of LTDB digital section of LTDB is shown in Fig. 32. It has two signal flow paths: the data link and the control (or TTC) link. The digital processing chain which drives the data link is responsible for signal digitization and transmission. Super Cell signals are multiplexed and serialized in LOCx2, and transmitted via the optical transmitter over optical fibers. The TTC link is responsible for transmission of clock signals, slow control and monitoring communications.

4.1.3.3.1 TTC and slow control The TTC signals will be delivered to the LTDB via optical fibers. The Control Link is illustrated in Fig. 32. It consists of 3 components: the VTRx, the GBTx, and the GBT-SCA. Since the PIN diode detector in the VTRx optical receiver is also an efficient

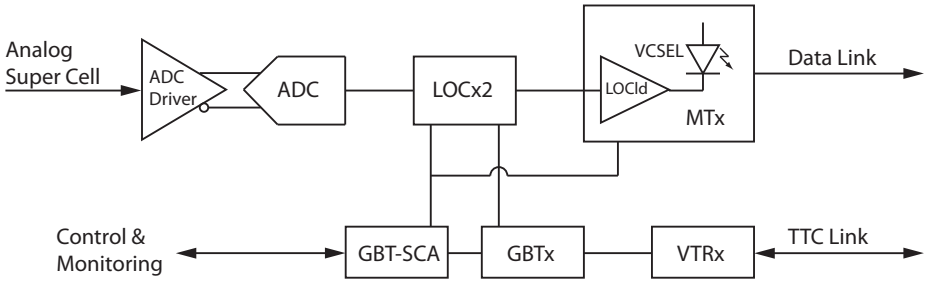


Figure 32. The LTDB digital section includes two signal flow paths: the data link and the control (TTC) link. Super Cell signals are digitized by the ADC, reorganized and serialized by LOCx2, and transmitted via the MTx over fiber optical links. The TTC link is responsible for clock distribution, slow control and monitoring; it is composed of the GBTx, GBT-SCA and VTRx. The GBTx is used to interface to the back end of the TTC system via VTRx over duplex fiber optical links; the GBTx and GBT-SCA chipset is used to provide clock distribution, slow control and monitoring on the LTDB.

particle detector, one requires a transmission protocol to detect and correct bit errors caused by radiation. The GBT ASIC is the only development that addresses this issue. The GBT ASIC family [23] developed by CERN consists of the following ASIC chips (dies): the GBTx, a serializer and de-serializer with a custom transmission protocol to mitigate SEUs especially in the receiving side on the detector front-end; the GBT-SCA, a dedicated ASIC for slow control and monitoring; the GBLD and GBTIA, both dedicated ASICs for the optical transceiver VTRx, which is being developed by the common project Versatile Link and is to be used with the GBTx in an optical link system.

The GBTx will be used to provide clocks for the LTDB. The GBTx deserializer has clock outputs at 4 frequencies (40, 80, 160, 320 MHz). Each is phase adjustable with a 50 ps step. The random jitter of the 40 MHz output clock is measured to be 4.07 ps (rms), meeting the requirement of the serializers and ADCs. There will be 4 GBTx chips on each LTDB to provide enough clocks for all ADCs and LOCx2 serializers. The GBT-SCA (Slow Control Adapter) will be used for slow controls on the LTDB. The GBT-SCA with 16 I2C masters will control 20 ADC chips (assuming 4-channel ADC chips), 5 LOCx2, 10 LOCld inside 5 MTx, all on one 1/4 slice LTDB. The power supply voltages and temperatures inside some ASICs (for example, the LOCx2) and a few points on the LTDB will be monitored. Each SCA has 32 channels of slow ADCs for monitoring purposes. The BCID counters in the LOCx2 need to be reset synchronously (within an LHC clock cycle). The GBTx data output, which is synchronous to the LHC clock, will be used as a reset.

The GBT and VTRx are evaluated to be radiation tolerant for applications on the ATLAS detector front end.

The control link optical power budget will follow the guidelines from the Versatile Link Project [24].

4.1.3.3.2 Digitization Super Cell signals must be digitized at 40 million samples per second (MSPS) by the ADC on the LTDB. This ADC must meet the stringent requirements outlined in the first two columns of Table 10, as well as a radiation tolerance (both the total ionizing dose, TID and single event effects, SEE) that meets the LAr front-end electronics requirement for Phase-I and Phase-II operations. The input clock to the ADC will be the LHC clock, and the chip will have serial output using either the LVDS or SLVS standard[5]. The ADC word will be either 12-bit or 16-bit in one

[5]LVDS and SLVS are industrial standards for high frequency digital signals which are carried over twisted pair cables. LVDS has been in use for the past two decades, and SLVS is a lower power standard adopted more recently.

frame, with a frame clock at 40 MHz and a bit clock at 480 MHz (12-bit case) or 640 MHz (16-bit case). The bit clock will be generated either by the ADC itself, by the GBTx (320 MHz), or by the LOCx2 (640 MHz).

The development of high-precision fast ADCs for the LAr readout has been pursued for several years with future electronics upgrades (through Phase-II) in mind. The main challenge is to cover the full 16-bit dynamic range with one or more ADCs per channel. In any case, the low power requirement is essential; this has been the main purpose of the LAr custom ASIC R&D efforts and will continue to drive the design effort for the main readout of the calorimeter in Phase-II. This long-term development has given rise to the design of a fully operational multi-channel 12-bit device that could be used for the Phase-I trigger electronics upgrade with the potential for a significant reduction in power consumption. However, given the uncertainty and cost associated with a custom chip design, an extensive search has been conducted for a commercial off-the-shelf (COTS) option meeting the electrical and radiation requirements.

There are two custom ASIC developments, based on the IBM CMOS8RF (130 nm) technology, which has been chosen because of its established CERN procurement contract, its radiation tolerance for digital circuits, and its anticipated use for LHC upgrades, enabling sharing of experience and re-use of building blocks developed by others. The two ASIC approaches are at different stages of prototyping and are described below. A COTS option (the Texas Instruments ADS5272) has been also identified as candidate for the LTDB. A demonstrator LTDB is being designed with this ADC (see Appendix D).

The LAr Collaboration will make the final decision on the ADC for the LDTB when test results are available from the two ASIC ADCs and experience is obtained with the system implementation of the ADS5272. The schedule for this decision is discussed in Chapter 6.

Table 10. Specifications for the ADC. The ADC must have a serial output using either standard LVDS or SLVS technology. The ADC word must be either 12-bit or 16-bit in one frame, with a frame clock at 40 MHz and a bit clock at 480 MHz (12-bit case) or 640 MHz (16-bit case). The latency is the time between the first sample and the last bit out. The power consumption is given per ADC channel at 40 MSPS. For comparison, values for the COTS TI ADS5275 ADC are given in the third column.

Parameters	Requirement	ADS5272
Sampling rate	$\geq$ 40 MSPS	40 MSPS
Dynamic range	12 bits	12 bits
Resolution (ENOB)	$\geq$ 11	11.5
Differential Nonlinearity	$\leq$ 1 lsb	0.3 lsb
Integral Nonlinearity	$\leq$ 1 lsb	0.4 lsb
Latency	$\leq$ 200 ns	162.5 ns
Power consumption	$\leq$ 145 mW	113 mW

COTS TI ADS5272 ADC

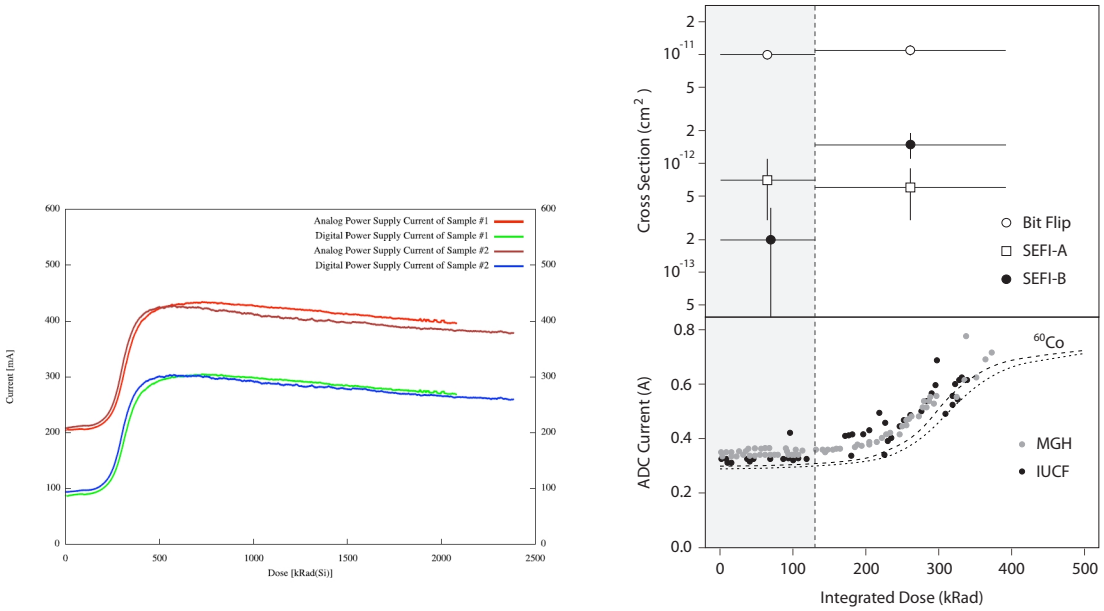
After screening a total of 17 COTS ADCs from different manufacturers with dynamic range, latency and sampling rate meeting the requirements to be used on the LTDB, the TI ADS5272, with one frame clock and one bit clock for the 8 channel serial outputs in an 80HTQFP package, was identified to be the best COTS candidate that is radiation tolerant (both in TID and SEE).

At the end of the HL-LHC operations (i.e., an integrated luminosity of $3000\,\text{fb}^{-1}$), the estimated TID is approximately 100 Gy(Si) and the estimated hadron flux is 1.3×10^{13} particles h/cm^2 (>

20 MeV). Applying recommended safety factors [6] that take into account simulation uncertainties (1.5), low dose rate effects (5), and lot-to-lot variations (4), the total TID qualification dose is 3.0 kGy(Si). If the 5,000 ADC devices needed for the LTDB production can be made with a single wafer production batch, the total TID qualification dose is reduced down to 750 Gy(Si) or 75 kRad. If the devices satisfy ATLAS policies [25] to establish the sensitivity to enhanced low dose rate effects, the qualification dose cold be further reduced down to 150 Gy(Si) or 15 kRad.

The 17 COTS ADCs were subjected to ^{60}Co gamma irradiation. One device, the TI ADS5272, outperformed all other tested ADCs, surviving after 88 kGy(Si), while the next best device failed after 23 kGy(Si) and the majority of the devices stopped working after less than 2 kGy(Si). Following this selection, more extensive TID and SEE tests are being performed on the ADS5272 in order to measure radiation sensitivity to all relevant ADC characteristics. Power consumption, signal amplitude and noise were measured as a function of the dose up to 25 kGy(Si) at dose rates of 140 Gy/h (Fig.33(a)). Subsequent irradiation of up to 3 kGy(Si) at a dose rate of 12.6 Gy/h was also carried out to identify possible low dose rate effects. Results from these tests have shown no significant difference from the tests at the higher dose rate. Tests under conditions described in [25] are also showing that no significant degradation of the performance before and after accelerated aging under bias.

Initial SEE testing used a spallation neutron source with a maximum neutron energy of 800 MeV (the energy spectrum is similar to the one expected at the LHC at the position where the LTDB will be placed). These tests identified 13 instances of SEE after 2×10^{13} n/cm^2. Results of more extensive tests conducted at 200-MeV high-flux proton facilities are summarized in Fig. 33(b) and identified two types of Single Effect Functional Interrupts (SEFIs): SEFI-A, after which a reset signal was enough to restore the device to its functional state, and SEFI-B, after which a power cycle needed to be issued to restore the ADC.



(a) (b)

Figure 33. (a) Current drawn by 2 TI ADS5272 test samples as a function of irradiation dose (^{60}Co). (b) Results of SEE performed at two different 200 MeV high flux protons beam facilities (MGH and IUCF). Besides single bit-flips, both SEFI-A (reset signal recovered upsets) and SEFI-B (power-cycle recovered upsets) were detected during these tests. The increase of power consumption due to the absorbed dose follows the one observed during ^{60}Co irradiation (dotted line).

ASIC ADC Developments

4-stage SAR-based pipeline ADC

The development is based on the IBM CMOS8RF technology and aims at developing a 12-bit digitizer based on 4 pipeline stages each followed by a successive approximation register (SAR) ADC block. Three test ASICs have been fabricated:

- The nevis09 chip contained an amplifier design which is at the core of the ADC's pipeline stages, and crucial to the ADC accuracy. This chip focused on the core of the design, but also allowed the team to learn about the technology, acquire experience with testing of high precision analog devices, and verify the radiation tolerance of IBM CMOS8RF technology for analog designs.

- The nevis10 chip [26] contained two ADC channels, each with four stages at 1.5 bits/stage, designed to determine the four most significant bits. The analog residue was sent to a commercial ADC to determine the lower eight bits. In each stage, having three possible output codes ("1.5 bits") to resolve one bit allows the application of digital error correction, which is necessary to compensate for the limitations in capacitor matching in the chosen technology. Extensive testing and side-by-side comparison with a commercial 12-bit ADC showed that the analog performance of the nevis10 chip was at least as good as that of the commercial device, reaching 11.7 ENOB at full scale with an integral nonlinearity (INL) just below one lsb and a differential nonlinearity (DNL) at 0.3 lsb. The chip was tested for cross-talk but none could be seen. Furthermore, no measurable degradation in performance was observed after irradiation up to 10 MRad.

- The nevis12 chip, shown in Fig. 34, implements two 12-bit ADC channels, each with four pipeline stages (similar to those in nevis10) followed by an 8-bit successive approximation register (SAR) ADC block, and includes all necessary infrastructure blocks (V and I reference, on-chip digital error correction, output serialization). The chip consumes under 50 mW per channel and has a latency of 87.5 ns. In terms of analog performance, nevis12 has so far been measured to reach at least 11 ENOB, and two limiting factors have been identified: the impedance of the reference voltage drivers and the distribution of the 640 MHz clock. The Fast Fourier Transform result for a 10 MHz sine wave is shown in Fig. 34. Testing for SEE sensitivity is scheduled for September 2013.

Solutions to the two factors limiting nevis12 analog performance have been designed and will be implemented in a quad-channel prototype chip which will also include an I2C control interface. This chip will probably be submitted in late 2013.

A full SAR-based architecture ADC

This design employs a full SAR architecture with a fully differential configuration to reduce power consumption and minimize latency. This ADC is named PEALL for a Power Efficient and Low Latency analog to digital converter.

The primary known advantages for a classical SAR ADC are low power consumption, low latency, high resolution and accuracy, and a small footprint. The SAR architecture offers the major advantage that any error or drift from the reference nominal values produces just a simple offset in the output characteristics, but will not lead to nonlinearities.

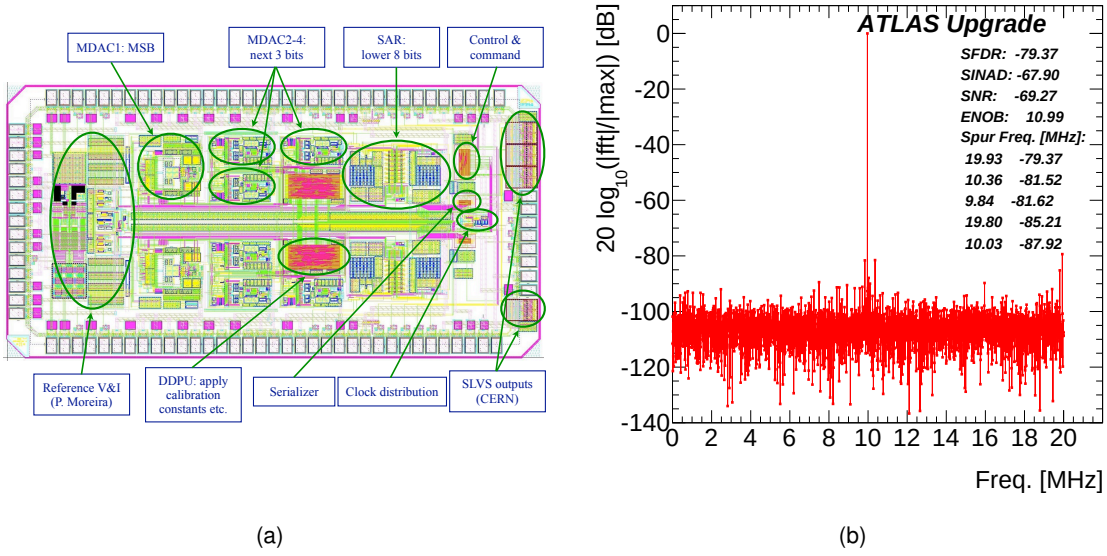


Figure 34. (a) Layout of the nevis12 chip; (b) Fast Fourier Transform result from the nevis12 chip for a 10 MHz sine wave input.

The main limitation of the SAR architecture is the requirement that the DAC block must be as accurate as the overall converter. Therefore, a careful layout is necessary. The comparator must be fast and must display low noise features. Also, the reference voltage drivers need to be capable of providing a very high frequency current pulse to the DAC capacitors.

The IBM CMOS8RF technology chosen for the PEALL ASIC appears to be fast enough to increase the sampling rate up to 40 MSPS. To deal with the matching limitations, a set of MIM capacitors is used for the differential DAC with a trimming feature to adjust the mismatch problems. The layout is carefully designed to reduce the effect of parasitic capacitance.

An important point of this design is the management of the high speed clock that is necessary to reach 40 MSPS. Usually, in order to obtain a 12-bit resolution, a 480 MHz clock is required, which consumes power. In this design, a local clock generator is already embedded. From the basic 40 MHz, it produces all the high speed clock phases for the SAR steps. No external clock management chip is necessary. A simplified scheme for one converter channel is shown in Fig. 35.

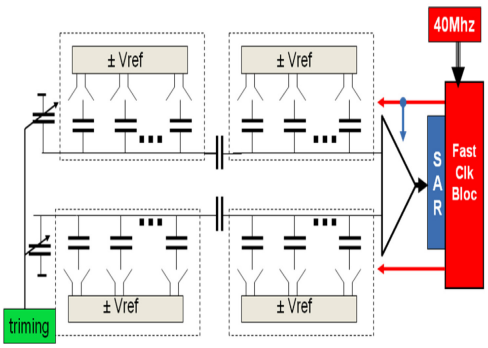


Figure 35. PEALL ADC simplified block diagram

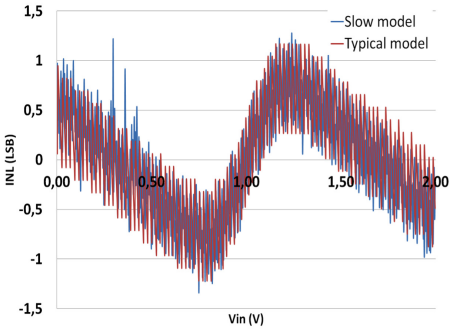


Figure 36. Linearity simulations for PEALL4

The first prototype with two 12-bit ADC channels was tested extensively in May 2013, reaching a

sampling frequency of 20 MSPS. These tests confirmed that the local clock generator was working properly. The power consumption per SAR ADC channel was estimated to be below 10 mW, the Total Harmonic Distortion (THD) was -60 dB and the spurious-free dynamic range (SFDR) was 60 dB. However, this design suffers from sampling noise at the reference voltage nodes located on the outside of the chip. The INL measured over the full range was about ± 4 LSB.

The most recent test chip, PEALL4, is a four-channel ADC design and will be available for testing by the end of November 2013. This new design includes an embedded reference voltage which was added in order to avoid the noise issues observed in the first design and also to improve the linearity. However, this can only be achieved at the expense of extra power consumption. The total power dissipation is expected to be below 30 mW/ch (including reference voltage). The linearity simulation results are shown in Fig. 36. The INL is about ± 1 LSB for both the typical and slow model configurations. These simulations confirm the robustness of the new integrated reference, which will be verified through measurements.

4.1.3.3.3 Digital data preparation As shown in Fig. 32. there are two optical links that connect the LTDB with the backend electronics. The data link transmits data from the LTDB to the back end, while the control link provides the TTC signal to the LTDB and transmits control and monitoring information between the LTDB and the back end.

The two-channel serializer ASIC, called LOCx2, is being designed to perform the data preparation and serialization. It has 5 key functional blocks: (1) the LOCic (discussed below), (2) an 8:1 multiplexier, (3) a clock unit called LC-PLL, (4) a CML Driver, and (5) an I2C Slave. The block diagram for this ASIC is shown in Fig. 37. The two channels share one LC-PLL based clock unit to save power. This ASIC is especially designed to transmit the ADC data, and the input matches the choice of ADC for the LTDB. Also taken into consideration are low power dissipation and low transmission latency (the parallel input to the LOCx2 runs at 640 MHz). The choice of 0.25 μm silicon-on-sapphire CMOS technology provides the needed radiation tolerance for LAr [27].

Digital data from the ADC comes in LVDS or SLVS format with a bit clock and an ADC-serial-output-frame clock. These data are prepared for high speed serial transmission over fibers in which there are no separate channels to transmit the two clocks, so they are encoded by the Frame Builder into the serial bit stream and are recovered at the receiving end of the optical link. In framing the data, a BCID and a CRC (cyclic redundancy check) are also inserted. Finally the framed data is scrambled to maintain DC-balance in the transmission. The diagram in Fig. 38 illustrates the functions of this data preparation unit, called the LOCic, embedded in the serializer ASIC.

Prototypes of the multiplexer, the CML driver, the LC-PLL clock unit, and the I2C slave exist, and all are measured to meet the design specifications. The multiplexer and CML driver have been demonstrated to operate above 8 Gbps. The LC-PLL clock unit is checked to run at 4 GHz with a tuning range of about 20%, suitable for a data rate of 8 Gbps. The design of the LOCic has passed post layout simulation and will be prototyped with a multi-project wafer run in Oct. 2013.

If the LOCx2 chip does not become available on the required time scale, we have considered the problems associated with using the ASICs and optical transmitters being developed by CERN and the Versatile Link Collaboration for the LTDB data link. Using the GBTx and the VTTx in the transmitting side of this link has been investigated with the three ADC candidates and the three GBTx data encoding modes. In all cases involving the GBT, the latency of the transmitting side would vary from 212.5 ns to 237.5 ns, depending on the GBTx encoding mode, whereas the latency using the LOCx2-MTx combination is 75.9 ns. The power consumption using the GBTx and VTTx is estimated to range from 48 W (with an ASIC ADC and the GBTx in wide bus mode) to 96 W (with the ADS5272 and the GBTx in FEC mode), whereas the power consumption for the LOCx2-MTx pair is estimated to be no greater than 32 W. The GBTx is a general purpose serializer and de-serializer

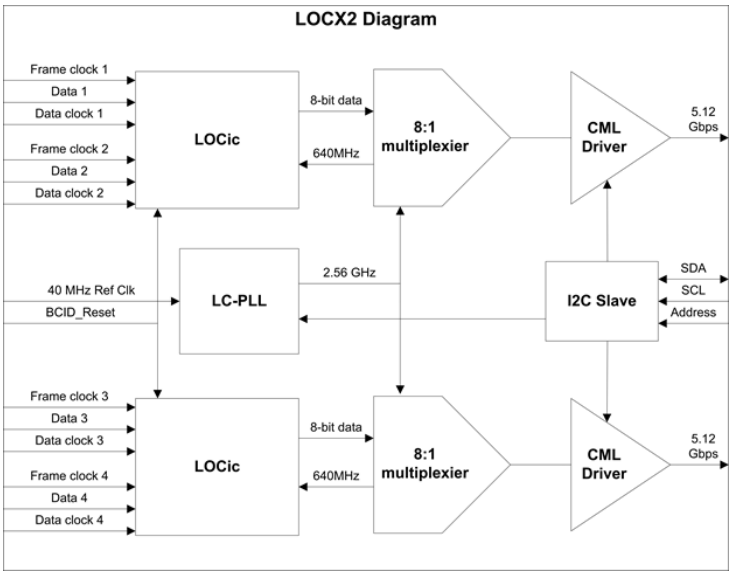


Figure 37. LOCx2 block diagram. The ADC data and clocks come from the left into the LOCic, the interface unit that prepares the ADC data for serial transmission. Downstream of the LOCic, data is serialized into a bit stream by an 8:1 multiplexer. The CML driver sends the 5.12 Gbps serial data out of the ASIC. The two data channels share the LC-PLL based clock unit that provides all the clocks needed in this ASIC. The entire chip is controlled by the I2C slave.

ASIC with its custom e-port I/O interface. To use the GBTx on the LTDB, this e-port will either need to be integrated into the ADC ASIC, or a special ASIC will need to be developed to interface the GBTx to the ADS5272. Should the LOCx2-MTx based solution to the data link not be available, the group working on the LOCx2-MTx solution could investigate a GBT-VTTx based solution, as this same group is using the GBT and VTRx (see Sec. 4.1.3.3.1) for the control link. Were an ASIC ADC candidate to be chosen, that ADC would need to incorporate the e-port in its circuit, or an interface ASIC would need to be designed to translate the ADC output data (described in Sec. 4.1.3.3.2) to the input of the GBTx.

4.1.3.3.4 Digital data transmission After the data preparation described above, data of 8 ADC channels are multiplexed into a bit stream of 5.12 Gbps and sent out of the LOCx2 in CML format. This electrical signal is amplified by the VCSEL driver ASIC, LOCld, that provides current swings of sufficient magnitude to modulate a VCSEL. The VCSEL converts the electrical signal into an optical signal and launches it into an optical fiber. The LOCld ASIC and the VCSEL are assembled into an optical subassembly, called MTx. A mezzanine for the MTx is used because the VCSEL requires manual soldering to the PCB, and the testing of optical coupling and adjustments to the VCSEL must be carried out manually. Other reasons for the MTx to be a mezzanine card are integrity of the fast (5.12 Gbps) signals and a routing of the fiber from the VCSEL to the LTDB front panel which respects the minimum fiber bending radius.

The LOCld is prototyped to operate above 8 Gbps. A full LOCld design with I2C and configuration has been evaluated in the lab. This prototype chip will be packaged in QFN-28 and further tests will follow.

There will be 20 MTx modules per LTDB to transmit the data to the back end. Each MTx contains 2 optical channels driven by the dual output of the LOCx2. There is not enough front panel space to accommodate 20 panel-mounted units and thus the MTx must be board mounted. The

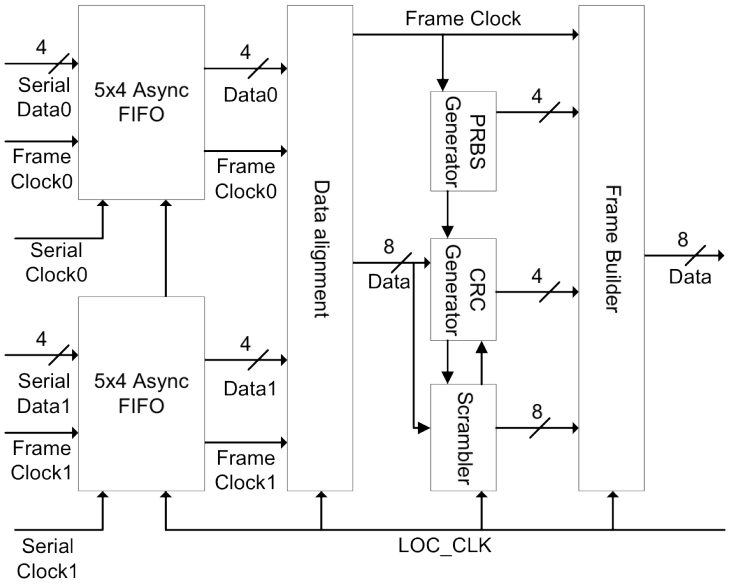


Figure 38. Block diagram of the LOCic, a digital unit in LOCx2 that prepares the ADC data for the serializer. The dual-clock asynchronous FIFO is required to be able to function with ADCs with a 12 bit output at 480 MHz bit rate. Four extra bits are inserted to change the bit rate to 640 MHz and to provide space for framing the data for serial transmission. In the case of the ASIC ADC with 16 bit output of which 14 bits are valid data (12-bit in data mode and 14-bit in calibration mode), the 2 bits that are not valid data in the ASIC output are used for data framing. Data alignment is only needed with the 4-channel ADC to align the two ADC chips (8 channels total) for the serializer. A fixed 4-bit plus the pseudo-random bit sequence are used as the framer, as well as the BCID counter. A pipeline structure is used in the CRC generation and scrambling of the data bits to achieve 640 MHz processing speed. Finally the framer is added to scrambled data to form an 8-bit parallel transmission frame.

Table 11. Data link optical link power budget for the LTDB (MTx) and LDPS (microPOD) connection.

Parameter	Spec	Note
Min Tx Optical modulation amplitude (OMA)	-5.2 dBm	Conservative value taken from triple tradeoff curve (RMS spectral width, center wavelength, Tx OMA)
Max unstressed Rx sensitivity	-10.4 dBm	Spec'd at 10G, can run better at 5 Gbps
Power budget	5.2 dB	
Fiber attenuation	0.3 dB	70 meter, OM3, 3.5dB/km
Connector loss	1.5 dB	3 connections if 0.5dB per insertion loss 4 connections if 0.375dB per connector
Link penalties	1.0 dB	Fiber bandwidth limit not reached, most contribution from noise rather than closure (ISI, etc.)
Jitter contribution	0.4 dB	If microPOD as backend. To be verified.
Radiation penalties	0.1 dB	Calorimeter grade, mostly from fiber
Margin	1.9 **dB**	

clearance between the cooling plates and the LTDB motherboard is 6 mm. To avoid a cut-out (see Sec. 4.1.3.5.2) in the LTDB motherboard which could compromise its mechanical integrity, an MTx is being developed with a form factor that is defined by the size of the LC packaged TOSA. The size of the MTx is 15mm $\times$ 45 mm $\times$ 6.3 mm. The height of the MTx could be trimmed down to 6.0 mm if needed. A prototype MTx based on a COTS VCSEL driver has been tested up to 10 Gbps, demonstrating that the driving circuit and the optical coupling of the MTx meet the requirement of 5.12 Gbps data transmission.

Table 11 lists the optical power budget to ensure proper function of each fiber channel.

4.1.3.4 Power and cooling Since the new LTDB will have to operate after the Phase-II upgrade, the design of the power scheme will have to take into account this forward compatibility. A modular design is being considered that would allow the power modules to be replaced during the Phase-II upgrade to accommodate the voltage rails from a new low voltage power supply for a FEC. Both point-of-load converters and linear regulators developed by CERN will be used; the former is favorable for high efficiency, and the latter is preferred to achieve better analog performance.

The estimate of the total power consumption of a 320-channel LTDB is shown in Table 12, where one sees the total power budget is ~ 156 W. This estimate takes into account the power dissipation of the voltage regulator and the efficiency of the point of load converter, and the power loss due to these converters is also shown in the table.

Six of the seven voltage lines from the low voltage power supply are used in the LTDB (+6 VA, +6 VD, +4 V, -4.25 V, +7 V, and -7 V). Regulated power is required at the following voltages: $\pm$5 V, $\pm$2.5 V, +1.5 V, +2 V, +2.5V, and +3.3V.

Concerning the availability of units, the CERN linear voltage regulators are becoming available; ST has fabricated chips which, at the time of this writing (July 2013) are being evaluated for radiation tolerance. The CERN POL converter is being designed, and a prototype should become available at the end of 2013. A project is under way in which LAr will utilize the POL controller ASIC developed at CERN and rearrange the components to make a POL suitable for LTDB usage. Even though the CERN POL converter and linear regulators meet the LAr specifications for the LTDB, COTS units are being actively investigated to mitigate the risk of failure or delay of the custom components. In one of our present designs, we will require 24 POL modules and 3 voltage regulators of each polarity per LTDB.

The use of the current cooling system for the FE electronics is foreseen. As in the FEBs, water channelled through aluminum cooling plates will be used to cool the LTDB in the FEC. The fabrication of cooling plates will use known technology from the cooling plates production for the FEBs: roll-bonding with tungsten inert gas (TIG) aluminum welding on the inlet/outlet channels. The cooling blocks are injection molded using Ultem GM plastic, they will be used to interface the cooling plates to the flexible hoses and ultimately to the cooling manifolds installed in ATLAS. Two water cooling channels will be implemented on the new plates to take care of ~ 160 W power dissipation. A thermal study will be conducted once the mechanical model of the LTDB is available; this will provide guidance for a new cooling plate design.

The current operation of the FE electronics requires cooling of approximately 160 kW of electrical power generated mostly at the FEBs (125 kW) and the FE power supplies (35 kW). This is achieved with a heat exchanging system which typically operates at a capacity of 210 kW from a mixed water source running 600 l/min and allowing for a 5^oC water temperature increase in the heat exchanger (corresponding to only a 2^oC increase in the FE water flowing through the cooling plates). These values are to be compared with an increase of 20 kW (156 W*124 LTDBs) consumption which can well be taken care of allowing for a slight increase (0.5^oC) in the heat exchanger temperature gradient. The excess cooling capacity was built into the original system to allow for possible increases

of the FEB consumption after radiation, which does not appear to be needed. Thus there is some headroom available.

Table 12. Estimate of the total power consumption of a 320-channel LTDB. Estimates of power consumed by the circuitry (regulated power) and the that consumed by the converters (POL and voltage regulators) are shown separately.

Section	Reg. Power (W)	Converters (W)	Total Power (W)
Analog Section	29.4	12.2	41.7
COTS ADC	37.0	9.2	46.2
Data link	28.7	7.2	35.9
TTC link	22.1	5.5	27.6
Aux	4.0	1.0	5.0
Total	121.1	35.2	156.4

4.1.3.5 Implementation of the LTDB The way in which the LTDB circuitry should be implemented has not yet been decided, as there are research efforts under way to understand a variety of issues, some associated with performance, others associated with availability of components, and still others with manufacturability, reliability, and maintainability of the system. Currently there are within the LAr Front End Electronics two systems which may be taken as models for the LTDB system: the FEB, with a common motherboard for all types of calorimeters with analog mezzanines to meet different requirements for different subdetectors, and the TBB/TDB system, where analog components are mounted directly on the motherboard, and different flavors of motherboard are used in each of the different subdectors. Both of these systems have performed remarkably well with low maintenance since the beginning of the experiment.

One of the most challenging technical requirements for the LTDB is the optical data link. Within the LAr community there has been a long-term effort for the development of an optical link system that is able to transmit data from the LTDB to the LDPS at a data rate of 5.12 Gbps per fiber, or 217.6 Gbps per LTDB using 40 fibers. The R&D has concentrated on the ASIC technology evaluation [27], two ASIC prototypes, LOCx2 and LOCiC, discussed above (in Sec. 4.1.3.3.3) and a small format optical transmitter module, the MTx.

Indeed, one of the key issues for the LTDB is the physical size of the optical transmitter for the data link and how it relates to the geometry of a water-cooled module in the FEC. In order to be able to mount the transceiver on the motherboard, the maximum acceptable height is close to 6 mm, and a unit of this size does not yet exist. In order to use existing transceivers (in particular the VTTX of the Versatile Link Project) it is necessary to modify either the motherboard or the cooling plate to accomodate the transmitter. The MTx is specifically designed to be small enough to fit in the space between the LTDB motherboard and the cooling plate. Thus one of the concepts for the LTDB (LTDB with digital motherboard) which relies on the successful development of the MTx is to develop a system like the FEB, where a common motherboard containing digital components is used in all regions, with analog mezzanines to handle the various requirements of the different subdetectors. The other concept (LTDB with analog motherboard) is to develop a module which can accept a larger optical transmitter by using a digital mezzanine board with a cutout in the motherboard to utilize all of the space between the two cooling plates. Each approach has its strengths and weaknesses, and both are being pursued in order to understand them better. Based on this research, the collaboration plans to reach a decision on which path to follow in 2014, as is detailed in Sec. 6.2. A brief account

of each of these research efforts is given in the following two sections.

4.1.3.5.1 LTDB with digital motherboard In order to reduce development effort, it is desirable that the different flavors of LTDBs share a common design as much as possible. One solution is to use a common digital motherboard with analog mezzanine cards. The digital motherboard is responsible for signal digitization, data aggregation and serialization, and optical transmission. The analog mezzanine card will receive Super Cell signals, form layer sum signals, and drive the ADC. It is expected that different analog mezzanine cards may be used in different LAr sub-detectors, however a precise implementation will follow a detailed design.

With the digital motherboard solution, major components of the digital section will be placed on the motherboard. For the data link path, this includes the ADC, LOCx2 and MTx described above. The TTC link path is mainly comprised of components developed by CERN. The GBTx and GBT-SCA chipset will be implemented on the motherboard, whereas the VTRx will be mounted on a small mezzanine card to offset the large stacking height which prevents the component to fit into the envelope of the existing mechanical assembly of cooling plates. However a repackaging of VTRx is also being investigated, aiming to have the mechanical design of the optical transceiver optimized to a small form factor, in which case the VTRx will also be mounted directly on the motherboard.

The common digital motherboard of the LTDB will have four sub-sections; each sub-section can process up to 80 Super Cell signals. Analog mezzanine boards contain 40 channels and will be mounted on both sides of the digital motherboard. Each LTDB will have a maximum of 8 analog mezzanines, with 4 on each side. Each optical link will run at 5.12Gbps which can transmit samples of 8 Super Cells. Thus a total of 40 optical links or 20 MTx will be used to transmit data out of detector to the backend Digital Processing System (DPS). There will be one TTC link for each of four sub-sections, with the GBTx and GBT-SCA responsible for configuration of custom chips, clock distribution and monitoring. With a dedicated TTC link for each sub-section, the four sub-sections on LTDB will be independent in terms of communication with the backend system.

Some of the advantages of the digital motherboard implementation are :

- A common digital motherboard design can be used for all sub-detectors, and no board level reconfiguration is needed; different analog treatments for different sub-detectors are realized through the use of different flavors of analog mezzanines.
- The motherboard layout has four identical but independent 80-channel sections that can be populated based on the needs of different sub-detectors; thus economies can be realized if certain assembled LTDB modules are dedicated for certain sub-detectors.
- Although a detailed design has not yet been carried out, our goal is to use a common layout for all flavors of the analog mezzanine board through the use of different component stuffing options.
- With a stacking height of 6 mm for the MTx design, all major digital components can be mounted directly on the motherboard, thus requiring no cut-out of the motherboard which could compromise the mechanical integrity of the LTDB.
- The MTx is itself an optical mezzanine assembly; it can be mounted directly on the motherboard, which avoids reliability issues associated with mezzanine-on-mezzanine design.
- The analog mezzanine board can use a low density connector with low current per pin requirements. A stacking height of 3 mm will permit components to be mounted on both sides of the board, thus increasing the effective board area, which permits a reduction in component density.

- With a low power mezzanine board, no special care is needed for board level cooling; the existing aluminum roll bonding technique will be adequate for cooling plate construction.

- Since digital circuits consume approximately 3/4 of the LTDB power budget (see Table 12), mounting these components on the motherboard simplifies the design of power distribution and eliminates the need for a high current per pin mezzanine connector.

- A digital motherboard with analog mezzanine makes for efficient development, evaluation and acceptance testing. The analog mezzanine design can be evaluated and optimized thoroughly before final integration on the digital motherboard, while the digital motherboard will be developed and evaluated separately with a focus on its digital functions. This approach has been proven to be successful during the current FEB design and production.

As stated above, a goal of the analog mezzanine design is to have a common layout with different component population options to equip different parts of the various sub-detectors. Assuming that a different gain is required for each value of η, each analog mezzanine on the LTDB will have a specific configuration, which will result in 8 different flavors of analog mezzanine on a 320-ch LTDB. A summary of different analog mezzanine types is shown in Table 13, where it is seen that a total 920 analog mezzanine boards with 44 different flavors will be needed to equip the full LAr detectors. Alternatively, if the analog gains are uniform and the pseudorapidity-dependent part of the calibration applied in the backend electronics, the number of analog mezzanine flavors could be optimized and reduced. For the existing EMB and EMEC standard baseplane layouts, the number of flavors could be reduced from 16 to 4. This is ongoing work, and the mezzanine flavors required for other sub-detectors will be examined once the design of the baseplanes are completed.

A 1/4 slice LTDB prototype has been built and is being tested. A picture of this board is shown in Fig. 39. It has one digital motherboard and two analog mezzanines. The 1/4 slice digital motherboard hosts 10 COTS ADC, TI ADS5272, servicing a total of 80 channels, and 1 Xilinx Kintex-7 FPGA which is used to reorganize and serialize the ADC data. The serialized ADC data is transmitted by an Avago PPOD optical transmitter via an optical link to the backend DSP. The TTC link is implemented by an SFP optical transceiver which communicates with a CERN-developed GLIB board. Each analog mezzanine board processes 40 channels of Super Cell cell signals, and the ADI AD8011 and Intersil HFA1134 are used to buffer and sum Super Cell signals, while the TI THS4522 is used to drive differential signals to the ADC. A digitized waveform produced by this unit is shown in Fig. 40.

The 1/4 slice LTDB serves as a test bed for a proof of principle design of the LTDB, though some components on the digital motherboard are not radiation tolerant. The analog waveforms can be digitized and read out correctly, and a more detailed test is ongoing now. The test results will feed back to the design of full size LTDB demonstrator which is planned to be installed on detector by mid 2014 (see appendix).

4.1.3.5.2 LTDB with analog motherboard Another possible implementation for the LTDB is to separate the analog and digital functionalities, putting all the analog functionalities on a motherboard, and the digital processing of the analog signals on mezzanines.

A sketch of this implementation is given in Fig. 41. Going from top to bottom, the analog signals coming from the calorimeter go first through the Front-End crate baseplane. They are then processed by the analog section of the LTDB, where the sums are performed, as discussed in Sec. 4.1.3.2. In addition to the analog sums, the analog section does the required conditioning before each individual signal is digitized and digitally processed : the analog signals are shaped by a $\simeq$ 15 ns pole (see Sec. B.1.2.2) and then sampled by the ADCs of the digital section.

Table 13. Summary of different analog mezzanine flavors, assuming the pseudorapidity-dependent gain adjustment is required, in which case each LTDB analog mezzanine board will have its own specific configuration. For this reason, this table represents an upper limit to the number of analog mezzanine flavors required. Note: Suffixes "0" and "1" serve to distinguish LTDB modules in cases where two LTDBs per baseplane are required.

Sub-detector	No. of types	No. of boards/type	Total No. of boards
EMB	8	64	512
EMEC Std	8	32	256
EMEC Spc 0	6	8	48
EMEC Spc 1	4	8	32
HEC	6	8	48
FCAL0	6	2	12
FCAL1	6	2	12
Totals	44		920

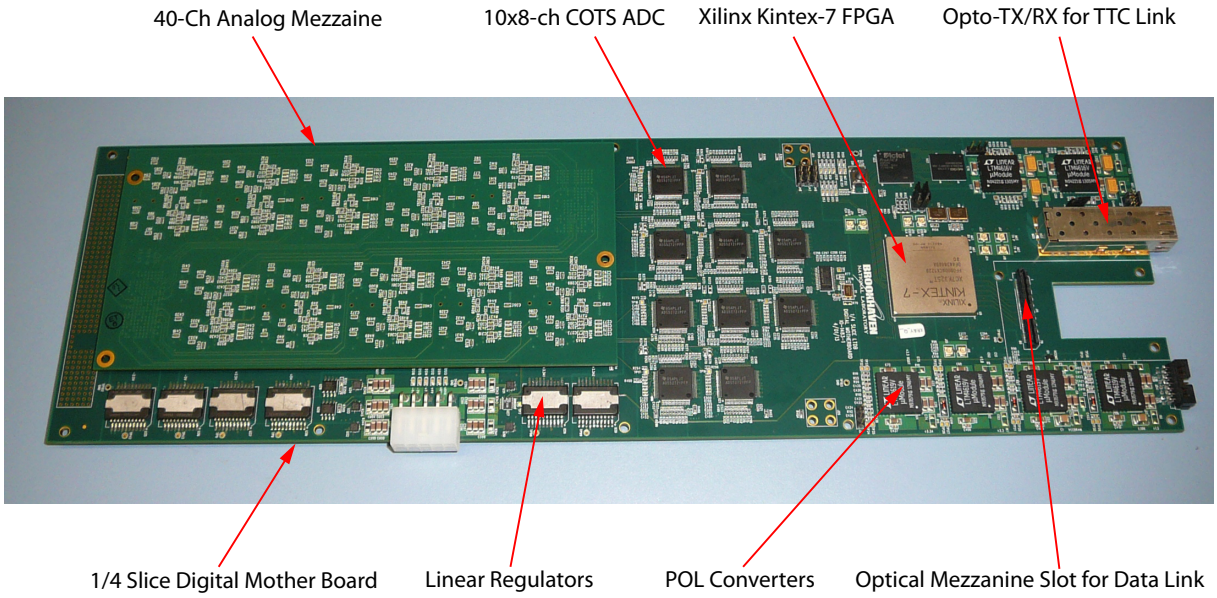


Figure 39. Photograph of the 1/4 slice LTDB prototype, which has one digital motherboard and two 40-channel analog mezzanines to process 80 Super Cell signals.

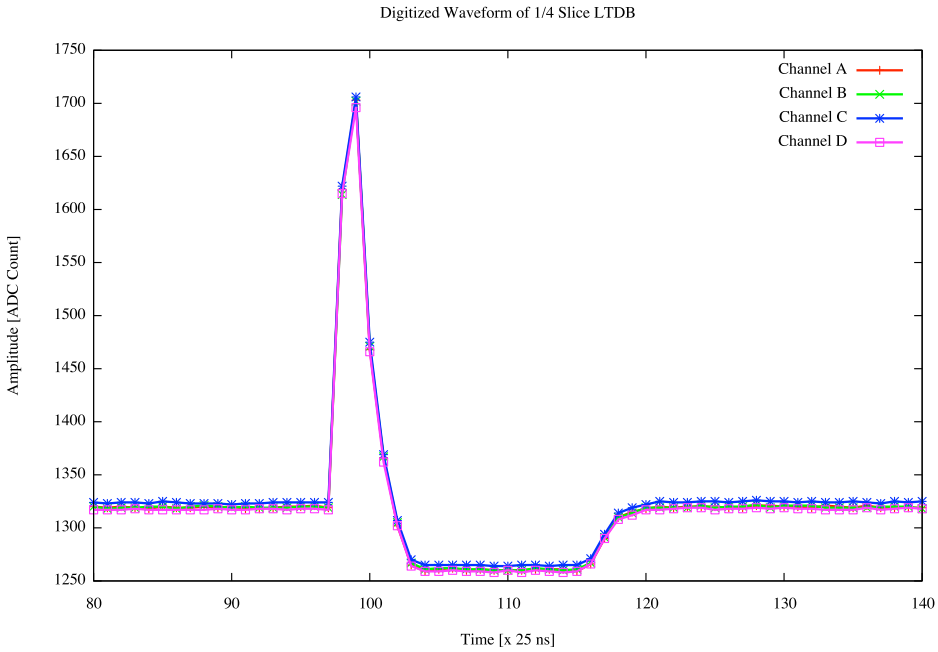


Figure 40. Four channels of a digitized waveform of the 1/4 slice LTDB prototype. The LAr detector signal is generated by an LTSpice simulation and then sent to a DAC running at 1.2 Gbps to inject the analog signal to the 1/4 slice LTDB. This signal is processed by the analog mezzanine, then digitized by the ADC on the digital motherboard. The digital data are read out by an on-board FPGA.

This digital section will be implemented as a mezzanine connected to the motherboard through a low profile connector. Each mezzanine will feature 32 ADC channels which digitize the analog Super Cell signals coming from the analog motherboard, and the required serializing means and optics drivers to prepare data to be output through an optical link. In addition, the digital mezzanines will feature timing and control circuitry.

There are several advantages to the analog motherboard solution, some of which are:

- The analog signal path is quite direct and simple. The analog signals transit from the analog to the digital section on differential lines through a connector, and high speed digital signals stay confined on the mezzanine. This minimizes possible interferences between the analog and digital sections, and leads naturally to low cross-talk, which is particularly important, since cross-talk generated on the LTDB could potentially be reinjected in the TBB, potentially modifying the performance of the legacy trigger system.

- The analog circuit would benefit from lower inductance grounding to the baseplane than one where the grounds must pass through a connector.

- The analog section is implemented with only simple, well understood components, such as op-amps, resistors and capacitors. The reliability of these components makes the analog section of the LTDB the right part to be put on the motherboard where repair and exchange of any part is potentially the most difficult.

- Since digital mezzanines have an offset with respect to the motherboard, they ease the integration of optical transceivers. Preliminary integration studies indicate that standard height (11 mm) optical transceivers can be accomodated without difficulty.

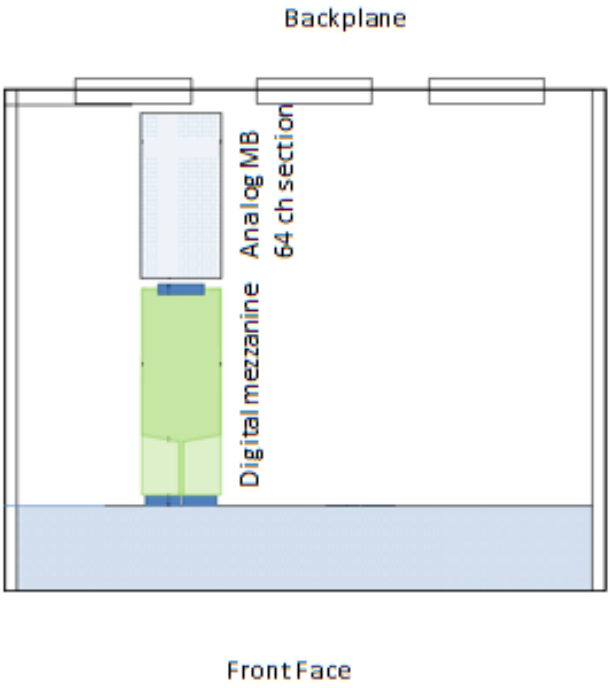


Figure 41. Global implementation of the analog motherboard solution. The green shaded region, indicating where the digital mezzanine board is located, corresponds to a cut-out in the motherboard.

- Digital components have on average significantly higher power dissipation than analog components (see Table 12). Since the dominant cooling mode in the Front-End crate is thermal conduction to the cooling plate, the dominant factor in cooling performance is the proximity to a cooling plate. From this point of view, digital mezzanines which reduce the slot gap, naturally favor cooling of the components.
- Digital components come in highly integrated packages. Having these components on digital mezzanines ensures better yield at the manufacturing stage, and easier rework if needed.
- Maintenance is generally more efficiently carried out when components are mounted on mezzanine boards.
- Finally, the digital section implements all the functionalities that are most likely to evolve over the future lifetime of ATLAS. Having these functionalities on a mezzanine will make the implementation of any evolution easier, since only the mezzanines will have to be redone.

The analog section implements for each Super Cell signal a constant gain (which will depend on pseudorapidity in the case where the lsb is fixed in transverse energy), an offset necessary to place the LAr signals in the full dynamic range of the ADCs, a single ended to differential conversion, and a $\simeq$ 15 ns pole, as on the schematics of Fig. 42. Other (passive) implementations of the pole have also been studied. For each group of four channels, there are two THS4522 differential op-amps plus a few resistors and capacitors. The summing of the four channels will make use of an AD8011 operational amplifier plus an HFA1135 limiting amplifier. It has been checked by designing and routing a 64 channel (1/5 of a full LTDB) prototype (see Fig. 43) that the available space for the analog section is sufficient.

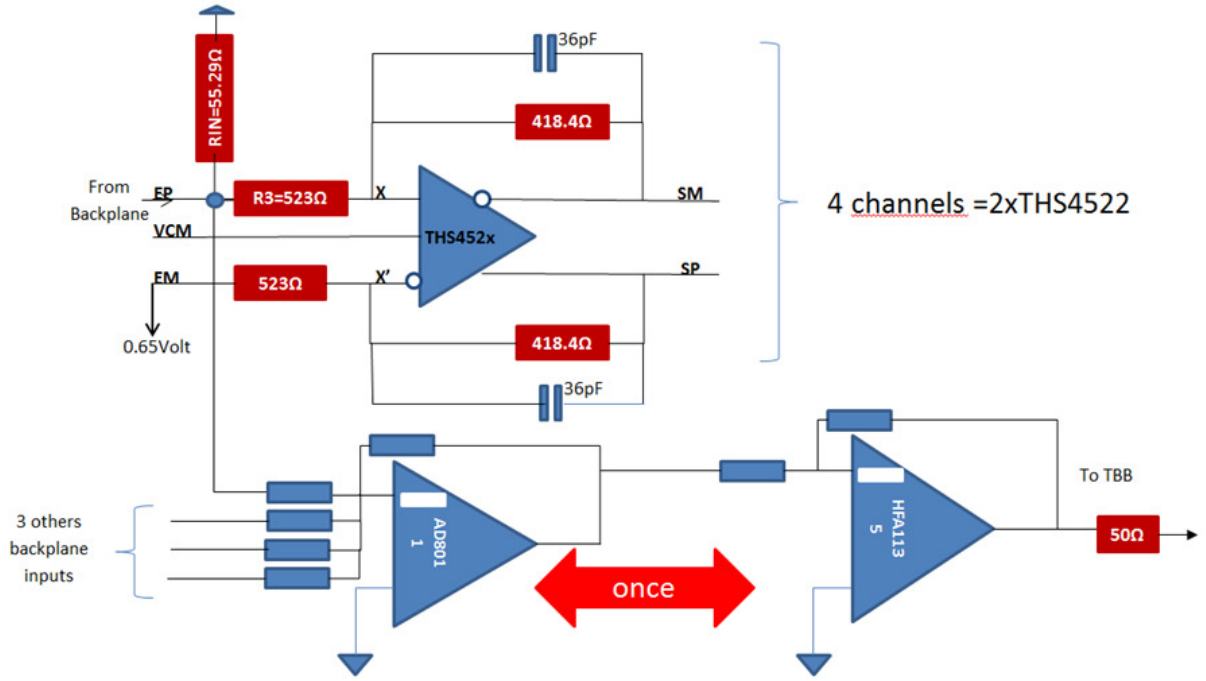


Figure 42. Schematics of the analog section, featuring a four channel summation

The global layout of the board, in accordance with the ten digital mezzanines is ten groups of 32 independent channels. Each of the ten groups features itself sub-groups of four channels, making the design very modular and easy to adapt to the different baseplane configurations. The mother board is fully symmetric with respect to its mid-plane, and is actually made of two (almost identical) six-layer PCBs stuck together.

Each of the ten groups of 32 channels will be connected to a digital mezzanine. There are five mezzanines on each side of the motherboard, connected through low profile connectors. Available candidate connectors have been identified and are under evaluation, like the Panasonic AXN400330S 100 pin 0.8 mm pitch connector. The two digital mezzanines facing each other will have their optical transceivers positioned head to tail.

There will be only one type of digital mezzanine, and typically seven types of motherboards, one each for the EMB, HEC, and EMEC standard baseplanes, and two each for the FCal and EMEC special baseplanes.

The motherboard will have a cut-out on the front-face edge about 70 mm wide to accommodate the routing of the optical fibers and optical transceivers. Special care will be taken to ensure the integration and mechanical integrity of the board, as well as an easy mounting in the Front-End crate, since the link between the Front-End crate guiding rails is ensured mainly by the part of the motherboard that is not cut out at the edge.

Four channels of the analog section have been built using evaluation kits. Preliminary tests have shown the performance to be perfectly adequate for the LTDB requirements, with a noise less than $\simeq$ 150 μV and a cross-talk of less than 0.1% . Particular attention will be paid to the potential noise and cross-talk coming through the voltage reference line.

The design of a prototype 64 channel motherboard section (see Fig. 43) has shown that the available space is sufficient for the implementation of the analog functionality, while leaving some margin for voltage references, power etc, and additional parts, in case the final analog design would require more components than described here. There is also adequate space to provide for the

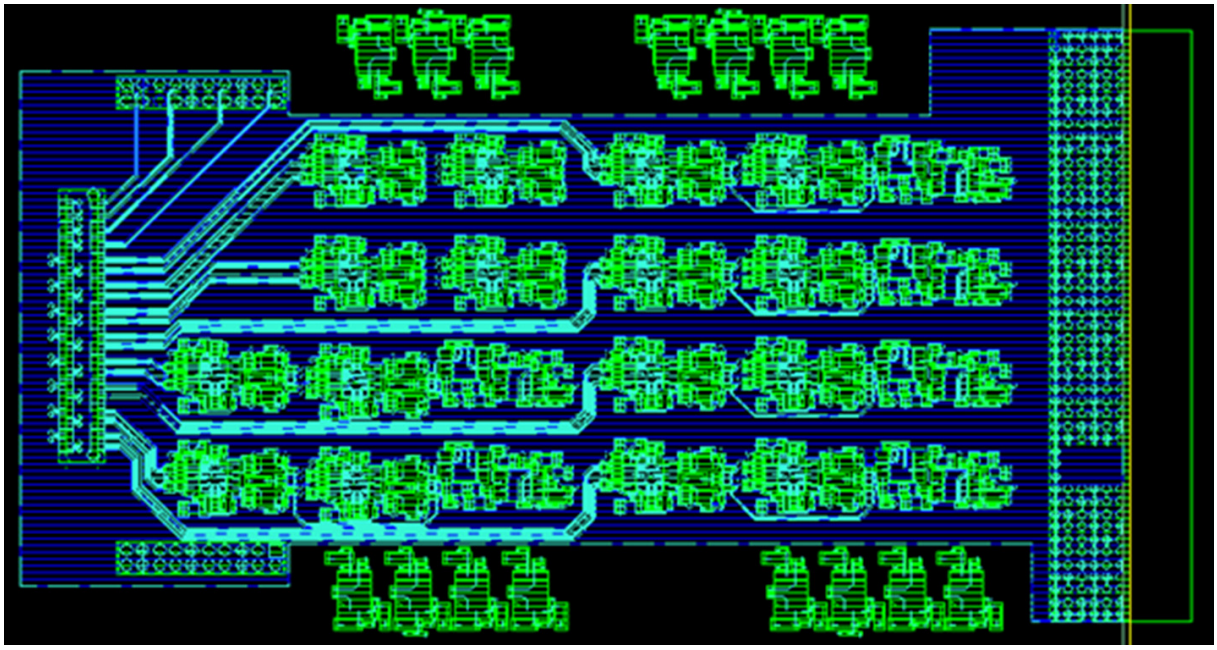


Figure 43. View of one face (representing 32 channels) of a 64 channel section motherboard prototype

crate monitoring functions discussed in the following section. A digital mezzanine, based on non rad-hard FPGAs and the chosen COTS (see Sec. 4.1.3.3.2) ADS5272 ADC is under design. The foreseen optical transceiver is the CERN standard VTTX. This mezzanine will be mated and tested with the analog motherboard prototype by october 2013. In parallel, the mechanical integration, the rigidity and the board insertion into a Front-End crate will be tested with a mechanical prototype by the end of 2013. At the same time, a full size 320 channel analog motherboard will be designed, produced and tested, also by the end of 2013.

4.1.3.6 Crate monitoring The Crate Monitoring Board (CMB) is a simple PCB installed in the FEC, which is used to access the FEC voltages and interface to the ELMB for monitoring. There is one CMB installed in each of the 58 FECs. Since no connection to the baseplane is required, the CMB is not a full-sized FE board. The CMB provides filtering of the FEC power via 500 μF ceramic capacitors mounted on each of the seven voltage lines. In addition, the CMB provides attenuated (202:1) copies of the voltages on an additional connector which is connected to the ELMB. The CMB uses the +11 V line from the FEC to power the analog section of the ELMB.

In the Phase-I upgrade, the CMB will be removed to free up a slot for the LTDB. Thus the LTDB design will include the functionalities of the current CMB for filtering, monitoring of front end low voltages, and supplying analog power to the ELMB.

4.1.3.7 Crate powering The electrical power required by the FE electronics is delivered by a "Low Voltage Power Supply" (LVPS). The LVPS is powered by 280VDC generated in USA15; it is made of DC-DC converters mounted on the detector adjacent to the corresponding FEC. A total of seven low voltage outputs of the LVPS are delivered via 10 2/0 AWG wires (1.5 m long) to the power busbar mounted on the FEC. All LVPSs have been exchanged in the LS1 with newly produced devices replacing the original ones which operated in ATLAS during the years 2010-2012 but had issues dating back to the design time.

During Phase-I operation, the LTDBs will need to draw their power from the LVPS on the detector.

The current power consumption amounts to less than 75% of the nominal power these supplies can deliver (3.2 kW), so sufficient power reserve for LTDB operation is available. However, this power will need to be drawn from voltage lines where current is available. On the 6V line, 64 amps are drawn from the 100A available; on the -4V line, 140A are drawn from the 180A available, and on the +4V line, 100A are drawn from the 130A available. Drawing current from these lines will also help to overcome the current limitations of 8A per pin on the connector which brings current from the power bus into the LTDBs.

4.1.4 Optical fibers

Fiber cables will need to be installed to dispatch the optical link signals from UX15 to USA15. As was done for the main ATLAS installation, the most convenient repartition is to route one cable to each FEC, with enough ribbons (and spares) to serve all connections. Thus a normal cable would need 10 12-fiber ribbons (plus spares) to connect to the two LTDBs in that crate. The choice of the fibers themselves is guided by radiation tests which have been performed for the ATLAS ID group[28].

The routing of these fibers will be rather important in order to limit the transit time (and therefore trigger latency). The fibers will be directly routed through the holes in the UX15-USA15 wall. The fiber cables from the EndCap calorimeters will need to be placed in the Sector 9 cable chain (which is the shortest) and from there traverse the holes to USA15. Preliminary studies have shown a possibility to place such fibers in the cable chain slots of the cryogenic pipes, with a pre-installation of a guiding system to insure a correct movement of all pipes and cables with the whole EndCap calorimeters onto garage or maintenance positions when opening up ATLAS. Some special effort might be needed to install these cables on inaccessible parts of the chains due to muon chambers, for example pulling the cables while moving the calorimeters and chains to their end-positions.

The length of the cables is well known from the original ATLAS installation and cables can be ordered complete with connectors. The ends of the cables with the connectors are protected during the placement.

The mapping of cables (LTDBs) to the back end electronics modules (see section 5.2.2) (LDPBs) will not be one-to-one; instead, it will be guided by optimal placing of Super Cell to Trigger Tower in a contiguous $\eta \times \phi$ space. It is inevitable to have mapping adjustments between LTDB output optical links and LDPS input optical links, for example, to have data from both EM barrel and EMEC processed on the same backend module to cover the transition region of EM calorimeter. A patch panel for these interchanges is envisaged. An alternative would be to explore the routing of fiber ribbons which come from different cables to a common location in the backend electronics.

4.2 System Integration of the FE electronics upgrade

4.2.1 EM Barrel Calorimeter

The electronics for the EM barrel (EMB) calorimeter are contained in 32 Front End Crates (16 on either end), each of which contains two baseplanes, all 64 of which are identical. The Super Cell dimensions for the EM barrel calorimeter are given in Table 14 for each sampling layer: presampler, front, middle, back, in units of $\Delta\eta \times \Delta\phi$ and in terms of the number of elementary of detector cells. The Super Cell dimensions correspond to dividing the current trigger tower layers ($\Delta\eta \times \Delta\phi = 0.1 \times 0.1$) in pseudorapidity by 1, 4, 4, and 1, respectively. In the barrel end region ($|\eta| > 1.4$), 4 Super Cells are produced from the front and middle layers for the LTDB as explained in Sec. 4.1.1.4.

With this granularity, the total number of Super Cells for a $2\pi/64$ section of the barrel EM calorimeter is 145. The signals from two such sections are handled by half a Front-End Crate, in which the corresponding trigger signals are handled by one LTDB (and one TBB).

Table 14. Size of the Super Cells in the EM barrel calorimeter, in terms of both elementary cells and $\Delta\eta$ and $\Delta\phi$. The number of Super Cells per LTDB are given in the column labelled N.

		Elementary cell	Super Cell		
η-range	Layer	$\Delta\eta \times \Delta\phi$	$n_\eta \times n_\phi$	$\Delta\eta \times \Delta\phi$	N
0-1.4	Presampler	0.025×0.1	4×1	0.1×0.1	28
	Front	0.003125×0.1	8×1	0.025×0.1	112
	Middle	0.025×0.025	1×4	0.025×0.1	112
	Back	0.05×0.025	2×4	0.1×0.1	28
1.4-1.5	Presampler	0.025×0.1	4×1	0.1×0.1	2
	Front	0.025×0.025	1×4	0.025×0.1	6
	Middle	0.075×0.025	1×4	0.075×0.1	2

The summing of detector cells to make Super Cells is done in the Layer Sum boards. Where necessary, the summing of Super Cells to make a trigger tower (TT) layer is done in the LTDB, in order to feed the Tower Builder Boards with signals identical to the present ones. For the PS, the TT layer is identical to the Super Cell: it is made by the Layer Sum Board and transmitted by the baseplane directly to the TBB, and the LTDB input is picked-up at high impedance from the baseplane line. It has been checked that the perturbation of the signal is negligible (see Sec. 4.1.3.2.1.

The output of the LTDB consists of 290 digital signals, with 8 channels multiplexed on one optical fiber. The fibers are grouped in 4 ribbons of 12 fibers (10 data + 2 control). Two ribbons handle the signals from cells at $|\eta| < 0.8$ and two ribbons that of cells at $|\eta| > 0.8$. In this way the barrel end cells can be brought close to the arrival point of the neighboring endcap cell fibers, to ease the treatment of the mixed trigger towers.

4.2.1.1 EMB Layer Sum Boards There are three types of LSBs in use in the EM Barrel. The presampler utilizes the S1x16H, with gain=2, the front layer requires the S2x8, the middle layer requires the S1x16L, and the back layer requires the S2x8D. At the barrel end, a special LSB, S2x2+S1x4 is required to handle the special geometry for that region, as discussed in Sec. 4.1.1.4. The numbers of boards to be installed are listed in Table 15.

Table 15. Number of LSBs required in the EM Barrel calorimeter, listed by layer.

Layer	LSB type	Number per half-FEC	Total
Presampler	S1x16H	2	128
Front	S2x8	14	896
Middle	S1x16L	7	128
Back	S2x8D	2	448
Barrel End	S2x2+S1x4	2	128
Totals		27	1728

4.2.1.2 EMB Baseplane The new EMB baseplane shown in Fig. 44, will have the same number of slots (19) as the current baseplane. Room for the LTDB is provided by a previously unallocated slot at one end of the baseplane. The Front and PS slots remain unchanged, while the other boards

will be shifted to allow for the LTDB to be located between the TBB and Controller, at a rather central position. The warm cable connections beneath the baseplane will need to be shifted by at most one slot; the feasibility of this operation has been verified in the lab. The new baseplane will route 290 Super Cell signals from the LSBs on the FEBs to the LTDB, and 116 layer sum signals from the LTDB to the TBB. It is advantageous to have the LTDB located next to the TBB to minimize trace lengths for high impedance spectator channels (see Sec. 4.1.3.2).

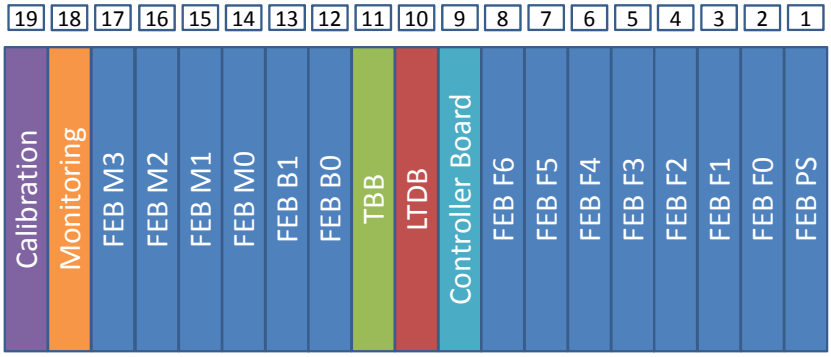


Figure 44. Slot assignments for the new EMB baseplane.

4.2.2 EM Endcap Calorimeter

The EM endcap calorimeter (EMEC) has a more complex geometry than the EM barrel. It is constructed of two wheels: the outer wheel, which covers $1.375 < \eta < 2.5$, and the inner wheel, which covers $2.5 < \eta < 3.2$. The complexity affects all sampling layers. The first layer has a pattern which changes with pseudorapidity, both in the outer and inner wheels. The presampler covers only the region $1.5 < \eta < 1.8$. At large values of pseudorapidity, the cells increase in size to $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and the number of layers decreases to two. The Super Cell granularity is similar to that of the barrel for lower values of η but at high values of η the granularity necessarily decreases.

The front end electronics for the EMEC is contained in two types of FECs, called the EMEC standard crate and the EMEC special crate. The former contains electronics for the region $1.6 < \eta < 2.4$, while the latter covers the rest. The standard crate, of which there are 16 in the system, strongly resembles the EM barrel FEC and contains one LTDB per baseplane. The special crates contain one baseplane for the EM calorimeter, with two LTDB modules, and another baseplane for the HEC electronics. There are 8 special crates in the system.

The Super Cell dimensions are given in Table 16 for each sampling layer, along with the number of Super Cells per LTDB of each type.

4.2.2.1 EMEC Layer Sum Boards The LSB requirements for the EMEC standard crate are similar to those for the EM Barrel (see Sec. 4.2.1.1), with the exception of the special LSBs required for the region $1.8 < |\eta| < 2.0$ as discussed in Sec. 4.1.1.4. In Table 17 are given the number of each type of LSB for this crate, listed by layer.

For the EMEC Special crate, the Presampler FEB requires only 1 LSB, as there are only 16 PS Super Cells in that front end board. The first layer at the lowest value of $|\eta|$ ($1.4 < |\eta| < 1.5$) requires a (partially populated) S1x16L LSB. In the next region $1.5 < |\eta| < 1.6$ the treatment is the same as the front section in the EMB, so S2x8 LSBs are used. For the second layer, the treatment is the same as that of the middle layer of the EMB for the region $|\eta| \leq 2.5$. For the inner wheel $(2.5 < |\eta| \leq 3.2)$,

Table 16. Size of the Super Cells in the EM endcap calorimeter, in terms of both elementary cells and $\Delta\eta$ and $\Delta\phi$. The notation (0.05)0.025 stands for a Super Cell composed of 1 cell of $\Delta\eta$=0.05 and 3 cells of $\Delta\eta$= 0.025. The number of Super Cells per LTDB are given in the columns labelled N_{Std}, N_{Spc0} and N_{Spc1} for the standard and 2 special FECss, respectively.

η-range	Layer	Elementary cell	Super Cell				
		$\Delta\eta\times\Delta\phi$	$n_\eta\times n_\phi$	$\Delta\eta\times\Delta\phi$	N_{Std}	N_{Spc0}	N_{Spc1}
		Outer Wheel					
1.375-1.5	Front	(0.05)0.025 × 0.1	4 × 1	0.125 × 0.1		16	
	Middle	(0.05)0.025 × 0.025	1 × 4	(0.05)0.025 × 0.1		64	
1.5-1.8	Presampler	0.025 × 0.1	4 × 1	0.1 × 0.1	8	16	
	Front	0.003125 × 0.1	8 × 1	0.025 × 0.1	32	64	
	Middle	0.025 × 0.025	1 × 4	0.025 × 0.1	32	64	
	Back	0.05 × 0.025	2 × 4	0.1 × 0.1	8	16	
1.8-2.0	Front	0.004167 × 0.1	4 × 1	0.0167 × 0.1	48		
	Middle	0.025 × 0.025	1 × 4	0.025 × 0.1	32		
	Back	0.05 × 0.025	2 × 4	0.1 × 0.1	8		
2.0-2.4	Front	0.00625 × 0.1	4 × 1	0.025 × 0.1	64		
	Middle	0.025 × 0.025	1 × 4	0.025 × 0.1	64		
	Back	0.05 × 0.025	2 × 4	0.1 × 0.1	16		
2.4-2.5	Front	0.025 × 0.1	4 × 1	0.1 × 0.1			16
	Middle	0.025 × 0.025	1 × 4	0.025 × 0.1			64
	Back	0.05 × 0.025	2 × 4	0.1 × 0.1			16
		Inner Wheel					
2.5-3.1	Front	0.1 × 0.1	2 × 2	0.2 × 0.2			24
	Middle	0.1 × 0.1	2 × 2	0.2 × 0.2			24
3.1-3.2	Front	0.1 × 0.1	1 × 2	0.1 × 0.2			8
	Middle	0.1 × 0.1	1 × 2	0.1 × 0.2			8

the S1x16L LSB is used for both layers, and each element is a Super Cell. The numbers of LSBs required for the EMEC Special Crate is shown in Table 18.

4.2.2.2 EMEC Baseplanes

4.2.2.2.1 Standard front-end crate EMEC standard: the new EMEC standard baseplane (see Fig. 45) will have the same number of slots (19) as the current baseplane, and has a layout similar to that of the EMB baseplane. The new baseplane routes 312 Super Cell signals from the LSBs on the FEBs to the LTDB, and 104 layer sum signals from the LTDB to the TBB.

4.2.2.2.2 Special front-end crate EMEC special: the new EMEC special baseline, shown in Fig. 46, will have 25 slots, two more than the current baseplane. There will be two new LTDB slots allocated on the new baseplane (for LTDB0 and LTDB1). The warm cable connections beneath the baseplane will need to be shifted at most by two slots. The new baseplane will route 240 Super Cell signals from the LSBs on the FEBs to LTDB0, and 96 layer sum signals from LTDB0 to TBB0. It will

Table 17. Number of LSBs required in the EMEC Standard Crate, listed by layer.

Layer	LSB type	Number per half-FEC	Total
Presampler	S1x16H	1	32
Front	S2x8	8	256
Front	S1x6+S6x1	4	128
Middle	S1x16L	8	256
Back	S2x8D	4	128
Totals		25	800

Table 18. Number of LSBs required in the EMEC Special Crate, listed by layer.

Layer	LSB type	Number per half-FEC	Total
Presampler	S1x16H	1	8
First Layer, $1.4 < \|\eta\| \leq 1.5$	S1x16L	4	32
First Layer, $1.5 < \|\eta\| \leq 1.6$	S2x8	8	64
First Layer, Inner wheel	S1x16L	2	16
Second Layer, $\|\eta\| \leq 2.5$	S1x16L	12	96
Second Layer, Inner wheel	S1x16L	2	16
Third Layer	S2x8D	4	32
Totals		33	264

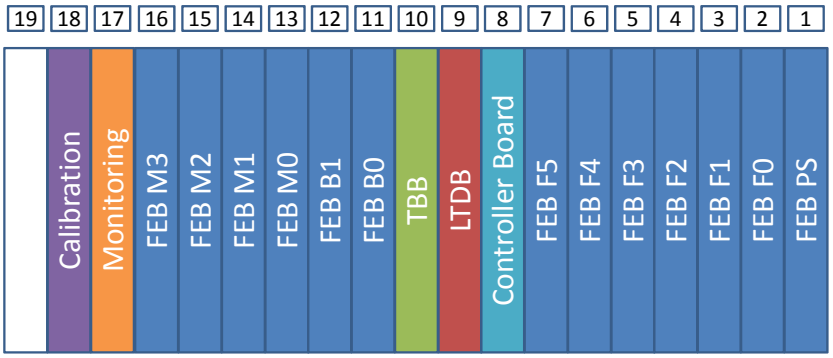


Figure 45. Slot assignments for the new EMEC standard baseplane

Table 19. Size of the Super Cells in the hadronic endcap calorimeter, in terms of both elementary cells and $\Delta\eta$ and $\Delta\phi$. Summing by layers is done in the linear mixer, as indicated by the index n_L. The number of Super Cells per LTDB are given in the column labelled N.

	Elementary cell	Super Cell		
η-range	$\Delta\eta\times\Delta\phi$	$n_L\times n_\phi$	$\Delta\eta\times\Delta\phi$	N
1.5-2.5	0.1×0.1	4×1	0.1×0.1	64
2.5-3.2	0.2×0.2	4×1	0.2×0.2	32

also route 160 Super Cell signals from the LSBs on the FEBs to LTDB1, and 112 layer sum signals from LTDB1 to both TBB1 and TBB2.

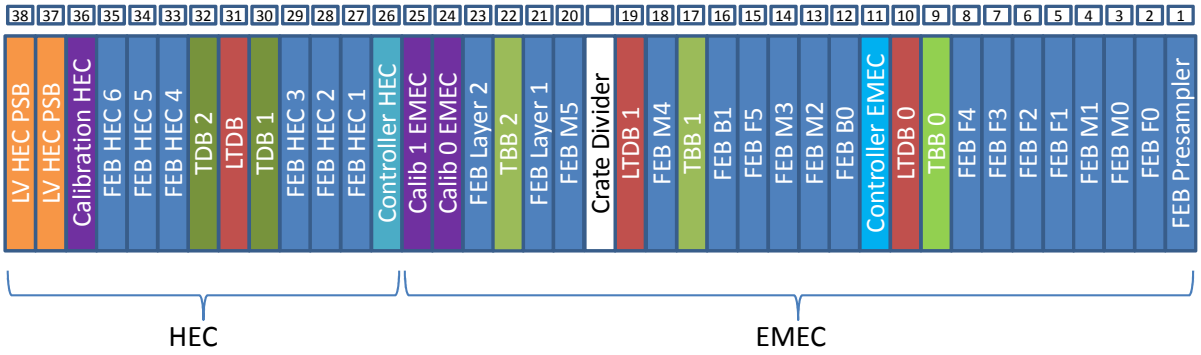


Figure 46. Slot assignments for the new HEC and EMEC Special baseplanes.

4.2.3 Hadronic Endcap Calorimeter

HEC: the HEC baseplane shares a FEC with an EMEC special baseplane. Correspondingly, the new HEC baseplane will have 13 slots, two less than the current baseplane. There will be one new LTDB slot on the new baseplane while one empty slot, one monitoring board slot and one controller board slot are eliminated. The warm cable connection beneath the baseplane will need to be shifted by two slots maximum. The new baseplane will be routing 192 SC signals from the LSBs on the FEBs to the LTDB, and 192 layer sum signals from the LTDB to both Tower Driver Boards TDB0 and TDB1. Elementary cells and Super Cell have the same size, as shown in Table 19.

4.2.3.1 HEC signal organization Each HEC quadrant has 768 readout channels (some of them are empty) and 192 L1 trigger channels. All are processed by 6 FEBs and two TDBs installed in the EMEC-special/HEC front-end crate. There are 8 such crates in the system and 1 HEC baseplane per crate.

There is no plan to increase HEC trigger granularity in the Phase-I upgrade: every readout tower (four longitudinal compartments of one η-ϕ cell) generates the L1 trigger signal, as there is no summation across either η or ϕ in the HEC. The only possible increase of HEC trigger granularity would be to introduce longitudinal segmentation; such a change is not possible without re-building HEC FEBs because currently all 32 FEB outputs to the baseplane are used. Re-design of the FEBs is not considered for the Phase-I upgrade.

All 192 HEC quadrant trigger signals can be read out by one LTDB module. Since all trigger lines already see 50Ω terminations at the TDB inputs, all HEC LTDB channels must have high input impedance. For a 1kΩ input impedance of LTDB, all HEC L1 signals will be reduced by 5%. This drop is small enough to be handled by the existing L1 system, since the receiver is used to complete the transformation of E to E_{T}, and these gain constants can be modified.

The η-dependent gain factors in HEC trigger sums are adjusted by choosing proper gain settings in the linear mixer and further in LSB channels. This adjustment is done in such a way that all channels have E_{T}response equalized within a factor of 2. The final adjustment is done in the receivers. The LTDB does not have such functionality; instead, a wider dynamic range for the ADC can be used so that this adjustment can be done digitally in the LTPB. A similar adjustment is needed for all LAr calorimeters, so there is no HEC-specific requirements for the LTDB design.

4.2.3.2 HEC Layer Sum Boards For the HEC, the FEBs and LSBs are unchanged from their configuration in the current system. The layer sum boards for the HEC are all of the same configuration, S1x16, but there are a mixture of high gain, low gain, and mixed gain boards. In this calorimeter, the cells are the size of trigger towers, and the sum performed by the Linear Mixer is over the layers in depth. The signals at its output are proportional to E, and the LSBs are used as a step in the transformation of E to E_T. This differs from the usage of LSBs in the EM calorimeter, where the LSBs have uniform gain and the transformation from E to E_T is carried out in the Tower Builder. For the HEC legacy electronics the fine gain adjustment, which completes the transformation, is performed by the variable gain amplifier in the Receiver. For the upgraded system, it is done for the HEC (and perhaps the EM calorimeters) in the back end electronics.

There are a total of 96 LSBs used in the HEC, 32 of each type (S1x16L, S1x16M, S1x16H).

4.2.3.3 HEC Baseplane The HEC FE electronics share a FEC with the EMEC-special partition. Currently the HEC part occupies 14 slots; there is one empty slot and one CMB. The upgrade of the EMEC baseplane requires one extra slot, and therefore only 13 slots slots will be available for the HEC. In order to fit the HEC boards into 13 slots, one CMB will be removed. The layout of the HEC-EMEC baseplane is shown in Fig. 46.

In this layout the LTDB is placed in between two TDBs. This is the only possible location of the LTDB because the TDB baseplane connectors are not equipped with shielding springs and therefore the LTDB connectors can fit into this space (see Sec. 4.1.2.1). The placement of TDBs in slots neighboring to the LTDB is also preferable to minimize the effect of reflections in traces connecting TDB (with 50Ω termination) and the LTDB (high-Z termination). Spice simulations show that in this layout signal shapes are distorted by not more than 1-2% compared to the present case of a single-point 50Ω termination.

The HEC FEBs 1-3 are placed at the TDB1 side in order to minimize the crossing of traces. The majority of FEB 1-3 trigger signals are sent to TDB1. The same is true for FEBs 4-6 and TDB2. With respect to the present HEC portion of the FEC layout, the boards are moved by not more than 2 slots, hence existing warm cables can be used for new connections to feedthroughs. HEC baseplane prototyping shows that all signal traces can be placed on 4 PCB layers, as in the present baseplane. However, the final design will likely be done with 5 signal layers in order to reduce trace density and crosstalk between channels.

4.2.4 Forward calorimeter

Two effects make the FCal trigger inputs more complicated than those of the EM or HEC calorimeters:

- The calorimeters measure energy but the trigger is designed to receive transverse energy (E_{T}). The FCal trigger path is unique in that the inputs to the analog trigger sums are first weighted by $\sin\theta$ in order to improve the E_{T} resolution.
- The $x-y$ translational symmetry of the FCal unit cells leads to an irregular division into $\eta-\phi$ trigger cells.

In the present (legacy) electronics, analog summing in the FEC is performed in only two stages. Each shaper chip forms an unweighted sum of four readout cells. These shaper sums are then fed to the layer sum boards which form the weighted sums. There is no summing on the Tower Driver Boards. Additional summing is carried out in USA15: summing in rapidity is performed for FCal2 and FCal3 in the Receiver and the longitudinal summing of these signals is carried out the the L1 preprocessor after digitization.

4.2.4.1 FCal signal organization The forward calorimeter (FCal) covers the range $3.0<|\eta|<4.9$ at each end of the detector. This coverage is nearly 40% of the η range of the whole detector. Because the particles from minimum bias events are approximately uniformly distributed in η, the occupancy of a given calorimeter cell is roughly proportional to its area measured in $\eta-\phi$ space. The Level-1 trigger cells in the present FCal are so large (roughly 0.5×0.4) that the occupancy is over 100%, *i.e.* more than one low E_{T} particle per crossing at the LHC design luminosity of 1×10^{34} cm^{-2} s^{-1}.

The η granularity in the FCal trigger towers will be increased in order to reduce the occupancy, thereby reducing the pileup. For FCal1, rather than the present 4 divisions in pseudorapidity there will be 12. Table 20 summarizes the proposed improvement in granularity.

Table 20. The present and the proposed granularity of FCal trigger cells at each end of the ATLAS detector.

	FCal1	FCal2	FCal3	Total
FEBs	8	4	2	14
Shaper Chips	256	128	64	448
LSBs	16	8	4	28
Existing				
Eta divisions	4	4	4	
Phi divisions	16	16	16	
Total cells	64	64	64	192
Proposed				
Eta divisions	12	8	4	
Phi divisions	16	16	16	
Total cells	192	128	64	384

4.2.4.2 FCal Layer Sum Boards For the FCal there are 14 Front End Boards (FEBs) at each end of ATLAS with two Layer Sum Boards (LSBs) each. Thus there are 56 FCal LSBs in all.

The linear mixer outputs (sum of four readout cells) of the shaper chips are routed to the LSBs. There the signal is weighted by $\sin\theta$ and then added to other weighted sums to form an FCal trigger sum. All of the present LSBs will be replaced with boards which produce finer granularity. These upgraded boards will receive the same number of inputs (16) but will deliver more outputs, on average twice as many.

In the present FCal scheme there are 48 different types of FCal trigger sums. In the legacy system, because weighting for some inputs was sufficiently similar to that of others there are only 7 different types of LSBs. In the proposed scheme there will be 96 different types of Super Cells. It is yet to be decided how close Super Cells must be to each other in order to treat them as identical inputs to the LSB. There will be at least 7 different types of LSBs, but symmetry considerations dictate that there will be no more than 14 different types.

The upper end of the dynamic range for the L1 signals is presently 256 GeV in E_{T}. At this value the kinematic limit will be reached at $|\eta| \approx 4.0$ when the LHC operates at 14 TeV. For the Phase-I upgrade, the dynamic range of the ADCs in the FCal LTDBs has not yet been decided, but is likely that it will be set at the kinematic limit for LHC operation at 14 TeV.

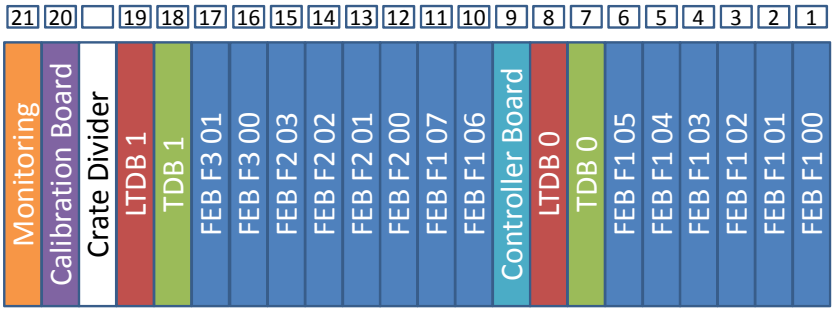


Figure 47. Slot assignments for the new FCal basplane.

4.2.4.3 FCal Baseplane The new FCal baseplane will have 20 slots, one more than the current baseplane as shown in Fig. 47. There will be two new LTDB slots allocated on the new baseplane. The warm cable connections beneath the baseplane will be shifted by two slots maximum. The new baseplane will be routing 192 SC signals from the LSBs on the FCal1 FEBs to LTDB0, and 64 layer sum signals from LTDB0 to TDB0. It will also be routing 192 SC signals from the LSBs on the FCal2 and FCal3 FEBs to LTDB1, and 128 layer sum signals from LTDB1 to both TDB0 and TDB1. The number of baseplane PCB layers required to properly route these additional signals has not yet been determined.

The FCal calibration strategy is unique in that the calibration pulse is introduced directly onto the FEBs. The severe radiation environment at the FCal modules precluded the routing of calibration pulses to the electrodes, as is done in the other calorimeters. Therefore the FCal baseplanes have special distribution boards mounted under the PCB used to route the trigger sums, in order to deliver the calibration pulse to the FEB signal connector pins. The irregular geometry of the trigger cells also makes the routing of the LSB outputs to the Tower Driver Boards (TDBs) more complicated.

The trigger upgrade requires two additional slots in the FCal Front End Crate (FEC) to accommodate the two LTDBs. In the current system the 19 FCal boards all fit within a half-crate. This is convenient because it allows the use of identical baseplanes on each of the EndCap cryostats. Since each half of the Front End Crate will accept only 19 modules, an additional module in the FCal electronics would need to be mounted in a 1-slot baseplane located in the other half of the crate (which is empty). Because of the symmetries involved, this extra slot is adjacent to Slot 1 for the C-end and Slot 19 for the A-end. In order to utilize a common baseplane for the two ends, the calibration board will be assigned to the 1-slot baseplane. The calibration signals will be sent over two ribbon cables to the position of the controller board, whose baseplane connectors which access the traces in the calibration board are not used. These ribbon cables will be routed through the pedestal

space, where they must pass around the pedestal cables. The monitor board will also reside on the other side of the crate divider, but it does not use any baseplane connectors, as it is connected only to the power harness. Alternatively we could build separate baseplanes for the A and C ends, which would be single boards which span the two sides of the crate. This would avoid the need for the two ribbon cables routed through the pedestal space.

Because of the special problems associated with the FCal FEC, one and perhaps two prototype baseplanes are planned to test construction strategies, to check mechanical robustness, and to test for correct signal connectivity.

5 Back End electronics

The Phase-I upgrade to the LAr calorimeter back-end (BE) electronics system, called the LAr Digital Processing System (LDPS), must receive the digital signals from the 124 LAr Trigger Digitizer Boards (LTDBs), extract the transverse energy for each Super Cell ($E_{\mathrm{T}}^{\text{Super Cell}}$) every 25 ns, and transmit these data to the Level-1 calorimeter trigger system (L1Calo), as illustrated in Fig. 48. The LDPS configures and monitors the LTDBs while providing trigger, timing, and control (TTC) signals. Finally, the LDPS provides the capability to buffer the Super Cell data in various formats (upon a Level-1 accept from the trigger system) for monitoring, calibration, and potential use by the high-level trigger system.

The main challenge for the LDPS is the efficient handling of the large data volume: the reception of ~ 25 Tbps for $34,000$ Super Cells and the transmission of ~ 41 Tbps over optical fibers to the Level-1 Calorimeter Trigger System (L1Calo). The system must also be integrated in the ATLAS data acquisition system, synchronized with the LHC clock, and will provide monitoring capabilities.

To accomplish this endeavor, the hardware implementation will be based on the ATCA (Advanced Telecom Computer Architecture) platform [29] that supports the design of high-density, high-speed communication boards and is the replacement for VME within ATLAS. The proposed LDPS is made up of 31 LAr Digital Processing Blades (LDPBs) housed in three ATCA shelves. Each LDPB consists of one carrier board equipped with four Advanced Mezzanine Cards (AMCs), for a total of 124 AMCs. The AMC is designed around a powerful FPGA with high-speed transceivers that will process the data of up to 320 Super Cells within the latency budget summarized in Table 2 of this document. These new components will be located adjacent to the legacy BE system, off the detector in the USA15 counting room.

The upgrade LAr BE electronics system is described in the following sections. Section 3.1.2 in Chapter 3 provides a brief description of the legacy BE electronics; this main readout path will remain intact. In contrast to the FE electronics upgrade components, the LDPS is essentially independent of the main readout system. An overview of the LDPS is presented in Sec. 5.1. The hardware components of the LDPS are described in Sec. 5.2, while the general infrastructure, timing and control infrastructure, and configuration are described in Sec. 5.3. The data flow through the BE system is presented in Sec. 5.4. Section 5.5 pertains to the FPGA firmware, while a variety of transverse energy reconstruction algorithms are presented in Sec. 5.6. Section 5.7 presents potential variations on the baseline design as well as compatibility with the Phase II upgrade. A brief conclusion is given in Sec. 5.8.

5.1 LAr Digital Processing System Overview

A detailed overview of the functionalities of the overall system is presented in Fig. 49. These functionalities include:

- Reception of the ADC data from the LTDBs and transmission of the computed results ($E_{\mathrm{T}}^{\text{Super Cell}}$ and $\Sigma E_{\mathrm{T}}^{\text{Super Cell}}$) to L1Calo.
- Distribution of the ATLAS Trigger, Timing and Control (TTC) signals to the LTDBs and LDPBs.
- Configuration of the various boards in the system.
- Monitoring of TDAQ (ATLAS event) and other data, where a selection of events is written to the ATLAS event and/or to the PC farm, for analysis and monitoring purposes.
- Sending hardware status information to the ATLAS Detector and Control System (DCS) [30] for slow control purposes.

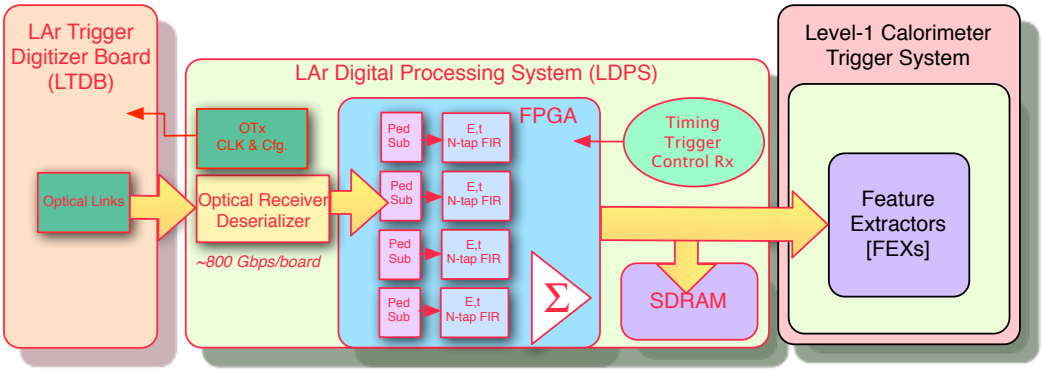


Figure 48. Block diagram of the proposed LAr Digital Processing System (LDPS), which receives digital Super Cell data from the LTDBs of the upgraded FE system, reconstructs $E_{\mathrm{T}}^{\text{Super Cell}}$ (the transverse energy of each Super Cell), and transmits the results to the Level-1 Calorimeter Trigger System every 25 ns.

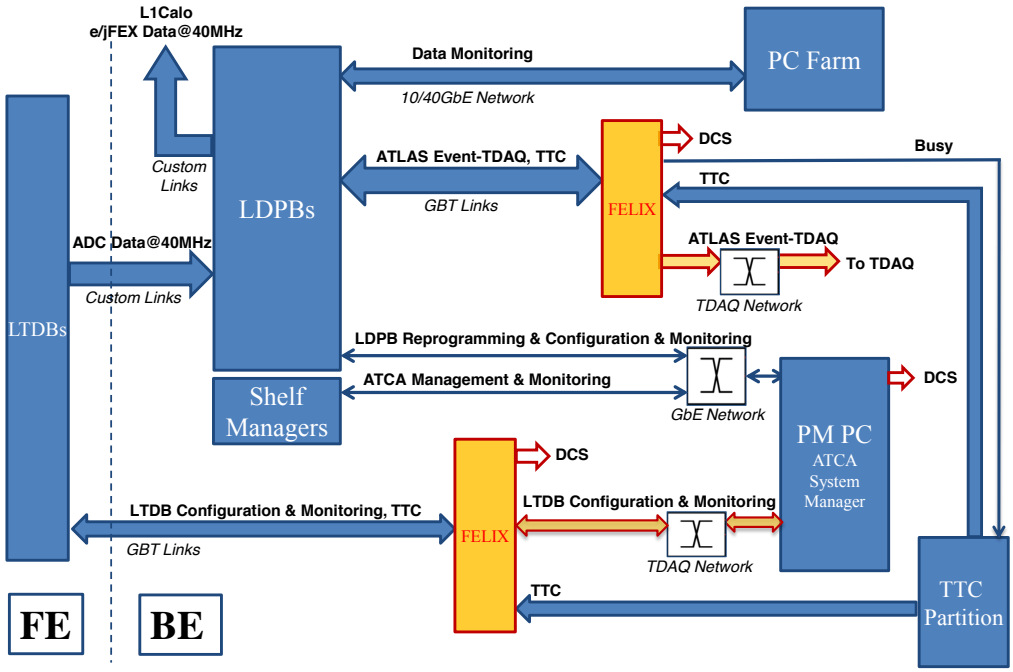


Figure 49. Schematic overview of the LDPS system. The physical elements are represented in boxes: LDPB, Shelf manager, Partition Master (PM), TTC partition, PC farm in blue and FELIX [31, 32], which is under TDAQ responsibility [4], in yellow. The links and networks are represented as arrows. The description of the data is written above the arrow and the type of link in italic below the arrows. See text for details.

The overall system is made from the following physical components (represented in Fig. 49):

LDPB The LAr Digital Processing Blade

FELIX The Frontend Link Interface eXchange [31, 32], developed by the ATLAS TDAQ group [4]

TTC partition TTC signals are delivered by the TTC partition to FELIX.

Partition Master PC The Partition Master PC (PM PC) manages the configuration and monitoring via GbE (Gigabit Ethernet) and TDAQ networks and also acts as the ATCA system manager.

PC farm The PC farm treats and analyses events received from the Data Monitoring path on the 10/40 GbE network.

Shelf Manager The shelf manager controls the ATCA shelf. It is connected to the ATCA system manager through the GbE network.

These components are interconnected by fast links:

- Custom links, as described in the FE chapter 4, are used for ADC data between the LTDBs and LDPBs.
- Custom links, which will be defined together with the L1Calo group, are used to transmit FEX data to L1Calo.
- A 10/40 GbE network is used for LDPB data monitoring by the PC farm.
- GBT links are used between LDPBs and FELIX and the TDAQ network from FELIX to TDAQ, to send data to ATLAS events.
- The GbE network is used by the Partition Master PC for LDPB reprogramming, configuration, monitoring, and ATCA management.
- GBT links are used between LTDBs and FELIX and the TDAQ network from FELIX to the PM PC, for LTDB configuration and monitoring.

5.2 Upgrade Back End electronics components

The hardware components of the LDPS are described in this section: first, a general introduction to the ATCA platform is given in 5.2.1, and then the LDPB is described in 5.2.2. The main component of the LDPB is the Advanced Mezzanine Card (AMC) (Sec. 5.2.2.1) which receives ADC data from the LTDBs, reconstructs $E_{\mathrm{T}}^{\text{Super Cell}}$, and transmits the results to L1Calo. The carrier board is described in Sec. 5.2.2.2.

5.2.1 ATCA platform

The ATCA (Advanced Telecom Computer Architecture) platform supports the design of high density communication boards; it is reliable while providing hot swap capability and real time diagnostics. ATCA is the replacement for VME within ATLAS [33].

Each ATCA shelf (crate) is 12U or 13U (rack units) high and can house up to 14 blades (boards). Within a shelf, each ATCA backplane is divided into three zones (cf Fig. 53) that provide connector interfaces for the blades:

Zone 1 is for power and control signals.

Zone 2 is divided into *base* and *fabric* interfaces. The base interface provides peer-to-peer Gigabit Ethernet (GbE) connections between the blades and the switch blades (or switch). The *fabric* interface provides fast peer-to-peer connections between the blades and the switch blades. The 10 GbE protocol is commonly used, but the 40 GbE protocol is becoming more widely available. The term 10/40 GbE is used in this document to refer to this network.

Zone 3 is for user-defined connections, and can be configured for use with or without a Rear Transition Module (RTM), as described in Fig. 5.3.1.

Two common options are defined for the Zone 2 *fabric* interface: *dual-star* and *full-mesh*. The *dual-star* backplane provides communication among 12 blades through two switch blades, while the *full-mesh* backplane provides full inter-communication among the 14 blades. The *full-mesh* option allows for configuration of the backplane in *dual-star* mode (the reverse is not true).

The LDPBs will be installed in three ATCA shelves with *full-mesh* backplanes that will be configured in *dual-star* mode. The shelves will house 12 LDPBs and two switch blades for two of the shelves; the third shelf will house seven LDPBs and one or two switch blades.

In the ATCA standard, a *shelf manager* controls the different ATCA elements inside a shelf. The shelf manager is connected via the Intelligent Platform Management Bus (IPMB), to an IPM controller (IPMC) mounted on each blade. The IPMC is connected to the AMC through a Module Management Controller (MMC) mounted on the AMC, which is connected to a local IPM bus (IPML).

5.2.2 LAr Digital Processing Blade (LDPB)

Each LAr Digital Processing Blade (LDPB) consists of an ATCA carrier board equipped with four Advanced Mezzanine Cards (AMC). The design of the AMC and carrier board are described in the following sections.

5.2.2.1 Advanced Mezzanine Card (AMC) The Advanced Mezzanine Card (AMC) conforms to the standard ATCA protocol and measures 156 mm $\times$ 73.5 mm to allow four AMCs to fit on a carrier board. The design of the AMC for the LDPS (see Fig. 50) is built around one FPGA with large capabilities for internal logic and memory, DSP processing for signal reconstruction algorithms, and high-speed communications.

5.2.2.1.1 FPGA In order to perform the required functions of the AMC, the chosen FPGA must have 54 transceivers (48 for signals, 4 for one fast link, and up to 2 for the GBT link), sufficient DSP processing power, and ample memory in RAM blocks. The FPGA is associated to external memories like Flash, DDR3 (Double Data Rate type-III) or SDRAM (Synchronous Dynamic Random Access Memory) for firmware and temporary buffering. Particular attention is given to the distribution of the clocks (TTC, oscillators, PLL), especially the clocks driving the FPGA high-speed transceivers. The FPGA transceivers must run at compatible link speeds, 5.12 Gbps for the receivers and 10 Gbps for the transmitters.

Table 21 summarizes the estimate of the total required resources for the FPGA and compares it to two high-end FPGAs expected to be available in the years 2014-2015. A break-down of the estimate by required function is given in Table 24 of Sec. 5.5.1. The selection of the FPGA to be used will be based on the available technology fulfilling the needs mentioned above.

Developments made so far have used FPGAs from the Altera [34] and Xilinx [35] families: Xilinx Virtex-7 [36] and Altera Stratix IV [37]. FPGAs from each family have been tested and shown to meet the requirements, though no full scale test has yet been made. Progress on the FPGA market is rapid; for instance, Altera has announced a new generation ARRIA10GX [38] (20nm technology) that will be available in 2014, indicating that the choice of the FPGA is not a critical one.

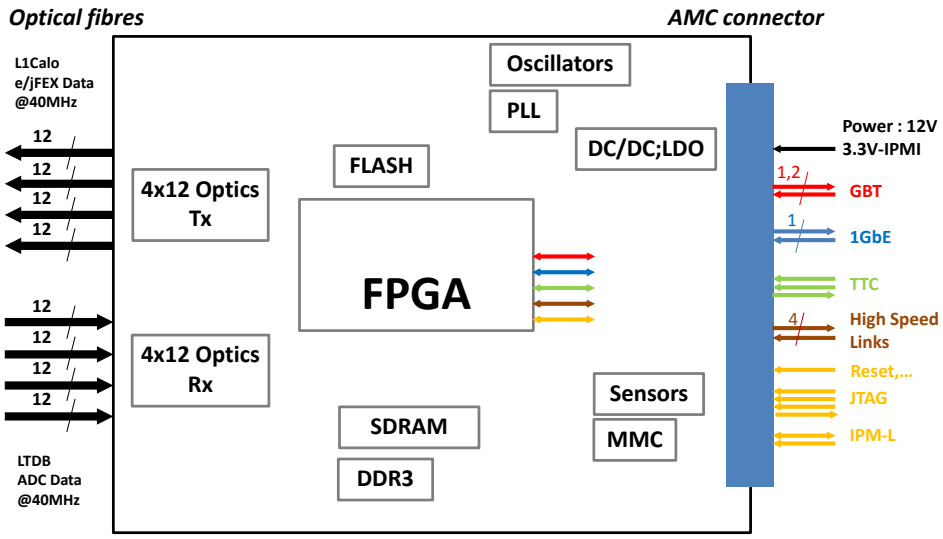


Figure 50. Block diagram of an AMC, centered around a high-bandwidth FPGA. The AMC receives (transmits) data over 4×12 Rx (4×12 Tx) optical fibers.

Table 21. Summary of the total estimated resources needed for the firmware running in the AMC FPGA and specifications of commercial high-end FPGAs from Xilinx and Altera. FPGA-I and FPGA-II are from the datasheets for Xilinx Virtex-7[36] (currently available) and Altera ARRIA-10 [38] (announced), respectively. In each case, the specifications of the FPGAs exceed the estimated requirements. (*) The numbers of DSP cells between the two types of FPGAs are not directly comparable since they are integrated in multi-functional processing blocks.

Resource	Estimated Requirement	Specification	
		FPGA-I	FPGA-II
Register [10^3]	184	1424	1300
LUT [10^3]	120	712	900
TX/RX	54	96	96
DSP	778	3360(*)	1518(*)
BlockRam [Mbit]	13.5	67.7	57.0

5.2.2.1.2 Optical reception and transmission The reception (transmission) of the ADC data from the LTDB (to L1Calo) is performed through high-density optical receivers (transmitters). In order to maximize the density of components, and to minimize the size of the system (also considering its cost), the baseline design is that each AMC will handle 48 fibers for reception (Rx) and 48 for transmission (Tx). In addition, given that the granularity of commercially available optical components and connectors is usually 12-fold, four optical receivers and four optical transmitters will be mounted on the AMC. These will be connected to 48 Tx and 48 Rx high speed serial links on the FPGA. This choice was guided by the LHCb collaboration's experience [39] having successfully built and tested AMCs with 2×36 fibers, and by results obtained from tests on smaller connectors (i.e., the recent availability of the MicroPOD [40] rather than LHCb's implementation using the MiniPOD). This granularity of 2×48 fibers per AMC is also well-suited for mapping the FE signals.

The baseline choice for the 12-fold fiber connector is the MicroPOD optical connector which has a package dimension of 7.6 mm $\times$ 7.6 mm $\times$ 3.9 mm (length $\times$ width $\times$ height), but which must be embedded in a heat sink due to its significant power consumption ($\lesssim$ 3 W per component). Commercial options for a heat sink have been investigated, but the dimensions of 12.5 mm $\times$ 25.0 mm $\times$ 12.2 mm for each heat sink would prevent the placement of four MicroPODs in row on an AMC (which is 73.5 mm). Another important consideration is the total width of the ATCA shelf slot (30.48 mm), which limits the height of components on the AMC; this constraint may be incompatible with the height of the commercial heat sink option. In order to avoid this conflict, a custom heat sink has been designed for four MicroPODs which measures 20 mm $\times$ 62 mm $\times$ 7.9 mm in total.

Figure 51 shows a test board for the MicroPOD transmission test equipped with two sets of transmitters and receivers of the MicroPOD connectors and the custom-designed heat sink.

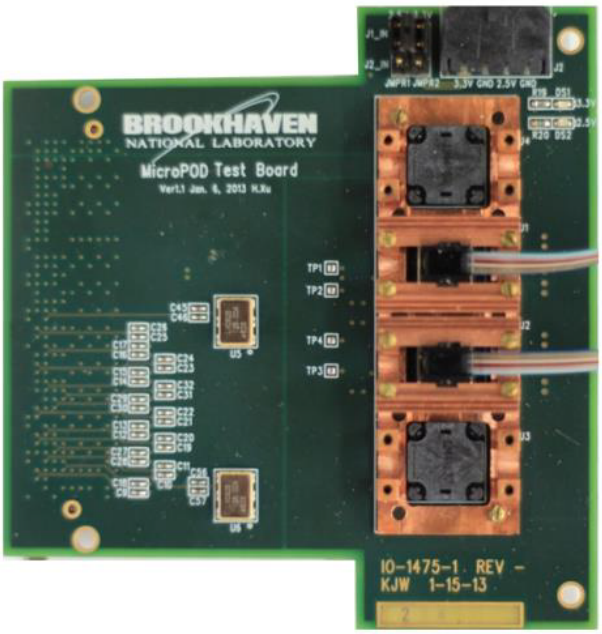
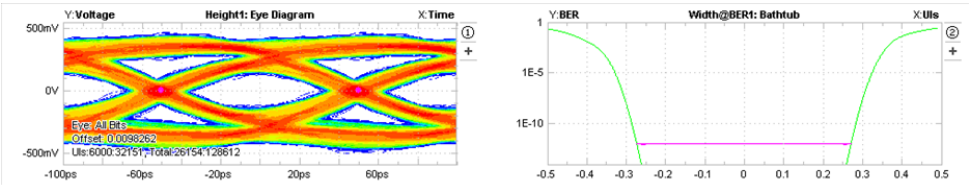
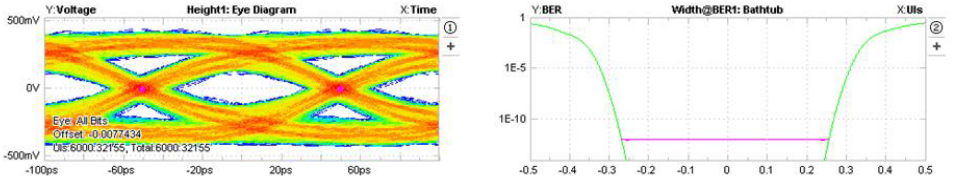


Figure 51. Test board for transmitting data with the MicroPOD. Two sets of transmitters and receivers with a custom-made heat sink are shown. There are four places for the MicroPODs, upper two places for transmitters and bottom two places for receivers. One of each are now connected (with copper fixture with cable connected). Size of the board is 89 mm $\times$ 85 mm. The heat sink is for four set of the MicroPODs, 20 mm $\times$ 62 mm $\times$ 7.9 mm (height). The grade of the PCB material is FR-4 in this version.

Figure 52 illustrates the results of transmission tests made between two test boards. The test board is mounted on the Xilinx[35] evaluation kit, KC705, and evaluated with the Xilinx IBERT (The LogiCORE Integrated Bit Error Rate) which can evaluate up to 12.5 Gbps. There was no error observed for a 2.6-day run, corresponding to a BER (Bit Error Rate) of less than 1×10^{-15}. The test has been performed with several settings of the lengths of the routes and the number of vias. There was no noticeable difference in BER between routes with vias (up to 5) and configurations with route lengths < 130 mm. The PCB material for this test configuration is standard grade FR4[6].



(a) Test results with route lengths of 69 and 25 mm for the carrier board and daughter board, respectively, with 5 vias.



(b) Test results with route lengths of 71 and 53 mm for the carrier board and daughter board, respectively, with 4 vias.

Figure 52. Results of MicroPOD transmission tests with two different configurations (a) and (b). For each configuration, the left figure shows the Optical Modulation Amplitude (OMA) as function of time. The distance between the up (1) level and down (0) level, and the clarity of the transition (the blank region, or “eye") are crucial features. The right figures show so-called “bath-tub" curves that illustrate the width of the eye opening, BER, as a function of the offset phase.

5.2.2.1.3 Interfaces to carrier board Figure 50 also illustrates various interfaces between the AMC and the carrier board through the AMC connector:

- power conversion from the AMC 12V supply to the necessary voltages for components, which is performed by the DC/DC convertor and the Low Drop Out (LDO) regulator.
- one or two GBT based links to the carrier board (each GBT link uses one FPGA transceiver). The choice between one or two links depends on the amount of data to be sent to the ATLAS Event.
- one GbE link connected to the FPGA for configuration and monitoring of the AMC, and for reprogramming the Flash memory.
- TTC commands and the clock that are routed from the carrier board to the AMC FPGA.
- high-speed links, each of which use four high-speed transceivers, connected to the FPGA on the AMC, to send monitoring data to the ATCA carrier board.

[6] This is the standard PCB material in the market, not the high performance material described in Fig. 5.2.2.2. This test result gives some relief on the requirement on the PCB material to deal with the high-speed link on the AMC.

- one single-ended link for signals like a boundary scan bus (JTAG) that allows for the initial programming of the FPGA, the IPM-L (local IPM) bus, and resets.

The MMC is in communication with the IPMC on the carrier board with the IPM-L bus. The MMC manages and monitors all ATCA aspects on the AMC and reads out sensors (temperature, voltage, current) via the I2C bus.

5.2.2.2 LDPB carrier board Each carrier board holds four AMCs (as described in the previous section) and provides a variety of different communication functionalities as shown in the schematic diagram in Fig. 53. Achieving a reliable high rate of transmission for clock distribution and data rates at 10/40 GbE is a challenge on large boards (the standard ATCA carrier board measures 322 mm x 280 mm). This issue dictates specific manufacturing requirements, such as using a PCB material with a relative dielectric constant of ~3 e.g. NELCO4013EPSI[41].

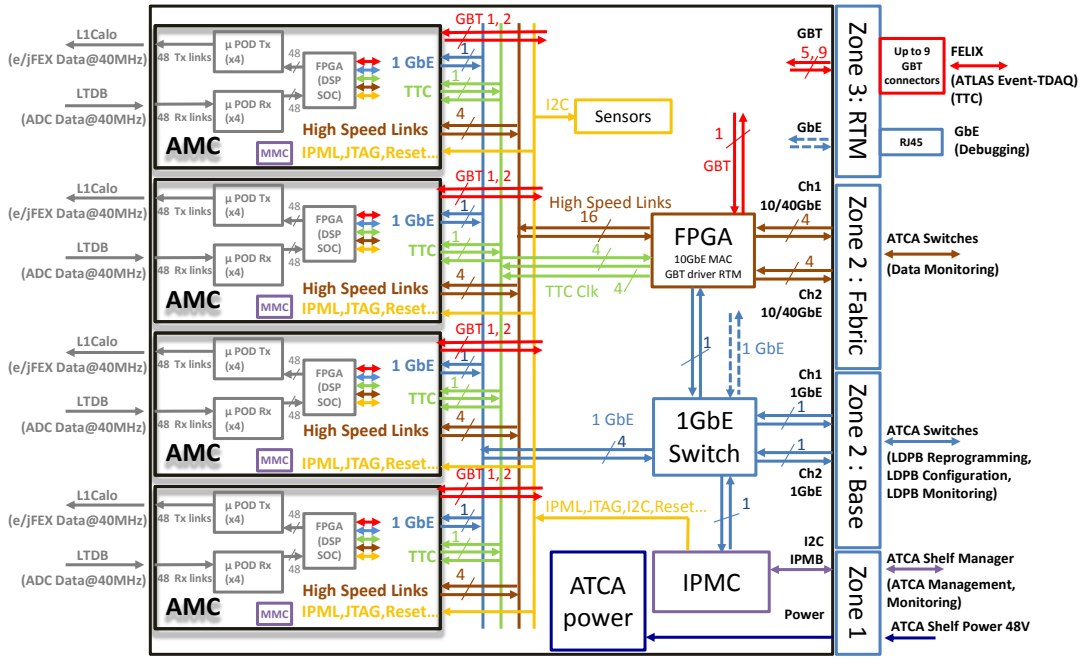


Figure 53. Schematic diagram of the implementation of the LDPB in which four Advanced Mezzanine Cards (AMCs) are mounted on a carrier board. The various line colors represent different communication functionalities: FPGA programming through GbE (light blue), monitoring data through high speed links and 10/40 GbE (brown), distribution of trigger, timing, and control (TTC) information (green), ATCA management and JTAG (orange) and data to ATLAS Events with GBT based links (red).

The main components on the carrier board are (the colors indicated refer to those in Fig. 53):

FPGA (brown) The FPGA has two main functions: (1) to interface the high-speed links coming from the AMCs to the 10/40 GbE network for data monitoring, and (2) the transmission of the TTC information (green) from the GBT link (red) to the AMCs.

1 GbE Switch (light blue) Configuration, monitoring and reprogramming of AMCs and carrier FPGAs are done through this switch, which also interconnects the AMCs, the IPMC and the carrier FPGA with the ATCA switches.

IPMC (purple) The ATCA management is performed by an IPMC [42] mezzanine that is in communication with the shelf manager through the IPMB. A prototype of the IPMC mezzanine has been built as shown in Fig. 54. Production of the final version is underway.

ATCA power block (dark blue) This block provides power to the carrier components and to the AMCs (12V) from the 48 V shelf power.

In order to have a very stable clock at the level of the AMC, with minimal impact on the AMC layout occupancy, it is foreseen to decode and clean the clock on the carrier blade and distribute a clean signal to the AMC. A clock cleaner component will be added on the carrier board to clean the clock signals decoded by the carrier FPGA.

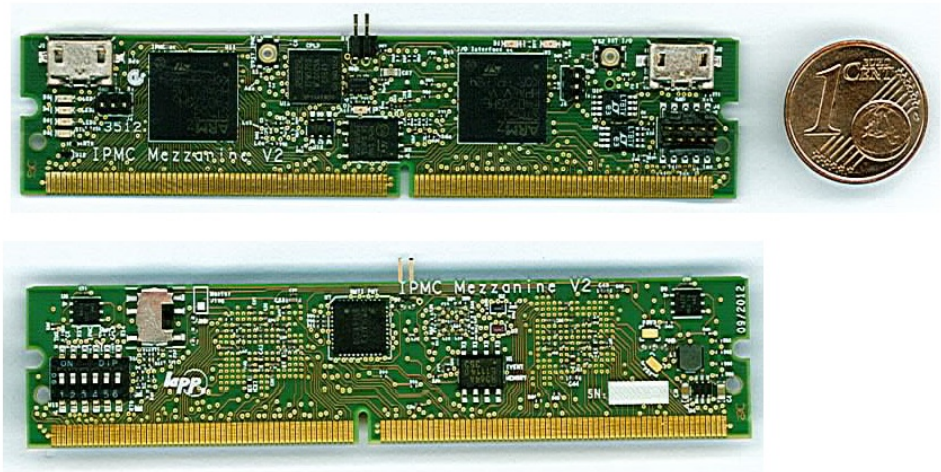


Figure 54. Photograph of the Intelligent Platform Management Controller (IPMC) mezzanine card which controls the carrier board and generates alarms. The one cent coin provides the scale.

There will also be a direct connection of the GBT based links between zone 3 and the AMCs (red). This path will be used to transfer data to TDAQ through FELIX. Whether the GBT links will go through a Rear Transition Module (RTM) or will be connected directly to FELIX is under consideration.

5.2.2.3 Carrier board pre-prototype In order to evaluate a possible LDPB layout, one ATCA board with three Altera Stratix IV FPGAs [37] has been designed, built and tested with fibers running up to 8.6 Gpbs. The two front FPGAs are connected to 24 transceivers. A photograph of this board is presented Fig. 55. Four boards have been produced and are being used for test purposes. The following tests have been successfully performed:

- Tests of the physical links (1 and 70 meters long) up to 8 Gbps, using 8b/10b encoding.
- The FPGAs have been configured to receive and transmit data at two different link speeds: 5.1 Gbps on input and 6.4 Gbps have been successfully configured.
- Data transmission and reception at 8 Gbps between two FPGAs on the board.

- Master clocking was tested with both a local oscillator and using the clock extracted by a clock data recovery chip from the TTC system.

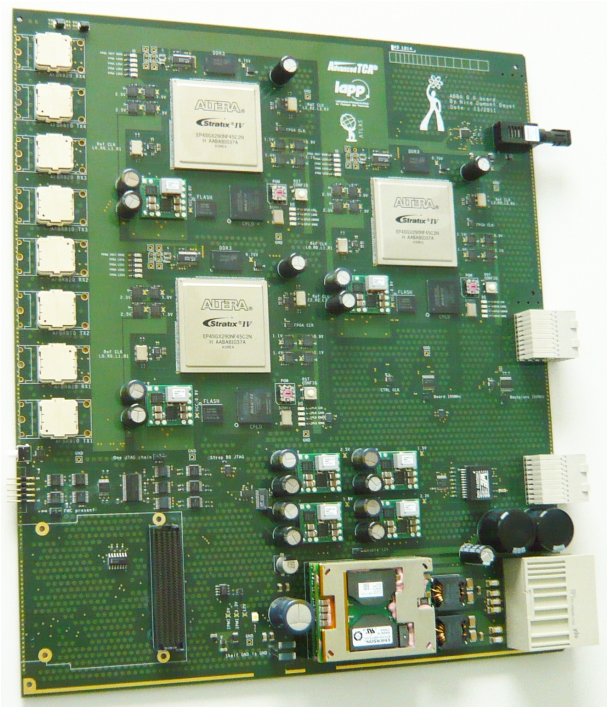


Figure 55. Photograph of the LDPB pre-prototype equipped with three FPGAs of the Stratix-IV family. The size of the board is that of a standard ATCA board, 322 mm $\times$ 280 mm.

5.3 LAr Digital Processing System Integration

The LDPS acts as the main interface between the FE and TDAQ, and thus must be integrated with the FE LTDBs, TDAQ (through FELIX), the ATLAS TTC system, and the ATLAS Detector and Control System (DCS) [30].

5.3.1 FELIX

The design presented in this TDR relies on the development of a FE Link Interface eXchange (FELIX) [31, 32], developed by the ATLAS TDAQ community [4], for data transmission to TDAQ (for monitoring and readout data), configuration of the FE LTDBs, and communication with the DCS system.

As depicted in Fig. 49, ATLAS event data are sent from the LDPB to FELIX via GBT links [23]. For the entire system, up to 279 high-bandwidth FELIX connections from the LDPB (carrier board or AMC) to TDAQ may be necessary.

For the configuration of the FE LTDBs, the distribution of the clock and the hardware monitoring of the boards, up to 496 GBT links from FELIX to the FE could be necessary. As opposed to the readout data transfer links, these configuration links should be connected to FELIX boards with many connections but relatively low bandwidth in such a way that the whole LAr configuration system could be placed in a compact housing. The configuration of the FE LTDBs is driven from the Partition

Master PCs. It would be useful to have a standard ATLAS FELIX board, equipped with enough fiber connectors so that the LAr configuration system would be housed in few PCs.

5.3.2 Trigger, Timing, and Control

A dedicated TTC partition to control the new LTDBs and LDPBs is necessary. Currently, LAr is organized with six partitions: EMB, EMEC, HEC/FCal for each side (A and C) of the detector. The two current partitions EMEC and HEC/FCal will be grouped, freeing one partition per side for the new boards. From the experience acquired in the first years of commissioning and data taking, the loss of flexibility has been judged acceptable. Under this configuration, the TTC signals for the LTDBs and the LDPBs will be distributed from the FELIX boards on GBT links.

As data will be written to the ATLAS event via TDAQ, a Busy system needs to be implemented. Each LDPB will generate its Busy (when the memory buffers are not being emptied fast enough by the FELIX TDAQ system) that will be transmitted over the GBT link through FELIX, to the TTC partition. This possibility is under investigation by the FELIX team. Figure 56 shows the system for distribution of the TTC and Busy signals as proposed for Phase-I. The evolution for Phase II, where the signal source (LTP, TTCvi,..) will be replaced, should be transparent as taken care by the FELIX interface.

5.3.3 Infrastructure

The 31 blades of the LDPS will be housed in three ATCA shelves. The system is designed to be compact and therefore minimizes the number of boards. Because of the constraints in USA15 (19" rack size), ATCA shelves with 14 slots will be used: 12 slots for ATCA carrier blades and two for switch blades. Since each rack can house two shelves, two racks will be necessary. An illustration of the distribution of the LDPBs is shown in Fig. 56.

ATCA shelf managers are connected to the external network via the base interface backplane and the switch blade. A system manager will be implemented on the Partition Master (PM) PC connected to that network. This supervision is needed in order to ensure common orders, e.g. fan speed. Part of this control and monitoring information will be transmitted to/from the ATLAS DCS system.

The shelf manager and the IPMC control the ATCA blade, the IPMC and the MMC control the AMCs. Blade configuration is normally done once, but modifications might be required e.g. for alarm threshold changes. Initial configuration of the carrier and AMC FPGAs will be done using the GbE from the base interface connected to the IPMC and the JTAG bus. Update of the FLASH configuration memory of these FPGAs will be done directly from the GbE.

From measurements done so far, the power consumption for a fully equipped ATCA shelf is expected to be 220 W for one LDPB. Manufacturers specify a power of 400 W per blade for ATCA shelves. The ATCA standard imposes a uniform resistance across one blade and among blades and slots; in particular fake blades have to be installed in empty slots as pictured on Fig. 56. A heat flow analysis will have to be carried out to define the cooling power required for the LDPS.

5.3.4 Configuration of FE and BE electronics

The configuration of the LDPBs consists of loading the calibration constants for $E_{\mathrm{T}}^{\text{Super Cell}}$ reconstruction and possibly parametrization of histograms, and link configuration (such as enable). It will be driven by the LAr Partition Master PC which will send the parameters via the GbE base interface network. The FE LTDBs are configured by the Partion master PC through the TDAQ network, by FELIX and the GBT links.

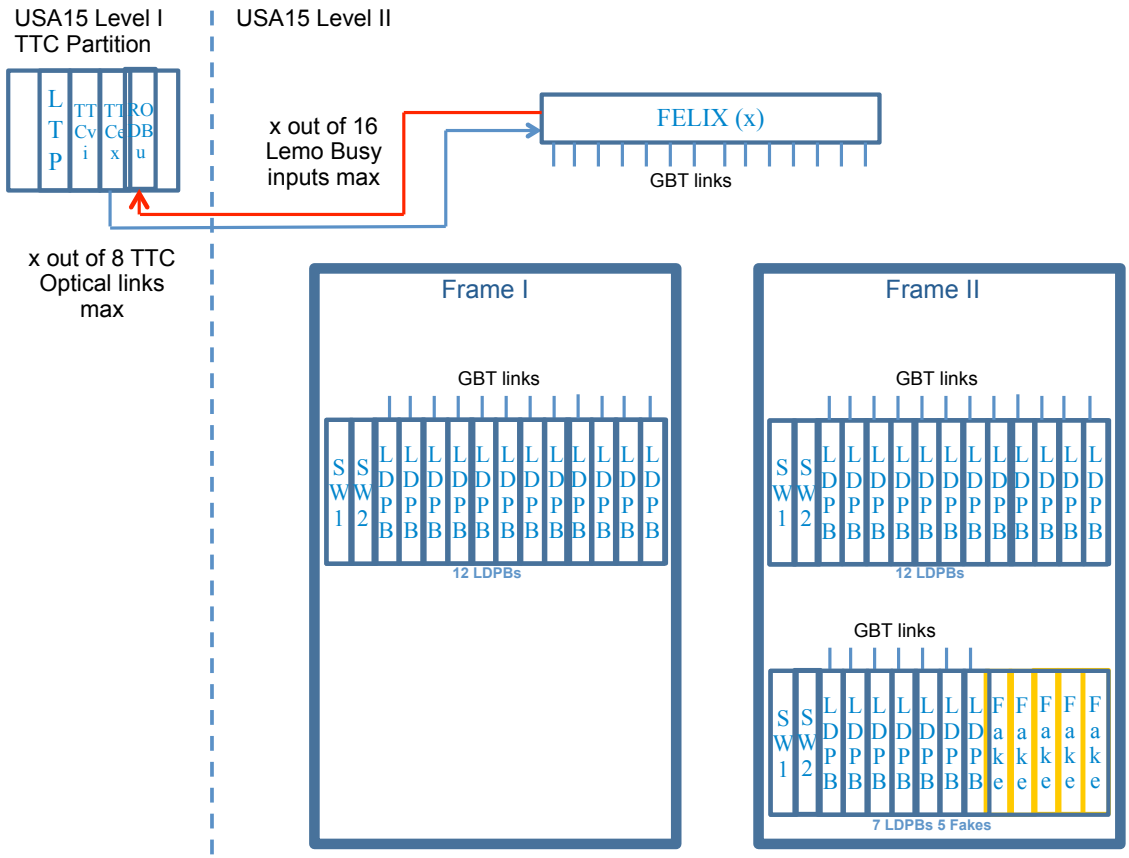


Figure 56. The LAr Digital Processing System (LDPS) in two frames (racks) and three shelves (crates), along with the TTC and Busy signal treatment for Phase I. The evolution for Phase II should be transparently handled by the FELIX interface. The blades labelled SW1 and SW2 are the two switches (switch blades). The slots labeled “fake" indicate dummy blades that act as placeholders.

5.4 Data flow through the BE system

A schematic representation of the data paths through the LDPS is presented in Fig. 57:

ADC Data The ADC Data from the LTDBs are received on the AMCs front face (~ 25 Tbps for LDPS) at 40 MHz (pink arrow).

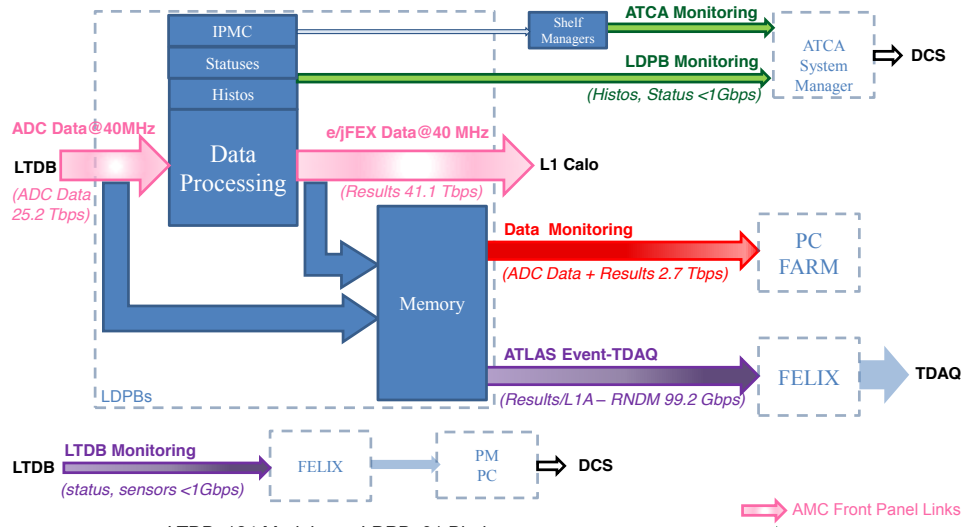
L1Calo e/jFEX Data $E_{\mathrm{T}}^{\text{Super Cell}}$ Data are transmitted from the AMCs front face (~ 41 Tbps for LDPS) at 40 MHz (pink arrow).

LTDB Monitoring Slow control data are transferred from the FE to the Partition Master PC (purple arrow).

Data Monitoring A subset of ADC Data and e/jFEX data are transmitted to the PC farm (i.e. not written to the ATLAS events).

ATLAS events A subset of ADC Data and e/jFEX data are transmitted via the LDPB zone 3 of the ATCA crate backplane to FELIX and are included in the ATLAS event by TDAQ.

BE DCS Status words and histograms from the LDPB, and ATCA status from the shelf manager are sent to DCS.



Data Flow Rates	ADC Data @40MHz	e/jFEX Data @40MHz	LDPB Monitoring	Data Monitoring	ATLAS Event-TDAQ	LTDB Monitoring	DCS
LTDB	204 Gbps	-	-	-	-	<<1 Gbps	<<1 Gbps
LDPB	814 Gbps	1.3 Tbps	<<1 Gbps	82 Gbps	3.2 Gbps	-	<<1 Gbps
GLOBAL	25.2 Tbps	41.1 Tbps	<1 Gbps	2.7 Tbps	99.2 Gbps	<1Gbps	<<1 Gbps

Figure 57. Schematic representation of the data paths and associated data flows of the LDPS. Data paths are represented as arrows; the data path name is written above the arrow and the nature of the data, with the total data flow rate, below the arrow. The data sources of the LDPS are represented as blue boxes. The hardware elements of the LDPS are with dashed lines. The table summarizes the data flow rates per LTDB and LDPB for each data path. The last row gives the total rate for the system.

Table 22. Organization of cables between the FE and the BE system for the different sub-detectors. The EM is divided into three parts: the barrel (Barrel EM), endcap (Endcap EM) and overlap (Overlap EM) regions. An AMC receives four or five ribbons from up to three LTDBs. The detailed organization for HEC and FCal is still under discussion.

Sub-detector	# of ribbons from LTDBs to one AMC	per AMC		Number of AMC
		# of ribbons	# fibers	
Barrel EM	2×2	4	40	32
Overlap EM	$2 \times 2 + 1$	5	48	32
Endcap EM	$4 \times 1 + 1$	5	45 (max 48)	32
HEC	8	tbd	tbd	tbd
FCal	4	tbd	tbd	tbd

5.4.1 Digital Super Cell Data from the FE system

An AMC receives 12-bit ADC data at 40 MHz from a maximum of 320 Super Cells through four sets of twelve-fiber ribbons, at 5.12 Gbps per fiber. Typically a total of 40 fibers are used to read out each LTDB by the AMCs.

The mapping between the Super Cell position on the detector and the channel in the L1Calo processing is currently being defined by a LAr-L1Calo working group. For an efficient treatment at L1Calo, Super Cells from one Trigger Tower ($\Delta\eta \times \Delta\phi = 0.1 \times 0.1$) are sent to the eFEX on one fiber. Whenever possible, adjacent regions from the calorimeter are grouped onto one AMC (for example, the overlap region between the EMB and the EMEC).

Table 22 shows a summary of the organization of fiber cables from LTDBs to AMCs. Each LTDB has four sets of twelve-fiber ribbons which connect to two or more AMCs. There are three types of connections for the EM part, the barrel (EMB), the endcap (EMEC) and the overlap regions. In the central barrel part, an AMC is filled with four ribbons from two LTDBs with two ribbons from each LTDB. In case of the intermediate region an AMC receives an additional ribbon from the endcap part raising the total number of ribbons to five. For the endcap region, four ribbons from an EMEC standard LTDB plus a ribbon from an EMEC edge LTDB connect to one AMC.

The current version of the mapping, which is well advanced for the EM but not yet fully studied for the HEC and the FCal, thus requires a connection of up to three LTDBs onto one AMC. The details are currently being worked out. With this model, on one AMC the total number of fibers (up to 48) in some cases originate in five separate ribbons. The connectivity arrangement with the use of pigtails on the AMC needs to be further studied, in order to end up with four 12-fiber ribbons connecting to the four 12-fold receivers[7].

A maximum of 124 AMCs are needed to receive the ADC data of 34k Super Cells from 124 LDTBs corresponding to 25.2 Tbps. This optical cabling to be made on the small size AMC will need to be carefully studied in the design phase and tested on prototype AMC boards.

5.4.2 Data flow to L1Calo

The Super Cell transverse energy ($E_{\mathrm{T}}^{\text{Super Cell}}$) is transmitted to L1Calo FEXs at 40 MHz directly from the AMC. There are three potential destinations: $E_{\mathrm{T}}^{\text{Super Cell}}$ to the eFEX (electron feature extractor),

[7] The feasibility of this pigtail connectivity still needs to be studied and proven. A possible fallback solution is to install a custom-built patch-panel splitting individual fibers from ribbons and grouping them back into new ribbons with the correct connectors.

Table 23. Summary of configuration of the data transfer on the AMC

	from LTDB	to eFEX	to jFEX	to gFEX
transfer speed	5.12 Gbps	10 Gbps	10 Gbps	10 Gbps
# of fibers for single set	40	16	2	1
duplication requirement	no	yes	yes	no
Total # of fiber per AMC	40	32	4	1

$\Sigma E_{\mathrm{T}}^{\text{Super Cell}}$ of Trigger Tower to the jFEX (jet feature extractor) and $\Sigma E_{\mathrm{T}}^{\text{Super Cell}}$ over an $\eta-\phi$ area of 0.2×0.2 to the gFEX (global feature extractor).

For the eFEX, the Super Cell transverse energies are calculated with a filtering algorithm described in Section 5.6, encoded in 10 bits as required by L1Calo, using 10 Gbps data links. In the baseline design, 11 bits (10 bits for $E_{\mathrm{T}}^{\text{Super Cell}}$ and 1 quality bit) are generated and sent to the eFEX. A requirement from L1Calo is that the transverse energies of the Super Cells in one Trigger Tower (e.g. containing 10 Super Cells in the EMB and the EMEC) must be sent on one fiber. On one fiber, the information for two Trigger Towers is grouped together and either eight or ten overhead bits are assigned to the data. Thus the transfer rate for two Trigger Towers corresponds to $(10$ Super Cells $\times$ 11 bits $\times$ 2 Trigger Tower $+10$ overhead bits$)\times$ 40 MHz $= 9.2$ Gbps per fiber. A further L1Calo requirement is that all outputs need to be duplicated, to resolve edge effects in the search algorithms. The 32 Trigger Towers on an AMC are sent on 2×16, i.e. 32 fibers, with a total rate of ∼300 Gbps.

For the jFEX, the Trigger Tower sums of the Super Cell transverse energies with 14 bits are sent. In this case, sums for 16 Trigger Towers can be carried on one fiber at 10 Gbps (including again 8 or 10 bits for overhead). Two fibers would be needed for 32 Trigger Towers. Again the duplication of outputs is needed, thus four fibers at 10 Gbps are required from one AMC to the jFEX.

2×2 Trigger Tower sums of the Super Cell transverse energies with 14 bits are required for the output to the gFEX. The data size is reduced by a factor of four compared to the jFEX, and the fiber duplication requirement is not needed, therefore only one fiber at 10 Gbps from each AMC to the gFEX is necessary.

In summary, as shown in Table 23 from each AMC, 32 fibers for the eFEX, four fibers for the jFEX, and one fiber for the gFEX all at 10 Gbps transmission connect to the FEX system.

5.4.3 Data to TDAQ

The proposed routing of the data towards FELIX and TDAQ on the ATCA carrier blade is outlined in this section. We have identified three use cases to send data to TDAQ after the Level-1 trigger has fired (a "Level-1 accept").

The first use case is to check the data transmitted to L1Calo. In order to validate data transmission from AMC towards FEX, $E_{\mathrm{T}}^{\text{Super Cell}}$ for all Super Cells and for all Level-1 accept (Level-0 accept for Phase-II) events will be part of the ATLAS event. The typical unit of data transfer towards the TDAQ readout corresponds to the transverse energy of each Super Cell coded onto 16 bits for a Level-1 accept (Level-0 accept in phase II) from one LDPB, i.e. 100 kHz $\times$ 320 Super Cells $\times4$ AMCs $\times$ 16 bits $\simeq 2$ Gbps. This leads to 2 Gbps per LDPB (62 Gbps for the entire system) in Phase-I, and 10 Gbps per LDPB (248 Gbps for the 31 blades) in Phase-II.

The second use case is for monitoring the calorimeter noise. We require that the RNDM triggers will fire at ∼1 Hz as during Run 1. Upon a RNDM trigger, all Super Cell raw data are transmitted (as currently done in Run 1 and Run 2 for the *standard readout*), in particular to permit to overlay minimum bias events and to measure the pileup noise. We assume that 10 ADC samples are transmitted per Super Cell together with its reconstructed energy. The associated bandwidth is

~ 230 kbps per LDPB (7 Gbps for the 31 blades). These data will be part of the ATLAS event and written to the RNDM stream. The average Super Cell transverse energy for random events is small ($\sim 1GeV$). The events from the RNDM stream will therefore only allow the validation of the $E_{\mathrm{T}}^{\text{Super Cell}}$ reconstruction for low energies.

The third case is to compare the $E_{\mathrm{T}}^{\text{Super Cell}}$ calculation from the trigger chain to the main readout. To accomplish this, a randomly selected set of events ($\simeq 1\%$) for which 10 samples (ADC values) for Super Cell with $E_{\mathrm{T}}^{\text{Super Cell}} > E_{\mathrm{T}}^{\text{thr}}$ will be included. Assuming that the requirement selects 1% of the Super Cell, this leads to $\simeq 1$ Gbps for each LDPB ($\simeq 30$ Gbps for the total system). This would allow the comparison of the $E_{\mathrm{T}}^{\text{Super Cell}}$ measured in the trigger chain with the E_{T} reconstructed from the main readout. The scheme will catch a fraction of saturated pulses which can then be analyzed offline.

In total, from these three cases, the expectation is to send ~ 100 Gbps to TDAQ from the LDPB.

In the main LAr ROD system, data from one FEB are processed by one DSP on one Processing Unit. The DSP computes ΣE_x, ΣE_y, ΣE_z, ΣE for the 128 channels of each FEB and transmits these results to the ROS. L2 algorithms can get hold of this summary data when computing global variables like ΣE_T, $E_{\mathrm{T}}^{\mathrm{miss}}$, and jet energy. The preparation of such global variables in the framework of the Phase-I trigger upgrade still needs to be addressed. Such calculations would have a small impact compared to the overall processing inside one FPGA. As a guideline in the current DSP processing, the time to compute the global variables is $\sim 5\%$ of the total processing time.

5.4.4 Data monitoring on LDPB

We keep the possibility open to develop a monitoring path with high bandwidth via the ATCA carrier fabric interface, exploiting the ATCA capability to drive a 10/40 GbE link. For instance, we may sample Super Cells, at 40 MHz, to verify the $E_{\mathrm{T}}^{\text{Super Cell}}$ reconstruction online. As an example, we may consider to transfer 10 samples for Super Cell with $E_{\mathrm{T}}^{\text{Super Cell}} > E_T^{\text{thr}}$ leading to a data bandwidth of 82 Gbps/LDPB (2.5 Tbps for the 31 blades) for 1% of the Super Cells. To reduce further this bandwidth, the threshold can be increased or only a fraction of these events can be recorded. Another possibility, often referred to as *oscilloscope mode* is to select one given Super Cell and transmit data at 40 MHz. The dataflow for this scheme is of order of ~ 1Gbps. The installation of a PC farm to read out these monitoring data is foreseen.

5.4.5 Slow control

To survey the hardware state of the various boards, a selection of status data, from both LTDBs and LDPBs, are transmitted to the PM PC which selects a small fraction of them to be sent to the ATLAS Detector Control System (DCS). As depicted in Fig. 57, two paths have been defined: one for the LTDBs and one for the LDPBs.

The LTDB monitoring consists of reading parameters associated to the hardware state of the board (e.g., the temperature or link status). These data are read out at a low frequency from the LTDB using GBT links, received by a FELIX board and then treated by the PM PC (see Fig. 57). A fraction of these data will be transmitted to DCS for archiving and global monitoring; others will be managed locally by the PM PC.

The hardware states of the LDPB carrier board and AMC will be read out at low frequency via GbE to the PM PC. Part of these data will be transmitted to DCS for archiving and global monitoring; others will be managed locally by the PM PC.

Finally, the AMC FPGA will fill histograms as another strategy to monitor the history of all input data.

5.5 Firmware

The development of firmware that is capable of handling a large number of high speed links is an essential aspect of the LDPS that must progress in parallel to the hardware design. As mentioned in Sec. 5.2 there are two noteworthy FPGAs in the LDPS: the FPGA on the AMC and the FPGA on the carrier board. The development of the firmware for the FPGA on the AMC is the most advanced, since this FPGA is on the critical path for the data flow to the L1Calo system. An overview of the strategy and estimated resource usage for this firmware is presented in Sec. 5.5.1, and the status of the firmware development is presented in Sec. 5.5.2.

5.5.1 Firmware on AMC

As described earlier in this chapter, the firmware on the AMC performs four main functions, the details of which are described in other sections:

- it handles a number of high speed links in the input from the LTDB (see Sec. 5.4.1),
- it performs a filtering algorithm to reconstruct the $E_{\mathrm{T}}^{\text{Super Cell}}$ every 25 ns (see Sec. 5.6),
- it outputs results and output to the L1Calo FEXs (see Sec. 5.4.2), and
- it processes and buffers the readout and monitoring data to be sent to TDAQ after a Level-1 accept (see Secs. 5.4.3 and 5.4.4, respectively).

Figure 58 shows a schematic block diagram of the AMC firmware.

The first step in the FPGA processing is the deserialization and demultiplexing of the incoming data. The data is output by the LOCic on the LTDB (see section 4.1.3.3.3); the exact output format of the LOCic serializer is given in the LOCic specification [43]. The 12-bit ADC data at 40 MHz for each channel must be aligned accordingly for the application of the filtering algorithm.

Next, the Super Cell transverse energies are calculated with filtering algorithms described in Sec. 5.6. The $E_{\mathrm{T}}^{\text{Super Cell}}$ encoding into 10 bits needs to be performed without losing the benefit of the fine energy granularity in terms of cluster reconstruction. The size of the quantization scale for each layer is also under discussion.

Algorithms for converting the Super Cell ADC data to the transverse energy in each Super Cell have been studied and are summarized in Sec. 5.6. The baseline algorithm to extract the $E_{\mathrm{T}}^{\text{Super Cell}}$ from the digitized samples every 25 ns is a Wiener filter with active forward correction. This algorithm has the following features:

- It outputs the $E_{\mathrm{T}}^{\text{Super Cell}}$ every 25 ns with a five-stage filter (the ADC data from five bunch crossings are used).
- It has the ability to identify pileup pulses over-wrapped in time.
- There is no offset on the energy due to pileup.

The performance of the filtering algorithm on the energy resolution and timing jitter based on simulations are summarized in Sec. 5.6.2.

An important point of discussion in Sec. 5.6.2 is the case of saturated input which have different shapes than nominal pulses. The filter algorithm may return the transverse energy in the wrong bunch crossing. To recover this wrong assignment, the proper bunch crossing can be recuperated from a neighboring Super Cell (either from a different calorimeter layer or from another Super Cell in the same layer).

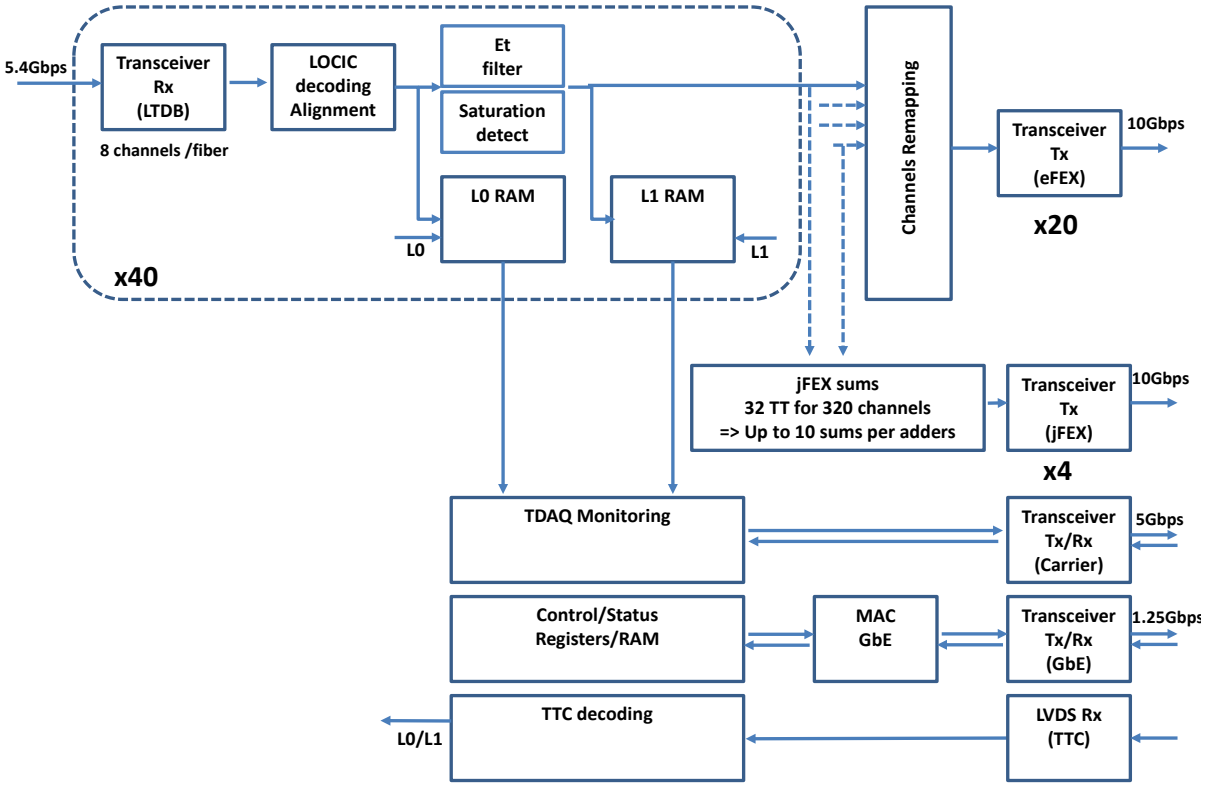


Figure 58. Schematic diagram of the firmware for the AMC FPGA.

Table 24. List of estimated resources needed for each block of the AMC firmware and specifications of FPGAs from Xilinx and Altera. Numbers in parentheses indicate the unit amount. FPGA-I and FPGA-II are from the datasheet for Xilinx Virtex-7 [36] and Altera ARRIA-10[38], respectively, which are currently the high-end FPGAs in the market or announced. (*) The number of DSP cells between the two types of FPGAs is not directly comparable.

resource	from FE	to FEX	Filtering	Monitor	1 GbE	GBT	Total	FPGA-I	FPGA-II
amount	48 (1)	48 (1)	48 (1)	1	1	1		1	1
Register (10^3)	96 (2)	26 (0.5)	52 (1)	5	4	1	~184	1424	1300
LUT (10^3)	48 (1)	23 (0.5)	38 (0.8)	5	3	2	~120	712	900
TX/RX	48 (1)		0 (0)	4	1	1	54	96	96
DSP	0 (0)	0 (0)	768 (16)	10	0	0	778	3360(*)	1518(*)
BlockRam (kbit)	0 (0)	3500 (72)	4320 (90)	5000	92	630	13500	67700	57000

The general feasibility of implementing the baseline algorithm has been demonstrated, respecting the latency requirements [44]. In the current implementation of this filter, 16 DSP blocks (see Table 24) are needed to evaluate one Super Cell. These results are very encouraging and give confidence that such a scheme is possible. The crucial limit of 6 bunch crossings processing time is also fulfilled by the Wiener filter with the active forward correction which is accomplished in only 5.75 bunch crossings. Studies will continue to further reduce this latency. The effects coming from the sporadic noise and noise bursts (observed during 2011-2012 data taking) needs to be investigated. More developments and tests are necessary to run the processing of 320 Super Cells in parallel with the baseline algorithm.

As also discussed in Sec. 5.4.2, Super Cells from one or more Trigger Towers will be grouped and summed for transmission to each L1Calo FEX. Serialization, multiplexing and remapping of the Trigger Tower results are necessary.

And finally, the input waveform data and the filtering outputs must be buffered pending an event accept (Level-1 accept at Phase-I, Level-0 accept at Phase-II). Sufficient memory resources exist on the FPGA so that all data can be buffered on the FPGA itself. The input waveform and filtered output is used to monitor and debug the filtering process as discussed in Sec. 5.4.4. Also, these data need to be handled to be sent over GBT links (see Sec. 5.2.2.2).

This configuration introduces one important functionality requirement: the FPGA transceivers must run at compatible link speeds, 5.12 Gbps for the receivers and 10 Gbps for the transmitters in the baseline choice (other lower speeds are also possible). In addition, the associated firmware will be developed such that one transceiver is used for TTC signals and four transceivers will be used for each GBT link for the data flow to TDAQ (see also Sec. 5.2.2.1.1).

Table 24 summarizes the current estimate of the resource use of the FPGA in each firmware block. This count is based on initial trials for which the design has not yet been optimized. On top of this estimation, a safety factor of 1.5 to 2.0 should be applied on the resource use (except number of links). Including contingencies for expected changes during Phase-II, the resource needs for the AMC FPGA seems to be fulfilled with the currently available high-end FPGAs.

5.5.2 Firmware developments

The current status of the firmware development effort are summarized:

- Transverse energy reconstruction in the presence of high pileup has been tested, applying a selection of filters, in a Xilinx evaluation kit, Xilinx KC705. This includes decoding and deserializing pseudo data from the LTDB; therefore, this latency has also been evaluated for one single channel.

- One overall VHDL infrastructure for the full 320 channels has been coded and is shown in Fig 59. This includes all aspects of AMC operation: receiving data, decoding and deserializing, filtering algorithm (in this case a FIR filter with χ^2 maximum detection), use of memory for the monitoring stream, transmitting encoded transverse energies to eFEX and jFEX with multiplexing, channel re-mapping and synchronizing with TTC clock. Based on this work, we have evaluated the FPGA resources use which is shown in Table 24.

- A test of the high-speed transmission with a MicroPOD, a crucial aspect for data transfer from LTDBs to AMCs and from AMCs to FEXs. The test is described in Sec. 5.2.2.1. The reception of data at 5.12 Gbps and transferring with 10 Gbps with a FPGA has been verified.

- A system test, though with data transmission only (i.e. no reconstruction) is being developed for tests at ATLAS LAr Electronics Maintenance Facility in Autumn 2013 - Spring 2014. The firmware is run on the ALTERA FPGAs of the LDPB pre-prototype board of Fig. 55.

5.6 Signal reconstruction

In the AMC the information from several consecutive bunch crossings are accessible, whereas further downstream in the FEXs the trigger decisions will be taken for each bunch crossing on the basis of Super Cells energies in larger $\eta - \phi$ regions without taking into account values from consecutive bunch crossings. The aim of the signal reconstruction on the AMC is therefore to deliver the energy that was deposited in each bunch crossing as precisely as possible while reducing to a minimum the contributions of pileup in the current and consecutive bunch crossings.

5.6.1 Signal characterization and filter requirements

The digitized Super Cell signals have a bipolar shape that typically extends over 25 bunch crossings. In the dominant number of LHC bunch crossings, the amplitude spectrum and signal rate is given by the low-energy background from inelastic proton-proton collisions, as well as electronic noise [45].

In this environment, the goal of the signal reconstruction is to extract the signal energy deposits such as electromagnetic showers of electrons and photons, hadronic tau decays, quark and gluon jets, as well as total and missing energy. These energy deposits must be reconstructed with the best possible resolution and assigned to the correct bunch crossing with a high efficiency and low misidentification rate.

The requirements of the energy reconstruction algorithm are that it should run stably in all ATLAS running conditions and be as insensitive as possible to saturation and irregular detector noise like spikes and ringing. The algorithm should correctly reconstruct the energy regardless of the bunch-crossing position within the LHC bunch structure. Finally, the implementation should be consistent with the latency budget of at most 5-6 bunch crossings between the input and output of the result.

To meet these requirements, digital filtering techniques can be applied in order to suppress in-time noise from the electronics and pileup events, as well as to correct or suppress out-of-time signal pileup effects. These techniques can also be implemented in modern FPGAs. The proposed hardware solution provides sufficient resources such that the proposed algorithms can be further optimized and adjusted to future requirements, which may evolve with the experience with the trigger and detector systems. A variety of digital filtering techniques have been explored, and are presented in the following section.

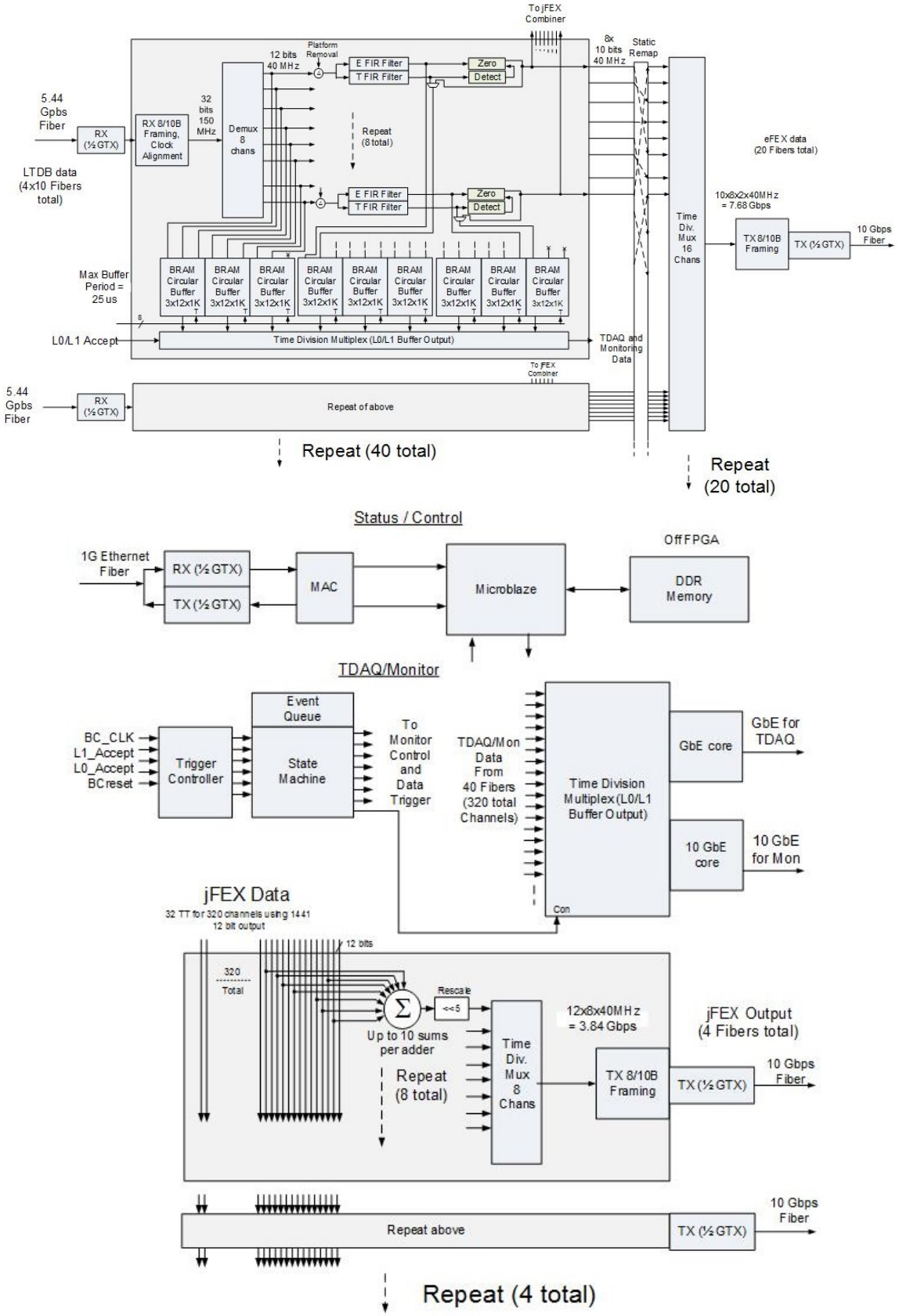


Figure 59. A possible firmware implementation for the AMC, designed for 320 channels on a Xilinx Virtex-7 FPGA.

5.6.2 Filter algorithms and performance

Performances of various digital filters are compared. All filters fulfill the requirement of latency when restricted to a certain filter depth, respectively to a given number of input signals, s_i, of at most 5 after the given bunch crossing. The bunch crossing identification is implicitly performed by producing ideally exactly one valid filter output with a fixed time delay with respect to the rising edge of the Super Cell signal pulse. For all filters, the detailed parameter settings and noise suppression mechanisms need to be studied not only with respect to energy reconstruction and signal identification, but also taking the subsequent trigger feature extraction into account.

The following filters are studied for implementation in the LDPS system:

- The optimal filter technique [7] is used for the first set of filters. They apply a linear combination of the input signals, s_i,

$$E = \sum_{i=1}^{n} a_i s_i \,, \tag{7}$$

$$\tau \times E = \sum_{i=1}^{n} b_i s_i \,, \tag{8}$$

  where a_i and b_i are the filter coefficients such that E and τ are the energy and the time of the signal. The filter depth (n) is typically 5. This filter has a finite impulse response (FIR). The filter coefficients are optimized for total (electronics and pileup) noise suppression and insensitivity to time shifts. The energy measurement is unbiased for an infinitely long bunch train. For bunch trains with finite length, the bias (positive/negative at beginning/end of the train) will be proportional to the bunch intensity, unless a bunch crossing dependent correction is applied.

  While the energy measurement of the optimal filter method represents the best estimate of energy deposition in the current bunch crossing in the presence of electronic and pileup noise, additional requirements can be used to reject cases in which the energy measurement is severely distorted by noise.

  OF$_{\mathbf{max}}$ The reconstructed energy E_j in bunch crossing j is required to be the *maximum* value in a sequence of 3 reconstructed energies:

$$E_j = \max(E_j, E_{j-1}, E_{j-2}) \tag{9}$$

  As a consequence, signals in subsequent bunch crossings can not all be detected and transmitted. A gap of at least one bunch crossing between two output signals appears. The decision with a maximum search intrinsically has an additional latency of 1 bunch crossing.

  OF$_{\chi}$ The measured signal s_i ($i = 1,\ldots,5$) should be compatible with the normalized pulse shape, g_i, expected for the given Super Cell at selected sampling points:

$$|\chi_i| = |S_i - E \cdot g_i| \leq \frac{1}{2^N} |S_i| \text{; for } i = 1,\ldots,5 \tag{10}$$

  The exponent N is a free parameter for a relative precision requirement. It is chosen to be easily implementable in hardware, namely carrying out a bit shift of N bits instead of a division. The second free parameter is the number of sampling points $m = 1\ldots5$ required to fulfill the precision requirement. For the value of $N = 2$ and $m = 3$ a good compromise between signal detection and fake efficiency is observed.

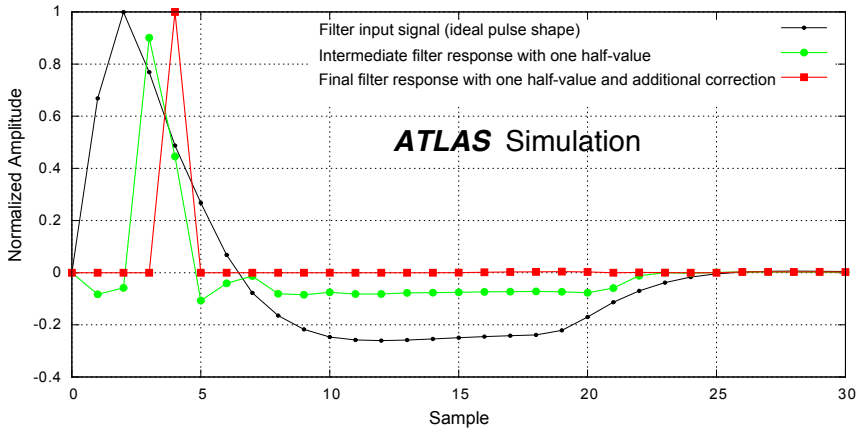


Figure 60. Input pulse (black) sampled at each bunch crossing together with the output of the first (green) and second (red) stage of the Wiener Filter with forward correction. The connecting lines are included to guide the eye.

OF$_\tau$ The measured peak time τ can be required to be compatible with zero: $|\tau| < 5$ ns. The timing condition implicitly requires the agreement of the reconstructed pulse shape with the expected pulse shape.

In both the OF$_\chi$ and OF$_\tau$ methods, significant out-of-time pileup causes a loss of measurement of the in-time signal.

- A Wiener filtering technique with an active forward out-of-time pileup correction is used for the second type of filter:

WF$_{fc}$ For the Wiener filter with forward correction, first a Wiener filter is applied:

$$E = \sum_{i=1}^{n} a_i s_i \text{ , with } n = 6, \tag{11}$$

where the filter coefficients a_i are trained to transform the ideal input signal pulse shape into an output of a single peak E_j followed by a value E_{j+1} half its amplitude, as illustrated by the green points in Fig. 60. Electronics noise is also considered in the filter training.

After the application of the Wiener filter stage, input pulses that do not have the expected shape (a peak followed by a value half its amplitude) are rejected. The required ratio of $E_{j+1}/E_j > (0.5 - m)$ (instead of 0.5) allows additional room for noise and in-time pileup. Good performance with the margin parameter $m = 0.15$ is seen, but may also be varied in different scenarios.

Furthermore, when a signal pulse passes the ratio requirement, an active forward correction of out-of-time pileup is applied. The first Wiener filter can not fully compensate when the incoming pulse shape and a trailing non-zero output is produced. Therefore a correction stage levels out the non-zero tail by applying two additional FIR filters and a constant to compensate for the negative lobe. In this way, one single output signal is produced at given distance in time to the bunch crossing, while all out-of-time pileup contributions are actively removed. In case of gaps in the bunch crossing sequence, caused e.g. by the bunch train structure, effects from overcompensation of out-of-time pileup,

like for OF-based filters, do not occur. The final output is illustrated by the red points in Fig. 60. Note that all of the outputs are ~ 0 except for the single peak signal.

One disadvantage of the active correction is the infinite impulse response (IIR) that may lead to a run-away of the filter output in case of incoming pulse shapes that do not match the expected shape. In case more than a configurable number of measured signal values above an also configurable threshold are detected (e.g., four energies in a row above 20 GeV), the forward pileup correction stage is reset. This reset condition has not been observed in simulations of a regular event sequence with 10 million bunch crossings. The active correction of out-of-time pileup improves the energy reconstruction in case of non-equidistant bunch-crossing configurations, e.g. at the beginning of bunch trains.

The performance of the different filters is simulated using a sequence of 10 million bunch crossings with $\langle\mu\rangle = 80$. The simulations use the PYTHIA [10] Monte Carlo generator and the full detector simulation of the energy deposits in each Super Cell with GEANT4 [9] in the Athena software framework [8]. The pulse shapes studied here are from the central barrel calorimeter region (at $\eta = 0.1$) and from the endcap calorimeter region (at $\eta = 2.4$) in the front and middle layers. The rise time after shaping is 27 ns in the front layer and 40 ns in the middle layer. Signal pulses in the energy range up to 100 GeV are furthermore injected such that these do not overlap in time. The input pulses are discretized with a least significant bit (lsb) of $E_{\mathrm{T}} = 32$ MeV in the front layer and $E_{\mathrm{T}} = 125$ MeV in the middle layer.

Figure 61 shows the energy resolution for the injected signals in the middle layer using different filter implementations. All filters show a similar performance, with an intrinsic relative resolution of better than 2% above $E_{\mathrm{T}} = 4$ GeV. The $\mathrm{WF_{fc}}$ filter has a $10-30\%$ worse resolution compared to an optimal filter method, depending on the energy corresponding to the least significant bit and on the exact pulse shape. The E_{T} difference as a function of input E_{T} for the $\mathrm{WF_{fc}}$ filter is also displayed in Fig. 61, for all input energy values of the simulated event sequence.

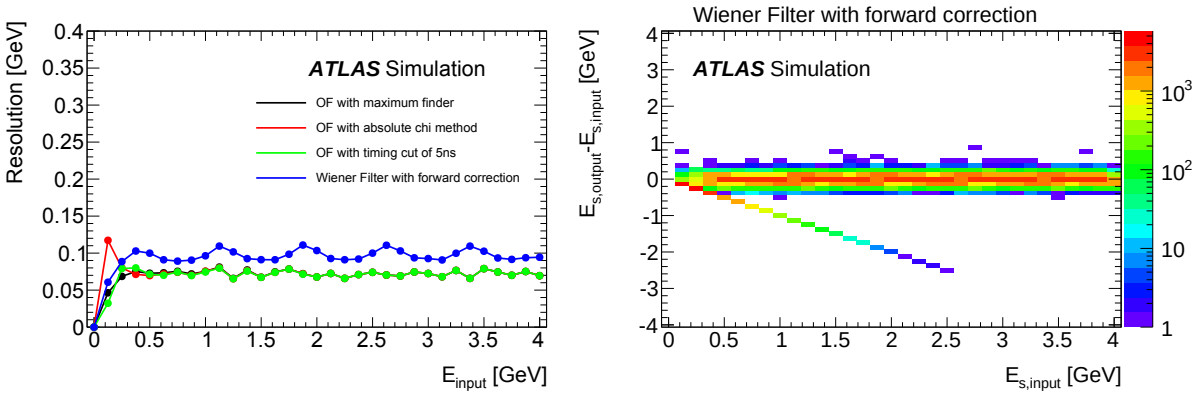


Figure 61. (a) Transverse energy resolution of different filter implementations for a middle layer pulse with a least significant bit of 125 MeV. The structure observed is due to this bit resolution effect and is much reduced for a least significant bit of 32 MeV, as applied in the front layer. (b) Difference in transverse energy with respect to the input pulse for the Wiener Filter with forward correction ($\mathrm{WF_{fc}}$). Vanishing filter output values for non-zero input energies are also displayed.

The pulse detection efficiency is determined as the fraction of reconstructed signals which are detected at the correct bunch crossing and in agreement with the expected E_{T} to within 20% or $3\,\sigma$

of the relative resolution. Figure 62 shows the detection efficiency for the OF_{max} and the WF_{fc} filters for fast (27 ns) and slowly rising pulses (40 ns). The inefficiencies at very low energies are due to electronics noise and due to the cancellation of the average bipolar signals from pileup events. The OF_{χ}, OF_{τ}, and WF_{fc} filters reach full efficiency only at slightly higher energies than the OF_{max} algorithm since they have stronger requirements on the reconstructed pulse shape. The performance of cuts on $|\chi|$ or timing appear to be more influenced by the pulse shape. On the other hand, they are able to detect pulses in a nearby bunch crossing, while the OF_{max} filter necessarily has a gap of at least 1 bunch crossing between subsequent reconstructed pulses. The WF_{fc} filter can even reconstruct energies in every bunch crossing properly. This is illustrated in Fig. 63, which shows the gap between two reconstructed signals. With the OF_{max} and OF_{χ} methods, the energy measurement following a reconstructed signal is completely suppressed, while with WF_{fc} and OF_{τ} methods, two consecutive signals can still be reconstructed.

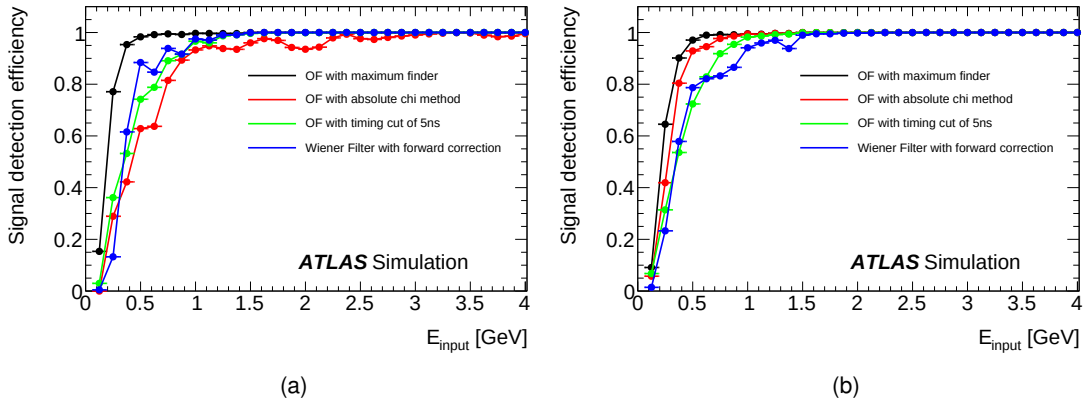


Figure 62. Signal detection efficiency for the optimal filter with maximum peak finder (OF_{max}), $|\chi|$ criterium (OF_{χ}) and timing cut (OF_{τ}), as well as for the Wiener filter with forward correction (WF_{fc}), for fast (a) and slowly (b) rising pulses. In-time and out-of-time pileup effects as well as electronics noise are included.

Furthermore, the rate of fake output from the filters is studied. Figure 63 displays the rate of filter output without any input as a function of incorrectly reconstructed E_{T}. The Wiener filter with forward correction generally produces less fake signals at zero input.

Filter output signals which are above the input E_{T} by more than 20% (3σ of the relative resolution) appear only at very low energies, close to the E_{T} equivalent of the least significant bit. However, such small energy signatures may contribute to the shower shape reconstruction of electrons or taus. This effect should be investigated further.

The dynamic range of the digitized pulses will be optimized for the overall performance by taking into account the effect of noise due to the least significant bit and second stage noise in the amplifiers, and to the signal reconstruction for saturated pulses. Current studies assume a least significant bit (lsb) of transverse energy equal to 32 MeV and 125 MeV in the first and second layer, respectively. With a 12-bit range, E_{T} values up to 102 GeV and 400 GeV in the corresponding calorimeter layers will be properly processed without loss of precision. Very energetic electrons, which have a more concentrated shower than taus or jets, may exceed these values. In addition, saturation of the analog electronics leads to a distorted pulse shape after analog shaping of the linear mixer stage, and a truncation of the pulse after passing the pre-amplifier stage, which is illustrated in Fig. 64. Simulations of electromagnetic showers from 7 TeV electrons at different η show that the most energetic Super Cell around the reconstructed electron reaches 5.2 TeV in the middle layer, as shown

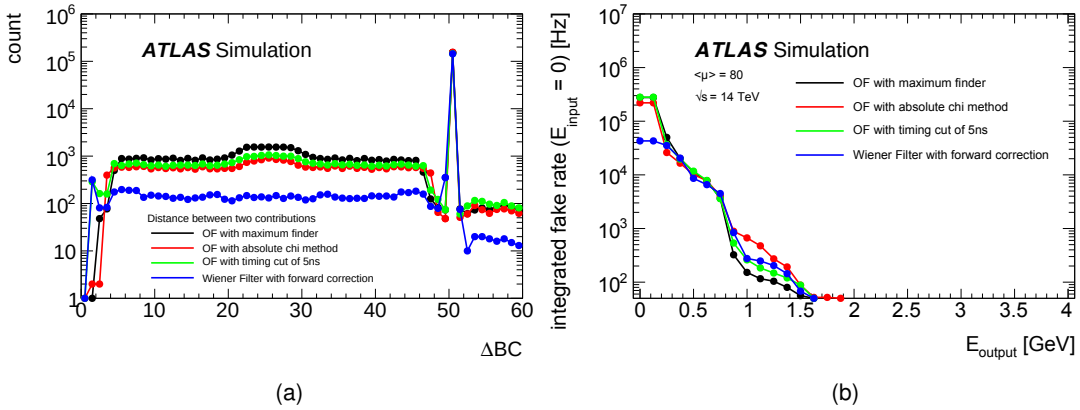


Figure 63. (a) Distance in bunch crossings between two reconstructed energies for the different signal filters under study. The spike at 50 represents the separation between two reconstructed injected signals, while other points represent the reconstructed energy from the pileup. For OF_{max} and OF_{χ}, $\Delta BC = 1$ is completely suppressed. (b) Rate of fake response on zero input for the optimal filter with maximum peak finder (OF_{max}), $|\chi|$ criterium (OF_{χ}) and timing cut (OF_{τ}), as well as for the Wiener filter with forward correction (WF_{fc}). In-time and out-of-time pileup effects as well as electronics noise are included.

in Fig. 65. The maximum energies in the presampler, front, and back layers are 50 GeV, 450 GeV, and 200 GeV, respectively. Saturation starts at 700 GeV in the middle layer and at 500 GeV in the front layer. Therefore, saturation effects are only expected in the Super Cells of the middle layer.

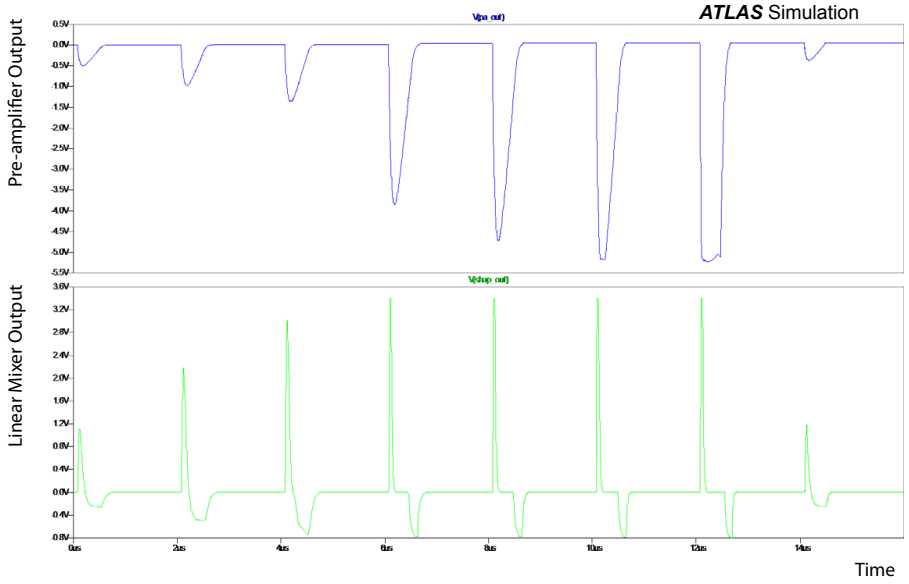


Figure 64. Output signals from the pre-amplifier and linear mixer at $\eta = 1$ in the middle layer, for a sequence of Super Cell energies with 256 GeV, 500 GeV, 700 GeV, 2000 GeV, 2500 GeV, 3000 GeV, 5200 GeV, and finally 256 GeV. Saturation effects are visible above 700 GeV.

With the given digitization range, saturated pulses in the middle layer can thus be identified by

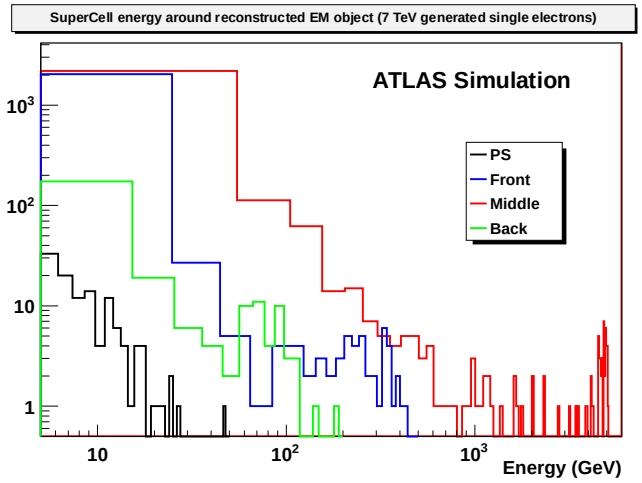
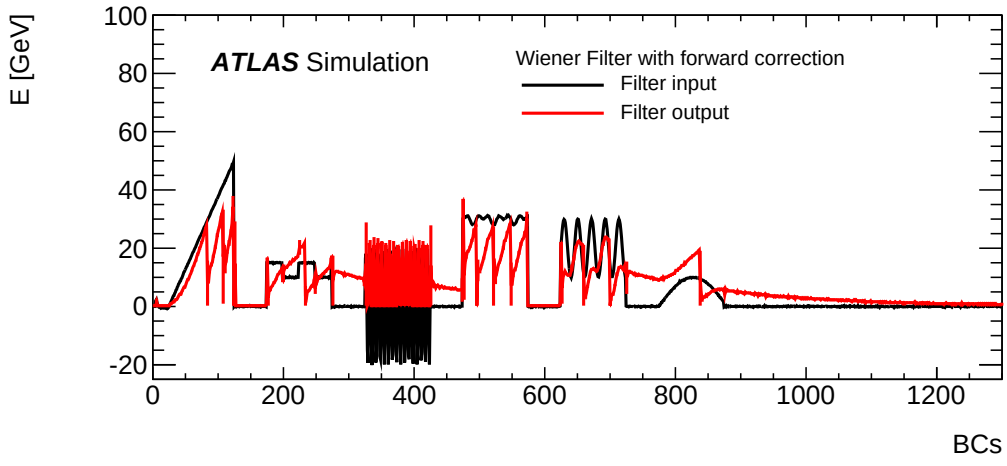


Figure 65. Energy deposit in Super Cells in the four layers of the LAr Calorimeter from electromagnetic showers of 7 TeV electrons. The corresponding signal amplitude may be driven into saturation only in the middle layer.

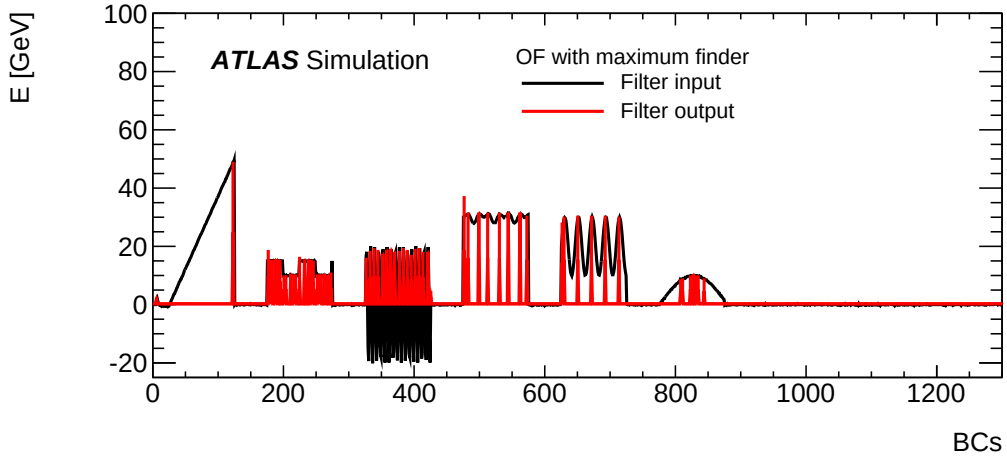
their amplitude reaching a given threshold value, or simply by the most significant bit being set. In the case of an irregular pulse shape, the signal reconstruction algorithms will typically fail to extract the correct energy, which is less important in this energy range, but more importantly will also fail to identify the correct bunch crossing. The bunch crossing may then be determined from neighboring cells processed within one FPGA, or by extracting the correct bunch crossing from the pulse itself. In case of the OF_{τ} method, the distorted pulse will result in a bias in the timing measurement, which may be taken into account when identifying the bunch crossing for saturated pulses. The other filters may deal with saturation effects e.g. by restricting the pulse reconstruction to the rising edge of the signal when performing the bunch crossing identification.

The energy and timing resolution has a weak dependence on the phase of the sampling time relative to the peak of the signal, as long as the pulse shape is well understood, and the shift is stable and can be determined experimentally. Extensive experience with the calibration of calorimeter cell readout can be directly applied to that of Super Cells. The optimal filter method has been demonstrated to be insensitive to timing jitter (within a few ns), because the optimal filtering procedure allows the signal to be slightly out of time.

Irregular inputs to the filter algorithms, like noise spikes, ringing and saturated pulses, prevent the algorithms from extracting the energy deposit correctly. Filters with a finite impulse response, like the optimal filter-based algorithms, are relatively robust against such inputs since such events can not affect the filter output for longer than the number of input samples used in the filter. However, the feedback loop of the Wiener filter with the forward correction introduces an infinite impulse response. A priori, an irregular pulse will influence all subsequent measurements. Figure 66 (a) shows the response of the WF_{fc} to noise spikes and ringing. The stabilization of the WF_{fc} depends on the shape of the injected noise pattern, and may take up to 300 bunch crossings using the filter implementation at the time of this proposal. For comparison, the OF_{max} algorithm is shown in Fig. 66 (b). In general, the filters can reject some irregular pulses online at signal reconstruction level, but fully efficient rejection of noise has to be carried in out offline by monitoring of input data with full event reconstruction.



(a)



(b)

Figure 66. Filter response to irregular noise patterns, like spikes and ringing, for the WF_{fc} (a) and the OF_{max} (b) algorithms. The WF_{fc} follows the noise pattern until a reset condition is applied. This condition can be optimized to the noise patterns observed in the detector. In certain cases the feedback remains active, and the noise output amplitude decreases only exponentially. The optimal filters intrinsically stabilize when the number of bunch crossings after the injected noise equals the filter depth.

5.7 Potential variations on the baseline design and compatibility with Phase-II

5.7.1 Variations on the baseline

The system described relies on the availability of transmitters running at 10 Gbps from the LDPBs to the FEXs. The data transfer speed to the jFEX and gFEX with 6.4 Gbps is possible. However, as described in Section 5.5.1, the baseline data transmission to eFEX is 2 Trigger Towers per fiber. The implication of running the LDPB to eFEX transmission at 6.4 Gbps is a significant reduction of data transfer rate per fiber. Possible mitigation solutions could be:

- Increase the number of fibers. Use 1 Trigger Tower per fiber which would require 64 fibers per AMC. This solution is difficult in practice, since the duplication of outputs would need to be reconsidered. Also passive optical splitting could be evaluated.
- Reduce the size of data to the eFEX with a specific algorithm, e.g. BCMUX as currently applied in L1Calo at Trigger Tower level. In principle, the BCMUX algorithm reduces the data size by almost one half, therefore data for 2 Trigger Towers could again be transmitted per fiber. However, this solution needs to be studied at the Super Cell level in order to verify that there is no degradation in the cluster energy resolution or isolation performance.

LAr will keep the baseline transmission speed, at 10 Gbps for the hardware developments and system tests. A firmware downgrading to 6.4 Gbps transmission speed is always feasible.

5.7.2 Compatibility with Phase II

5.7.2.1 Timing The Phase-I upgrade of the Liquid Argon electronics is designed to be compatible with the foreseen replacement of the LAr readout electronics in Phase-II where the original electronics (FE, BE, TTC) will be replaced. The Phase I L1 trigger electronics will remain in place to provide a L0 trigger. A few modifications will have to be implemented:

- The entire ATLAS TTC system will be replaced at Phase-II. In the presented design for the Phase-I stage, the TTC information is sent via FELIX to the LDPS and the LTDBs (see Fig. 56). Therefore the TTC upgrade will be covered by the FELIX system.
- At Phase-II the Busy for each blade will be transmitted on the return path of the TTC optical link within the upgraded TTC functionality.

5.7.2.2 Readout and Monitoring As described in previous sections, the monitoring and readout dataflows are driven by the Level-1 accept rate. The Phase-II Level-0 rate is expected to be ~500 kHz compared to the 100 kHz Level-1 rate in Phase-I. This rate, which is a factor of five times higher in Phase-II, would lead to a very large total amount of data (~200-300 Gbps) to TDAQ or local PCs. A strategy will need to be defined in due time.

5.8 Conclusions

The essential role of the LDPS is, at 40 MHz, to receive on optical fibers, data from the LTDBs, ~ 25 Tbps for 34k Super Cells, to compute the transverse energy in each Super Cell, $E_{\mathrm{T}}^{\text{Super Cell}}$, and to send these data, ~ 41 Tbps, again on optical fibers, to the Level-1 Calorimeter Trigger system (L1Calo). It also provides the surrounding infrastructure to this main task.

The LDPS is based on ATCA platform boards, powerful FPGAs and fast optical links. The ongoing developments which have been shown in this section give confidence that the design as presented can lead to an operational system for 2018.

In parallel to the hardware developments, first studies and tests of the associated firmware have been presented.

A demonstrator system is being setup at the LAr Electronics Maintenance Facility (EMF) with boards and software developed so far. It will be used in the validation of the FE elements (baseplane, LTDB) for a possible installation of one upgraded FE crate before the LHC restarts in 2015, as well as serving as a testbed for the LDPS development.

6 Project Organization and Milestones

6.1 Project organization and management

Figure 67 shows the organization of the LAr Phase-I Upgrade Project as endorsed by the LAr Calorimeter Group in the spring of 2013. The project is an effort organized and managed entirely within the LAr Calorimeter Group. Design and construction of the upgraded trigger readout electronics is deeply integrated in the existing readout system and in its operations, sharing significant resources and expertise. Thus a separated organization of the upgrade project would introduce additional complexity and potential risk, both from a technical and management point of view.

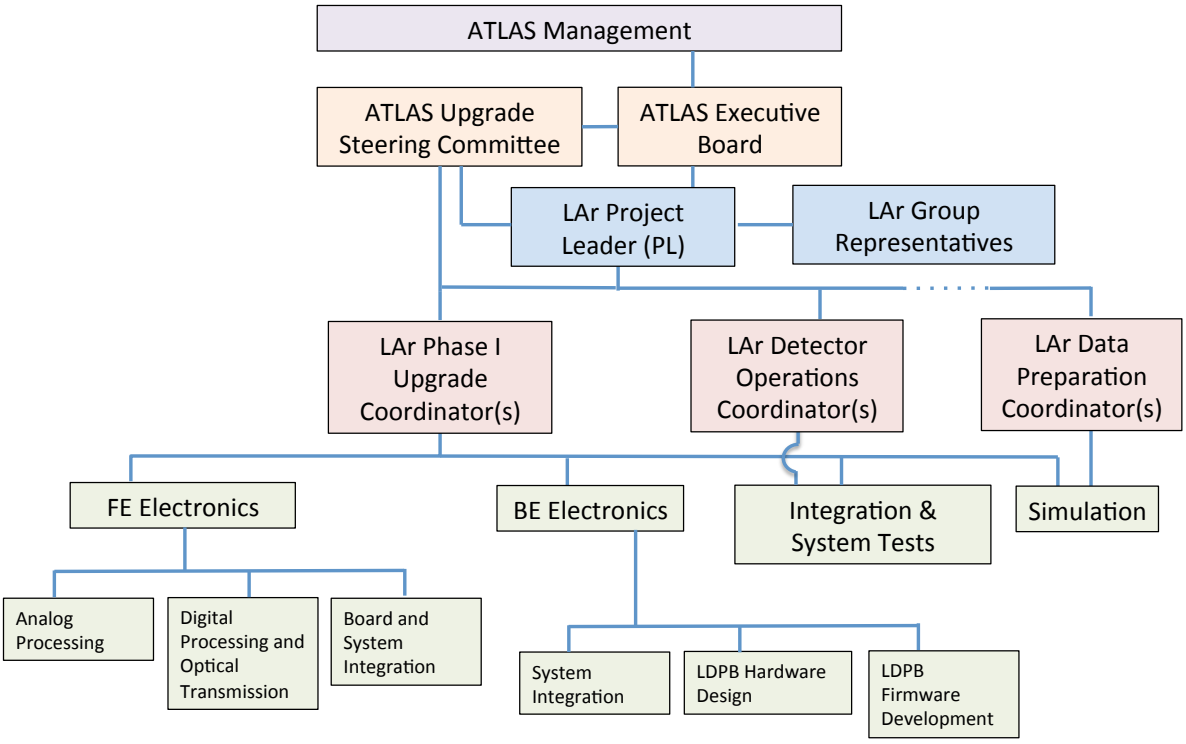


Figure 67. Organization and management structure of the LAr Phase-I upgrade project.

6.1.1 LAr Group Representatives

The institutional representatives of institutes participating to the LAr upgrade project are members of the LAr Group Representatives Board (LAr GroupReps) and are set on an equal footing with the other representatives of LAr Calorimeter Group institutes that built the current LAr Calorimeter and are participating and responsible for the operations of the LAr system. The LAr GroupReps is the formal body which endorses major technical issues and decides the allocation of resources and responsibilities following the recommendations by the LAr Project Leader and the LAr Steering Group (LASG). Participation of a new institute in the LAr upgrade project requires the institute to become an effective member of the LAr Calorimeter Group. The admissions process is consistent with the ATLAS policies [46]: new requests are reviewed and approved internally by the LAr GroupReps and discussed and endorsed by the ATLAS management.

6.1.2 Management structure

The ultimate responsibility of the LAr upgrade project belongs to the LAr Project Leader (LAr PL), the program manager of all LAr activities. The LAr PL is elected by the LAr GroupReps for a two year term (renewable) as prescribed by the ATLAS collaboration rules. Two LAr Phase-I Upgrade Coordinators (Level-1 managers in the project organization) are leading the LAr upgrade project and report directly to the LAr PL. They are ex-officio members of the LASG and of the LAr Management Group (LAMG), a restricted group of the LASG overseeing and organizing the LAr day-by-day activities and operations. One of the LAr Phase-I upgrade coordinators - together with the LAr PL - represents the LAr upgrade project in the ATLAS Upgrade Steering Committee.

The LAr Phase-I upgrade coordinators manage the activities of four sub-groups: (i) Front-End (FE) electronics, (ii) Back-End (BE) electronics, (iii) Integration & System Tests, and (iv) Simulation. Each of these sub-groups is led by one convener appointed by the upgrade coordinators. Each sub-group convener organizes and coordinates the work in his/her area of responsibility.

The Simulation sub-group convener manages the upgrade simulation performance studies and the upgrade software developments, reporting to both the LAr Phase-I upgrade and LAr data preparation coordinators. A further level of management has been defined for the FE and BE sub-groups to best match the project breakdown structure and the core deliverable tasks detailed in Sec. 6.2 and in Appendix C.

FE electronics sub-group

- Analog signal processing
- On-board (LAr Trigger Digitizer Board, LTDB) digital processing and optical transmission
- System integration of the LTDB

BE electronics sub-group

- LAr Digital Processing Blades (LDPB) Design
- LDPB Firmware development and interface to online software
- System integration aspects of the LDPB

Modifications of the project management structure may occur to optimize its efficiency as the project enters new phases (e.g. production, installation, commissioning) in the coming years.

6.2 Deliverables and Cost estimates

A detailed Product Breakdown Structure (PBS) of the project with milestone dates can be found in Ref. [47] and is included in Appendix C for completeness. The CORE cost profile for all of the elements of the project are summarized in Table 25.
Cost estimates are based on quotes of electronics parts where possible and on estimated construction costs for the options discussed in the Front-End and Back-End descriptions of Secs. 4-5.

6.3 Schedule and milestones

The main deliverables to be developed and key dates in the project are summarized in Table 26 and shown in Fig. 68. Included in this chart is a system validation step ("in-situ Demonstrator") we foresee to install in ATLAS at the end of LS1 and which is described in detail in Appendix D.

The dates presented here are driven by the timescales of the coming shutdowns and expected periods of access to the detector (see Sec. 6.3.2). The milestones should be taken as the latest

Figure 68. Time-line of project.

Table 25. LAr Phase-1 Upgrade summary CORE cost table in units of kCHF

PBS	Item	Cost	2013	2014	2015	2016	2017	2018
1.1	**Front-End electronics**							
1.1.1	Baseplane	1076	-	100	438	538	-	-
1.1.2	Layer Sum Boards	225	-	12	100	112	-	-
1.1.3	LTDB	2958	-	400	1079	979	500	-
1.2	**Optical Cables**	592	-	-	-	296	296	-
1.3	**Back-End electronics**							
1.3.1	ATCA+shelves	40	-	-	10	10	20	-
1.3.2	LDPB	2573	-	100	986	1086	400	-
1.3.3	RTM	55	-	-	27	28	-	-
1.3.4	TTC Optical Couplers	8	-	-	-	4	4	-
1.3.5	In-shelf switches	46	-	-	-	23	23	-
1.3.6	Receiver PC	14	-	-	-	7	7	-
1.3.7	Controlling PC	5	-	-	-	3	2	-
	Total	7590	-	612	2640	3086	1252	-

dates, while still including sufficient contingency. However, for such items where the design can be fixed early, it might be advantageous for reasons of cost-leveling to start production early.

As shown in Secs. 4 (Front End electronics) and 5 (Back End electronics), in some cases there are several options being explored for the final implementation. In the following cases final decisions cannot be taken at this stage, as work is still needed to determine the optimal solutions:

- ADC range implementation, E to Et weighting factor implementation
- ADC chip selection
- LTDB architecture choice
- FPGA model choice
- FELIX links interface implementation

In some cases, the choice among alternate solutions options may be straightforward, based on the development work and test results. In those instances those options will clearly be implemented as base solutions. In other cases, a decision process will need to be established through a preliminary design review (PDR). These reviews will formally evaluate test results and determine the implications for production, proposing recommendations to the management that will take a decision. This would be particularly important if a clear consensus does not emerge from the review. Some tentative dates for PDRs, where needed, are scheduled in Table 26.

Understanding and development of the firmware (FW) to operate the different FPGAs need to be pursued. However, detailed breakdowns with FW deliverables and milestones can be established at a later stage.

6.3.1 Construction

The deliverables are established and assessed through (i) a FDR (Final Design Review) where final plans for design are presented and agreed upon based on prototype test results, and (ii) a PRR

Table 26. LAr Phase-1 Upgrade key dates for main deliverables. As explained in the text, these dates take into account constraints arising from shutdowns and periods of access to the detector and as such represent the latest dates for which these activities should be scheduled

Item	# units	Prod end	Prod start	PRR	FDR	PDR
Front-End						
Baseplane	124	5-2017	11-2016	9-2016	2-2016	
LSBs	2328	9-2017	9-2016	7-2016	12-2015	
Integrated LTDB	124	9-2017	3-2017	1-2017	6-2016	5-2014
Analog section	124*4	1-2017	10-2015	9-2015	4-2015	
Digital Components						
ADC	124*80	1-2017	10-2015	9-2015	4-2015	3-2014
ASIC Serializer	124*20	1-2017	10-2015	9-2015	4-2015	
ASIC Laser Driver	124*40	1-2017	10-2015	9-2015	4-2015	
VCSEL mezzanine (TOSA)	124*20	1-2017	10-2015	9-2015	4-2015	
DC Powering	124	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	124*4	1-2017	7-2016	5-2016	10-2015	
Cooling plates	124*2	1-2017	7-2016	5-2016	10-2015	
Long Fibers	58	7-2017	1-2017	11-2016	4-2016	
Back-End						
LDPB	34	1-2017	10-2015	9-2015	4-2015	
AMC & FPGA	34*4	1-2017	10-2015	9-2015	4-2015	10-2014
IPMC	34*1	1-2017	10-2015	9-2015	4-2015	
MMC	34*4	1-2017	10-2015	9-2015	4-2015	
Optical pigtails	34*4	1-2017	10-2015	9-2015	4-2015	
MicroPod Cooling block	34*4*8	1-2017	10-2015	9-2015	4-2015	
Carrier Board & RTM	34	1-2017	10-2015	9-2015	4-2015	10-2014

(Production Readiness Review) which considers the final design pre-production experience and first test results with final components.

The PDR, FDR and PRR dates are milestone dates to organize the interfaces between different parts, in particular when built by different institutions.

Milestones for the production deliverables take into account the need for commissioning tests at CERN in preparation for installation on the detector. Finally, access to the detector determines the schedule for installation. This constraint is most severe for the Front-End elements, where account needs to be taken of the schedules for other installation activities being organized by ATLAS Technical Coordination

6.3.2 Installation and commissioning

The installation dates in LS2 are, to a large extent, driven by the availability of access to the front end crates. It is assumed that Run 2 ends December 5, 2017 and access to the FECs is granted from March 2018 to October 2018. See Chapter 8 of the ATLAS Phase-I Letter of Intent [2] for further details.

The installation operation follows the deliverables and covers the three parts of the system, each one with a different degree of difficulty

- Back-End electronics in USA15: access is basically always available, installation is rather simple and covers the placing of crates, boards, patch panels, fibers . . .

- Long fiber cables: the laying and routing of the cables is done by ATLAS TC team. The routing has to be understood beforehand to determine the exact fiber lengths and probably will differ slightly from the routing of the legacy installation since some areas (e.g. Tile Barrel) are not accessible. The EC fibers will need to be placed in Sector 9 cable chain, but probably guiding slots will need to be created close to the cryogenic pipes prior to routing. A particular issue to be addressed will be the manoeuvring and installation of the cables in the areas where the Sector 9 is inaccessible.

- Front-End electronics: this is clearly the most constrained installation since 58 FECs (∼1800 boards) must be modified. A modus-operandi is described in the following:

  1. Uncable crate, dismount all boards from the crate, bring to the surface
  2. Dismount cooling plates, exchange layer sum boards, remount cooling plates, test, bring the boards to UX15
  3. Disconnect warm flat cables, dismount baseplane from inside crate chassis
  4. Mount new baseplane, reconnect flat cables, test connections by TDR
  5. Remount all FEBs and other boards, recable, test

  The precise process itself, as well as time estimates, still need to be done and scheduled. Given the amount of effort and the limited time frame available, it will be imperative to operate with several teams on several FECs simultaneously.

  The calorimeter faces (EMBA, EMBC, ECA, ECC) have different accessibility periods mainly at the opening and closing of ATLAS to cope with other upgrade installations (e.g. new Muon Small Wheels). The plan shown in Ref. [47] takes advantage of these boundary conditions to maximize the time available for installation, mainly at the FE.

The full commissioning of the system starts at completion of the installation. However local FEC commissioning and step-wise testing of components is envisaged and will reduce the total commissioning load. A large effort will be needed to integrate the system into the ATLAS TDAQ and interoperate properly with the subsequent parts of the Level-1 trigger system.

6.4 Resources and Participating Institutes

It is planned that participating institutions share the financial costs of the LAr upgrade project. Discussions with the LAr management and between institutes and the corresponding funding agencies are being finalized. The detailed list of deliverables, responsibilities and project cost sharing for the entire LAr upgrade project, as well as the financial commitments of the contributing funding agencies will be established in the “Memorandum of Understanding” (MoU) of the LAr Phase-I upgrade project.

Table 27 lists the LAr institutes that are either already active in upgrade R&D, or expressed interest to commit financially and assume responsibilities for the LAr Phase-I upgrade project: the deliverables shown in Tables 25-26 and detailed in the Product Breakdown Structure tables of Appendix C are grouped in fewer areas of activity for clarity of information. Other essential activities and tasks related to integration, installation on ATLAS and commissioning, which will be part of the LAr operations, are not included in the table.

Table 27. List of participating institutes and areas of interest for the construction of the project deliverables.

		Front-End Electronics							Back-End Electr.			
				LTDB						LDPB		
Institute	Country	Baseplanes	Layer Sum Boards	Analog Section	Digital Section	DC powering	Board Mechanics, Cooling and Integration	Optical Cable Plant & Pigtails	ATCA shelves & Computing Infrastructure	AMC	Carrier Board (& RTM)	Firmware
Sao Paulo[a]	Brazil				x							
TRIUMF	Canada	x		x	x							
Victoria		x		x	x							
Annecy	France/IN2P3								x	x	x	x
Grenoble					x							
Marseille									x	x	x	x
Orsay-LAL		x		x	x		x					
Saclay	France/CEA	x		x			x					
Dresden	Germany								x	x		x
Milano	Italy	x				x						
Tokyo[a]	Japan				x					x		x
Dubna-JINR	Russia	x		x								
Moscow-Lebedev								x				
Novosibirsk-BINP											x	x
CERN	Switzerland							x				
Arizona	United States	x								x	x	x
Brookhaven					x	x	x			x	x	x
Columbia					x							
Oregon[a]												x
Pennsylvania[b]				x								
Pittsburgh			x									
SMU					x							
Stony Brook										x	x	x

[a] New institution joining LAr for the upgrade project
[b] Institution contributing to LAr upgrade project, associated to LAr through Brookhaven

7 Summary

This report demonstrates the need of an upgrade of the LAr Level-1 trigger capabilities for the high luminosity data taking planned during Run 3 of the LHC. Without any upgrade the Level-1 trigger thresholds of single and multi-objects would need to be raised significantly to keep the Level-1 rate below 100 kHz at an expected instantaneous luminosity of $\mathcal{L} = 3{\times}10^{34}$ cm^{-2} s^{-1} and an average $\langle\mu\rangle = 80$ interactions per bunch crossing. Such a raise in thresholds would go hand in hand with a significant loss of signal acceptance in many physics channels.

The report shows that the use of higher $\eta-\phi$ granularity and high precision data, which preserves also the LAr calorimeter longitudinal segmentation information, enables ATLAS to maintain Level-1 trigger thresholds at the levels required by the ATLAS physics program during operations with the LHC instantaneous luminosity expected after the Phase-I upgrades.

The proposed technical implementation uses a scheme based on (i) on-detector digitization of Super Cells at 40 MHz sampling rate and with a quantization scale at least a factor 4 finer than in Run 2, (ii) fast optical links to USA15, and (iii) an FPGA-based energy reconstruction in real time. This information is then transmitted to the L1Calo feature extractor system, which performs searches over the whole calorimeter for objects with varying thresholds and subsequently supplies the results to the ATLAS central trigger processors. It has been also shown that the proposed Phase-I upgrade for the year 2018 is fully compatible with plans for a Phase-II upgrade in 2022 or later and will then serve as a Level-0 calorimeter trigger.

Finally, the report also describes the organization of the proposed upgrade project including the interests of participating institutes and a total cost estimate. A more detailed description of responsibilities will be the content of a Memorandum of Understanding that will be signed by the participating funding agencies in the coming months.

The LAr Phase-I upgrade project is an essential component for the success of the ATLAS physics program in the mid- and long-term future.

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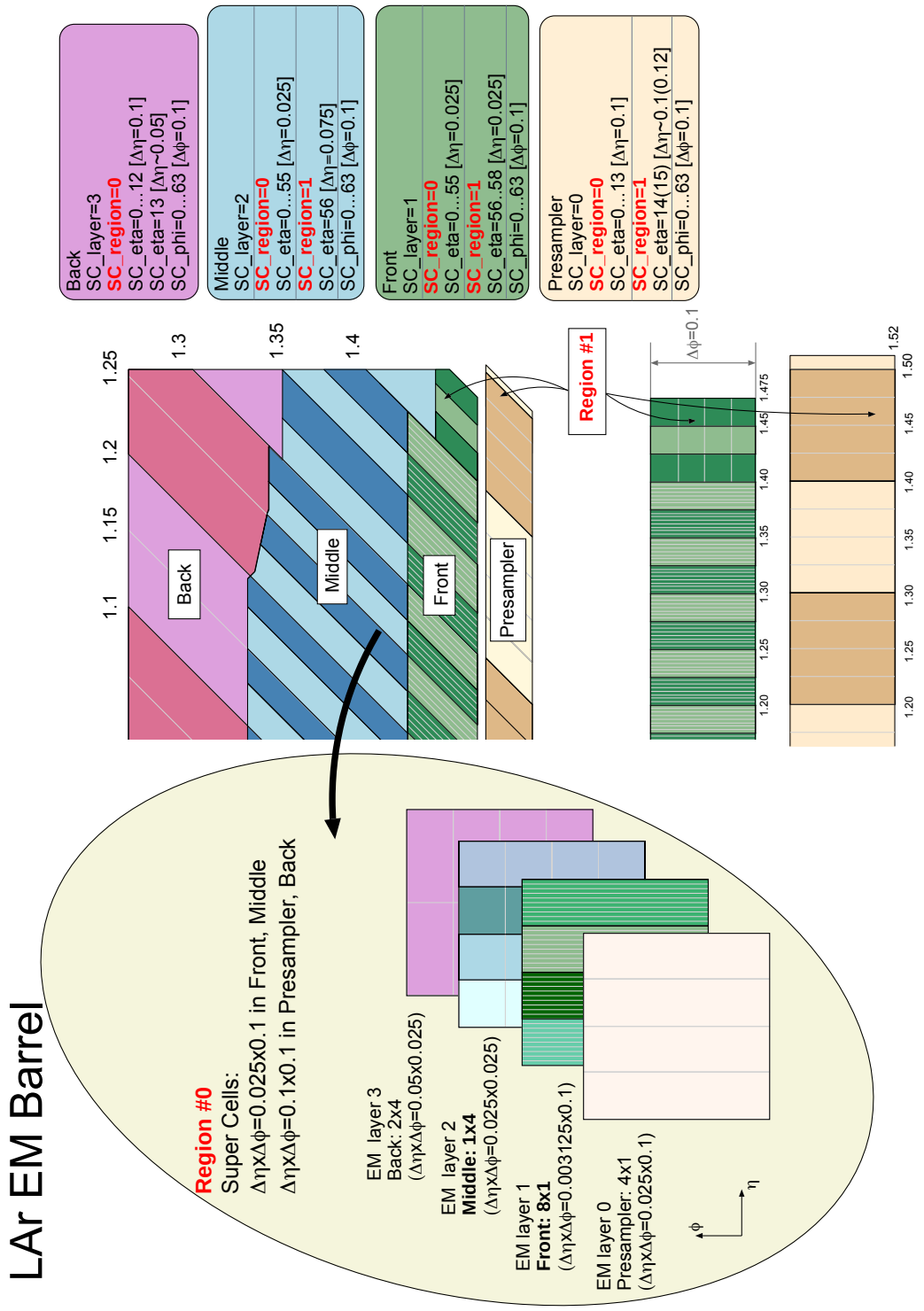
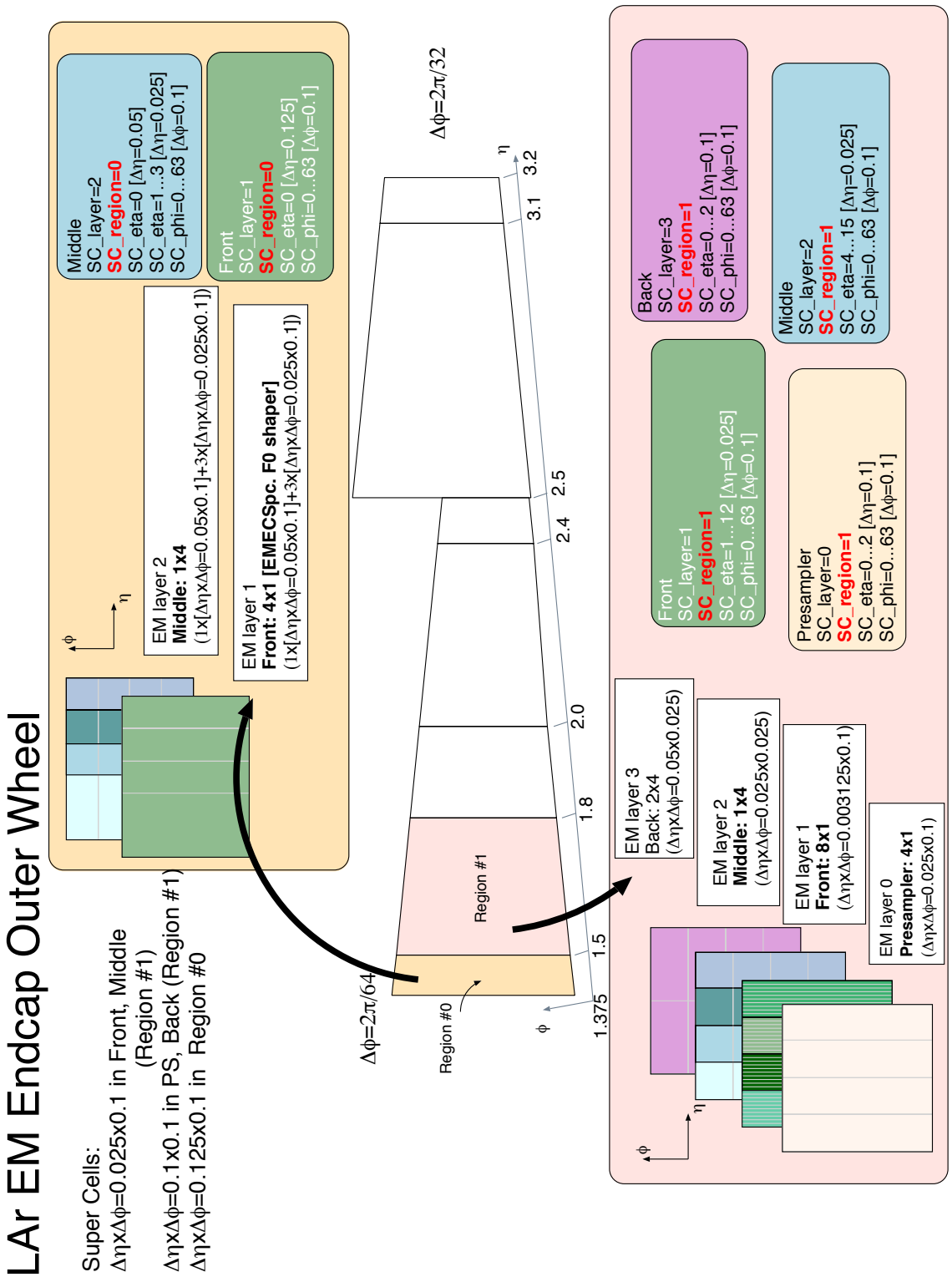
Appendix A Super Cell Layout

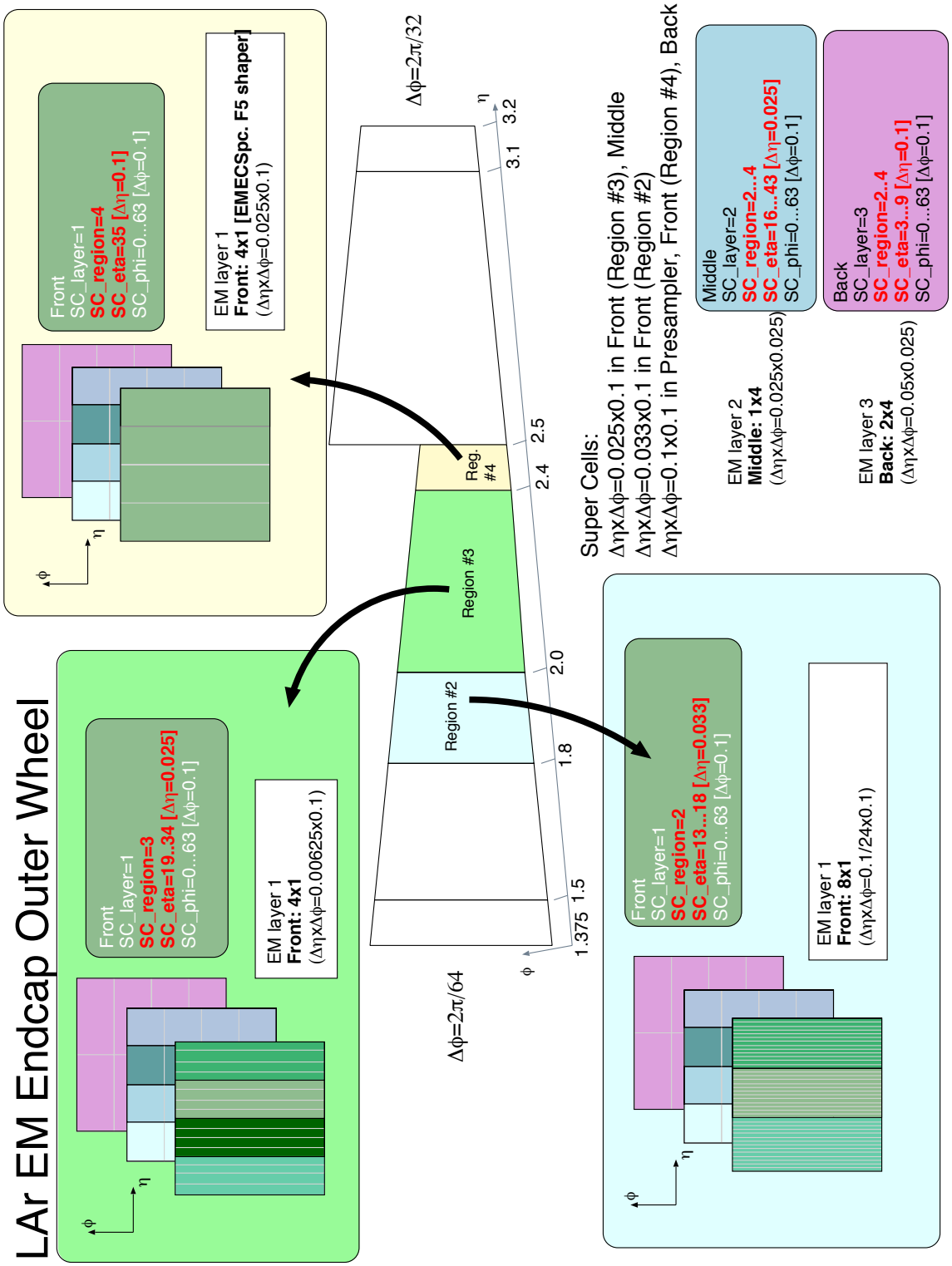
A few block diagrams of the granularity of the Super Cells in the different calorimeter of the LAr system are presented. More details can be found in [48].

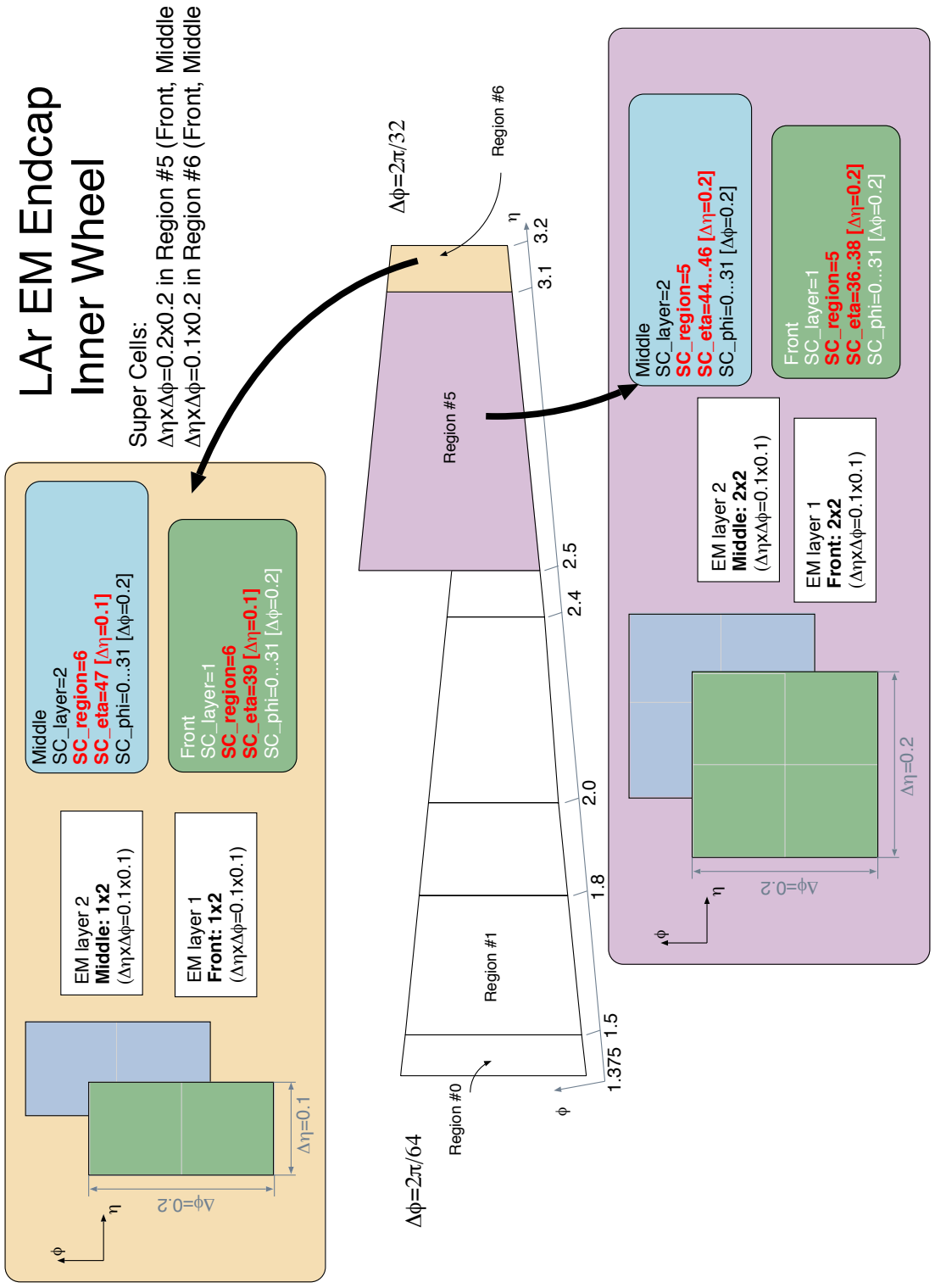
A.1 LAr EM Barrel Calorimeter



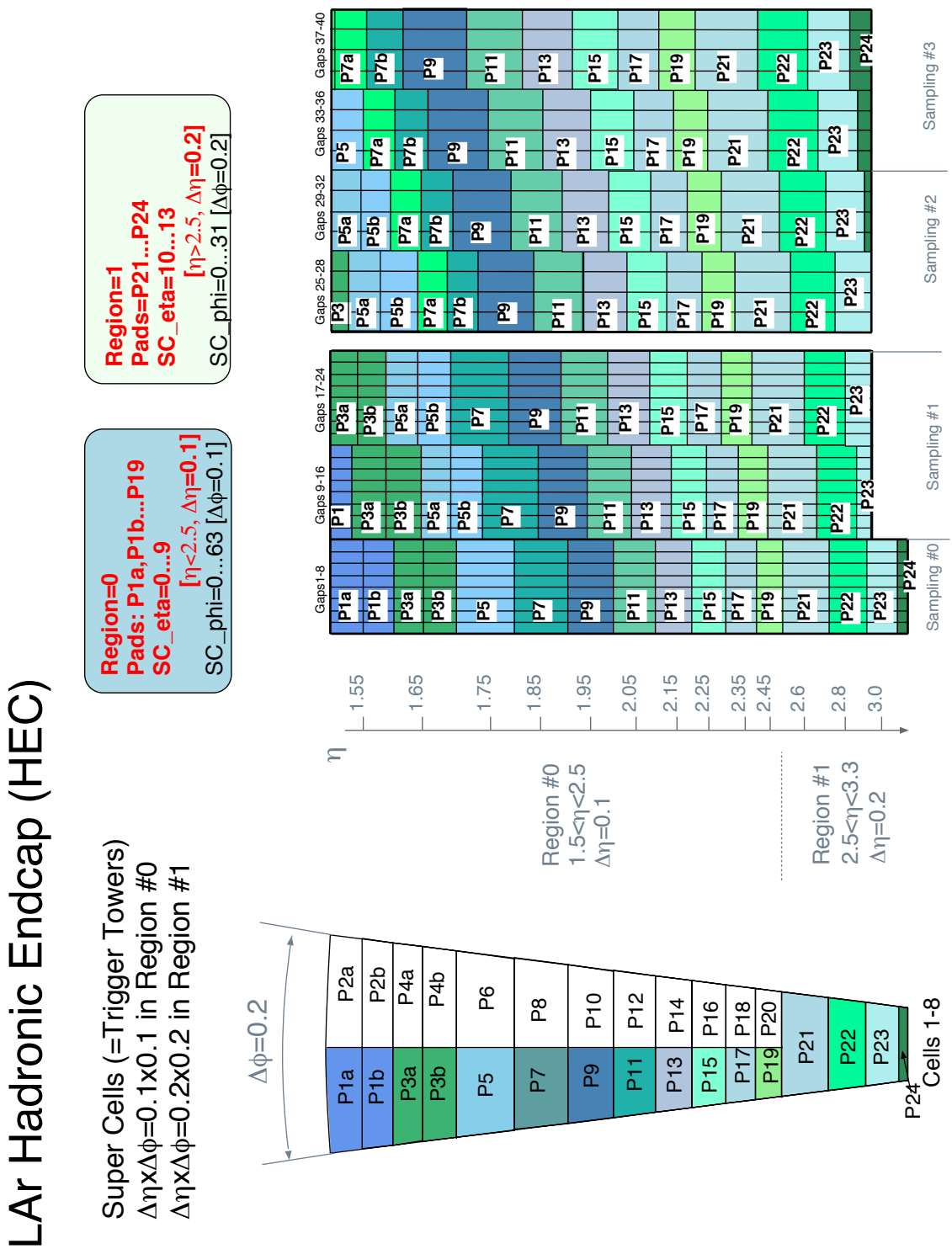
A.2 LAr EM Endcap calorimeter



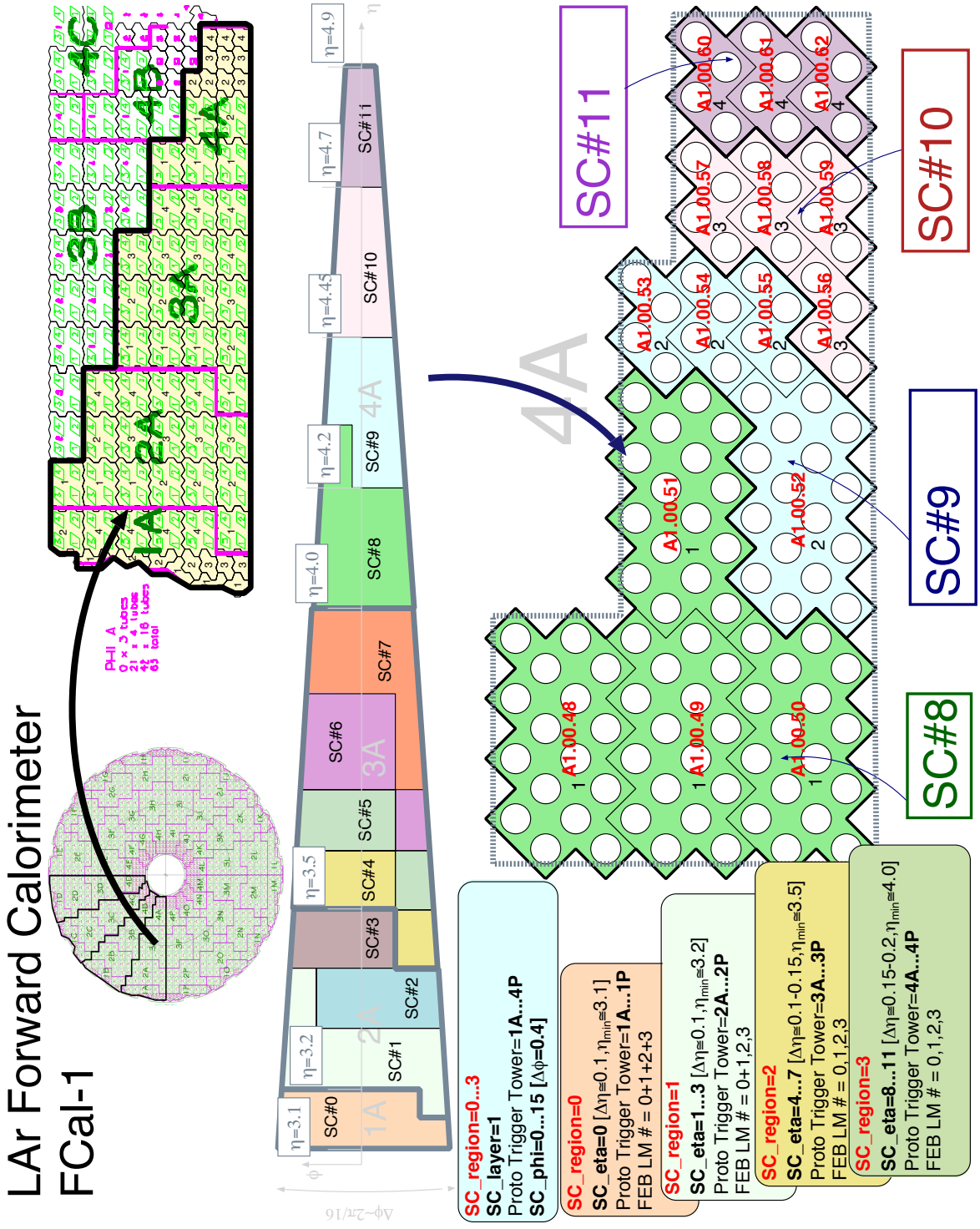

LAr EM Endcap Outer Wheel
Front
SC_layer=1
SC_region=3
SC_eta=19..34 [Δη=0.025]
SC_phi=0...63 [Δφ=0.1]
EM layer 1
Front: 4x1
(ΔηxΔφ=0.00625x0.1)
Front
SC_layer=1
SC_region=4
SC_eta=35 [Δη=0.1]
SC_phi=0...63 [Δφ=0.1]
EM layer 1
Front: 4x1 [EMECSpc. F5 shaper]
(ΔηxΔφ=0.025x0.1)
Δφ=2π/32
Δφ=2π/64
Reg. #4
Region #3
Region #2
η
φ
3.2
3.1
2.5
2.4
2.0
1.8
1.5
1.375
Super Cells:
ΔηxΔφ=0.025x0.1 in Front (Region #3), Middle
ΔηxΔφ=0.033x0.1 in Front (Region #2)
ΔηxΔφ=0.1x0.1 in Presampler, Front (Region #4), Back
Front
SC_layer=1
SC_region=2
SC_eta=13...18 [Δη=0.033]
SC_phi=0...63 [Δφ=0.1]
EM layer 1
Front: 8x1
(ΔηxΔφ=0.1/24x0.1)
Middle
SC_layer=2
SC_region=2..4
SC_eta=16...43 [Δη=0.025]
SC_phi=0...63 [Δφ=0.1]
EM layer 2
Middle: 1x4
(ΔηxΔφ=0.025x0.025)
Back
SC_layer=3
SC_region=2..4
SC_eta=3...9 [Δη=0.1]
SC_phi=0...63 [Δφ=0.1]
EM layer 3
Back: 2x4
(ΔηxΔφ=0.05x0.025)

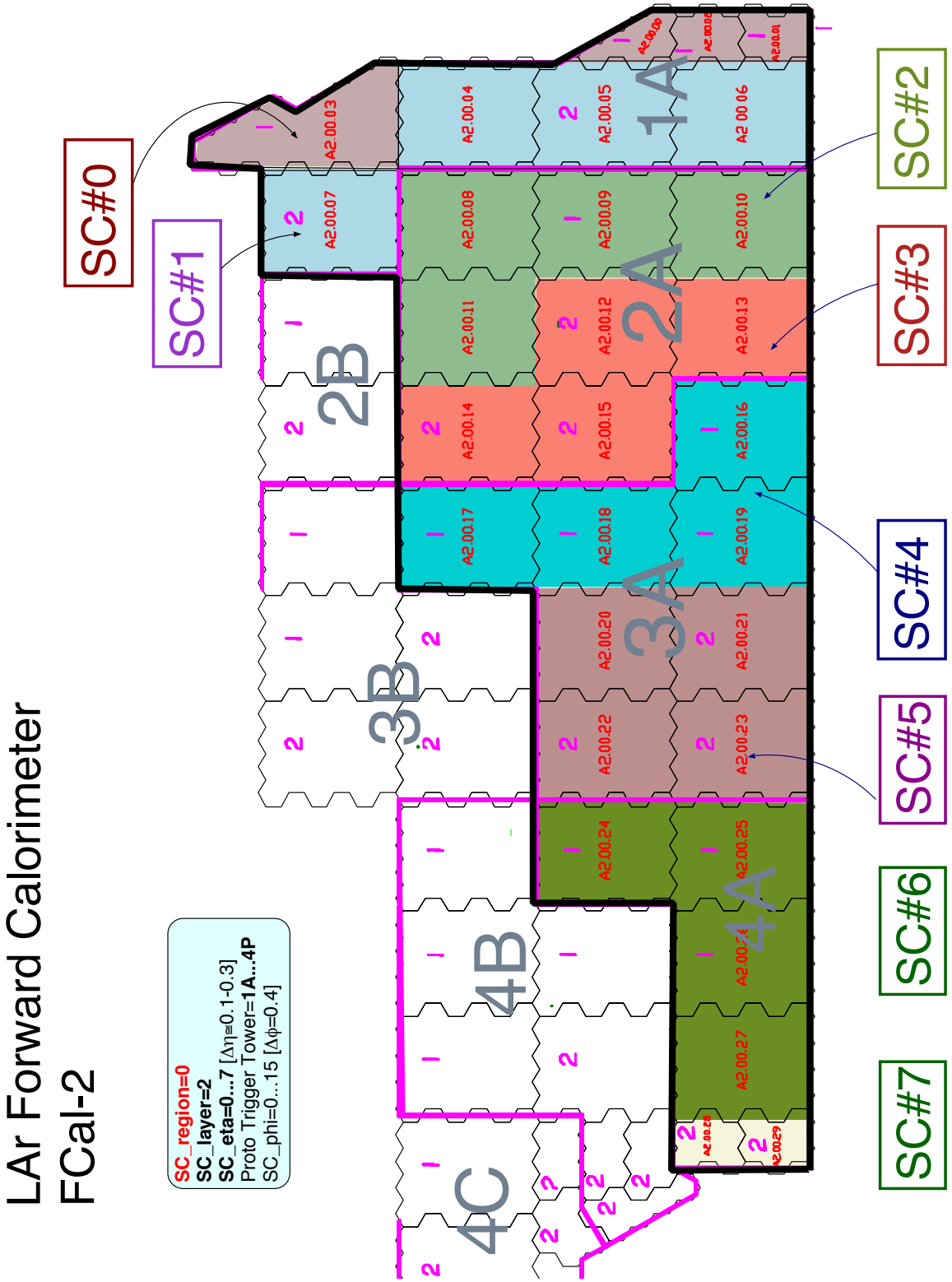

LAr EM Endcap
Inner Wheel
Super Cells:
ΔηxΔφ=0.2x0.2 in Region #5 (Front, Middle
ΔηxΔφ=0.1x0.2 in Region #6 (Front, Middle
Middle
SC_layer=2
SC_region=6
SC_eta=47 [Δη=0.1]
SC_phi=0...31 [Δφ=0.2]
Front
SC_layer=1
SC_region=6
SC_eta=39 [Δη=0.1]
SC_phi=0...31 [Δφ=0.2]
EM layer 2
Middle: 1x2
(ΔηxΔφ=0.1x0.1)
EM layer 1
Front: 1x2
(ΔηxΔφ=0.1x0.1)
Δη=0.1
Δφ=0.2
η
φ
Δφ=2π/32
Δφ=2π/64
Region #0
Region #1
Region #5
Region #6
1.375
1.5
1.8
2.0
2.4
2.5
3.1
3.2
Middle
SC_layer=2
SC_region=5
SC_eta=44...46 [Δη=0.2]
SC_phi=0...31 [Δφ=0.2]
Front
SC_layer=1
SC_region=5
SC_eta=36..38 [Δη=0.2]
SC_phi=0...31 [Δφ=0.2]
EM layer 2
Middle: 2x2
(ΔηxΔφ=0.1x0.1)
EM layer 1
Front: 2x2
(ΔηxΔφ=0.1x0.1)
Δη=0.2
Δφ=0.2

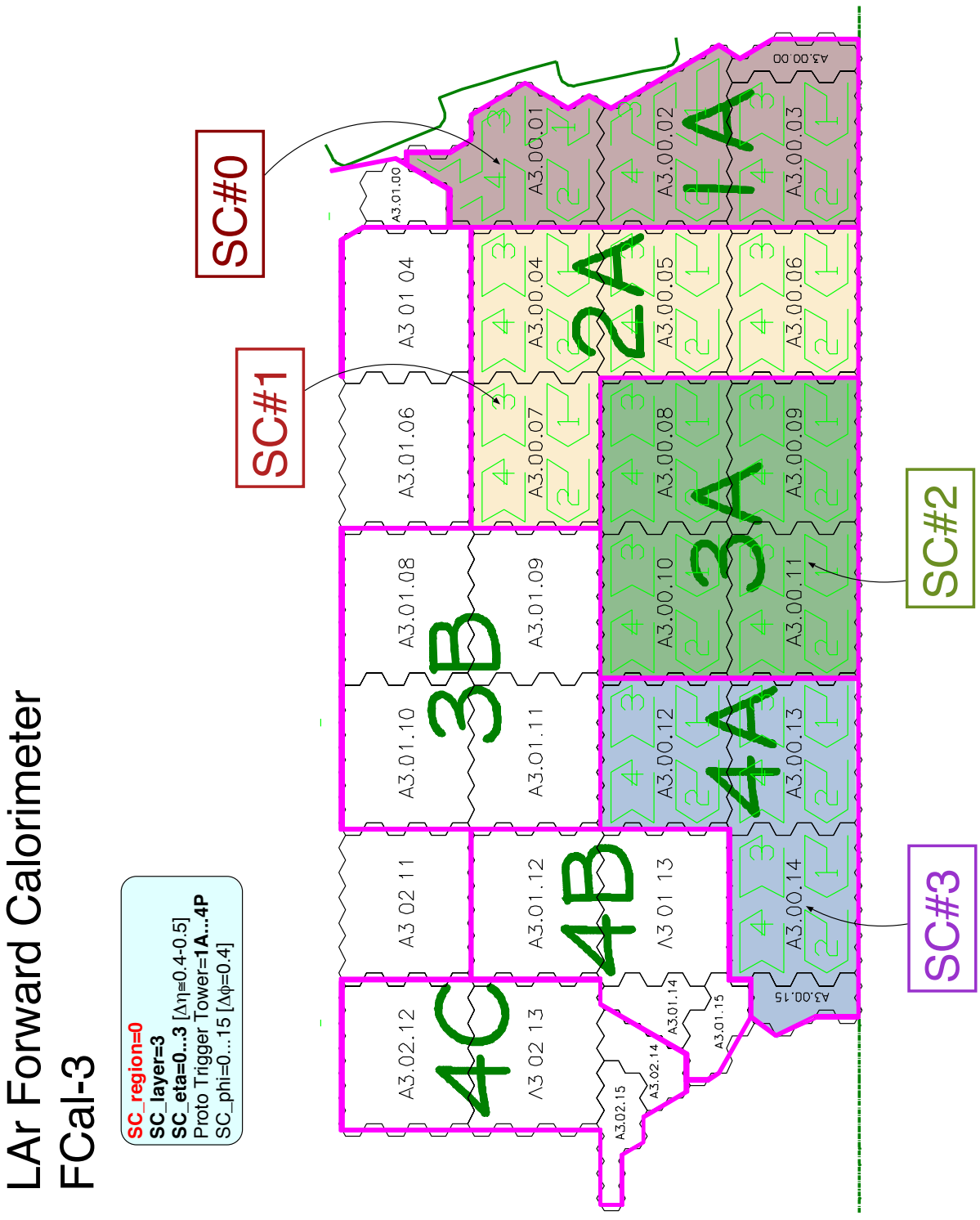
A.3 LAr Hadronic Endcap calorimeter



A.4 LAr EM Forward calorimeter




LAr Forward Calorimeter
FCal-2
SC_region=0
SC_layer=2
SC_eta=0...7 [Δη≅0.1-0.3]
Proto Trigger Tower=1A...4P
SC_phi=0...15 [Δφ=0.4]
SC#0
SC#1
SC#2
SC#3
SC#4
SC#5
SC#6
SC#7
1A
2A
2B
3A
3B
4A
4B
4C


LAr Forward Calorimeter
FCal-3
SC_region=0
SC_layer=3
SC_eta=0...3 [Δη≅0.4-0.5]
Proto Trigger Tower=1A...4P
SC_phi=0...15 [Δφ=0.4]
SC#0
SC#1
SC#2
SC#3
1A
2A
3A
4A
3B
4B
4C
A3.00.01
A3.00.02
A3.00.03
A3.00.04
A3.00.05
A3.00.06
A3.00.07
A3.00.08
A3.00.09
A3.00.10
A3.00.11
A3.00.12
A3.00.13
A3.00.14
A3.00.15
A3.01.00
A3.01.04
A3.01.06
A3.01.08
A3.01.09
A3.01.10
A3.01.11
A3.01.12
A3.01.14
A3.01.15
A3.02.12
A3.02.13
A3.02.14
A3.02.15

Appendix B Legacy front end electronics components

B.1 Front End Board

The Front End Board (FEB) is the major component of the LAr front end system. There are 1524 boards, configured in different ways to meet the various needs of the individual subdetectors. The FEB is described in detail in [49]. Here we describe only those components which are involved in the Phase-I upgrade, A description of the main readout is included, as use is made of these data in the high-level triggers, which are activated when saturated signals are encountered in the Level-1 trigger chain[8].

B.1.1 Preamplifiers

B.1.1.1 Warm preamplifiers The signals are sent from the cryostat feedthroughs to the baseplane of the Front End Crate (FEC) crate by transmission lines. Except for the case of the Hadronic End Cap (HEC), these are raw calorimeter cell signals and are subjected to several stages of analog processing in the FEB [50]. In the case of the electromagnetic (EM) and forward (FCal) calorimeters, room temperature preamplifier (hence the term “warm preamps") circuit hybrids constitute the first stage of this processing, terminating the long signal cables from the detector and amplifying the calorimeter signals. The warm preamp circuits are based on high speed silicon bipolar transistors and act as current preamplifiers. They convert to voltage the ionization current from the calorimeter, which has an amplitude ranging from few nA up to several mA. The current waveforms is triangular, with a rise time of a few ns, followed by a fall time of an approximately 400 ns, which is determined by the maximum drift time of electrons in the liquid argon gap.

Preamplifiers of three different gains – with either 25Ω or 50Ω input impedance – are used to match the different impedance, capacitance and dynamic range of the calorimeter signals, with circuits designed to provide low noise, high dynamic range and excellent linearity while consuming only about 50 mW per channel [51]. Although each individual readout channel can be precisely calibrated in software through the injection of a known amplitude signal, the Level 1 trigger signals are formed in hardware by the analog sum of several channels in the front end electronics and therefore depend on the gains in the trigger chain. For this reason, the gain variation between all channels must be less than 5%. The preamplifiers are constructed as thick-film hybrids housing 4 channels each and are socket mounted on the FEB. The noise of the whole readout chain is dominated by the preamplifier noise and, in the case of EM calorimeters, ranges from 10 MeVto 50 MeV, depending on the region [45].

B.1.1.2 Cold preamplifiers In the Hadronic Endcap Calorimeter (HEC) the first stage of amplification is done in preamplifiers located inside the cryostat within the LAr (hence the term “cold preamps"). HEC readout channels are formed by summation of up to 16 calorimeter cells. In order to minimize electronic and coherent noise, this summation is done in cold preamplifiers, mounted on preamplifier and summing boards (PSB). The PSBs are installed on the outer radius of the calorimeter wheel. The preamplifier ASIC, built using the GaAs TriQuint QED-A 1 μm process, consists of 8 identical preamplifiers and two drivers. The signals from a set of preamplifiers (2, 4, 8, or 16 for different regions of the calorimeter) are routed to and actively summed in a driver to form the output signal (in the case of the sum of 16, preamplifier outputs from two ASICs are routed to a driver of one of the ASICs). This signal is transmitted to feedthroughs by 50Ω cables of the same type as in other LAr detectors. Each HEC wedge (1/32 of wheel) is instrumented with 5 PSBs holding in total

[8] For single item and missing energy triggers, the Level-1 logic issues a Level-1 accept signal whenever a saturated trigger sum is encountered. The high level triggers, which do not saturate, then determine the fate of the event.

67 ASICs generating 96 output signals. Details of the HEC cold electronics can be found in Ref. [52].

In order to match the ASIC output with the LAr FEB, a special plug-in card, the preshaper, is used in the HEC FEBs instead of the preamplifier hybrids used for the rest of the LAr subsystems. The preshaper has various functions. Capacitance of the HEC cells varies from 20 pF to 470 pF and therefore the rise time of amplified signals varies from channel to channel between a few ns and 25 ns. In order to equalize the signal shapes so that summation of the signals over layers can be made in the linear mixer (see Sec. B.1.2.2, the preshapers include a pole-zero cancellation tuned to each type of HEC cells (14 different time constants). The preshaper also inverts signal polarity (the ASIC output is inverted) and provides additional gain to match the FEB dynamic range.

B.1.2 Shaper ASIC

The shaper chip is a 4-channel custom ASIC implemented in AMS 1.2 μm BiCMOS technology, providing amplification and shaping of the preamplifier output signals [45]. To prepare the signal for the trigger analog chain, the circuit can also sum and shape a combination of all 4 inputs by a linear mixer circuit. Any input may be disabled in this sum under software control, enabling problematic channels to be removed from the trigger. There are 32 shaper chips on one FEB.

B.1.2.1 Shaper After being processed by the preamplifier (or preshaper), the signals are AC-coupled into a 4-channel shaper circuit. To achieve the full dynamic range, each input signal is split and processed by 3 chains with overlapping linear gain scales (0.8×, 8.4× and 82×) [51]. Each one of the 3 branches applies a $CR-(RC)^2$ filter that was designed with one differentiation stage to remove the long tail from the detector response and two integrating sections to limit the signal bandwidth, hence reducing the noise. In order to correct for errors in capacitance which may occur in the fabrication process the shaper circuit implements a bank of trimming capacitors that can be adjusted during acceptance tests to keep the shaping time of the transfer function around 15 ns (close to the optimum for a luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$). The value of this time constant represents a compromise between minimizing the pile-up noise (which increases with slower shaping) and thermal noise (which increases with faster shaping).

To reduce low frequency noise, an additional reference output that is not connected to any input but has the same analog stage as the other 4 channels is provided as a reference to the Switched Capacitor Array or SCA (see Sec. B.1.3 below), allowing the implementation of “pseudo-differential” signaling between the shaper and the digitizer circuit.

B.1.2.2 Linear mixer The mixer stage of the shaper chip provides an additional output corresponding to a shaped sum of the 4 input channels [53], which is sent to the Level 1 (L1) analog trigger system. The chip can be programmed to enable or disable any of the inputs of the linear mixer in order to isolate faulty channels. It is also possible to select a gain of 1× or 3× by floating or grounding a control pin during the board assembly to accommodate the dynamic range of the signals from different sections of the calorimeter. Before being sent to the output, the summed signal is also subjected to a CR-RC filter. This filter is extended to a CR-$(RC)^2$ type immediately upstream of the ADC, where an additional pole is introduced to limit the noise produced by the summing amplifiers.

B.1.3 Digitizer for the main readout

The digitization system for the main readout in the FEB [49] is built around a custom-designed analog pipeline switched capacitor array (SCA) [54], implemented in 0.25 μm CMOS, and a commercial 12 bit ADC (AD9042). In this system, each calorimeter cell signal is sampled at a frequency of 40 MHz,

synchronized with the LHC clock, and the samples are stored in analog form during the L1 trigger latency [50]. The readout must be able to accommodate signals from the noise floor (10 to ~50 MeV) up to a few TeV signals (deposited in one cell from high energy electrons), which requires at least 16 bits of dynamic range [45]. This is obtained by sampling the outputs of the three gain scales from the shaper and using a gain selector circuit [55] to compare the peak value of the middle gain to pre-programmed thresholds in order to choose the highest unsaturated gain chain. During special calibration runs, it is possible to disable the automatic gain selection and transfer digitized samples from all three gain settings to the backend electronics.

Each SCA chip has 16 analog pipeline channels and each channel has three groups of 144 cells (one for each gain) based on 1 pF capacitors and associated switches to store a charge proportional to the voltage at a given sampling time. The system is designed so that one ADC operating at 5 MHz digitizes a group of eight channels. An external circuit (SCA Controller [54] controls the SCA channel and cell addressing during read and write operations. The SCA outputs operate in pseudo-differential mode, where the signal is provided with a "dummy" output as a reference. This improves the coherent noise and power supply noise rejection of the SCA. Pairs of operational amplifiers are used to interface the SCA pseudo-differential outputs to the single ended input of the ADC. This provides a high impedance load to the SCA output drivers and adjusts the SCA output voltage swing to the ADC input range. In order to measure both the positive and the negative regions of the signal, the operational amplifiers also introduce a pedestal, a positive offset of about 1000 ADC counts, into the signal.

During normal data taking, the digitization stage records 5 samples on the waveform, representing a compromise between the data volume to be processed by the backend electronics and the statistical error in the reconstructed amplitude and time. The timing of the ADC strobe is adjusted so that one sample is placed close to the peak of the signal. During calibration runs and special collision runs, when information on the complete waveform is required, up to 32 samples per signal can be digitized, at the cost of a much lower trigger rate. Many of the operational parameters of the board are controlled (and monitored) by the serial SPAC bus [56].

B.2 Calibration Board

The calibration board of the Liquid Argon calorimeter system is a high precision, highly stable circuit designed to inject a known amplitude signal as close as possible to the calorimeter electrodes [57]. The goal is to calibrate and monitor over the years of operation the electronic gain of each calorimeter cell with an error below 0.25% in order to keep the constant term of the resolution under 0.7%. The system is also used to calibrate and check the trigger chain.

To cover the full energy scale, a system with a dynamic range of 16 bits with an integral linearity better than 0.1% and stability within 0.2% was designed and installed in the front end crates, capable of distributing 128 calibration signals. Carefully trimmed cables bring the calibration pulses inside the cryostat, where precision resistors are mounted on the motherboards for termination and injection of the signal directly in the calorimeter cell [58]. The signal injected has an exponential shape, with a fast rise time (< 2 ns) followed by a long decay time (444 ns). The circuit used to generate this signal is based on a precise (and adjustable) DC current source and a parallel LC circuit. A switching circuit made of transistors is used to control the charge and discharge of the inductor from an external clock pulse. A 16 bit digital-to-analog converter (DAC) controls the pulse amplitude, and its signal is distributed over the calibration board by low-offset operational amplifiers. Since the calibration circuit needs to operate over the years without degradation of its characteristics when subjected to the LHC background radiation, custom-designed radiation-hard DACs and operational amplifiers were developed for this application.

Several operational parameters of the board are digitally controlled by the serial SPAC bus. In

addition to pulse amplitude and channel enable/disable, it is possible to control the phase of the injection pulse relative to the LHC clock in 1 ns steps, allowing detailed study of the signal shape.

B.3 Tower Builder Board

The Tower Builder Board (TBB) is a module which resides in the Front End Crate and receives analog trigger sums from the various layers through the baseplaneȦfter adjusting the shape and timing of these signals, it performs a sum over the layers for each of its 32 channels. It delivers a signal proportional to the transverse energy (E_{T}) deposited in a trigger tower, with saturation at or above 256 GeV. In the barrel, a trigger tower corresponds to $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and contains 4, 32, 16 and 8 elementary cells from the presampler, front, middle and back layers, respectively . The linear mixer (c.f. Sec. B.1.2.2) and the Layer Sum Board (c.f. Sec. 4.1.1) of the Front-End Boards sum signals from individual layers, and the TBB sums the four layers to a single value. There are a total of 120 TBBs installed: 64 in the 32 EMB crates, 32 in the 16 EMEC Standard Crates, and 24 in the 8 EMEC Special Crates.

If the E_{T} in any tower is saturated, or ≥ 256 GeV, the outgoing signal of the TBB is 2.5 V ± 5%, with a peaking time of 35 ns. The full-bandwidth noise of the whole electronic chain, at $\eta = 0$, must not exceed 400 MeV, or 4 mV, at the TBB output, and a saturated signal must not appear unless the energy deposit exceeds 256 GeV. For this reason, the TBB has its own clamping circuit using the HFA1335 op-amp which limits the positive peak to 3 V and the undershoot to 0.5 V.

The shape, delay, and gain of each channel and the peaking time of the signals issued from the Layer Sum Board strongly depends of the layer and value of η. For example, the capacitance of the detector at η = 0 is 160 pF on 50 Ω load in the presampler and 1355 pF on 25Ω load in the middle, leading respectively to 8 ns and 34 ns poles.

Each TBB has 128 inputs (32 per layer). The input impedance of each input is 50 Ω and the output impedance of each of the 32 output buffers of the TBB is also 50 Ω. The TBB first performs a reshaping on each of the four layers, then an adjustment of the delays between layers and sums the four signals at the end, with the aim to provide at the TBB output the standard L1 energy scale of 10 mV/GeV. The delay of each input channel is tuned by a delay line with 7 outputs, each being delayed by 2.5 ns compared to the previous one, and the output is selected by an ASIC (called BIMUX because it handles two delay lines) driven by the SPAC slow-control. After the final summation with output clamping described above, a final stage converts the single-ended signal to a differential one which is sent to the receiver system in USA15 over multiway individually shielded twisted pair cables.

B.4 Tower Driver Board

In general, trigger sums are formed by summing the longitudinal depth segments at the same azimuthal and pseudorapidity coordinates. In the HEC, this summation is performed by shaper chips in the FEB. In contrast to the EM calorimeters, where the TBB forms the longitudinal sums, no further summation of signals is needed for the HEC L1 sums. The same is true for the FCal. Therefore, instead of using a TBB as described in the previous section, the HEC and FCal crates include a Tower Driver Board (TDB). Two TDB boards are used in each HEC crate, so 16 boards serve both HEC wheels. In addition four TDBs of the same type (two per crate) are used in the FCal. The TDBs receive the (single-ended) trigger sums from the LSBs via the baseplane convert them into differential signals with approximately unity gain, and drive these differential signals over the 70 m trigger cables to the receiver system in USA15. The six output cable connectors are mounted on the front panel of the TDB.

The TDB is a purely analog board which requires no external control signals. The measured gain is 0.98 with channel-to-channel variation of 0.3%, well below the specified uniformity of 1%. Similarly, the mean measured rise time variation of 0.68 ns is well below the 2 ns specification. The TDB power consumption is very low (< 15 W), so the water cooling used for other boards in the FE crate is not needed. Instead, aluminum plates are mounted on both sides of each TDB. In addition to the air heat exchange, they provide electrical shielding as well as mechanical protection of the active components.

B.5 Receiver

The receiver system [59] is also part of the legacy FE electronics; it forms the boundary between the liquid argon electronics and the Level-1 calorimeter trigger electronics. Physically, the system is located in the USA15 cavern, at the receiving end of the trigger cables which are driven by either the Tower Builder Board (TBB) or the Tower Driver Board (TDB) located in the FE crates.

The receiver system has four basic functions: (1) to prepare the signal for transmission to the Level 1 Preprocessor, where it is digitized; (2) to carry out two-fold sums of signals which, for various reasons, cannot be summed in the front-end crates; (3) to change the order of the signals at the input, which is dictated by the cabling in the calorimeter and front-end crates, to the one at the output which is needed for the Level 1 trigger processor; and (4) to provide outputs for monitoring the calorimeter waveforms.

The signal processing involves one stage of integration and adjustment of the gain of the signal to bring it to the specified level (2.5 V for $E_{\mathrm{T}} = 256$ GeV). The summing function is limited to two instances. One is in the barrel-endcap transition region, where one half of a trigger sum is contained in the barrel and the other half is contained in the endcap. The other is in the FCal, where the number of η bins (four) defined by the sums in the front end crate exceeds the number of η bins (two) accepted by the Level 1 trigger system.

The required reordering of signals can be carried out entirely within each receiver module, and it is done through the use of a “remapping board”, which is, in most cases, a passive PC board which simply reroutes the signals between the input pins and output pins on its connectors. In cases where summing in the receiver is required, that circuitry is located on this board.

Appendix C PBS

PBS	Name	Dictionary
1	**ATLAS LAr Upgrade Project**	
1.1	**Front End Electronics**	
1.1.1	**Baseplane**	PC board that interconnects the warm cables from the feedthroughs to the FEB inputs, and route the signals from the FEBs to the Tower Builder and to the LTDB board
1.1.1.1	**Baseplane Barrel**	
1.1.1.2	**Baseplane EC-STD**	
1.1.1.3	**Baseplane EC-SP**	
1.1.1.4	**Baseplane HEC**	
1.1.1.5	**Baseplane FCAL**	
1.1.2	**LSBS**	Plug-in board on the Front-End Boards (FEB) to receive the signals from the shaper linear mixers and drive them to the LTDB/TBB. For the PS and 3rd layers of the EM calorimeter, also prepare layer sums (0.1x0.1 in eta/phi) [2944-616 to be resused]
1.1.2.1	**Components**	
1.1.2.2	**PCB**	
1.1.2.3	**Assembly**	
1.1.3	**LTDB**	LAr Trigger Digitizer Board, prepares and digitizes the analog signals of the Super-Cells and drives the digital samples to the Digital Processing System
1.1.3.1	**Analog Processing**	The analog front-end of the LTDB is designed as part of a mother board or a pluggable mezzanine. Receiving stages, partial layer sums and ADC drivers are implemented. Section will be customized for the different LTDB configurations (if needed) in the different calorimeter's regions, assume 40 ch
1.1.3.1.1	**Adder components**	
1.1.3.1.2	**Pole components**	
1.1.3.1.3	**ADC driver**	
1.1.3.1.4	**Connectors/mechanics**	
1.1.3.1.5	**PCB**	
1.1.3.1.6	**Assembly**	
1.1.3.1.7	**Standalone tests**	If HW is needed to perform standalone tests
1.1.3.2	**Digital Processing**	All the major components and sub-assemblies on possibly on a mezzanine board, assume 32 ch
1.1.3.2.1	**ADC**	Digitizer ASIC/COTS devices running @ 40MSPS and 12-bits, assume 4 ch per ADC. Assume COTS for the time being.
1.1.3.2.2	**ASIC Serializer**	The ASIC serializers receive the ADC data, reorganize and serialize them on a high speed serial link
1.1.3.2.3	**ASIC Laser Driver**	ASIC device that drives the optoelectronics components

PBS	Name	Dictionary
1.1.3.2.4	MTx	Transmitter optical sub-assembly with laser driver and VCSEL integrated (double device, assume 1 fiber out/8 ch)
1.1.3.2.5	TTC Link	Components needed to interface to back end TTC system, to provide timing, control and monitoring functions, including CERN developed GBTx, GBT-SCA and VTRx
1.1.3.2.6	Other parts	Other passive or active components
1.1.3.2.7	PCB	Print circuit board fabrication
1.1.3.2.8	Assembly	PCB assembly
1.1.3.2.9	Standalone tests	Test setup to perform standalone tests
1.1.3.3	DC powering	Powering devices and local regulation. Possibly implemented on mezzanine for forward compatibility when in Phase-II the power distribution in the front-end crates may change
1.1.3.3.1	DC/DC converters	Based on CERN designed POL converter, repackaged for LTDB usage
1.1.3.3.2	Linear regulators	CERN developed positive and negative voltage regulators
1.1.3.3.3	connectors in/out	Connectors for voltage inputs and regulated voltage outputs
1.1.3.3.4	Other parts	Other passive or active components (induction etc.)
1.1.3.3.5	PCB	Print circuit board fabrication
1.1.3.3.6	Assembly	PCB assembly
1.1.3.3.7	Standalone tests	Test setup to perform standalone tests
1.1.3.4	Optical pigtails	Optical pigtails are custom-made optical fibers that connect the different TOSAs to the front-panel optical connectors
1.1.3.5	Mechanics	Mechanical components for LTDB assembly
1.1.3.5.1	Cooling plates	Plates that interface thermally the electronics components to the cooling circuits, running at negative pressure. Likely meanufactured as roll-bonded Aluminum plates
1.1.3.5.2	Cooling blocks	Ultem GM plastic blocks that interface the cooling plates to the cooling manifolds installed on the TileCal through flexible hoses and quick disconnects
1.1.3.5.3	Front-panels and supports	Mechanical supports for the boards and connections through the front panel
1.1.3.5.4	Baseboard	Baseboard to connect to the baseplane and support the mezzanine or mezzanines. Includes connectors to baseplane and standoffs for mezzanines
1.1.3.6	LTDB Integration	joining the mezzanines and testing of the overall assembled LTDB board
1.1.3.6.1	Integration (small parts)	Integration of LTDB

PBS	Name	Dictionary
1.2	**Optical cables**	Optical fiber cables connecting the LTDB boards to theL DPS systems in USA-15
1.3	**Backend electronics**	
1.3.1	**ATCA shelves**	ATCA crates to be installed in the USA-15 racks
1.3.2	**LDPB**	The LAr Digital Processing System Boards receive the ADC signals and process them to extract the information for the Trigger Feature Extractors.
1.3.2.1	**AMC**	Advance Mezzanine Cards are the subassemblies containing the FPGA which handle the data processing and the conversion raw data samplse to calibrated energy for each SuperCells
1.3.2.1.1	**MAIN FPGA**	
1.3.2.1.2	**UPOD RX/TX**	
1.3.2.1.3	**UPOD Cooling block**	Optical recievers in MicroPod format including the mechanical support and cooling interface, Assume 1/ 4upod
1.3.2.1.4	**UPOD Sockets**	
1.3.2.1.5	**Memory**	
1.3.2.1.6	**MMC**	Management and Monitoring Card on each AMC for power control and monitoring
1.3.2.1.7	**Other parts (incl memory)**	
1.3.2.1.8	**PCB**	
1.3.2.1.9	**Assembly**	
1.3.2.1.10	**Standalone tests**	If HW is needed to perform standalone tests
1.3.2.1.11	**FW**	FW development
1.3.2.2	**IPMC**	Intelligent Platform Management Controller for configuration and control of the LTDPSB. Interface to the ATCA management
1.3.2.3	**Optical pigtails**	Custom-made optical fiber pigtails connecting the AMC optical connectors to the optical transceivers (48 ch)
1.3.2.4	**Carrier Board**	The main ATCA board of the LDPB and GBTD
1.3.2.4.1	**Main Central FPGA**	FPGA on carrier board to interface to AMC and controller blade through high speed serial links, e.g. 10GbE
1.3.2.4.2	**Slow Switch FPGA**	FPGA on carrier board to provide slow switch function
1.3.2.4.3	**Clocking components**	Receive LHC clock and distribute to AMC modules
1.3.2.4.4	**Main PCB**	Other passive or active components, including connector, power, monitoring etc.
1.3.2.4.5	**Other parts**	Print circuit board fabrication
1.3.2.4.6	**Assembly**	PCB assembly
1.3.2.4.7	**Standalone tests**	Test setup to perform standalone tests
1.3.2.4.8	**FW**	FW development
1.3.2.5	**LDPB board/blade integra**	Assembly and testing of the overall assembled LDPB board
1.3.2.5.1	**Integration (small parts)**	Integration of LDPB boards
1.3.3	**RTM**	Output interface to FELIX of TDAQ and input source of TTC
1.3.3.1	**UPOD RX/TX**	High speed parallel optical transceivers to interface to FELIX of TDAQ
1.3.3.2	**Main PCB**	Other passive or active components, including connector, power, clock, monitoring etc.
1.3.3.3	**Other parts**	Print circuit board fabrication
1.3.3.4	**Assembly**	PCB assembly
1.3.3.5	**Standalone tests**	Test setup to perform standalone tests
1.3.4	**TTC Optical Couplers**	Interface to the TTC system to transmit LHC clocks to the front-end LTDBs and other TTC information to the LDPS
1.3.4.1	Fibers	
1.3.5	**In-shelf switches**	In shelf 10GbE switches connected to the ATCA shelf fabric for I/O monitoring of the LDPB blades
1.3.5.1	Fibers	10GE fibers
1.3.6	**Receiver PC**	PC shelf to do shelf management and auxiliary monitoring/controlling functions
1.3.7	**Controlling PC**	PC (rack mounted or standalone) to control the USA-15 racks shelves and blades

Appendix D In-situ Demonstrator

In order to test and commission the proposed upgrade for Phase-I before ATLAS operation multiple tests will be needed all along the way. We propose to perform

- Extensive element testing
- Full lab system tests at the LAr Electronic Maintenance Facility (EMF)
- Installation of in-situ demonstrator during LS1
- Production tests of components

This section details the steps for an in-situ demonstrator which will consist of a Front End part (LTDB0) and a Back End part.

D.1 Motivation, risks, staged approach

As described in D.3.2 a full system test will be made at the EMF where the full electronics functionalities will be checked and validated.

After successful verification, the plan is to equip one FEC with the readout for the increased granularity, and install the boards required during LS1. For one FEC (probably in the EM Barrel, equivalent to $\Delta\eta \times \Delta\phi = 1.4 \times 0.4$) one would need to equip FEBs with new LSBs, install 2 new base planes, two LTDB0s, a long fiber cable towards USA15 where two pre-prototype LDPBs will be setup. While the LTDB0 will not have the components for the full series Phase-I boards, it will have a very similar functionality.

Before any decision is taken to install this demonstrator on detector, we propose to hold an ATLAS review.

We explain below the motivation for this in-situ demonstrator, the way to handle the associated risks and a staged approach, realizing that one FEC covers about 2 % of the trigger acceptance.

D.1.1 Motivation

All electrical functionalities will be tested on the surface (see section D.3.2). However there are several reasons why only an in-situ demonstrator will provide additional critical information:

- Collect data from the Super Cells and validate energy reconstruction and bunch crossing identification algorithms in FPGAs with the high pileup and saturated pulses occurring in LHC conditions
- Measure trigger efficiency and jet background rejection using various LDPB filters and selection algorithms deployed in the Feature Extractors.
- Learn about installation and operation of the apparatus in the ATLAS environment, well in advance of LS2, with potential feedback to the final design of the system or its components.
- With the new baseplane and LSBs in place, the LTDB0s can later be replaced by other prototype boards during later winter shutdowns.

D.1.2 Risks

As mentioned above there shall be no risk taken to disturb ATLAS data taking by the installation or operation of the demonstrator on the detector. The demonstrator installation is accompanied by sufficient test operations (see section D.3.4) to ensure no damage is done to the ATLAS HW. We think that after a successful validation of all design functionalities on the surface, there are only minimal risks involved, those connected with the operation of the boards on the detector:

- There might be a small risk of deteriorating the analog signals due to electronics noise or crosstalk induced by digital components on the boards on the detector. Of course the surface tests will allow us to measure and assess this risk before installation. In addition, we shall test in-situ before loosing access.
- During the design of the LTDB utmost care will be taken to preclude any failure from the digital components on the board from affecting the analog signals sent to the TBB. This property will also be validated during the EMF tests; nevertheless there might be residual risks arising from rare failure modes. These risks will be assessed before installation in the FEC.

D.1.3 Staged approach

Clearly the schedule for a demonstrator on the detector (see below, section D.2) in summer 2014 is very tight. However, in case of any doubt about the reliability of the system to be installed, we propose to step back and install only parts of the new system, keeping the option to upgrade in the following winter shutdowns.

We can foresee a reduced scenario where only the pair of new baseplanes is installed in the FEC. If the LSBs on the FEBs are not exchanged a pair of passive “jumper” boards in the LTDB slots could take care of the routing of the analog signals to the TBBs. Following such a preparation during LS1, FEBs could be modified with new LSBs and the two LTDB0s could be introduced in a subsequent yearly shutdown without further work on the FEC.

D.2 Demonstrator construction, parts used and timetable

The construction of the demonstrator and its validation initially with the system tests at the EMF and eventually in ATLAS will follow a set of milestones, for each of the demonstrator components, which will provide also technical solutions for several deliverables to the full project.

The front-end parts are obviously more challenging, both because of the radiation tolerance requirements and for the potential implications on the performance of the legacy Level-1 calorimeter trigger system. The focus of this section is limited to the front-end trigger electronics.

In the following we summarize for each deliverable, the current status and the plans on the short term scale, challenges and risks for the demonstrator and beyond.

D.2.1 Baseplane

There are 5 baseplane configurations. The process of validating the design has to be done for each flavor and through specific test stands at different levels. For the demonstrator a critical task is to validate the analog signal integrity through the readout chain with the EM barrel configuration. More specifically:

- Current status
  - The design of the EM barrel configuration is well advanced.

  - A baseline PC layout exists.
  - All the components and specifically the LTDB input connector have been specified
  - Optimization of the pin layout at the input of the LTDB has been finalised in first iteration (e.g. GND vs. analog input signal pins).
  - First prototype items have been ordered and are under production.

- Challenges and Risks
  - Integrity of the layer sum signals from the FEBs to the TBB has to be preserved: Moderate
  - Minimal Xtalk for the traces in the baseplane PC layout (approximately x2 number of signal traces in the new design): Moderate
  - Optimization of the baseplane connector pin assignment for proper routing in the LTDB PC layout: Low
  - Technical and schedule risk: Moderate - if specs parameters of the first prototype are outside the acceptance range, a second iteration may be required introducing a delay of 2-3 months.

D.2.2 LSB

In the EM barrel crates, the LSBs are in four flavors. The S1x16H, used in the PS section, and the S1x16L, used in the middle section, will be unchanged from their original designs. For the back section, two options are possible, either to reuse the original S2x8 LSB, adding an additional drive resistor in order to send the identical signal to both the LTDB and the TBB, or to design a new S2x8D board with a dual buffer to accomplish the same task. The LSB for the front section can be either the original S2x8 or a newly designed S2x8D. If boards of the original design are used, there are enough existing PCBs and parts on hand to construct all of the boards required for the demonstrator crate.

Independently on the design options, there are no real challenges or technical, schedule and cost risks associated with the LSB design for the demonstrator.

D.2.3 LTDB demonstrator

As a result of the open architectural options described in Secs. 4.1.3.5.1 and 4.1.3.5.2, two possible LTDB demonstrator boards are being studied and developed for both system tests at EMF and installation in ATLAS.

D.2.3.1 LTDB demonstrator with digital motherboard The design of the digital motherboard has started with 1/4 slice prototype. A 1/4 slice prototype has been designed and built, and it is currently under testing. This prototype has 80 channels with a motherboard housing the digitizers and all the other digital components, and two 40-channel analog mezzanine boards. A picture of this prototype is shown in Fig. 39 of Sec. 4.1.3.5.1. The lab test of the quarter slice prototype is proceeding smoothly; the preliminary test results show the rms noise is less than one half of an ADC count, and the cross talk is less than 0.1%.

The next steps will be to design and deploy a full board with 320 channels and local power regulation to be installed in system tests in EMF (December 2013). The prototype will allow system-wide measurements like electromagnetic compatibility, pick-up noise and cross-talk in a full front-end crate. The design has started, the schematics design is now (August 2013) being completed.

D.2.3.1.1 Analog input mezzanine In the current thinking the analog mezzanine processes up to 40 input channels, provides the 0.1x0.1 layer sums to feed the TBB inputs, and drives the individual SCs to the ADCs. While the final implementation may be through ASICs, the project's near term goal is to validate the design through COTS op-amps and prove its performance by the TDR on bench tests or preliminary system tests.

To validate the design and quantitatively assess the noise of the system with the final LTDB, a test with a purely analog carrier board may be needed to evaluate performance of the analog mezzanine alone.

- Current status
  - The design of the EM barrel configuration is relatively advanced.
  - Generic schematic and layout is in progress
  - SPICE simulations of the full analog readout chain is well advanced (signal characterization, noise analysis and signal saturation studies)
- Challenges and Risks
  - Low to Moderate risk associated.

D.2.3.1.2 Digitizers As explained above in Sec. 4.1.3.3.2 for the LTDB digitizers LAr is considering three options: 2 ASIC developments and a COTS solution. The demonstrator will use the COTS ADC (TI ADS5272) already discussed in the same section.

D.2.3.1.3 Interface IC and serializers The interface and the serializers ASICs proposed for the Phase-I upgrades will not be available on the time-scale of the demonstrator. This is true for both the ASIC design on SoS and for the GBTx developments.

For the demonstrator the solution based on a commercial FPGA (Xilinx Kintex-7 family) will be used, even though this device is not yet fully qualified for use at HL-LHC radiation levels. The K7 environment should allow evaluation of the full data flow from the ADC up to the LDPS, as in the final LTDB+LDPB system.

D.2.3.1.4 Optical transceivers The transceiver includes both the laser driver and the optical module itself (TOSA) integrated into a single unit. For the digital motherboard demonstrator a commercial (Avago) optical transceiver will be used packaged as PPod component, and the control link is implemented by an SFP optical transceiver which communicates with a CERN-developed GLIB board.

D.2.3.2 LTDB demonstrator with analog motherboard The design of a demonstrator based on the analog motherboard implementation is also under way. All the analog processing is done on the mother board. The 0.1×0.1 layer sums are sent directly to the TBB through the baseplane, and the SC signals are routed to the ADCs. The ADCs are located on digital mezzanines, each mezzanine featuring 32 channels, i.e. 10 mezzanines per LTDB.

The design is presently under validation. Electronics aspects (noise, cross-talk, linearity...), mechanical aspects (connectics, cooling, ...) and integration aspects in the FEC (insertion of the board) are adressed through realization of prototypes. The goal is to have a full-scale analog motherboard and mating digital mezzanines by the end of 2013, to be tested at the EMF.

- Current status

  - SPICE simulation of the analog chain completed. Cross-check under-way with the measurements done on a 4-channel prototype board.
  - Generic layouts have been defined for the various kinds of supercells.
  - A 64 channel board has been designed (1/5 of a full LTDB) and is under tests.
  - A mechanical prototype is under construction, to check the assembly of the complete LTDB and the mechanical insertion in the FEC.
  - A full size (320 channels) analog LTDB motherboard is under design.

- Challenges and risks
  - Low risk associated.

D.2.3.3 Digital mezzanine

A 32 channel digital mezzanine design is presently being finalized.

- Design characteristics and status
  - The design is based on a commercial FPGA and on a COTS ADC.
  - The design has the ability to accomodate any standard optical package. It is presently based on SMT, but can easily be modified to lower profile optical packages if needed.
  - The first complete digital mezzanines should be available by November 2013.
- Challenges and risks
  - Low to moderate risk associated.

D.3 Tests, further review, installation

D.3.1 Tests during construction

The design and construction phases will be preceeded and interleaved with component verification and testing and partial element functional tests to understand how the components can be used in the design. Partial subassemblies (e.g. mezzanines) will be separately tested at construction. Once assembled, the LTDB0 will be extensively scrutinised in the bench with test signals. Also functional tests of the optical links will need to be performed with some commercial optical receiver followed by an FPGA.

D.3.2 Tests at EMF

A half FEC will be available at EMF and will be fully instrumented with boards and a readout system equivalent to one of the half FECs operating in ATLAS. The calorimeter cells are simulated by a PCB which includes RC components and is plugged on the back of the baseplane and allows to use the calibration system to generate signals into the FEBs as if coming from the calorimeter. Multiple tests can be performed in this environment.

The setup will be established first as a benchmark as close as possible to the current ATLAS system, i.e. with a set of FEBs and auxiliary boards and a TBB board to make 0.1x0.1 energy sums, transmit them via 70 m analog cables to receiver boards, the output of which will be digitized at 40 MHz. In addition a standard readout by means of the RODs and further DAQ chain will provide the ATLAS like TDAQ environment. By carefully preparing this setup we should be able to measure current levels of noise, crosstalk... as in ATLAS and arrive to comparable results as in the full system.

We plan to have the system ready by September 2013 and perform validating measurements before the end 2013.

Once new demonstrator parts become available the setup will be modified to incorporate these. First the baseplane will be exchanged against a new Phase-I baseplane. The LSBs on the FEBS will be replaced and the new LTDB0 will be introduced in the system. A backend readout in an ATCA crate with an existing pre-prototype LDPB (Sec. 5.2.2.3) will receive the fibers and can be used to readout the digitised trigger signal samples. Full tests can be envisaged simultaneously via (i) the full readout, (ii) the "current" analog Trigger path and (iii) the "new" digital demonstrator path. We will perform measurements and studies like

- Noise, coherent noise studies
- Crosstalk studies
- Energy reconstruction and pulse shape studies

Note that a similar system was used during the main electronics design, validation and production in 2008.

D.3.3 Further review

Since the installation and operation of the demonstrator FEC can crucially affect the operation of the L1Calo trigger and in consequence the full ATLAS operation, it goes without saying every step in the process will only be addressed after a satisfactory completion of the previous one. A fully positive outcome of the tests at EMF will be a sine-qua-non condition to proceed with the installation of the demonstrator system on ATLAS. We propose the EMF test results and the installation operation planning be reviewed some 4 months before the end of the LS1 access to the calorimeters (the current planning would be for the review to be held in March 2014).

D.3.4 Installation and tests on detector

The installation of the demonstrator system on one FEC of the ATLAS detector will be a delicate operation. A sequence of operations with test steps should insure that LAr data is not compromised.

- Layout fiber cable for LDPB0 - USA15 communication.
- Uncable and dismount all boards from the FEC
- FEBs which need new LSBs will be modified and retested in a surface lab in parallel to the subsequent operations in the cavern.
- Remove warm cable connectors from lower baseplane face by hand manipulations from pedestal front face. The removal is in an ordered fashion removing the front row first and the back row later. Care must be taken not to stress in any way the other end of the warm cables (on the feedthrough pins connectors).
- Free and remove baseplane by unscrewing from inside the FEC chassis
- Install new baseplane and fix screws in place from inside the FEC chassis
- Reconnect warm cables on baseplane lower face, again in an ordered fashion, now back row first, and proceeding with connectors from right to left.

  Note the dismounting/remounting operation of a baseplane and its connected warm cables has already been proven at a mockup system in BNL

- At this point a TDR (Time Domain Reflectometry) test will be performed to ensure the connection to the calorimeter is arriving all the way up to the baseplane connectors. Such tests were performed at the original construction and are typically operated one slot at a time.
- Reinstallation of (modified) boards and LTDB0s
- Recabling
- Installation of an ATCA crate with pre-prototype LDPB(s) in USA15 and connection to a control system
- Further detailed tests with the full readout and trigger systems while access to the crate is possible.

Spare parts for all boards and equipment which need to be dismounted/remounted is available, should irreparable damage occur during the installation operations.

The last operation in the above list will be scheduled with enough time left up to the end of access to the FEC. Should unforeseen results from the full and detailed tests arise, we should be left with sufficient time to undo the modifications, i.e. re-install the original baseplanes and unmodified FEBs, thus fully restoring the original readout.