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Image Acquisition Module for uTCA Systems

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***Abstract*—The paper presents a prototype of Image Acquisition Module (IAM) dedicated for plasma monitoring. The complete frame grabber together with camera controller, timing and communication interfaces is fitted in one Advanced Mezzanine Card (AMC) to maintain compatibility with the Micro Telecommunications Computing Architecture (µTCA) standard.**

***Keywords*—image acquisition, frame grabber, mtca, utca, amc**

I. INTRODUCTION

The Micro-Telecommunication Computing Equipment (µTCA) and Advanced Telecommunication Computing Architecture (ATCA) standards (referred to as xTCA) are gradually gaining popularity in the industrial control systems. The number of compatible COTS Advanced Mezzanine Card (AMC) modules increases every year but there is still an important gap on the market. Currently there are no high-speed video acquisition cards available. The machine vision plays an important role in many industrial processes, hence the effort was taken to develop an AMC module offering possibility to interface high-speed high-resolution cameras.

Most Image Acquisition Systems (IAS) have to be scalable by design. Consider, for instance, the ITER thermonuclear reactor Instrumentation and Control (I&C) system. It is supposed to include about 20 video cameras with frame sampling frequencies of 1 kHz and approximately 400 high-resolution imaging devices providing data with throughput reaching almost 7 Gb/s [1]. Extending system by one camera shall require as small changes to the existing infrastructure as it is only possible.

II. GENERAL SYSTEM ARCHITECTURE

A. High-throughput Image Acquisition System

To fulfill the scalability requirement, the system shall have modular construction. This paper focuses on using the AMC standard as the base for Image Acquisition Module (IAM). The compliance with AMC standard helps to ensure high Reliability, Accessibility and Serviceability (RAS) of the final device. Such a module may interface with virtually any µTCA crate or ATCA carrier blade. The communication with the host system relies on the high-speed serial connectivity. The example AMC module is shown in the Figure 1.

The IAM has to interface one or more video cameras. Considering the multi-gigabit video streams and the connectivity available for AMC module it is justified to acquire data from a single camera at a time. The Camera Link has been selected as the video transmission interface. It has become an industrial standard for the low-distance high-throughput raw video transmission. It is relatively easy to be implemented in hardware, an off-the-shelf chipset is commercially available. The extended link provides throughputs up to 6.8 Gb/s [3] and allows for cable length up to 10 meters.

For a reliable transmission over larger distances the video data has to be captured and encapsulated in frames of higher-level data transmission protocol like Gigabit Ethernet or PCI Express. This defines the main task of the described IAM.

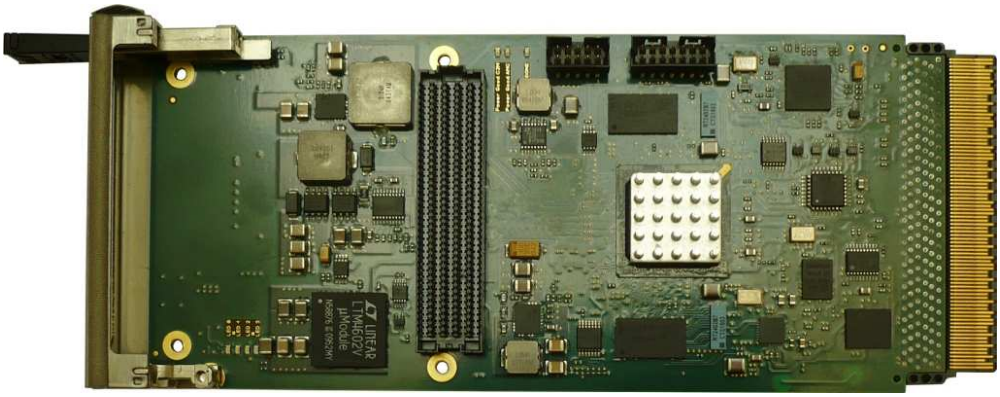

Figure 1. Commercial FMC carrier module compliant with AMC standard

B. Camera and Its Interface

The two types of fast cameras are available on the market. First type has an internal storage and offers high speed recording to its own RAM memory. These devices are usually capable of storing up to 32 GB of video stream and then make it available through some general purpose communication interface. Assuming resolution of 3 Mpx at the frame rate of 1000 FPS the memory can store only 11 seconds of recording.

The second type of camera provides whole video stream with latency kept as small as possible. The real-time operation is a fundamental requirement for plasma monitoring hence only this type of camera will be further considered. The available sensor resolutions are currently of the order of 1 to 5 megapixels with 8 to 10 bits per pixel. The sampling speed varies largely, but in most cases it is naturally limited by the throughput of the communication interface. The image sensor is usually sensitive to light in the spectral range of visible light or infrared. Several companies specialize also in the ultraviolet and X-ray wavelengths, but these devices are mainly low speed specialized sensors.

The following communication standards are often used in high-throughput machine vision systems:

- GigE Vision (up to 1 Gb/s)
- IEEE 1394 (up to 3.4 Gb/s)
- USB 3.0 (up to 5 Gb/s)
- Camera Link (6.8 Gb/s)

The Camera Link data transmission standard is hence the only choice for the top-notch video cameras.

C. AMC Framegrabber Card

There are no COTS video acquisition modules with Camera Link dedicated for the xTCA available. Nevertheless, there is an option to construct such a solution without having to design it from scratch. The AMC card can be an universal carrier board for other extension modules. The FPGA Mezzanine Card (FMC) standard addresses this need. The AMC / FMC modules provide board with an FPGA circuit together with many supporting blocks, like memory banks or clocking circuits.

The commercially available carrier modules offer Xilinx or Altera FPGA circuit. Considering Xilinx devices, the Virtex-5, Spartan-6 and recently Virtex-6 are mainly used. The boards offer a variety of communication standards. The most common options are Gigabit Ethernet, PCI Express and SATA. The actual number of links of each type is dependent on particular board design and availability of high-speed communication interfaces in particular FPGA device.

The boards usually provide SDRAM memory with DDR2 or DDR3 interface, well suited for supporting embedded processor designs and for use as general purpose data buffers. Several boards offer memory expansion by use of the SODIMM memory modules. The QDR SRAM memory is less common due to its high price per megabyte and low capacity. Nevertheless it does not require refresh cycles and supports simultaneous read and write operations. Higher bandwidth and low deterministic latency render it a convenient solution for implementing fast FIFO queues [2].

The plain FMC carriers are generally not able to acquire any data from the outside world. This functionality has to be provided by the small overlay modules. The FMC specification defines two types of connectors. A High-Pin Count (HPC) 400-pin connector is capable of passing up to 160 differential user-defined signals, several clocks and reference voltages. Optionally a Low-Pin Count (LPC) connector may be used. It has the same dimensions as HPC connector but only four out of ten contact rows are populated [5].

Integre Technologies developed an FMC module with Camera Link interface. The FMC-200 board, shown in Figure 2, was selected for the prototype system.

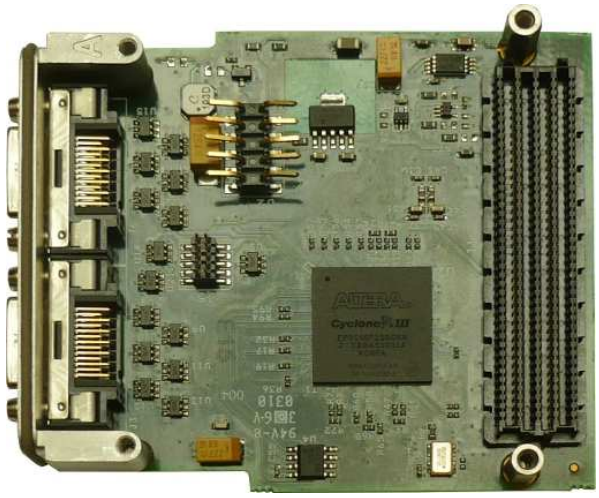

Figure 2. Commercial Camera Link FMC module

III. Image Acquisition Module

A. System Usage

The IAS system described in the paper is dedicated for observing the plasma in the toroidal thermonuclear reactor. Its task is to detect visible plasma instabilities and provide a detailed visual log of any unexpected event in the reactor chamber. The module will be further used for evaluating implementations of the lossless video compression and feature extraction algorithms.

B. High-Speed Camera

The developed IAS system uses Mikrotron MC3010 (grayscale) or MC3011 (color) camera shown in Figure 3. The device is capable of capturing frames of maximum resolution of 1696 x 1710 at the rate of 285 frames per second [3]. The user can reduce its region of interest increasing the frame rate up to 180 000 frames per second. The camera is capable of generating data streams reaching 6.6 Gb/s. The data is serialized over 15 pairs of Camera Link interface with the ratio of 7:1 and sent to host together with 3 independent clocks and control signals.

Figure 3. Mikrotron MC3010/MC3011 camera

C. *Camera-Link Interface Module*

The FMC-200 from Integre Technologies is the only FMC module with Camera Link interface that is currently available commercially. The module first captures high-speed video data from three links composed of four serial data lines and clock signal. Then it provides a bit permutation to get more intuitive data representation and finally serializes the data again using clock frequency of about 86 MHz. The video stream is transmitted farther using 11 links with serialization ratio of 8:1 with bit clock of 668 MHz. The module provides a set of configuration registers through legacy parallel interface (address bus, data bus, strobes).

The module simplifies the data capture process, by synchronizing data arriving from all the three channels. In case of cooperation with MC3010 camera this interface works properly only up to the frequency of 70 MHz. The tests performed in the 75 MHz to 85 MHz frequency range indicated presence of errors on one or more links to the carrier board. There are two evidences for this problem to be related to the link between camera and FMC-200.

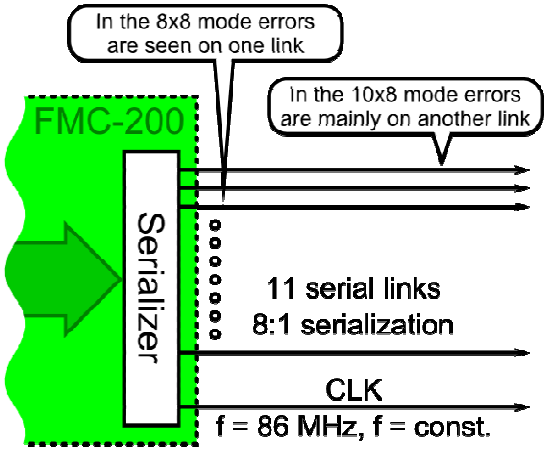

Figure 4. Errors seen at the FMC module output

The errors concentrate on different FMC-200 data output channels depending on the serialization configuration selected – see Figure 4 for reference. During the test the configuration is updated in the camera and in the FMC-200 module, but the deserializers implemented in TAMC631 remain unchanged. The FMC-AMC link parameters do not change during the switch hence the error probably appears earlier in the data path. If it were caused by wrong routing or errors in TAMC-631 firmware it should be always observed at the same channels.

Second evidence is that the errors presence is dependent on the camera pixel clock. The FMC to carrier board interface operates at constant bit rate. Its timing is independent of the camera to FMC link frequency, therefore this link should operate identically despite the change.

The FMC-200 also provides basic UART functionality for controlling the camera. This interface is only accessible by the module internal registers. The implemented controller cannot be bypassed, so the host system is forced to access this unit, even if it contains native UART interfaces – which is the case with MicroBlaze-based system.

D. *Data Acquisition Module*

The TEWS Technologies TAMC631-12R board was selected as a FMC carrier module. It offers a modern Spartan-6 FPGA circuit capable of capturing a high-speed serial transmission from FMC-200. The board is equipped with two banks of DDR3 memory (128 MB each). There is no QDR memory available. The majority of local clocks is provided by the universal configurable integrated clock generator. The module block diagram is shown in Figure 5.

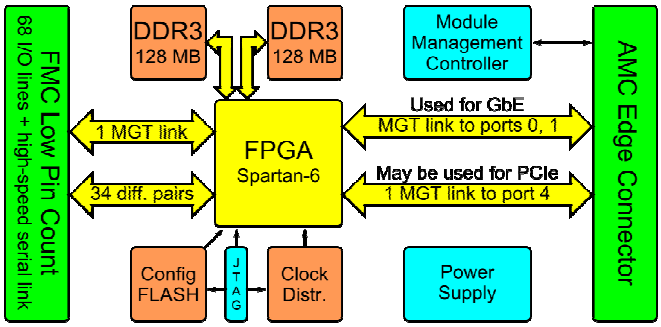

Figure 5. TAMC631 block diagram

The chosen FPGA circuit offers only four multi-gigabit links. One of them is connected to the FMC slot, others to the AMC connector. Two links are provided on the AMC ports 0 and 1 and may be used for Gigabit Ethernet connectivity. For backward compatibility reasons only one of them is used in the prototype system. The board offers one link on AMC port 4, which may be used to establish a PCI Express x1 connection.

The board is supervised by the Module Management Controller (MMC), according to the requirements of the AMC standard. The MMC circuit monitors the voltages, currents, temperatures and provides the hot-swap functionality. It is also responsible for identifying the FMC module and controlling the voltages provided to the overlay. Although the MMC seemed operating properly, it was unable to initialize the FMC module. The solution was to override the power requirement settings manually through the Intelligent Platform Management Bus.

IV. MODULE FIRMWARE

A. Overview

The FPGA firmware prepared for IAM is divided into four major components: data write path, memory controller, data read path and embedded microcontroller unit. Every component is composed of smaller functional modules, shown in the block diagram in the Figure 6.

Every of the major blocks is constrained to be placed in a distinct FPGA circuit area to avoid timing problems. The clock domains are not crossing the block boundary, until it is not absolutely necessary. The hardware debugging is possible with use of the integrated logic analyzers of the ChipScope Pro tool.

B. Write Path

The data arrives from the FMC-200 module in the form of 11 channels of 8:1 serialized data together with the reference clock signal. The data is first deserialized, and then the start of frame and data valid markers are extracted and provided to the write sequencer. Status bits are removed and the remaining bytes are aligned into the 128-bit long words. The aligner may be sourced from the actual camera data stream or use the built-in test data generator with six different patterns.

C. Video Frame Format

Every video frame is prepended with a header containing a number of 128-bit long rows (see Figure 7). The first row contains the frame signature, length of the payload data, count of provided sub-headers and header check sum. In the following row the video frame is characterized by its resolution, number of frames per second and a 48-bit long sequence number. Finally a time stamp row is appended. Currently it contains value of a free-running counter incremented by one every 50 ns. This value will be replaced by timestamp provided by dedicated synchronization IP-core.

The video data is transmitted in grayscale with 8 bits per pixel in the row by row manner. At the end, the data is padded with zeros to the next 128-bit word boundary.

Finally a 128-bit footer with 112 bits for the checksum is provided. The video stream with headers and footer is transferred to the memory controller module.

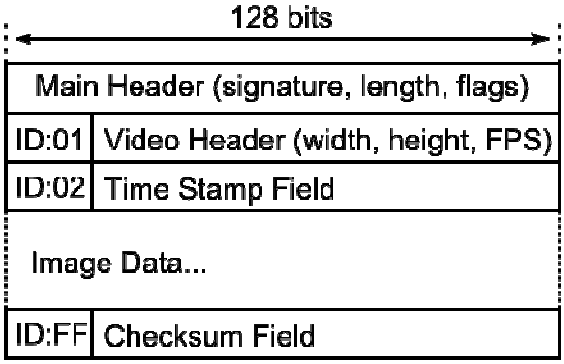

Figure 7. Video frame format

D. Memory Controller

The DDR3 memory interface is too slow to handle simultaneous data read and write operations at the full required throughput. For this reason, at a time only one memory may be written and only one memory may be read. The memory usage is governed by the memory arbiter. To utilize the available bandwidth effciently all operations are performed in the burst mode, therefore a dedicated read and write controllers are required.

The write path sequencer is instructed by the embedded mirocontroller how many frames it is permitted to store in the memory before it have to realease it. After that, the memory is marked as full and is made available for the reader module.

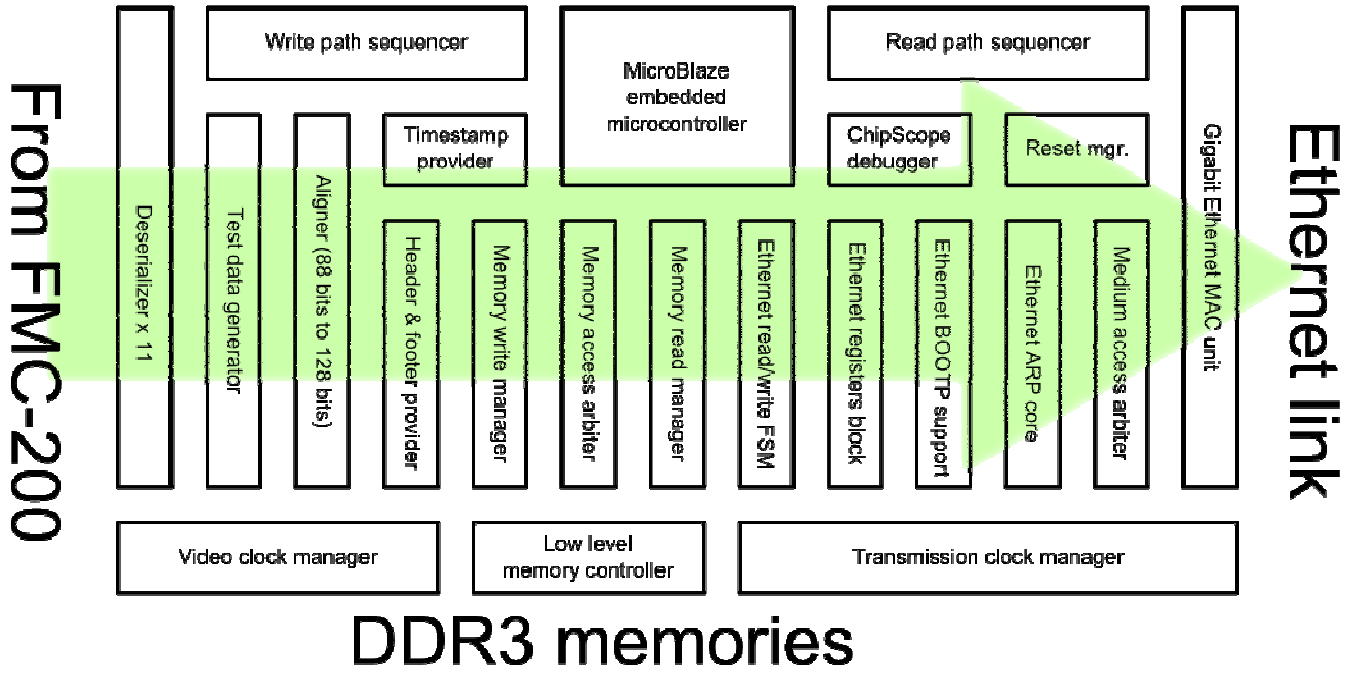

Figure 6. Image Acquisition System FPGA firmware block diagram

E. *Read Path*

The Ethernet module transmits the data using custom UDP-based protocol. The reliability and efficiency is ensured by data completeness test and retransmission mechanism [7]. The module is configured through a set of Ethernet-accessible registers. The firmware implements the BOOTP protocol client to automatically obtain IP addres. The ARP protocol is used to discover the MAC address of data destination host. The module also provides responses to the external ARP requests. The code employs the TriMode Ehernet MAC hardware block available in the utilized FPGA [8].

F. *Integrated Microcontroller*

The embedded microcontroller system uses the MicroBlaze soft-processor and provides multiple functionalities. The processor and its peripheral are shown in the Figure 8. The CPU governs the module initialization and reads the registers of Ethernet module. When a request for new configuration is detected it adjusts the FMC-200 module and the video camera to provide the selected data format. Alternatively it may switch the writer module to provide one of the test images. Finally it sets the number of frames to store in each memory and fills the dynamic fields of the data headers. When the system is ready it starts the acquisition with the next start-of-frame marker.

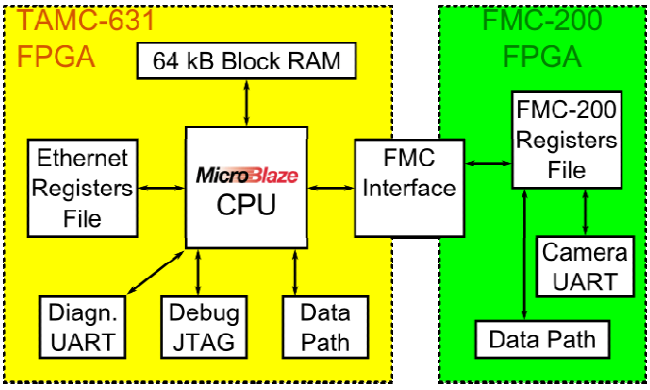

Figure 8. MicroBlaze-based control system

The system contains number of diagnostic features. The program execution can be monitored using the JTAG interface. The diagnostic messages and several test modes can be accessed via the traditional UART interface. The most timing critical signals are also monitored with the ChipScope Pro tool.

V. Results and Future Plans

A. *System Evaluation*

The IAM was tested in the laboratory and was proven to operate properly. In the test setup the module was inserted into the µTCA shelf. The data was transmitted over the backplane to the CPU module located in the same shelf, that also provided the BOOTP service. The demonstration shown that it is possible to acquire data stream from a top-notch high-speed camera using an AMC module operating in µTCA crate, using only off-the-shelf components. The full data stream (up to 7 Gb/s) was not transmitted to the CPU module due to limitation of using only single Gigabit Ethernet link. For the demonstration the frame rate was reduced to provide about 90% link saturation.

B. *Conclusion*

To achieve the full video stream throughput the external communication interface has to be upgraded. The PCIe x4 interface, with data transmission speeds of about 8 Gb/s, will be used in the next revision.

The system latency can be significantly reduced by replacing the DDR3 SDRAM memory with the QDR SRAM. The QDR memories allow for simultaneous read and write operations, therefore there is no need of filling the memory with preprogrammed number of frames. The data may be stored and retrieved in parallel with almost no delays.

The FMC-200 module errors seem impossible to be compensated. The new FMC module with Camera Link interface is under development.

Acknowledgment (Heading 5)

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