The Upgrade of the ATLAS Level-1 Central Trigger Processor

G. Anders[a,b], D. Berge[a], H. Bertelsen[c], M. Dam[c], E. Dobson[a], N. Ellis[a], P. Farthouat[a], C. Gabaldon[a], M. Ghibaudi[a], B. Gorini[a], S. Haas[a], M. Kaneda[a], S. Maettig[a,d], A. Messina[a], C. Ohm[a], T. Pauly[a], R. Pottgen[a,e], R. Spiwoks[a], M. Stockton[f], T. Wengler[a], S. Xella[c]

[a] *CERN,*
1211 Geneva , Switzerland
[b] *Ruprecht-Karls University*
69117 Heidelberg, Germany
[c] *Niels Bohr Institute, University of Copenhagen*
2100 Copenhagen, Denmark
[d] *University of Hamburg*
20146 Hamburg, Germany
[e] *Johannes Gutenberg University*
55122 Mainz, Germany
[f] *McGill University*
Montreal QC, Canada

E-mail: Stefan.Haas@cern.ch

ABSTRACT: The ATLAS Level-1 Central Trigger Processor (CTP) combines information from calorimeter and muon trigger processors as well as other sources and makes the final Level-1 Accept (L1A) decision. Due to the increasing luminosity of the LHC and the growing demands of physics and monitoring placed on the ATLAS Level-1 trigger system, the current CTP has reached its design limits. Therefore and in order to provide some margin for future operation, the CTP will be upgraded during the LHC shutdown of 2013/14.

KEYWORDS: Trigger concepts and systems (hardware and software); Digital electronic circuits

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1. The Current Central Trigger Processor

The ATLAS experiment [1] at the Large Hadron Collider (LHC) at CERN uses a three-level trigger system. The Level-1 trigger is a synchronous system operating at the bunch crossing frequency (BC) of 40.08 MHz of the LHC. It uses information on clusters and global transverse energy in the calorimeters and on tracks in dedicated muon trigger detectors in order to reduce the event rate to 75 kHz. Figure 1 shows an overview of the ATLAS Level-1 trigger system.

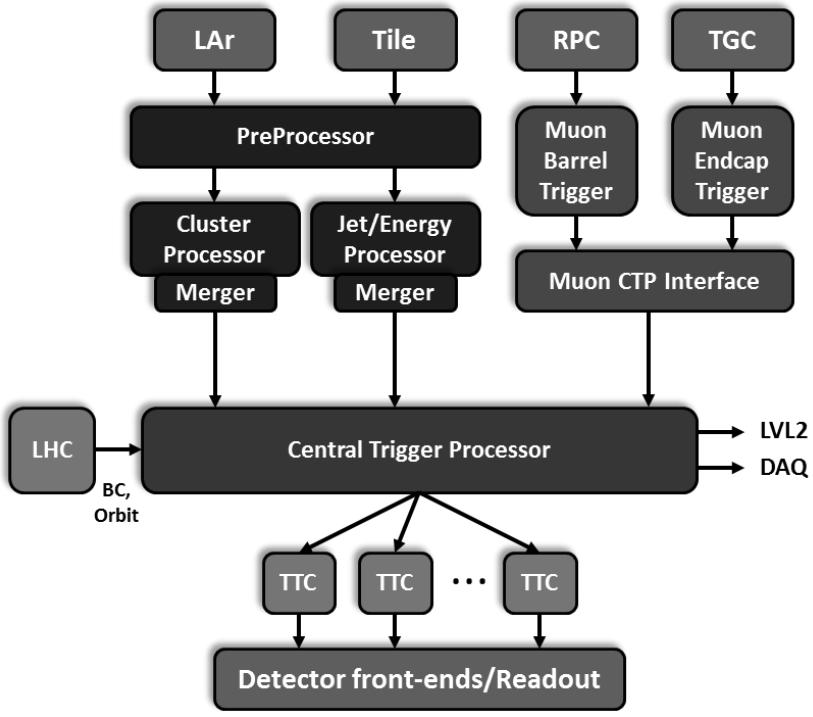

Figure 1: ATLAS Level-1 Trigger Architecture

The Central Trigger Processor (CTP) uses electron/photon, tau/hadron, and jet multiplicities, and transverse energy information from the calorimeter trigger processors together with the muon multiplicities from the muon triggers to make the final Level-1 trigger accept (L1A) decision in a latency of only five BCs. Trigger inputs from various other sources, such as luminosity detectors, minimum bias scintillators and beam pick-ups are also taken into account. The L1A decision is based on flexible logical combinations (a.k.a. trigger items) of the trigger inputs defined in a so-called trigger menu. The CTP can mask trigger items as a function of the LHC bunch structure, pre-scale them, and add preventive dead-time in order to protect the front-end buffers of the experiment from becoming full. The CTP receives timing signals from the LHC and distributes them, along with the L1A, through the trigger, timing, and control (TTC) network. It also sends trigger summary information to the Level-2 trigger and data acquisition (DAQ) systems. In addition, the CTP provides integrated and bunch-by-bunch counter values of the trigger, dead-time, and busy information for luminosity and background monitoring. For a full overview see [2].

The CTP consists of a single 9U VME64x chassis with three dedicated backplanes and eleven custom designed modules of six different types. Figure 2 shows the architecture of the CTP. The machine interface module (CTPMI) receives the timing signals from the LHC and distributes them over the COM (i.e. common) backplane to the other modules. Each of the three input modules (CTPIN) receives up to 124 trigger input signals, synchronizes and aligns them and sends selected trigger signals over the pattern in time (PIT) backplane to the monitoring and core modules. The monitoring module (CTPMON) performs bunch-by-bunch monitoring on the PIT signals. The core module (CTPCORE) generates the Level-1 accept signal (L1A) according to the programmable trigger menu and sends trigger summary information to the Level-2 trigger and the DAQ system. The four output modules (CTPOUT) distribute the trigger and timing signals through up to 20 cables to the sub-detector TTC partitions and receive busy signals and calibration requests from the sub-detectors. The calibration module (CTPCAL) time-multiplexes the calibration request signals from the CAL (i.e. calibration) backplane and performs level conversion of additional from panel NIM input trigger signals.

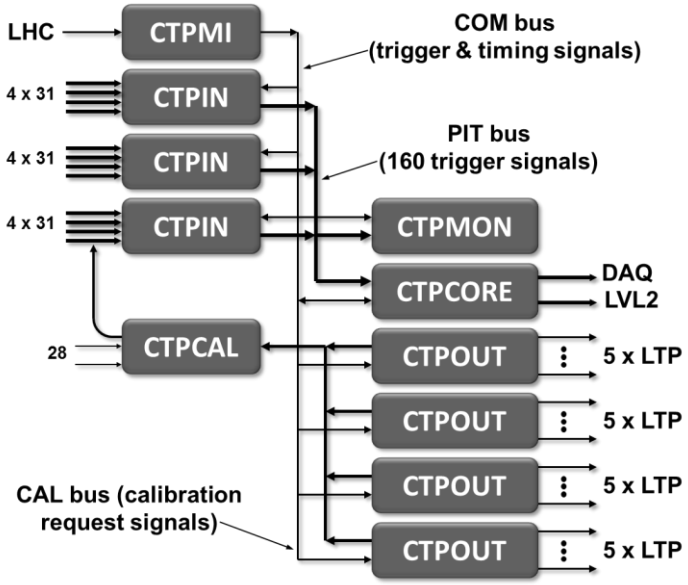

Figure 2: ATLAS Central Trigger Processor

2. The Motivation for the Upgrade

After the shutdown of 2013/14 the LHC will run at a centre-of-mass energy of up to 14 TeV, which is to be compared to the current energy of 8 TeV, and will provide a luminosity in excess of $2x10^{34}$ $cm^{-2}s^{-1}$, which is to be compared to a current maximum of $1x10^{34}cm^{-2}s^{-1}$. In order to preserve the physics capabilities of the ATLAS experiments a number of detector upgrades and upgrades to the trigger system are planned [3]. With view of the Level-1 trigger, and the CTP in particular, the following upgrades are foreseen: a new topological processor will be added to the Level-1 trigger which receives trigger inputs from the calorimeter trigger and coarse muon trigger information from the muon trigger which shall improve the multi-object selection for the increased luminosity [4]. At the same time the calorimeter trigger merger modules which send trigger input signals to the CTP will be replaced with new ones in order to provide the necessary input to the topological processor [5]. The Muon-to-CTP interface will also be modified in order to provide coarse geometrical trigger information to the topological processor. It is planned to upgrade the trigger rate to 100 kHz, the overall latency will however remain unchanged. The round-trip latency is 2.5 us and provides headroom of about 20 BCs as of today. The trigger rate is limited by the readout.

The CTP will have to be capable of receiving the additional trigger inputs from the topological processor and provide additional trigger items for these inputs. As can be seen from Table 1, which shows the CTP resources used by a recent trigger menu, the CTP is already working close to the limits of its capacity. In particular all of the PIT bus lines, which limit the number of useable trigger inputs, and almost all of the trigger items are currently used. Therefore the main motivation of the upgrade during the 2013/14 shutdown is to remove those limitations and increase the number of trigger inputs and the number of trigger items. In addition, the upgrade of the CTP will provide partitioning of the L1A generation for detector commissioning, an improved bunch group masking and bunch-by-bunch trigger item monitoring, and more outputs for sub-detector TTC partitions. In order to reduce the latency, direct electrical input from the topological processor to the CTPCORE is foreseen, as well as optional optical inputs to connect new or upgraded systems, e.g. the topological processor or the new calorimeter trigger merger module, if the latency allows doing so. The CTP upgrade requires a complete redesign of several modules, including the CTPCORE, the CTPOUT, and the COM backplane. The next major upgrade of the CTP is then only foreseen for 2022/24, when the Level-1 trigger architecture will change completely and the latency budget is likely to increase.

Resource	Used	Available
CTPIN input cables (partially used)	**9**	**12**
CTPIN input signals	**212**	**372**
CTPIN integrating monitoring counters	**138**	**768**
PIT bus lines	**160**	**160**
CTPCORE trigger items	**241**	**256**
CTPCORE bunch group masks	**8**	**8**
CTPCORE maximum number of AND terms	**6**	**256**
CTPCORE maximum number of bits in OR terms	**6**	**12**
CTPCORE per-bunch trigger item counters	**12**	**12**
CTPOUT cables to TTC partitions	**20**	**20**
CTPMON per-bunch monitoring counters	**88**	**160**

Table 1: CTP Resource Utilization

3. The Upgrade of the CTP

3.1 The Specification

The new CTP will provide 320 trigger inputs on the PIT bus backplane (cf. 160 today). This will be achieved by using double-data-rate signalling on the existing PIT bus backplane. An earlier study has provided of proof principle [6]. But a latency penalty of about 2 BCs will have to be taken into account. The new CTP will provide 512 trigger items in its programmable trigger menu (cf. 256 today). The CTP will further provide four trigger partitions using a common trigger menu and with each partition having a selection of trigger items and its own dead-time handling. Only the primary or physics partition will provide output to the Level-2 trigger and DAQ. The secondary partitions will be used for detector commissioning, calibration and other tasks. The new CTP will also provide 16 bunch groups for bunch-by-bunch masking of the trigger items (cf. eight today). There will be 256 bunch-by-bunch counters for trigger item monitoring (cf. 12 today). The CTP will provide 64 electrical LVDS inputs (for the topological processor) directly on the CTCPCORE and twelve serial optical inputs using ribbon-fibre receivers. The overall latency target is 7 BCs.

3.2 The CTPCORE++ Module

The block diagram of the new CTPCORE module is shown in Figure 3 below. The design is based on two Xilinx Virtex-7 FPGAs which implement the trigger path logic and the readout and monitoring functionality respectively. These are complex devices featuring 300k 6-input look-up tables, over 1000 RAM blocks of 36 kbit each and 20 multi-gigabit transceivers (GTX), thereby providing ample resources to implement the required functionality. An additional small FPGA is used to interface the processing FPGAs to the VME bus for configuration and control.

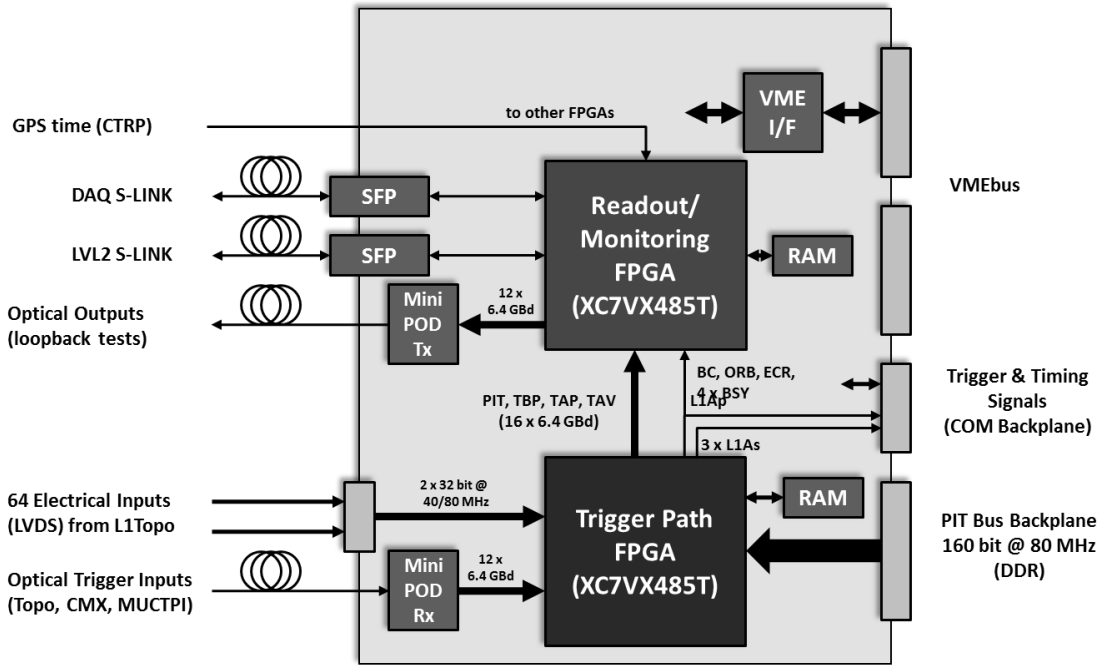

Figure 3: CTPCORE++ Module Block Diagram

The trigger path FPGA implements all of the latency critical real-time data path functionality. It receives up to 320 trigger inputs from the CTPIN modules through 160 PIT bus lines operating at 80 MHz. In addition there are 64 LVDS electrical inputs from a connector on the front-panel of module which are intended to connect to the topological trigger processor. These inputs are intended for the most latency critical trigger signal path, since they avoid the delay penalty for multiplexing and transmission over the PIT backplane. Finally there is also the option to connect trigger inputs optically through 12 serial links operating at 6.4 GBaud using a 12-way ribbon fiber receiver module. However there is a latency penalty of about 3 BCs associated with the serialization and deserialization in the on-chip gigabit transceivers that needs to be considered. High-density optical receiver modules (Avago MiniPOD) are used for the optical-electrical conversion. These modules have the advantage that they can be placed mid-board close to the FPGA, thereby reducing the required line length for the critical high-speed signals and easing potential signal integrity issues.

The trigger path FPGA generates the four L1A signals (one per trigger partition) and the associated trigger type word. These are then sent through the COM backplane to the output modules in the CTP crate. In addition this FPGA needs to send about 2000 bits per BC containing information about the trigger decision to the second FPGA. The required bandwidth of 80 Gbit/s is provided by 16 on-board high speed serial links which connect the two FPGAs and operate at a line speed of 6.4 GBaud with 8B10B encoding.

A second FPGA of the same type implements all the non-latency critical functionality such as readout and monitoring. Upon a L1A, RoI information and trigger summary information are sent to the Level-2 trigger and DAQ systems through two serial optical readout links operating at 2 GBaud. The data contains the 320 trigger inputs as well as the 512 trigger items both before and after masking and pre-scaling for each bunch in a programmable window. The S-LINK protocol implementation of the readout links (S-LINK) is fully integrated in the FPGA, as opposed to the previous generation, which was based on a mezzanine card. Only the primary or physics trigger partition can send data to the Level-2 and DAQ systems. The module also adds a precise time-stamp to each event, the GPS timing reference is received from an external card (CTRP) via General Machine Timing (GMT) system of the LHC.

The readout monitoring FPGA also implements comprehensive monitoring features: about 1800 integrating counters for monitoring the trigger rates on the data from the trigger path FPGA as well as 256 per-bunch monitoring counters. Each per-bunch monitoring counter builds a histogram of a selected trigger item as a function of the bunch number. About 50% of the available on-chip block RAM resources of the selected FPGA are required for this.

The CTPCORE++ module also includes various test and diagnostics features. Each FPGA interfaces to a DDR3 memory module which can be configured as playback and snapshot memories for system validation and diagnosis. This kind of feature has already been proven to be extremely useful in the current system [7]. The two memories provide sufficient bandwidth to source and sink the trigger path information of about 2000 bits per BC. In addition there is a ribbon fiber transmitter module which allows for loopback tests with the optical trigger inputs.

Figure 4 below shows the schematic view of the firmware of the trigger path FPGA. It receives and synchronizes 320 trigger input signals received from the PIT backplane. These are then combined in an array of Look-Up Tables (LUT) and a large ternary Content-Addressable Memories (CAM) to form 512 trigger items. This scheme allows for maximum flexibility in the logical combinations of the trigger inputs while respecting the tight latency constraint. A programmable bunch group mask (BGRP) is applied to the output of the CAM and each trigger

item can then be individually pre-scaled by fractional scalers (PSC). The outputs of the pre-scalers (TAP) are gated with a programmable mask, dead-time and busy signal (VETO) before they are ORed to generate the L1A signals. Preventive dead-time (DT) is generated to protect the detector front-ends and prevent buffer overflow and is a combination of a simple and two complex dead-time algorithms. Simple dead-time vetoes triggers for a fixed number of BCs after a L1A, while the complex dead-time is based on a leaky bucket algorithm to model the detector front-end buffers.

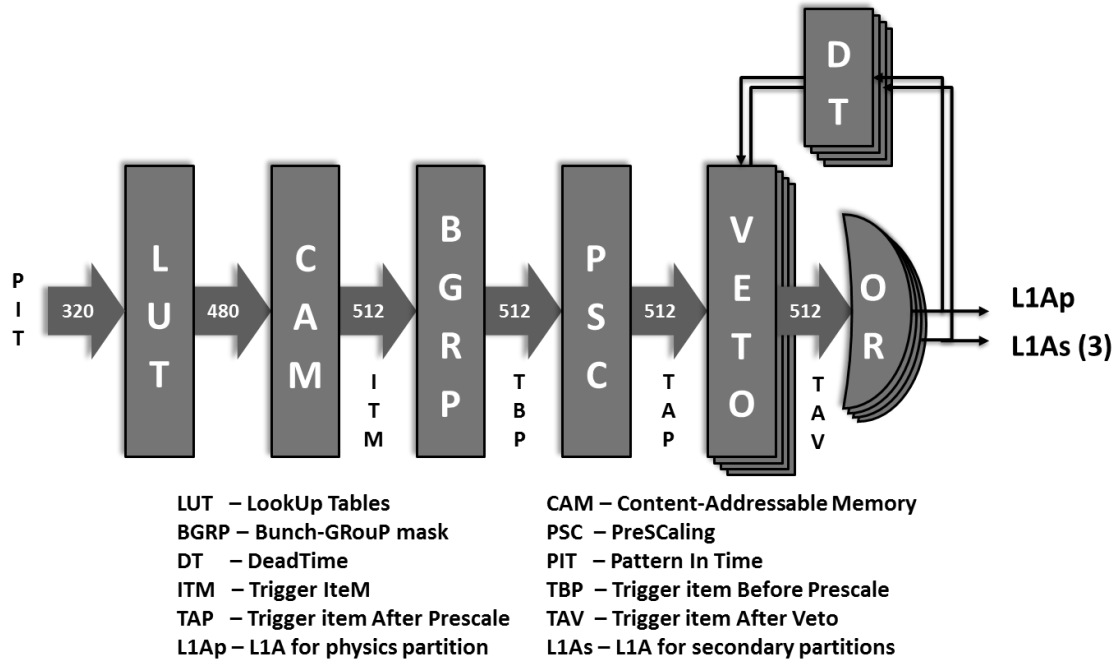

Figure 4: CTPCORE++ Trigger Path

The veto logic, dead-time generation, logical OR of the trigger-after-veto (TAV) bits and trigger type logic (not shown) are implemented independently for each of the four trigger partitions. All four partitions share the LUT, CAM and pre-scaler resources, the programmable mask defines which trigger items are included in the L1A generation for a given partition.

The initial implementation of the trigger path firmware requires about 40% of the distributed memory LUT resources of the selected FPGA which are essential to implement the large CAM. The latency of the trigger path logic is about two BCs.

3.3 The CTPOUT++ Module & Backplane

In order to provide support for more than one trigger partition, the CTPOUT modules as well as the trigger and timing distribution (COM) backplane also need to be replaced. A block diagram of the CTPOUT++ modules is shown in Figure 5 below. Each module feeds five sub-detector partitions through parallel LVDS cables. The module receives and fans out the timing signals, bunch clock, orbit and event counter reset to the cable connectors on the front-panel. Each output can be part of one of the four trigger partitions. This requires selecting the corresponding L1A and trigger type signals from the COM backplane to drive the output. Due to restricted number of connections possible on the backplane, the three secondary trigger partitions only support reduced trigger type functionality, where the 8-bit trigger type word can only be selected from a set of four pre-defined values programmed on the CTPOUT++.

At the same time the busy coming from the sub-detector needs to be steered to the correct trigger partition busy on the backplane. The multiplexing of the trigger signals will be implemented in a CPLD or a small FPGA in order to keep the latency low. The latency target is less than one BC from the backplane to the output connectors. A second FPGA implements the VME interface. Additional features include improved monitoring of the busy signals coming from the sub-detector partitions; in particular per-bunch monitoring will be possible. Finally a programmable pattern generator is foreseen, this can be useful for example for diagnosing issues with the TTC signal distribution to the sub-detectors.

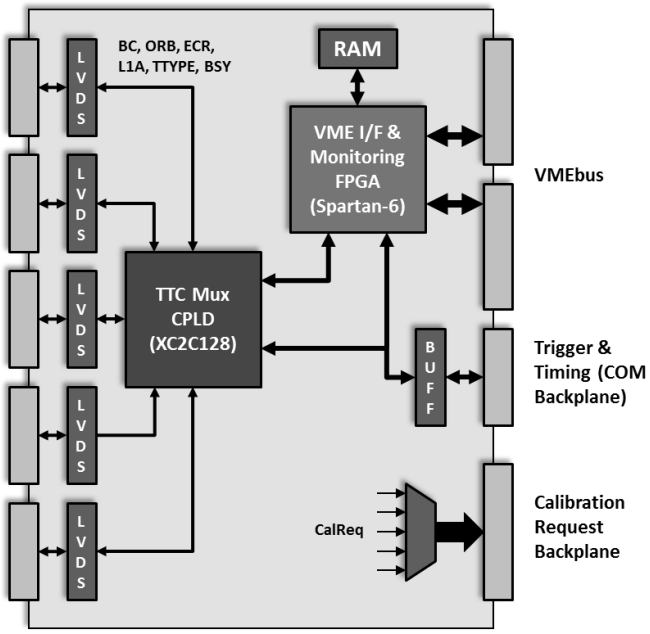

Figure 5: CTPOUT++ module block diagram

The COM backplane also needs to be replaced, since the existing one does not provide enough connections to distribute signals for the 3 additional trigger partitions from the CTPCORE++ to the CTPOUT++ modules. At the same time the number of output slots on the backplane will be increased to allow 25 instead of 20 sub-detector partitions to be connected.

4. Summary

An upgrade of the ATLAS Central Trigger Processor which will overcome the resource limitations of the current system in terms of trigger inputs and provide increased flexibility for the trigger menu has been presented. The upgrade requires the redesign and replacement of the CTPCORE and CTPOUT modules as well as the custom backplane used for timing and trigger signal distribution. The aim is to install the upgraded CTP in time to be ready for detector commissioning from the first quarter of 2014 onwards.

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