Recent developments for the Upgrade of the LHCb readout system

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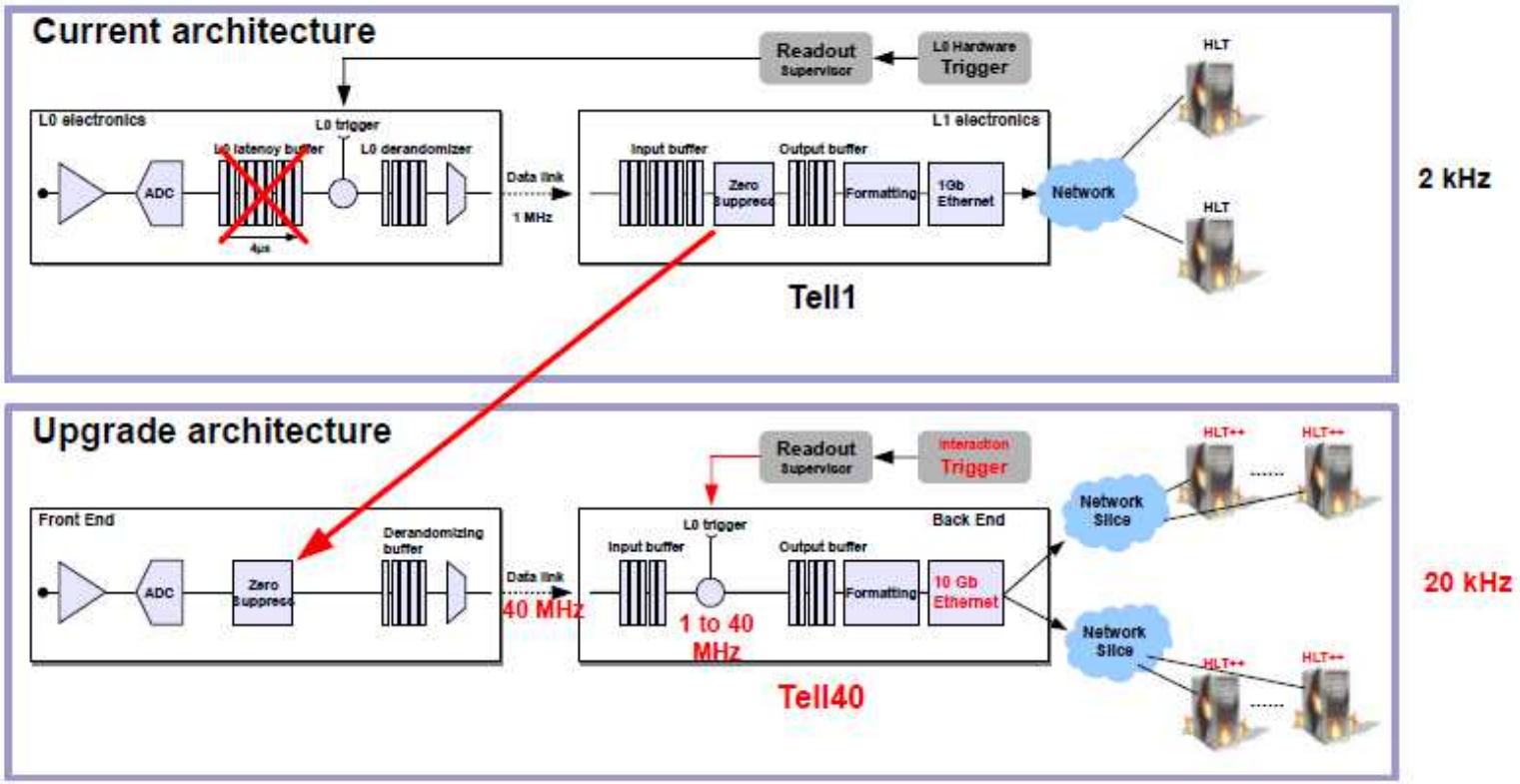
Outline

- **Readout system architecture**
  - Key points
  - Mapping over ATCA
- **Full scale prototype**
- **Measurements**
  - Clock phase stability over FPGA serial links
  - BER at 10 Gbps
  - Thermal
- **Firmware development**
- **Conclusion**

Architecture

LHCb readout upgrade



Migration to a trigger-free readout at the bunch crossing rate of 40 MHz

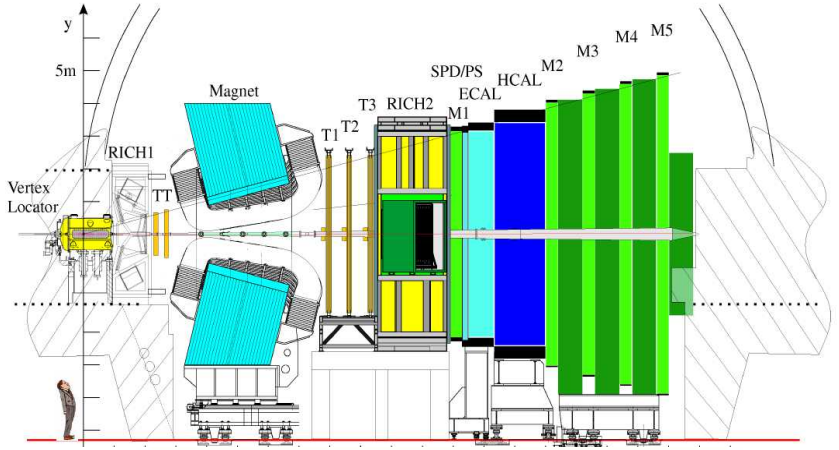
- Readout at 40 MHz instead of 1 MHz
- Compression in the front-ends
- 10 Gbits/s to the farm
- Event selection in the farm

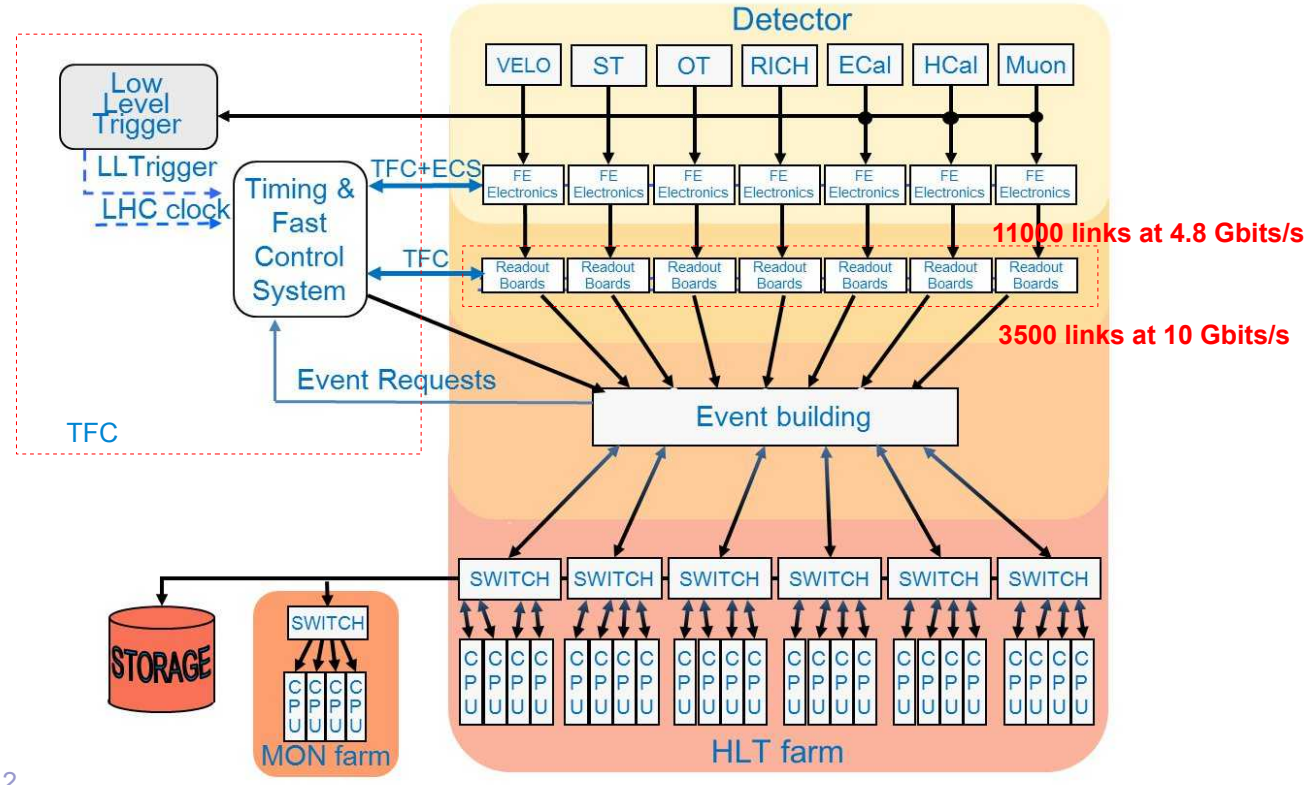
General architecture

5 main blocks :

- FE
- Readout boards
- TFC system
- Online network
- HLT Farm

LHCb Readout system





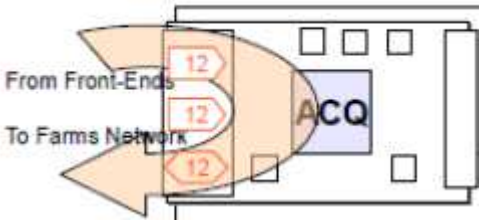
Keypoints of the architecture

Use of GBT links

- Bidirectional optical links 4.8 Gbits/s - 3.2 Gbits/s available BW
- Acquisition, Trigger and Fast Control, Slow Control on a same link
  - Use of a same generic hardware to implement the three functions

Acquisition

- Data compressed in the front end:
  Very high data throughput:
  output data flow ~ input data flow



  - Bandwith too large for transfering acquisition data through a backplane
  - Backplane well adapted for low jitter fast controls (clock, throttles etc) and supervision

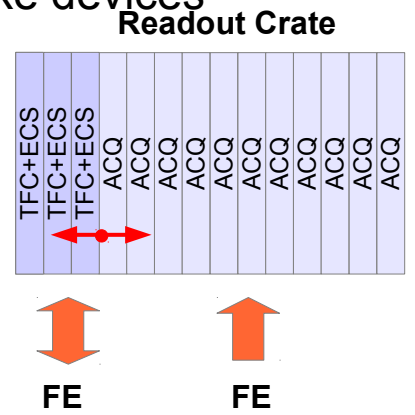
Interface to farms

- High speed commercial link:
  - State machine interface to 10 GbE, Infiniband, ..

Keypoints of the architecture

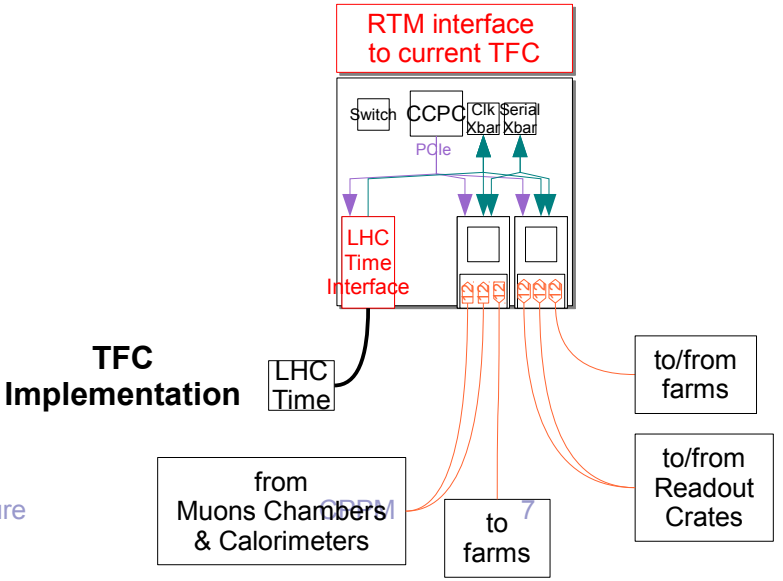
ECS/TFC bridges

- High density: 11000 optical links → use of SNAP12-like devices
- Approximately one ECS link (bidirectional)
  or TFC link (output)
  for 10 acquisition links (inputs only) :
  Use of SNAP12 makes difficult such granularity
  - Splitting of acquisition and TFC+ECS
    to optimize optical links



TFC

- Same hardware as acquisition boards
  - Limited addition of
    few special functions devoted to TFC
    (RTM interface to Current TFC,
    LHC Time interface, ...)



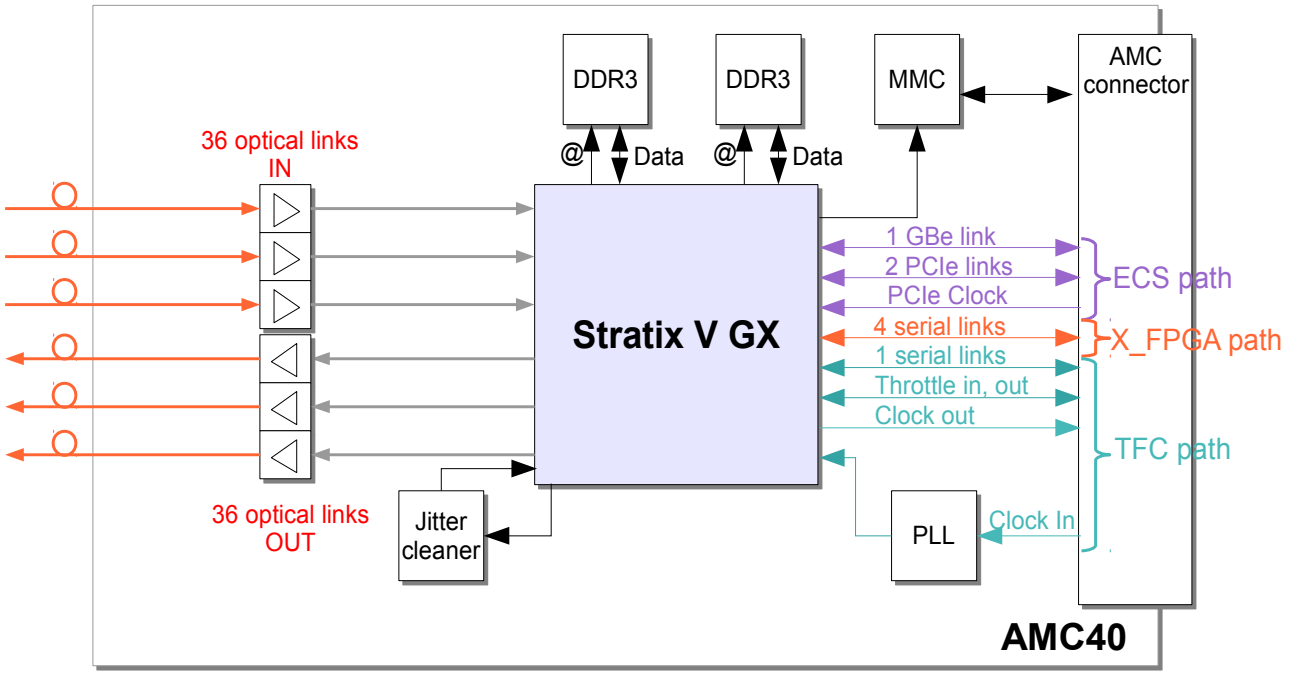
ATCA standard

The LHCb collaboration decided to implement the readout on ATCA

- Many advantages :
  - Robust and well defined mechanics
  - Adapted to recent components
    - Form factor lets more room for heatsinks
    - Power supply dimensionned for high speed components
    - Powerfull cooling
  - Standard backplane
    - Topology based on serial links
  - Standard mezzanines
  - Costs comparable to VME
  - Elaborate health monitoring system (IPMI)
- Difficulties
  - IPMI implementation quite complicate

→ Review of feasibility at the end of full scale prototype

Generic optical mezzanine: AMC40

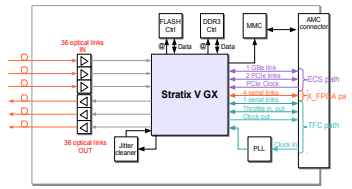


36 bidirectional optical links at up to 10 Gbits/s

622 kLE FPGA Stratix V GX: 5SGXEA7N2F45C3N

Generic readout board

AMC40

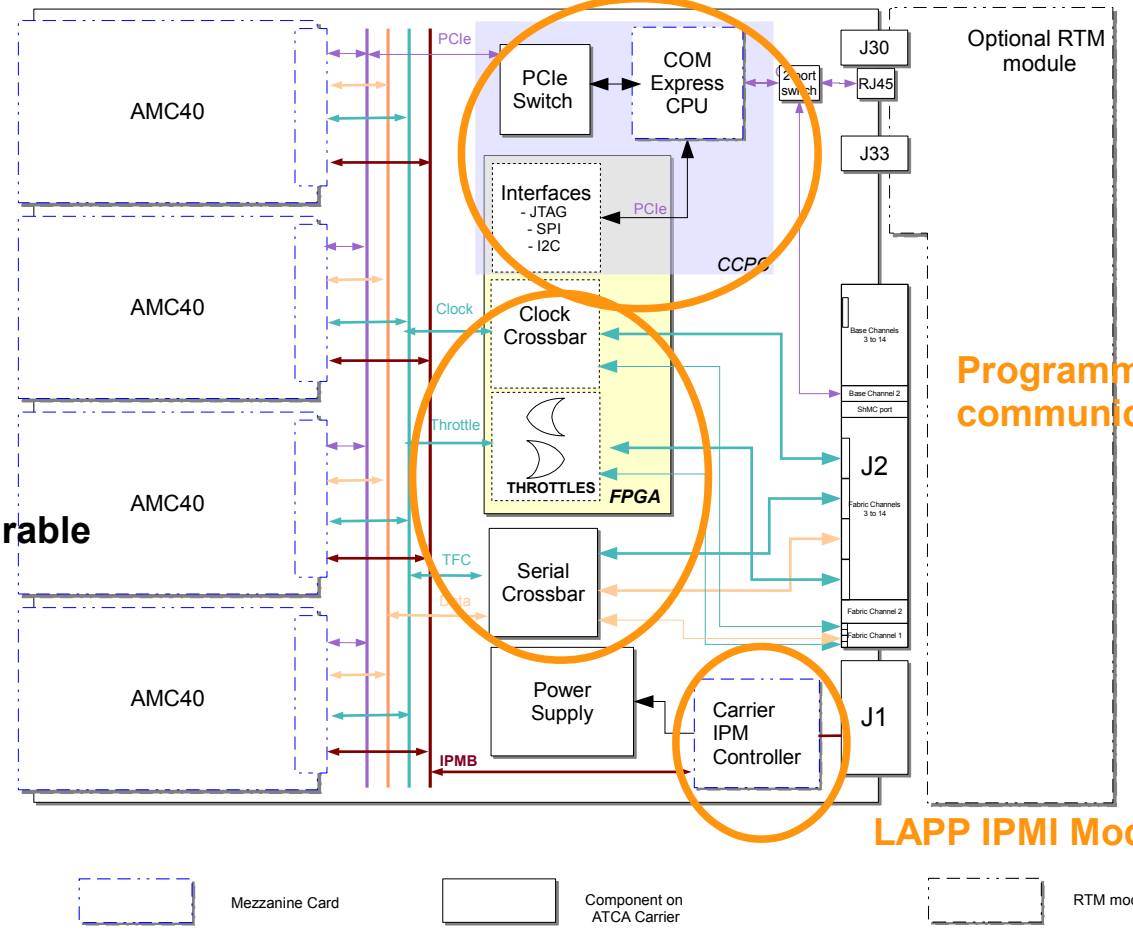


Flexible and reconfigurable carrier board

144 optical links :
- **96** GBT links
- **48** 10GbE links

ATCA40

COM Express for slow control



Programmable communication matrix

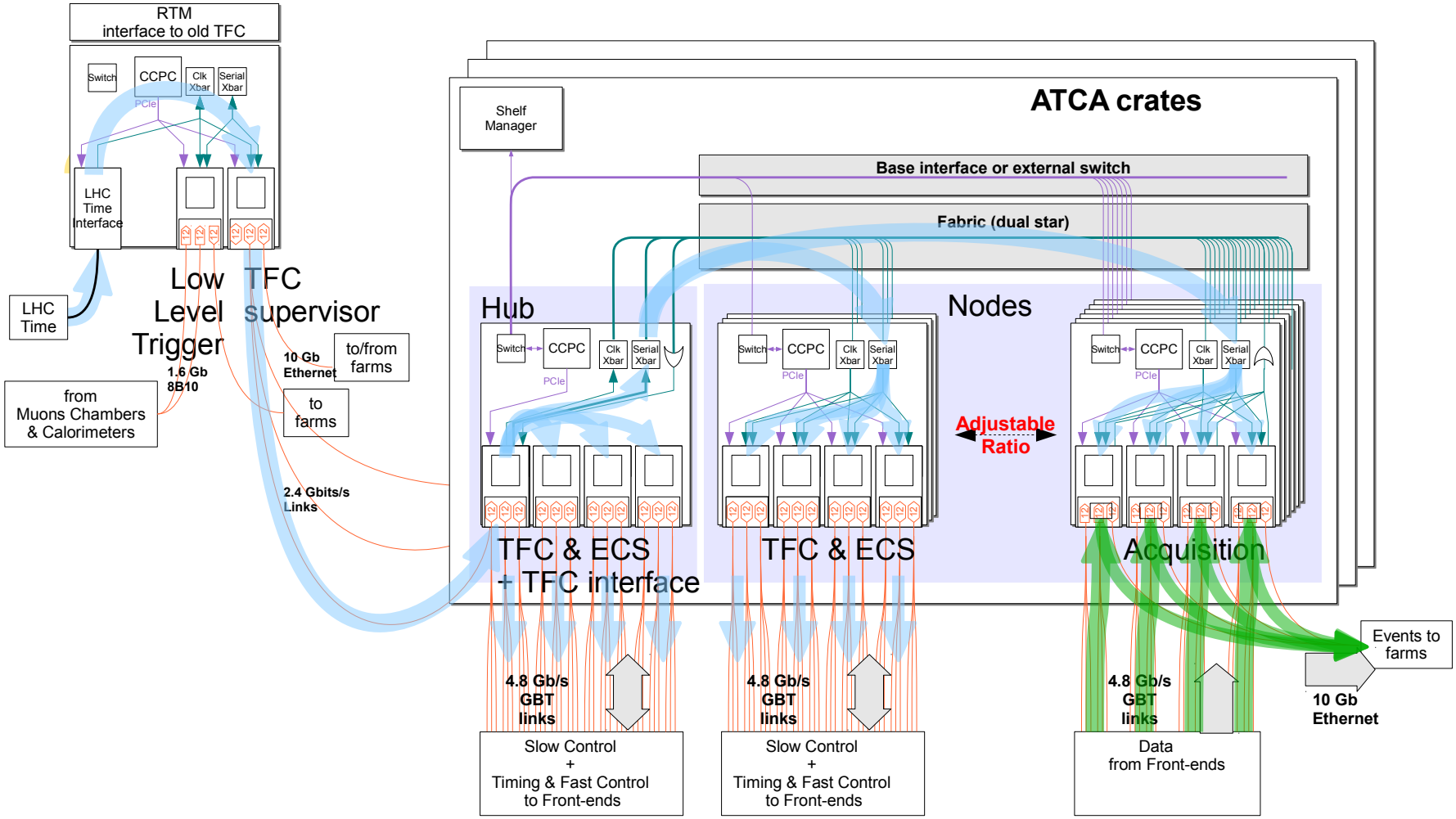
LAPP IPMI Module

Mezzanine Card | Component on ATCA Carrier | RTM module

Different firmwares to implement readout, time distribution, slow control, trigger interface

Data paths : Acquisition
Timing and Fast Trigger

Through optics, board and ATCA backplane fabric

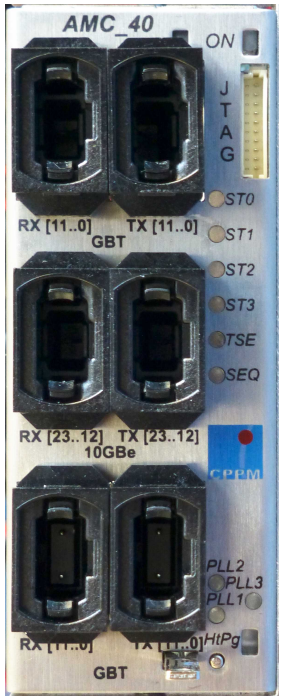


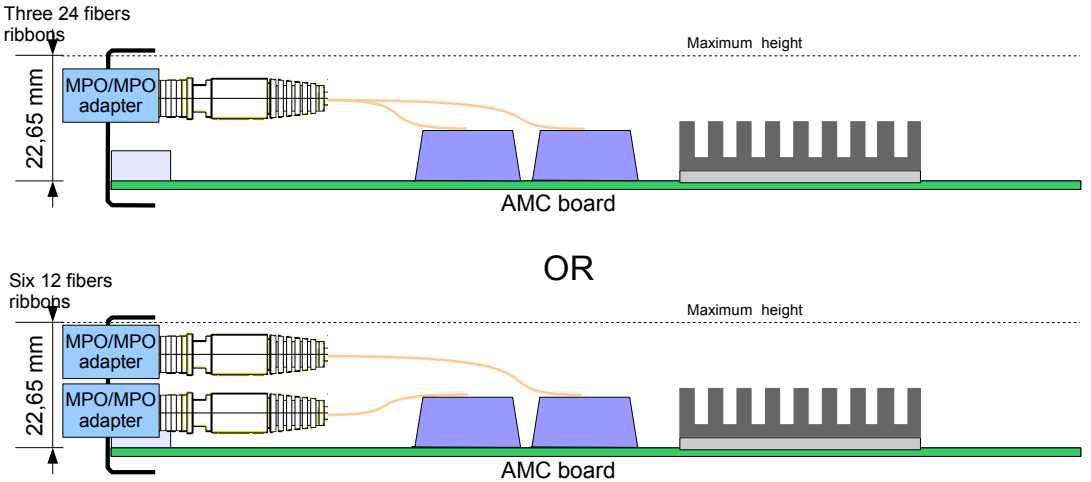
Full scale prototype

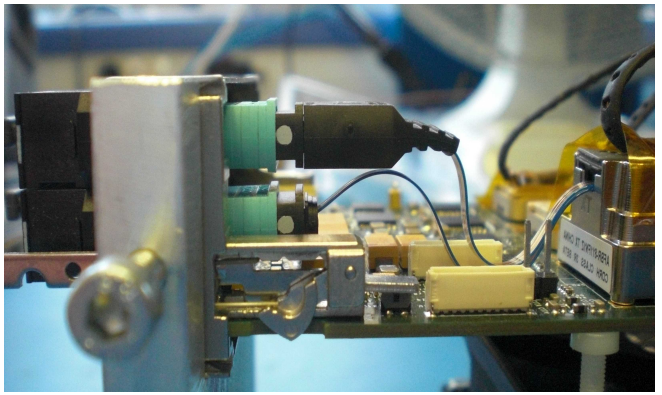
AMC40 first prototype

Front plate connectivity

Front plate



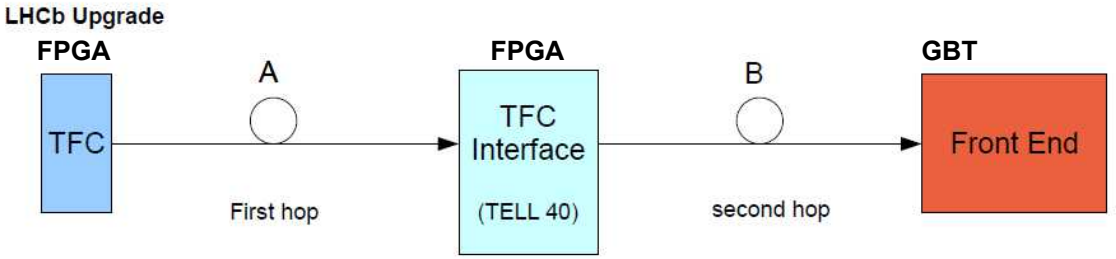




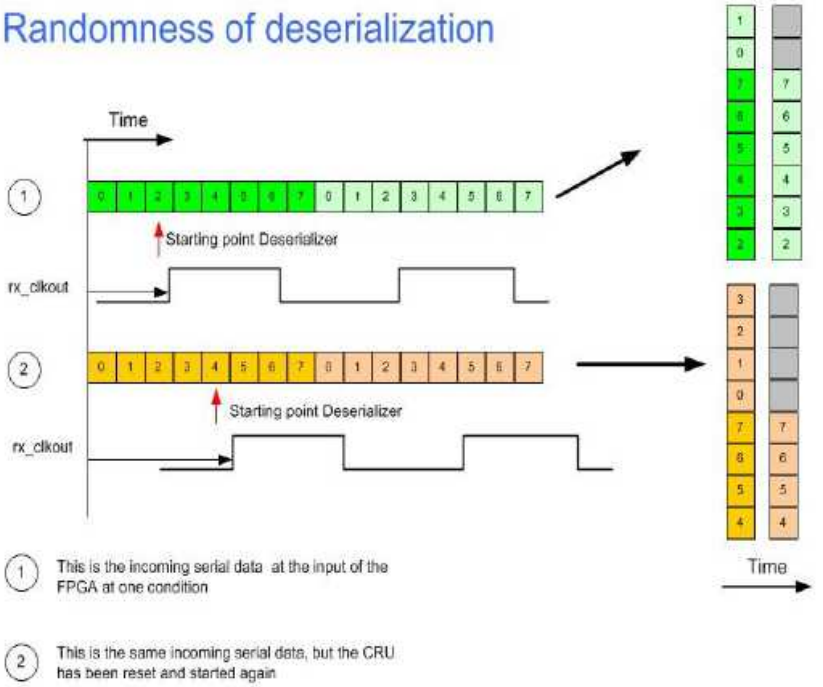
Measurements

Clock phase over serial links

Can we keep a fix clock phase over chained serial links when powering on and off the system ?



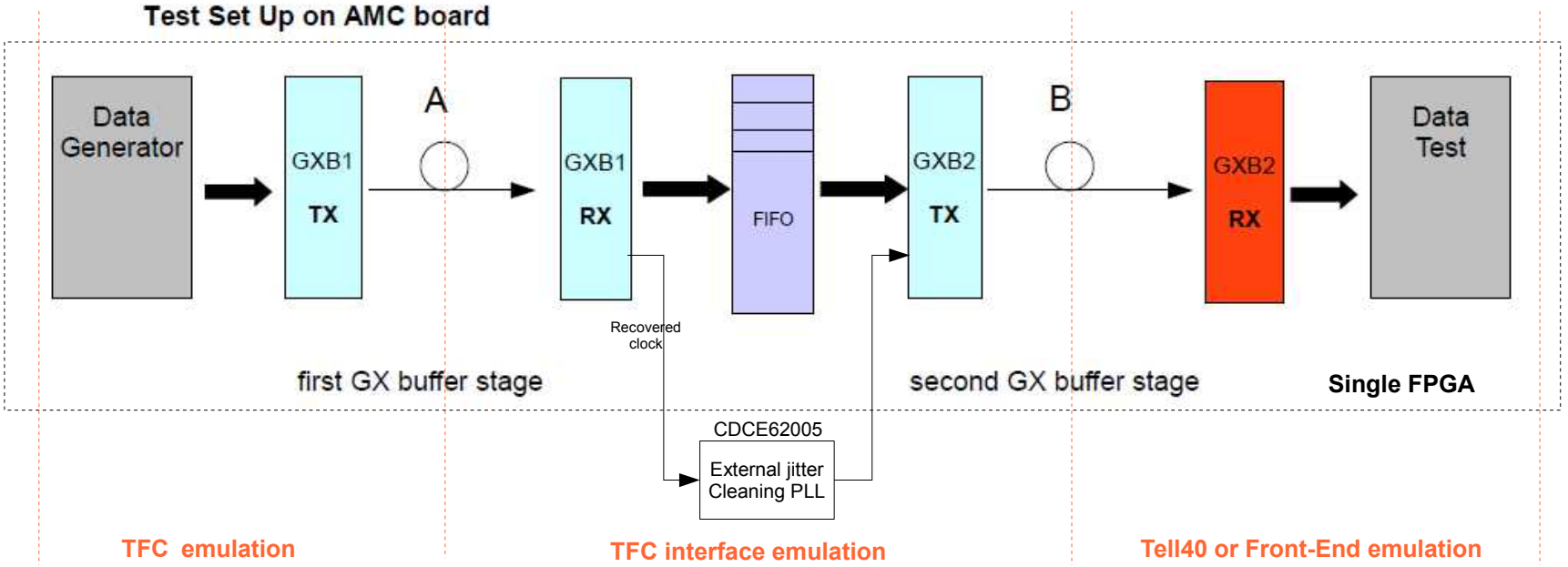
- Recovered clock phase is not constant in a FPGA deserializer



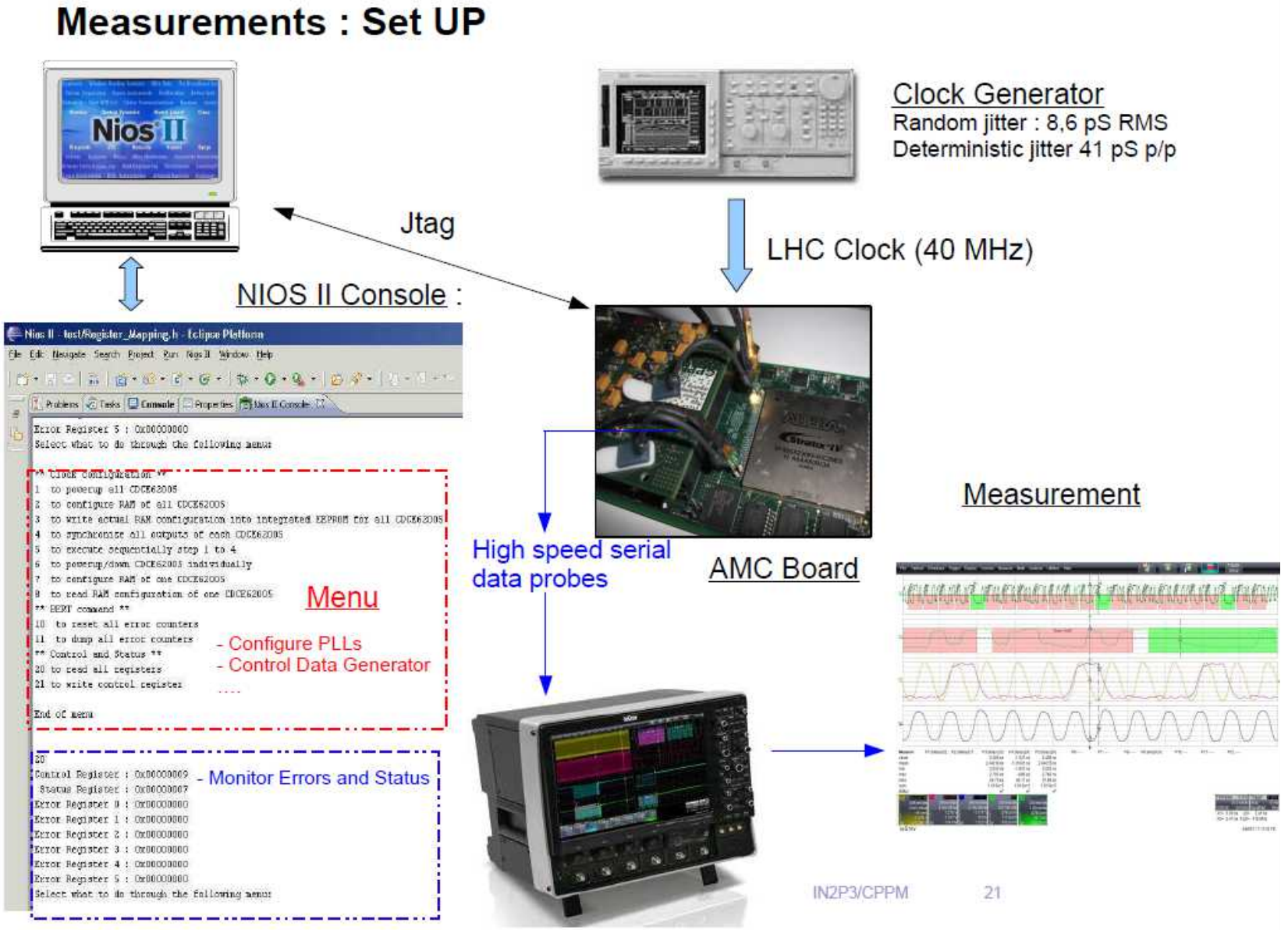
Methodology

Special mechanisms present in Stratix IV GX and V GX can be used

- Early tests made last year with Stratix IV GX
- Use of 8B10B code rather than GBT protocol to be able to detect the phase over a serial link
- Serial link speed : 2.4 Gbits/s
- Whole path emulated in a **single FPGA**



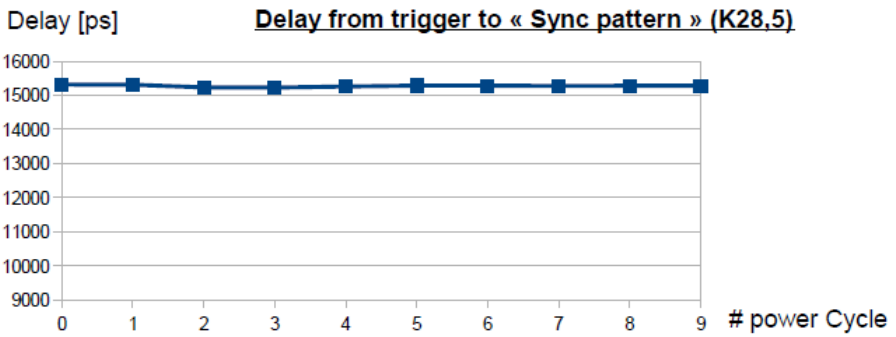
Test setup


Measurements : Set UP
Nios II
Clock Generator
Random jitter : 8,6 pS RMS
Deterministic jitter 41 pS p/p
Jtag
LHC Clock (40 MHz)
NIOS II Console :
Menu
- Configure PLLs
- Control Data Generator
- Monitor Errors and Status
High speed serial data probes
AMC Board
Measurement
IN2P3/CPPM 21

Results

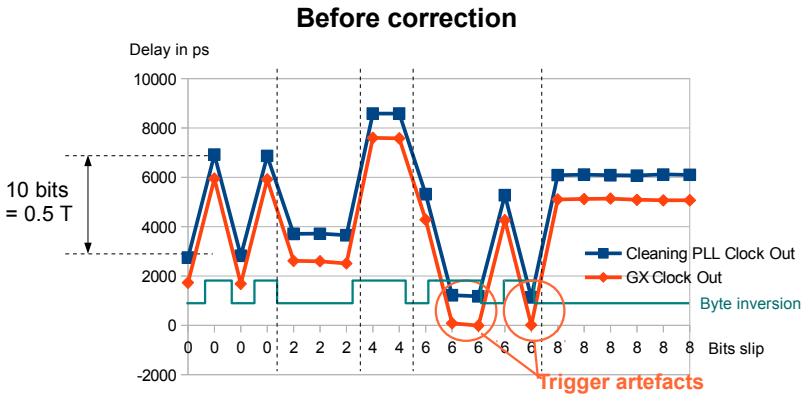
Phase of serial stream vs Tx_Clock

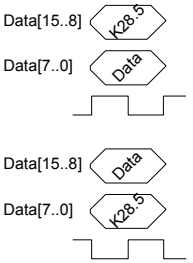
- Deterministic delay between clock and serial stream when powering on and off
- Phase variation: ± 50 ps

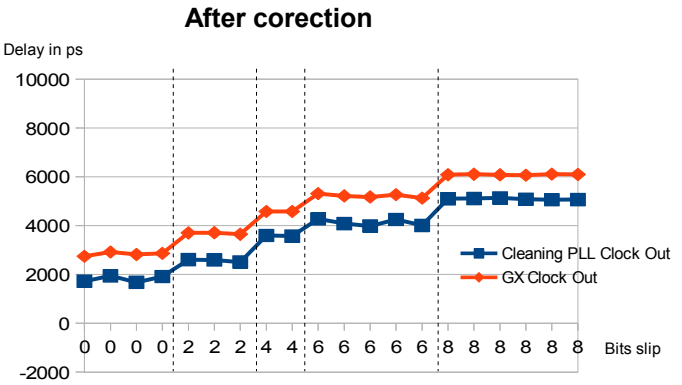


Phase of recovered clock vs Tx_Clock

- Delay = deterministic function of Bit slip out information from receiving GX + Control flags



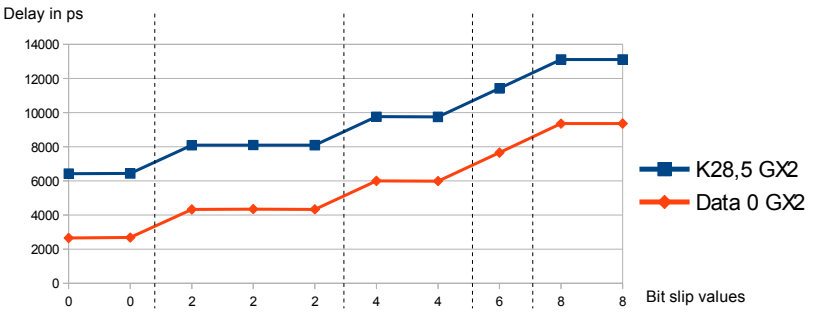




Locking the phase of two serial steams

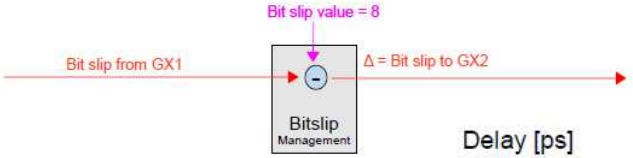
Phase of serial stream vs bit_slip_in

- Deterministic relationship

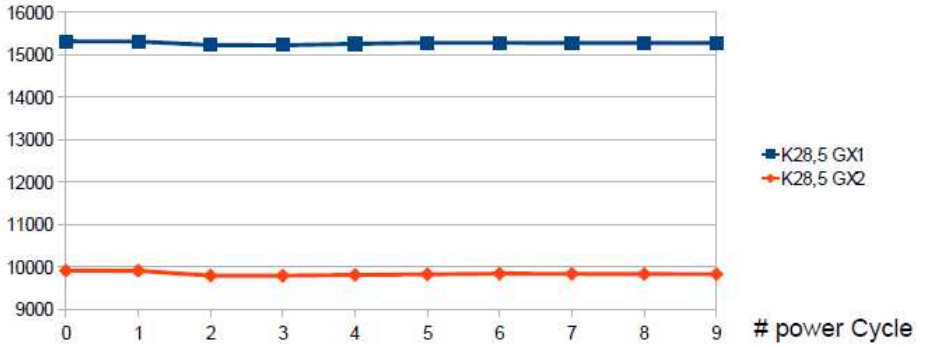


Phase of serial stream 2 vs serial stream 1

- With these two mechanisms, possibility to compensate before resending data



- Phase variation on second serial stream after compensation :
  ~ ± 50 ps RMS



Conclusion on constant phase

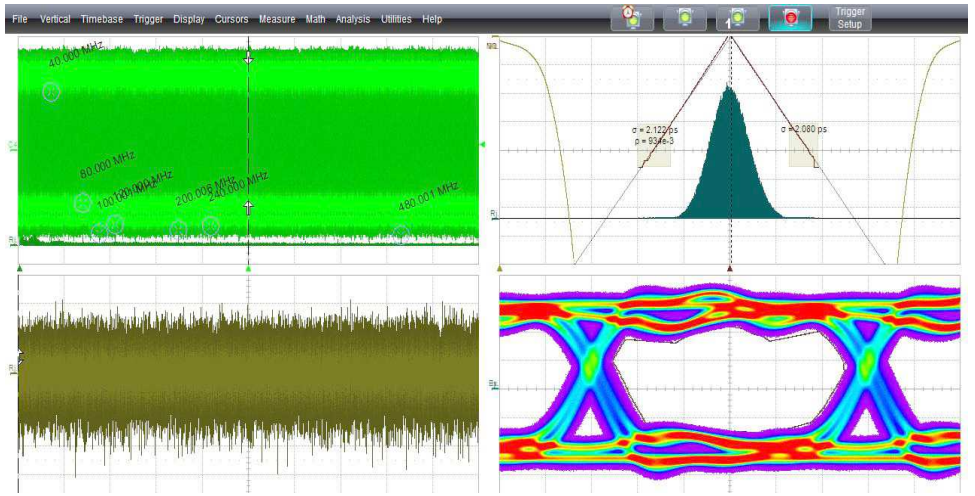
Prospective

- Preliminary results : need more statistics
- Port this design on Stratix V GX
- Measurements from chip to chip through backplane
- Implement equivalent mechanism on GBT protocol
  - Experimental on-going work on this topic by Federico Alessio and Richard Jacobsson (CERN)
    Use of a not interleaved GBT protocol at 2.4 Gbits/s

GBT links

Stratix V GX setup

- Data rate 4,8 Gbit/s
- GBT protocol
- External loopback :
  3 kinds of optical fibers used :
  - 10 meters OM3 optical fiber (laser optimized 50/125 µm)
  - 15 meters OM2 optical fiber (50/125 µm)
  - 90 meters OM1 optical fiber (62.5/125 µm)
- No significant deterioration of signal by optical link



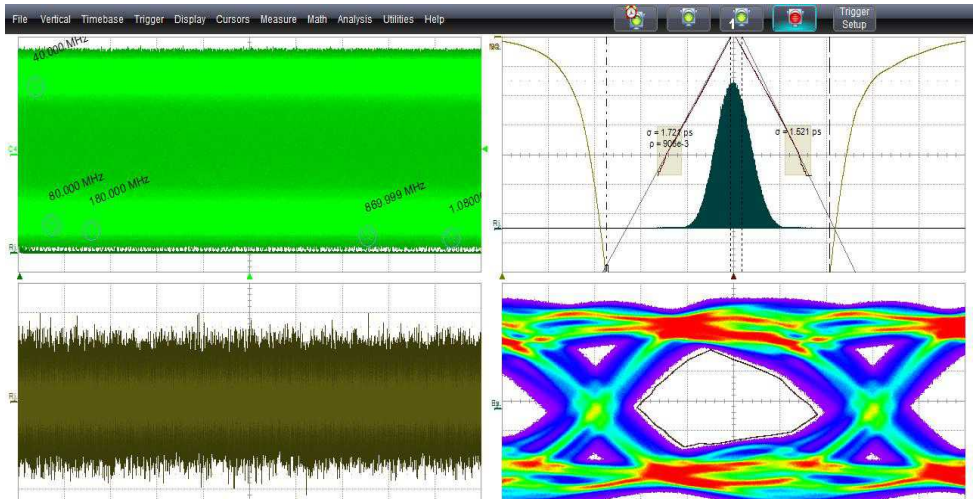
@4,8 Gbit/s :
Total Jitter ≈ 56 pS
Random Jitter ≈ 2,4 pS
Deterministic Jitter ≈ 24 pS
aperture : 0,65 UI@10^{-16}

BER better than 10^{-16} @.4.8 Gbits/s

10GbE links

Startix V GX setup

- Data rate 9.6 Gbit/s
- GBT protocol
- External loopback :
  10 meters OM3 multimode optical fiber



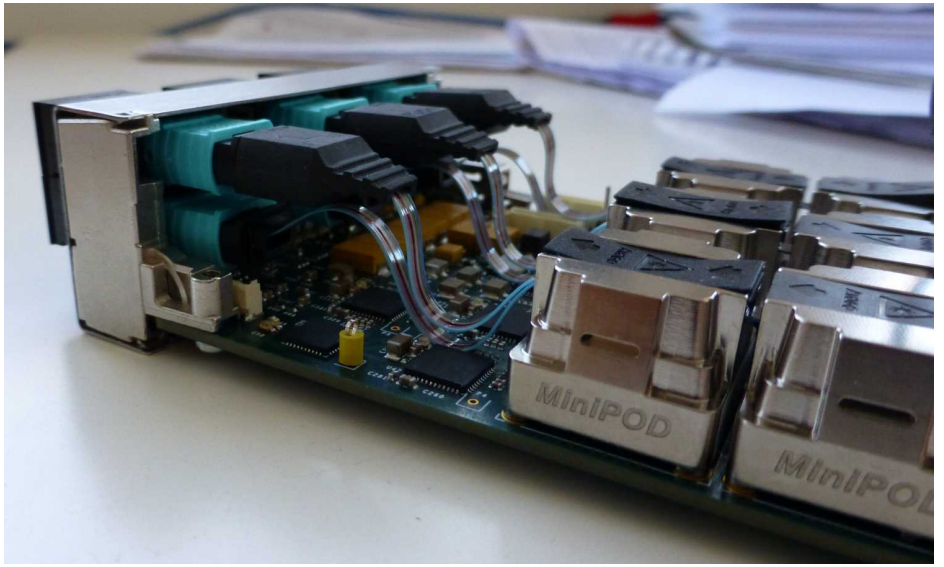
@9,6 Gbit/s :
Total Jitter *≈ 50 pS*
Random Jitter *≈ 1,3 pS*
Deterministic Jitter ≈ 31 pS
aperture : 0,48 UI@10^{-16}

BER better than 10^{-16} @.9.6 Gbits/s

Optical transceivers temperature

Setup

- No heatsink
  - Heat sink exists but too high: need to be tooled
- Measurements made with :
  - No cooling
  - Airflow cooling
- Operating speed : 4.8 Gbits/s and 9.6 Gbits/s



Cooling	Ambiant	Data rate	Rx	Tx
Natural convection	25°C	4.8 Gbits/s	41.5°C	42.5°C
		9.6 Gbits/s	44°C	48°C
With air cooling		4.8 Gbits/s	38°C	39.5°C
		9.6 Gbits/s	41°C	43°C

Minipod case temperature

→ Heatsink does not seem mandatory

Firmware development

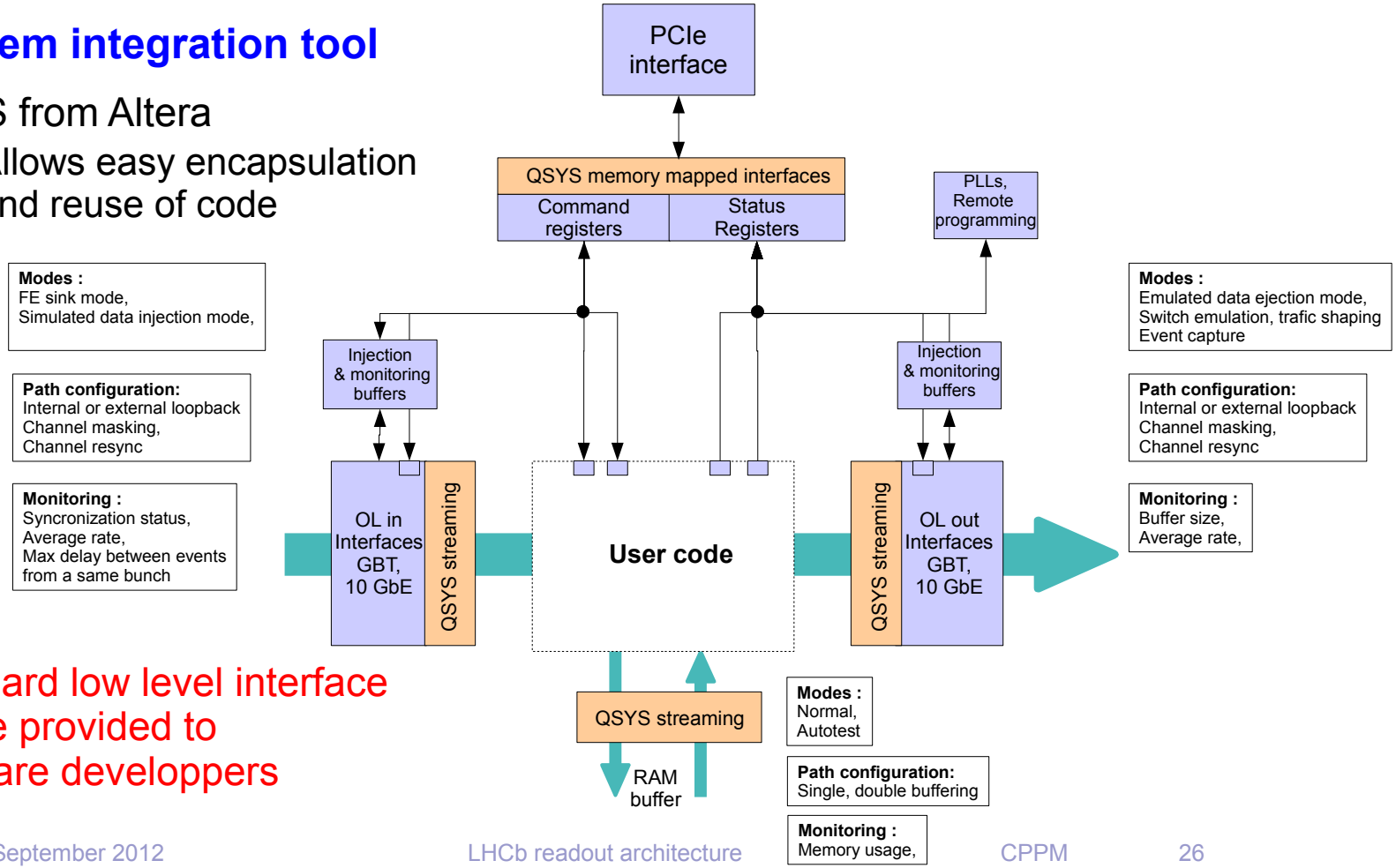
Firmware incremental methodology

Shared development in the Collaboration

- At least 11 firmwares to develop

Use of a system integration tool

- QSYS from Altera
  - Allows easy encapsulation and reuse of code



- Standard low level interface will be provided to firmware developpers

Conclusion

ATCA chosen by LHCb for implementing first version of the readout system

- Feasibility has to be demonstrated end 2012

Flexible architecture

- Single hardware, many firmwares
- Development spread in the collaboration

Encouraging early measurements

- Clock phase stability over serial link: ~ ± 50 ps RMS
- High speed BER < 10^{-16} at 9.6 Gbits/s
- Limited temperature for optical drivers without heatsink : ~ 48 °C

ATCA board soon to come

- Currently in routing phase