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Design of the ATLAS IBL Readout System

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Abstract

An Insertable B-Layer is planned for the upgrade of the ATLAS detector and will add a fourth and innermost pixel layer to the existing Pixel Detector. 12 million pixels attached to new FE-I4 readout ASICs will require new off-detector electronics which is currently realized with two VME-based boards: a Back Of Crate module implementing optical I/O functionality and a Readout Driver module for data processing. This paper illustrates the new readout chain, focusing on the design of the new Readout Driver Card, which, with a fourfold integration with respect to the previous design, builds up the detector data, controls the calibration procedures and interacts via Gigabit links with a novel calibration farm. Future prospects and back compatibility to the existing system are also addressed.

Keywords: ATLAS Insertable B-Layer, Data Acquisition, Readout Driver

1. Introduction

The ATLAS silicon Pixel Detector [1] is the innermost detector component of the ATLAS tracking system consisting of 3 barrel layers at average radii of 5 cm, 9 cm, and 12 cm from the beam line, and three disks on each side, between radii of 9 and 15 cm. It provides at least three space point measurements per track with high accuracy as needed for track and vertex determination. The layer closest to the beam pipe, the B-layer, is crucial for tracking, vertexing, and b-tagging capabilities of ATLAS especially at high

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luminosity. Due to the harsh radiation environment induced by the LHC, the detector performance will deteriorate with time with the B-layer being first one degrading in terms of efficiency with the increasing radiation damage. A new Insertable B-Layer (IBL)[2] is currently under development and will be installed along with a new smaller beampipe during the 2013 shutdown. The IBL, as the 4th innermost pixel layer will allow to keep and enhance the tracking performance despite effects arising from luminosity, hardware lifetime and radiation effects.

In this writeup we focus on the design and realization of the readout system of the IBL. The document is organized as follows. Section 2 briefly describes the readout system of the ATLAS Pixel Detector introducing the terminology and the main components. The new IBL front-end features are presented in Section 3 along with the implications and requirements to the readout system. In the later sections details on the new readout components, the improvements with respect to the previous version and new developments are described. These include also the procedures for calibration as described in Section 6. Finally, before concluding, an overview of the status of the art and an outlook are given in Section 7.

2. The Atlas Pixel Detector Readout

The ATLAS data acquisition system [3] is based on a three-level trigger, running at the LHC bunch crossing spacing of 25 ns and a level-1 trigger of up to 100 KHz. The readout of the Pixel Detector relies on the FE-I3 [4] front-end chip. Each FE-I3 contains 2880 readout cells of $50\mu m \times 400\mu m$ size arranged in an 18×160 matrix. A readout cell contains an analogue block where the sensor charge signal is amplified and compared to a programmable threshold by a discriminator. The digital readout part transfers, per double-column, the hit pixel address, a hit time stamp and a digitized amplitude information, the *time over threshold* (ToT), to buffers located at the periphery of the chip. Sixteen FE-I3 chips form a module and communicate with a *Module Controller Chip* (MCC) [5] using only digital signals. The readout chips receive a 40MHz clock signal, the level-1 trigger and a synchronization signal used to reset internal registers and transfer the hit data to the MCC. On the MCC the output data rate can be switched between 1×40, 2×40, 1×80 and 2×80 Mbit/s. Four pairs of copper cable establish the corresponding connections to an *optoboard* which serves as optical-electrical interface. Finally the fibers from the optoboards reach the dedicated off-detector electronics consisting of a Back Of Crate (BOC) and Read-Out Driver (ROD) cards which are hosted in VME [1] 64x 9U crates. The BOC carries the actual connections, i.e. the TX- and RX-plugins (respectively for clock, trigger, configuration data and event data for readout) and the S-Link [2] by means of which the level-1 accepted events are pushed by the ROD to the higher levels of the trigger and DAQ structure. The current ROD board hosts 11 Xilinx FPGAs [3] for data formatting, event fragment building and routing and 5 Texas Instruments Digital Signal Processors (DSP): one of them, the *Master DSP*, controls and coordinates the operations of the entire board, while the other 4, namely the *slave DSPs*, perform on-board event histogramming and fitting. The results of this computation are transferred to a *Single Board Computer* (SBC) via the VME bus. In the current readout system a BOC - ROD pair connects to up to 32 detector channels at 40 Mbit/s via optical links (or 8 channels at 160 Mbit/s). A schematic view of the components and the path described is shown in Fig. 1.

3. IBL Requirements and Readout Design

The existing Pixel Detector readout architecture has been designed for the nominal LHC peak luminosity of $10^{34} cm^{-2} s^{-1}$ and for an expected trigger rate of 100 kHz. For larger occupancies and luminosities, the bandwidth of the double-column bus in the FE-I3, sensitive to the occupancy, and the link from MCC to the off-detector electronics, sensitive to the occupancy and the trigger rate, start limiting the detector performance. The new front-end chip FE-I4[6] has been designed to overcome these limitations which for

[1] American National Standard for VME64, ANSI/VITA 1-1994.
[2] A general purpose high-speed optical interface specifically developed for LHC: `http://hsi.web.cern.ch/hsi/s-link/`
[3] Field Programmable Gate Array

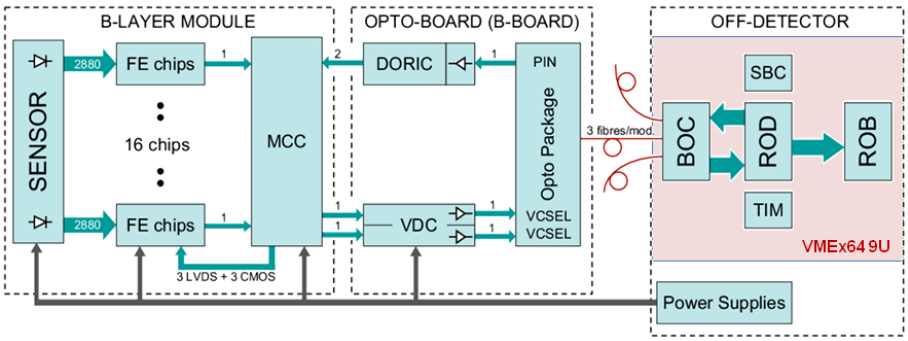

Fig. 1. Block scheme of the ATLAS Pixel Detector DAQ system from the front-end chip FE-I3 to the readout modules where full events are built and pushed to the higher trigger levels (ROB).

a detector located at 3.3 cm from the interaction point would be even more restrictive. Taking advantage of the new design several improvements including a smaller feature size, smaller pixel granularity, lower material budget leading to a simpler module design with no MCC. The FE-I4 has been added also with an 8b/10b encoding [7] before streaming out the data at 160 Mbit/s. This provides a data stream with proper engineering properties off-detector and should ease the clock reconstruction from the data stream in the off-detector system. Two FE-I4 chips form a detector module and are operated via a single clock and command line at 40MHz.

The use of the new FE-I4 requires multiple changes to the readout system for being operated. When specifying the design of the DAQ chain for the IBL, the first open question was whether the existing ROD could be sufficient or if a new one was needed. Although the existing ROD firmware could be modified to operate with the IBL module data format, the hardware of the board is designed to connect a maximum of eight 160 Mbit/s input links (from the modules) to one output S-Link, while, to respect the IBL natural modularity, sixteen 160 Mbit/s links to two S-Links have to be handled. This consideration, together with bandwidth limitation on the VME bus used in calibration runs and the obsolescence of the components, led to the decision of a new design. A look towards alternative standards was also considered; however, it was felt that a VME based architecture, possibly backward compatible with the BOC-ROD system (with modified firmware) in use in the ATLAS Pixel Detector and Strip Tracker would be more adequate. This choice would allow the IBL to be operated as part of the existing Pixel Detector making use of the same surrounding infrastructure (VME extended backplane, Single Board Computer operation, Clock, Trigger and Busy Handling). The BOC-ROD task subdivision would be kept as in the current readout chain, assigning the data path (optical link interface to the front-end chips and S-Links) to the BOC and the data processing and detector calibration to the ROD. The two boards would benefit from up-to-date programmable devices and technologies in order to increase the system performance and have a more compact size.

The block scheme of the new chain is shown in Fig. 2: while the BOC-ROD separation and the VME frame has been kept, the integration has increased by a factor 4. The whole IBL readout requires 14 BOC-ROD pairs hosted in a single 9U VME crate, where a TTC Interface Module (TIM) [8] distributes Clock and Trigger information to all the boards and handles their Busy and Errors conditions. Each BOC-ROD pair is able to readout data coming from 16 IBL modules for a total input bandwidth of 32×160 Mbit/s = 5.12 Gbit/s. The calibration tasks will no longer use the DSPs in favor of more powerful FPGA devices with an embedded hardware core and an external PC farm connected via Gbit links directly to the ROD. Below the new BOC and ROD systems are described more in detail.

4. The IBL Back of Crate Card (BOC)

The IBL BOC handles data from 32 FE-I4 chips. The BOC layout is segmented into two functionally equivalent sections. The core of each section is a Spartan-6 LX150T device. Receiving data from the

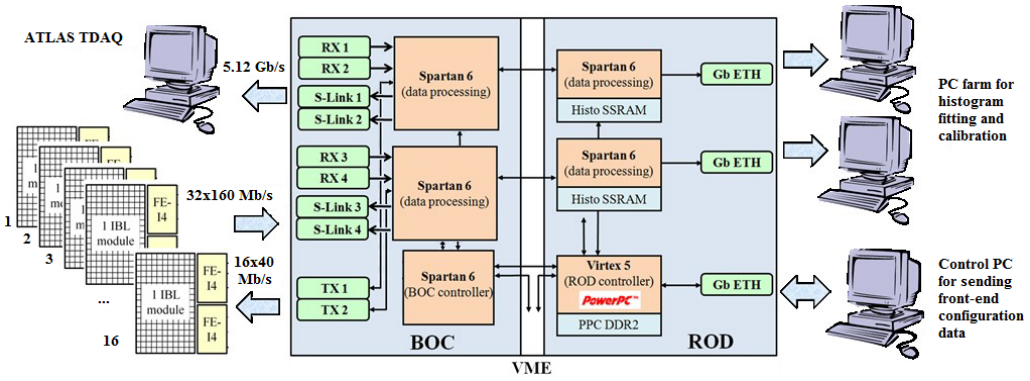

Fig. 2. Schematic view of the IBL readout system. From left to right the detector, the BOC, the ROD and the calibration farm. All detector and readout fibers are located at the back of the crate (BOC). New user-pluggable connections (GBit Ethernet) are on the front side (ROD). This configuration allows easy protection of critical connections within the crate by an interlocked door on the backside of the racks.

front-end is done via two commercial SNAP12 [4] RX modules while configuration data are sent either by a SNAP12 TX module or a TX plugin like the ones used on the current BOC. The Spartan-6 devices will replace all the functionality of the former custom made hardware (BPM encoding, synchronization, variable delays). The S-Link connection is established via Small Form-factor Pluggable [5] (SFP) transceivers. The configuration of the two Spartan-6 devices is handled by a third Spartan-6 (LX75T). As the IBL will return a balanced 8b/10b encoded stream at 160 Mbit/s per link, the new receiver circuitry can implement several advantages over the previous system:

- AC coupled receiver logic: due to the balanced encoding, the receiver circuitry can run AC coupled. It therefore delivers a bias free stream, automatically adapting to subtle changes in the data transmission line.
- Transition based code: regular transitions within the received stream allow to automatically synchronise the received data with a local clock, embedding standard synchronisation techniques into the BOCs central programmable device.
- Bytewise encoding: the receiver can be split into an 10b/8b decoder, delivering bytewise output and a formatting section, knowing the frontend data coding scheme. Therefore the individual logic blocks will get simpler in structure and easier to debug.

As for the detector link, the S-Link on the BOC will be implemented directly on the FPGAs and will support twin-channel operation to provide the data stream also to a *Fast Track Trigger* [9] when needed. In the BOC prototype one of the Spartan-6 connects to a single 1×4 SFP cage instrumented with 4 MGTs [6] while the second one connects to a quad opto-transceiver (QSFP[7]). The total data throughput (640 MByte/s) is 4 times larger than that of the existing BOC. For the interface to the ROD a so far unused connector (J0, 19×5 lines) was added and the data rate increased to 80 Mbit/s. New features are a Gbit Ethernet interface, 512MByte of DDR2 memory for each FPGA and an *Embedded Local Monitor Board* [10] to check temperatures and humidity.

[4] SNAP12: 12 Channel Pluggable Optical Module MSA, Rev. 1.1, May 15 (2002).
[5] Small Form-factor Pluggable
[6] Multi Gigabit Transceiver
[7] QSFP, Zarlink ZL60505MKDB

5. The IBL Readout Driver (ROD)

Built as a 14-layers 9U × 400 mm VME64x board, the ROD contains 4 FPGAs, 1 Texas Instruments DSP (for backward compatibility only), 3 Gbit Ethernet slots, one TTCrq [8]. A block diagram of the IBL ROD, with the main components listed, is shown in Fig. 3.

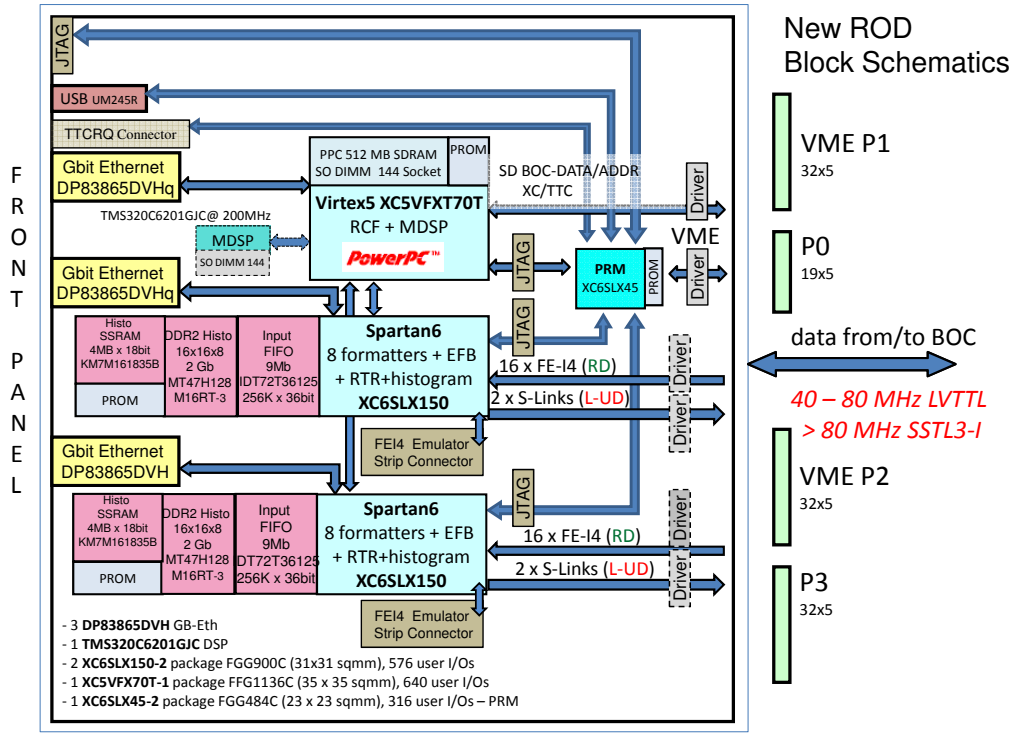

Fig. 3. New ROD block schematics. on the left side the front panel with 3 Gbit Ethernet, one TTCrq (for test beam running without the VME frame). On the rear size the VME backplane through which the communication to the TIM (Clock, Trigger, Busy etc), the BOC and the VME controller is performed.

The two Xilinx Spartan-6 XC6SLX150 are used for data gathering, event fragment building, and histogramming. For each of the two FPGAs a 2-Gbyte DDR2 chip (Mictor MT47H128M16RT-25E) and two 1Mx36 SSRAM chips (Cypress CY7C1370D-250AXC-ND) are available to store histograms and calibration data. With respect to the existing ROD the full data path is implemented in a single large FPGA in order to maximize the design flexibility and simplify the inter-communication between the components.

The core of the ROD is a Xilinx Virtex-5 XC5VFX70T which is used as ROD Controller. This FPGA also hosts, as an internal hardware core, a PowerPC which is in charge of system controls and non real-time functions, while the remaining FPGA logic performs all remaining real-time functions.

The PowerPC provides FE-I4 configuration to a command interface block using a serial port with data received from the VME host or from an external PC through a Gbit Ethernet connection, that can be used as a higher speed alternative to the VME bus. It also drives the calibration runs by providing software triggers through the same serial port and controlling that the data taking is working properly. The PowerPC core drives the setup buses used to read or control all the configuration registers on the ROD and BOC boards. A *bus arbiter block* controlled from VME decides whether the PowerPC is controlling the setup buses or if they are controlled by the VME host itself. The VME host is able to access the processor memory when needed in read/write mode. The PowerPC performance will be compared to the legacy Master DSP which might be left out in the final production.

[8] TTCrq: a mezzanine board containing a TTCrx and QPLL, developed by the CERN microelectronics group.

A further Xilinx Spartan-6 XC6SLX45 is used as *Program Reset Manager* device interfacing with the VME bus, the Master DSP and the ROD Controller. The data stream communication with the BOC is run at 40 or 80 MHz via CMOS drivers, i.e. twice the frequency of the existing system. A direct connection using SSTL-3[9] standard between ROD and BOC is considered as an option for higher speed.

Two main operating modes are foreseen. When run in *calibration* mode, the ROD is in charge of starting all procedures of detector initialization, clock and trigged generation, data gathering and event building, calibration and monitoring. All procedures as started as single commands or macros which involve operations on the detector front-end and on the BOC and ROD. When in *normal* data taking mode, clock and trigger signals are dispatched from the TIM and the ROD peforms all steps event driven.

Three Gbit Ethernet ports are available: one (connected to the PowerPC) allows the control from an external computer and receive front-end configuration data. The other two allow sending calibration histograms or event data to an external PC farm.

The presence of a TTCrq piggy back allows a third operating mode: with a dedicated firmware the ROD could be used as a standalone board outside of the VME frame with data formatted and shipped directly via Gbit ports to an external storage.

6. Calibration and Histogramming

As for the Pixel Detector, the calibration of the IBL detector is performed by repeating relatively short (100-1000) series of events, recorded while injecting a known charge into each pixel, and with different settings of the front-end parameters (e.g. different thresholds or different pre-amplifier feedback currents). This sequence, called calibration scan, generates a very large number of events, which have to be analyzed in order to extract the histogram showing how many times each pixel has registered a hit for a given setting. For this reason, in calibration mode, the data stream coming from the sensor is not sent over the S-Link, but pre-processed in the ROD, where the relevant histograms are produced. At the end of the scan, the histograms are transferred to an external farm via Gbit Ethernet for fitting and archiving. This approach promises a far better performance compared to the existing ROD. While on the existing ROD, the slave DSPs were used to build occupancy histograms which would then be transferred to the VME host computer, on the new system histograms and analysis on- ROD is proposed (see Fig. 4). The histogramming block receives the hits addresses and the ToT information. The new ROD executes the calibration loops to accumulate the per-pixel occupancies, sums of ToT and sums of $(\mathrm{ToT})^2$ parameters on the Spartan-6 FPGAs by using internal RAM and external SSRAM (Synchronous Static RAM) for data buffering. The histograms are eventually transferred via Gbit Ethernet as UDP packets to an off-line high-performance computer. First simulations support the novel approach which also overcomes the bottleneck of the VME bandwidth present in the existing ROD.

7. Present Status and Outlook

A testbed for the firmware of the IBL readout system has been setup for the BOC and the ROD. For the BOC the *Xilinx SP605 Evaluation Card* was used. All firmware blocks were adapted to the new hardware, loaded and simulated. For the ROD, the *Avnet Xilinx Virtex-5 FXT Evaluation Kit* was used to test the firmware blocks and to develop the new features like the Gbit Ethernet control interface and run a *linux* system onto the embedded PowerPC processor. So far results are very promising and no hiccups are expected.

Both BOC and ROD layouts were submitted in early summer and few instrumented boards are now available and being tested as shown in Fig. 5. Depending on the outcome of these tests a second pre-production or the final release will be submitted by end of 2011. A first front-end BOC-ROD integration in a complete test system is expected for Spring 2012.

[9] Stub Series Terminated Logic standard defined in EIA/JESD8-8 1996

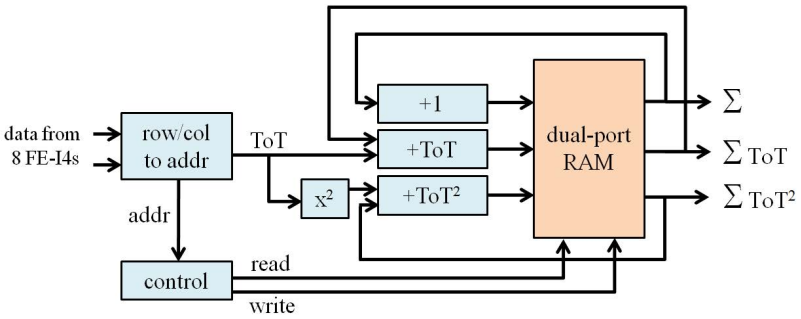

Fig. 4. Histogramming unit as implemented in the data path FPGA. Occupancy, ToT and $(\mathrm{ToT})^2$ histograms are produced requiring minimal resources. Data are stored in a dual-port memory and sent later to the external PC farm to for fits and extraction of the calibration constants.

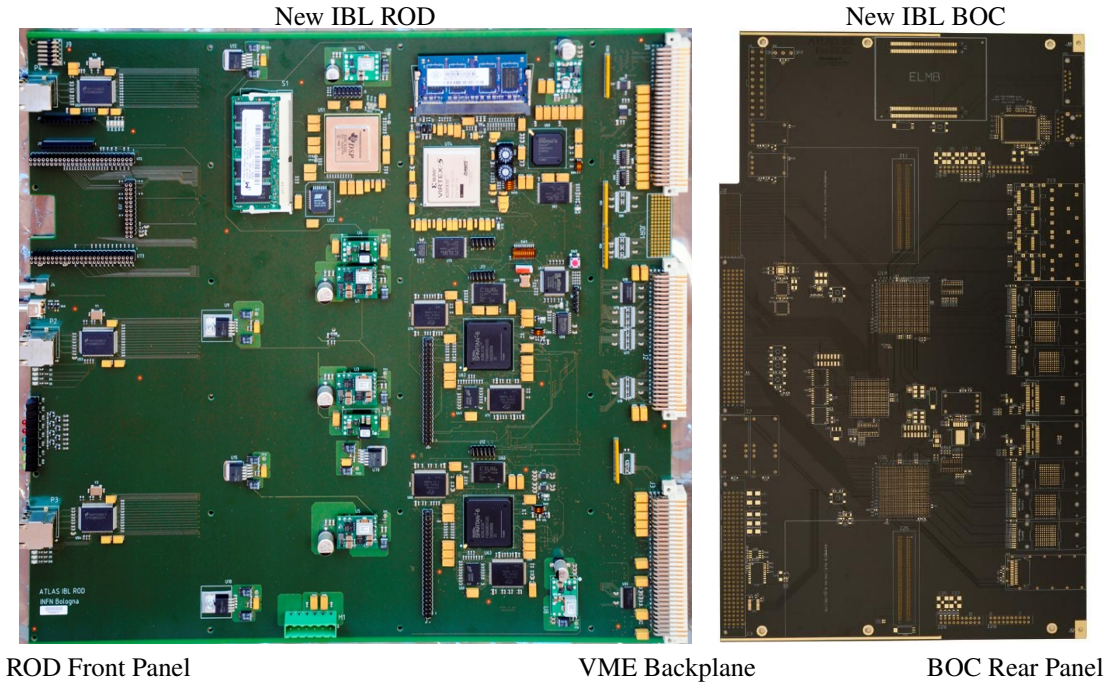

Fig. 5. Prototype Printed Circuit Boards of the new ROD (left) and BOC (right).

8. Conclusions

Despite the very tight schedule the IBL project is coming along well. The IBL will run after the shutdown planned for 2013 as part of the existing ATLAS Pixel Detector. The IBL readout provides an up-to-date version of the existing Pixel Detector system with important improvements and extensions: A fourfold integration along with a higher bandwidth allow to enclose the full IBL system in one single VME crate. The use of embedded hardware cores and an external processor farm provides a new concept for the detector calibration and standalone running. First prototypes of the final boards have been produced and are being tested in view of their integration in early 2012.

References

[1] The ATLAS Collaboration, "The ATLAS experiment at the Large Hadron Collider", JINST 3, **S08003** (2008).
[2] The ATLAS Collaboration, "ATLAS Insertable B-Layer Technical Design Report", CERN-LHCC-2010-013
[3] The ATLAS Collaboration, "ATLAS High-Level Trigger, Data Acquisition and Controls",CERN/LHCC/2003-022, Geneva, CERN, (2003)
[4] G. Aad *et al.*, "ATLAS Pixel Detector electronics and sensors", JINST 3, **P07007** (2008).
[5] R. Beccherle *et al.*,"The Module Controller Chip for the Atlas Pixel Detector", Nucl. Inst. and Meth. **A 492** (2002) 117-133
[6] M. Garcia-Sciveres, D. Arutinov, M. Barbero, *et al.*, "The FE-I4 pixel readout integrated circuit", Nucl. Instrum. Meth. **A636** (2011) 155-159.
[7] A. Widmer, P. Franaszek, "A DC-Balanced, Partitioned-Block, 8b/10b Transmission Code", IBM Journal of Research and Development **27** 440-451 (1983)
[8] J. Butterworth, J.B. Lane, M. Postranecky, M. Warren, "TTC Interface Module for ATLAS Read-Out Electronics", 10th Workshop on Electronics for LHC and Future Experiments LECC, 2004.
[9] A. Andreani *et al.* "Enhancement of the ATLAS trigger system with a hardware tracker finder FTK", JINST 5, bf C12037 (2010)
[10] B. Hallgren *et al.* "The Embedded Local Monitor Board (ELMB) in the LHC front-end I/O control system", in Proc. 7th Workshop on Electronics for the LHC Experiments, Stockholm, Sweden (2000)