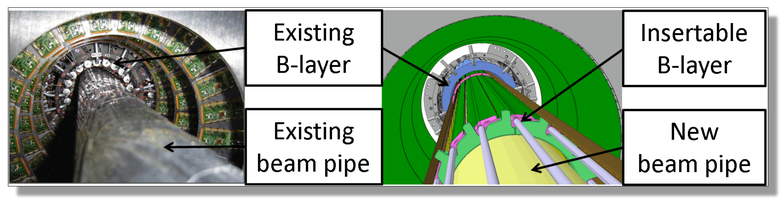
Characterization of new hybrid pixel module concepts for the ATLAS Insertable B-Layer upgrade

ATLAS IBL Upgrade

New Insertable B-Layer Upgrade installation planned for 2013 LHC shutdown.
→ Recover from eventual failures in present pixel system, esp. B-Layer.
→ Ensure excellent tracking, vertexing and b-tagging performance during LHC phase I.
→ Add to robustness of tracking with high luminosity pile-up.

Two sensor concepts under investigation.
→ Well known planar pixel sensor design (PPS).
→ New 3D silicon sensor technology (3D).

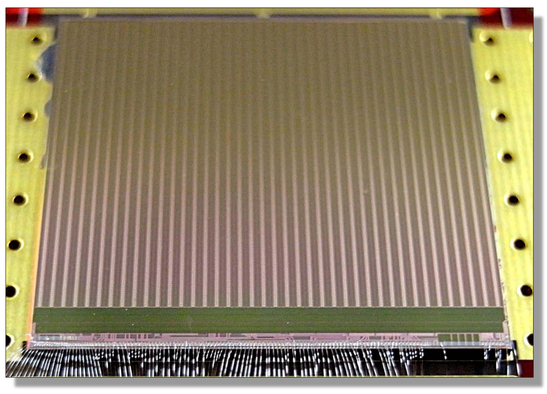


IBL design values: Peak luminosity 2-3x10^{34} $cm^{-2}s^{-1}$, integrated luminosity 700 fb^{-1}, fluence 5x10^{15} neq cm^{-2}, dose 250 MRad .

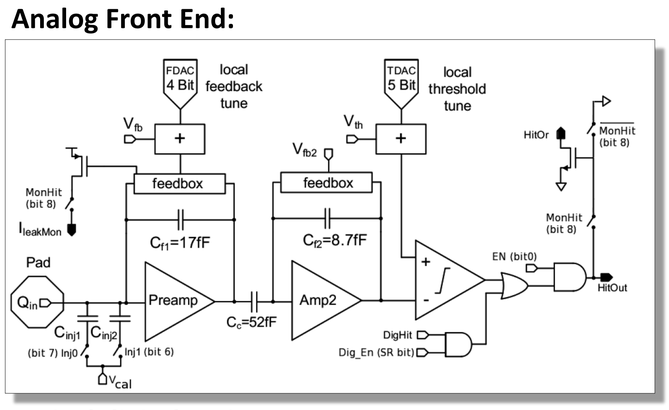
FE-I4 IC Architecture

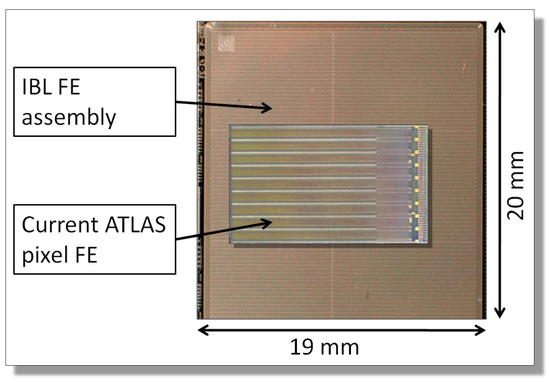
Technology:
CMOS 130 nm feature size process and thin gate oxide transistors for radiation hardness.

Geographical Design:
Large IC (20.2x18.8 mm^2) enables simplified module concept.
- Active area holding 80x336 pixels
- Periphery with ~2mm height
  → Active / Inactive area fraction is 90%.

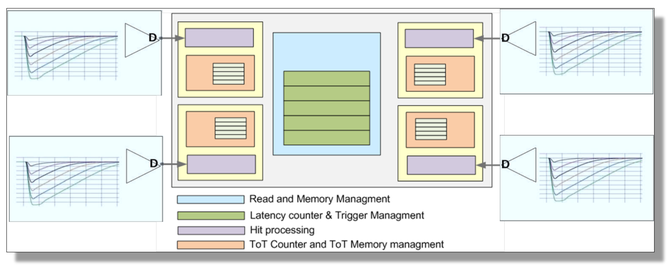


Analog Front End:





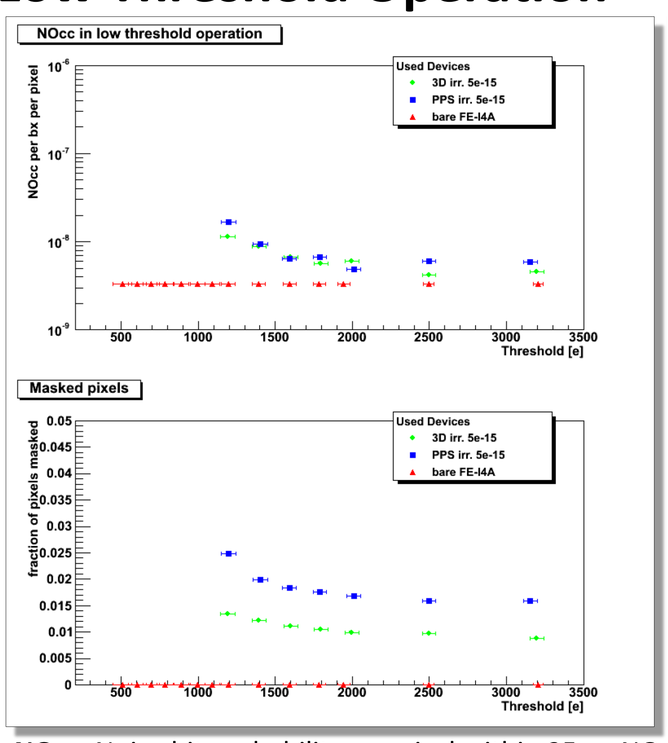
4-pixel digital region:
Transport of hits to periphery is the limiting factor for high hit occupancies in FE-I3.
New digital hit processing architecture developed for FE-I4:
- Hits stored on pixel level.
- Single LV1 counter for 4 analog pixels mirrors clustered nature of real hits.

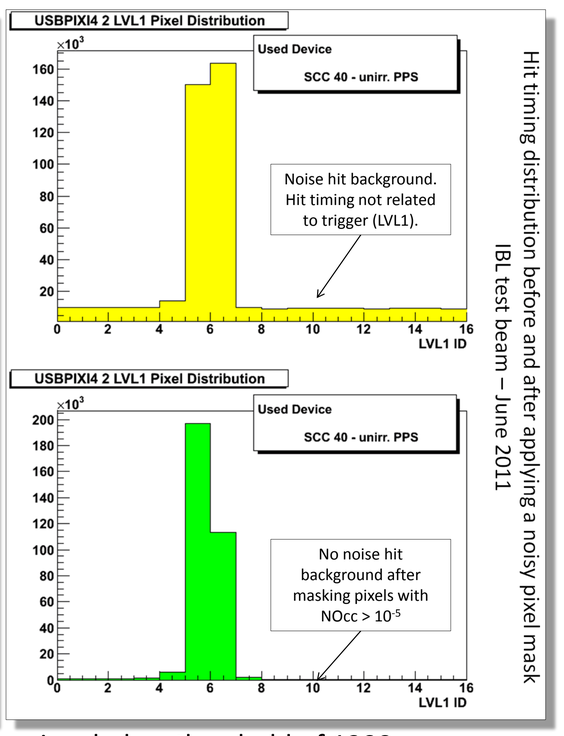


Pixel flavours:
Different flavours of the pixel cell has been implemeneted:
Another feedback capacitor in 19 out of 80 columns, low power discriminator in 2 columns and 15 columns with SEU hard pixel memory cells.

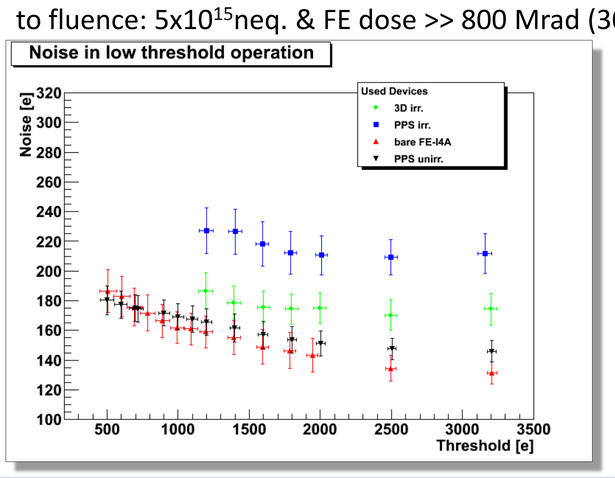
FE-I4A: First full scale prototype chip with this architecture.
→ FE-I4B will be the experiment chip for IBL.

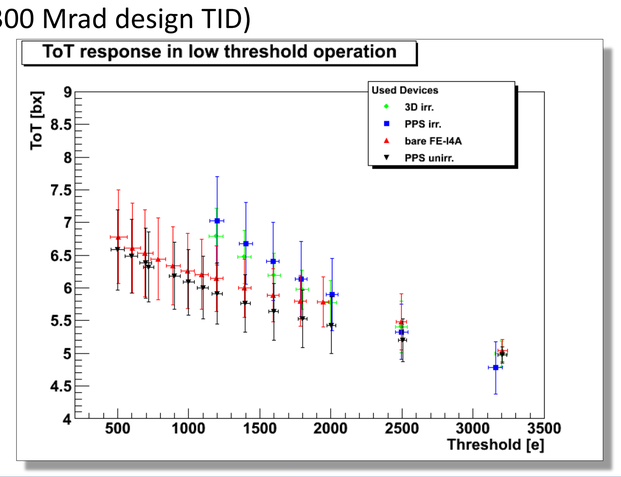
Low Threshold Operation



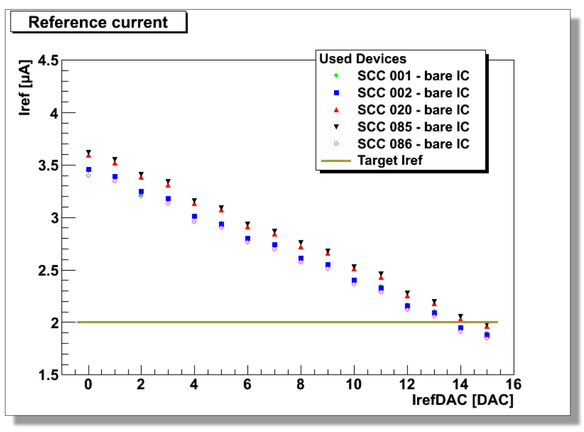


NOcc: Noise hit probability per pixel within 25ns; NOcc rises below threshold of 1200e.
1-2% dead pixel fraction independent from sensor technology seen in electronic devices irradiated to fluence: 5x10^{15}neq. & FE dose >> 800 Mrad (300 Mrad design TID)

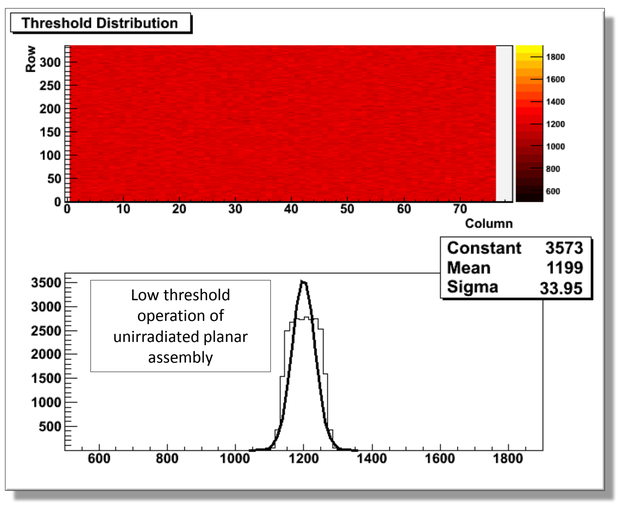


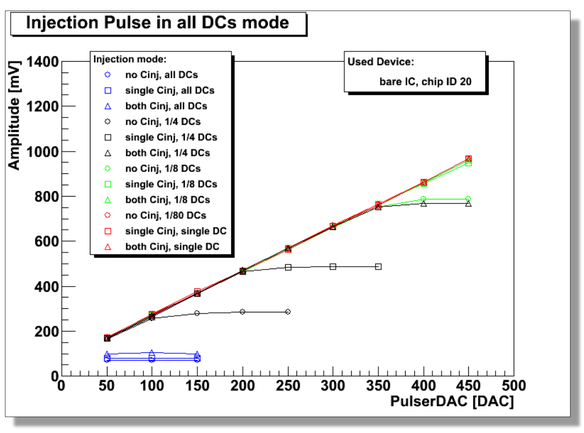


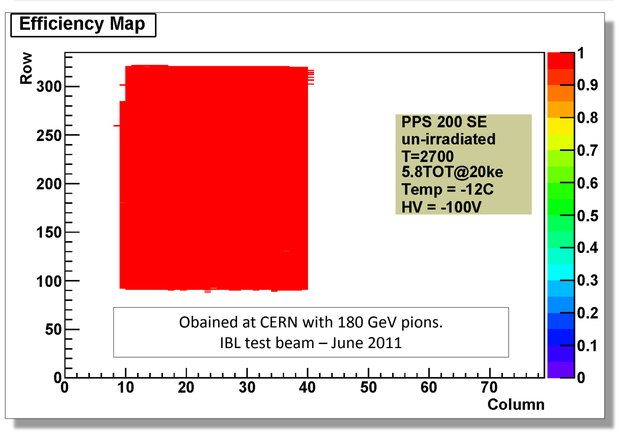
IC and Module Performance



- Reference current DAC needs to be adjusted on every chip to design value of Iref = 2 µA.
- DAC setting can be burned to EFUSE register.
- 2µA Iref on edge of dynamic DAC range.
  → Dynamic DAC range will centered in FE-I4B.



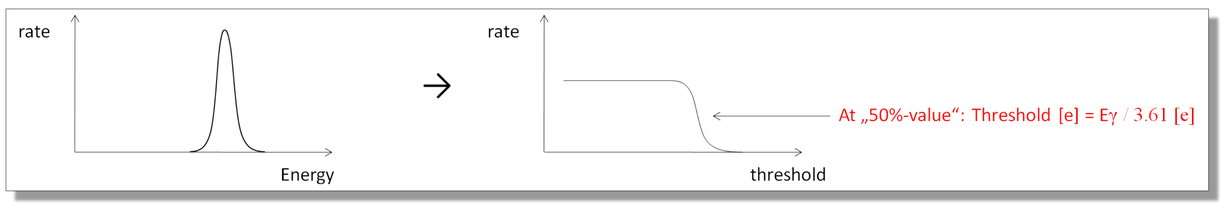




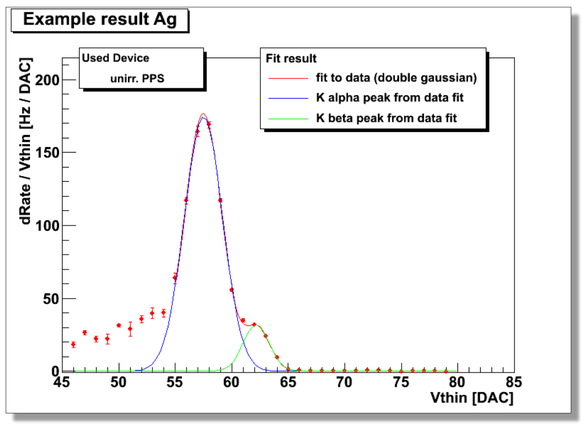
Saturation of pulse amplitude. Reason known and will be fixed in FE-I4B.
Pulse injection possible in 1/8 and single DC mode.
→ decreases scan speed.

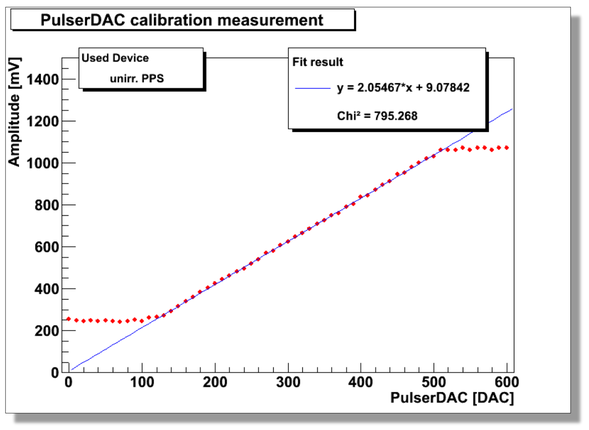
FE-I4A based prototype modules successfully operated at thresholds ~1600 electrons in IBL test beam conditions (IBL test beam – June 2011)

Calibration of the FE-I4



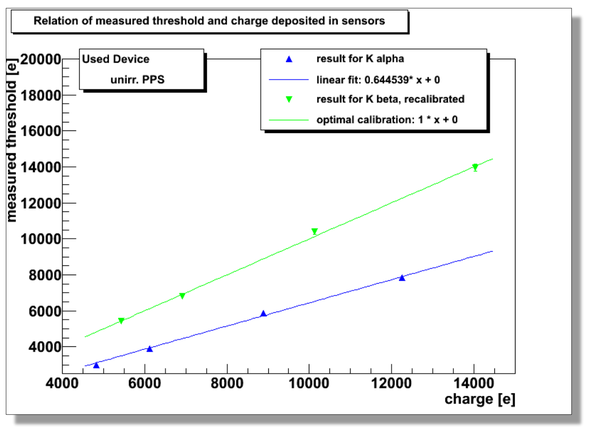
Get known spectra without using analog hit information (ToT) - calibration constant dependent.
→ Measure rate and change threshold DAC, measure threshold at peak DAC position.
→ Calculate injection capacitance.





Result:
- C_{inj} = 6.7 fF, 1.13 times larger then simulated (5.7 fF)
- Expected uncertainty of order 10%.
- Independent measurement confirmed this result.

→ Absolut discriminator threshold is known with 10% accuracy.



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9th International Conference on POSITION SENSITIVE DETECTORS, September 11 – 16, 2011 in Aberystwyth, UK

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