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Second generation monolithic full-depletion radiation sensor with integrated CMOS circuitry

J. D. Segal, C. J. Kenney, S.I. Parker, C. H. Aw, W. J. Snoeys, B. Wooley, J. D. Plummer

***Abstract*–A second-generation monolithic silicon radiation sensor has been built and characterized. This pixel detector has CMOS circuitry fabricated directly in the high-resistivity float-zone substrate. The bulk is fully depleted from bias applied to the backside diode. Within the array, PMOS pixel circuitry forms the first stage amplifiers. Full CMOS circuitry implementing further amplification as well as column and row logic is located in the periphery of the pixel array. This allows a sparse-field readout scheme where only pixels with signals above a certain threshold are readout. We describe the fabrication process, circuit design, system performance, and results of gamma-ray radiation tests.**

I. Introduction

Integrated monolithic silicon pixel detectors for particle physics and x-ray applications have several advantages, including low collection electrode capacitance and good spatial resolution. Previously, Snoeys reported on the first generation monolithic bulk pixel detector [1], and beam test results were reported in [2]. In this paper, we report results for the second generation sensor, with increased area and resolution, improved yield, and a more sophisticated circuit taking advantage of the integrated CMOS capabilities.

A. Sensor Structure Overview

Fig. 1 illustrates some of the key features of our detector. We start with 300 m thick high-resistivity p-type silicon wafers. During operation, the bulk is fully depleted from an n-diffusion on the backside. Within the pixel array, each pixel consists of a small p+ collection electrode surrounded by an n-well containing PMOS pre-amplifier circuitry. Full CMOS row and column circuitry and control logic are outside the array. The n-wells and p-wells containing the CMOS devices are implanted directly into the bulk silicon, which also supports the PIN diodes.

B. High Voltage termination structure

This structure requires double-sided processing, which is challenging because the backside of the wafer is placed on a variety of surfaces that can result in scratches and other mechanical damage. To reduce this risk, a simpler and more robust high voltage terminations structure was developed

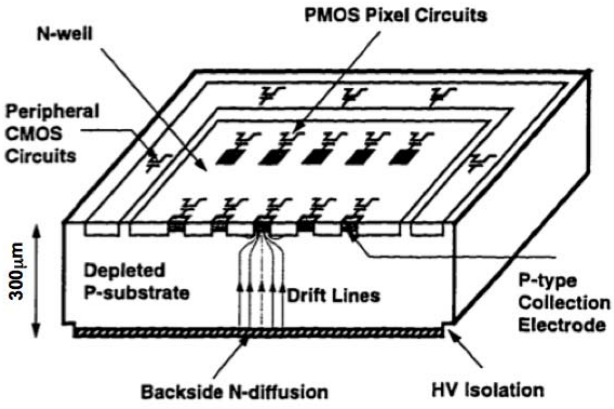

Fig. 1. Schematic illustration of the integrated sensor structure

using a vertical etch to define the edge of the backside diode

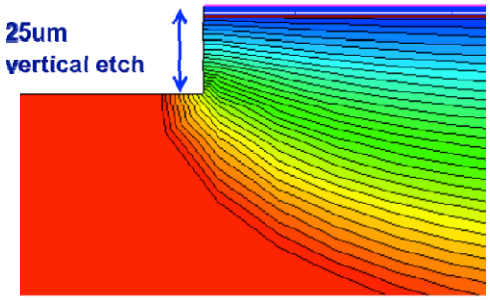

Fig. 2. Simulated equipotential contours for the vertical high voltage termination structure

[3]. The structure is illustrated in Fig. 2, which shows simulated equipotentials under bias. The vertical cut eliminates the curvature at the edge of the diffused diode that causes enhanced electric fields. After the vertical etch, the vertical plane must be passivated by subsequent thermal oxidation to prevent surface leakage, and in the case of p-type silicon, implanted with a boron surface implant.

This structure requires only one backside mask instead of three needed for the floating ring termination structure used in the previous generation [1]. The front side of the wafer, with more complex patterns and smaller geometries, is therefore subject to less damage, resulting in improved yield. Furthermore, this simplified backside structure is more robust itself, resulting in reduced yield loss from high-voltage diode shorts [3].

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	MASK#	PROCESS STEP	PARAMETERS
1		starting material	<100> p-type 12K-ohm wafers
2		initial oxidation	1hr 1000C wet
3		backside initial oxide strip	wet etch
4		backside n-implant	phosphorus 100keV 2E14/cm2
5		initial oxidation #2	1hr 1000C wet
6	MASK 1	N-well mask (topside) and etch	wet etch
7		N-well implant	phosphorus 100keV 2.5E12/cm2
8	MASK 2	P-well mask (topside) and etch	wet etch
9		P-well implant	boron 100keV 3E12/cm2
10		Well drive	30min 1000C wet, 16hrs 1150C inert
11		topside oxdie strip	wet etch
12		thin buffer oxidation	42min 950C dry
13		nitride deposition	800A front and back
14	MASK 3	field oxide mask and nitride etch	dry etch
15	MASK 4	field implant mask	boron 100keV 3E13/cm2
16		field oxidation	3hr 10min 1000C wet
17		nitride strip	wet etch
18		buffer oxide strip	short wet etch (leave field oxide)
19		thin clean-up oxide	14.5min 850C wet
20	MASK 5	NMOS threshold adjust implant	boron 35keV 1e12/cm2
21	MASK 6	PMOS threshold adjust implant	arsenic 80keV 1e12
22		thin oxide strip	short wet etch (leave field oxide)
23		gate oxidation	14.5min 850C wet
24	MASK 7	buried contact mask and etch	short wet etch
25		backside oxide strip	wet etch
26		polysilicon deposition	1500A front and back
27		nitride deposition	300A front and back
28		backside n+ implant	phosphorus 100keV 1E16/cm2
29	MASK 8	backside diode mask and etch	25um dry etch
30		smoothing trench oxidation	10min 1000C wet
31		backside oxide strip	wet etch
32		backside trench passivation	10min 1000C wet
33		backside field implant	boron 100keV 6E11/cm2 at 15deg, implant 4X, once from each direction
34	MASK 9	polysilicon mask and etch	dry etch through nitride and poly
35		polysilicon sidewall oxidation	6min 850C wet
36	MASK 10	n+ implant	arsenic 80keV 1e16
37		anneal/getter 1	30min 1000C inert
38	MASK 11	p+ implant	boron 15keV 2e15/cm2
39		anneal/getter 2	35min 900C inert
40		nitride strip	wet etch, front and back
41		selective tungsten deposition	front and back
42		LTO deposition	5000A oxide, front and back
43	MASK 12	contact mask and etch	dry etch
44		backside LTO removal	dry etch, leave trench passivation
45		metal 1 deposition	5000A Al/Si
46	MASK 13	metal 1 mask and etch	dry etch
47		LTO deposition	2000A undoped oxide + 5500 doped
48	MASK 14	via mask and etch	dry etch through nitride and poly
49		metal 2 depostion	1um Al
50	MASK 15	metal 2 mask and etch	dry etch

Fig. 3. Sensor process flow details

II. Sensor Process

The starting material is high resistivity float-zone p-type silicon. Twin wells are implanted and diffused directly into the bulk to support a 2 m CMOS process with double-layer metal interconnects. The process includes 15 masking steps, including one backside mask.

The backside mask (Mask #8) defines a 25 m vertical etch used to terminate the high-voltage junction. After the backside etch step, sacrificial oxidation is performed to smooth and clean the etched surface, followed by a second oxidation to passivate the surface. A shallow boron implant into the vertical surface is also required, and must be performed four times, once from each direction, to implant the four vertical faces.

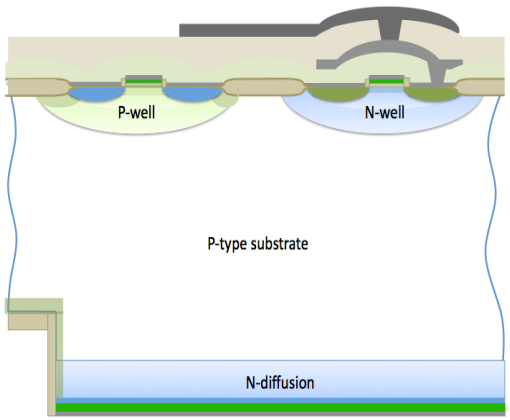

Fig. 4. Cross section of integrated sensor process

After the backside diode process is mostly completed, the backside surface, which comes into contact with equipment, is covered with either nitride or tungsten to prevent mechanical damage during subsequent processing.

Full details of the process are listed in Fig. 3. The final cross-section is illustrated in Fig 4. All processing was done at the Stanford Nanofabrication Facility (SNF).

A. Bulk Leakage Results

Backside leakage for the 29mm^2 sensor ranged from 10nA to 1 A. This measurement includes the diode perimeter current that constitutes the majority of the leakage current and does not affect sensor performance because it is collected by a guard ring. Leakage in the pixel array only, not including perimeter leakage, was estimated to be approximately 150nA/cm^3, corresponding to a lifetime of 15ms.

B. High Voltage Diode Results

Full depletion occurred at 40V to 55V applied to the backside diode. The backside diode is subject to mechanical damage during processing and high electric fields under bias. Nevertheless, the yield loss from backside diode shorts was less than 8% (0/12 detectors fail).

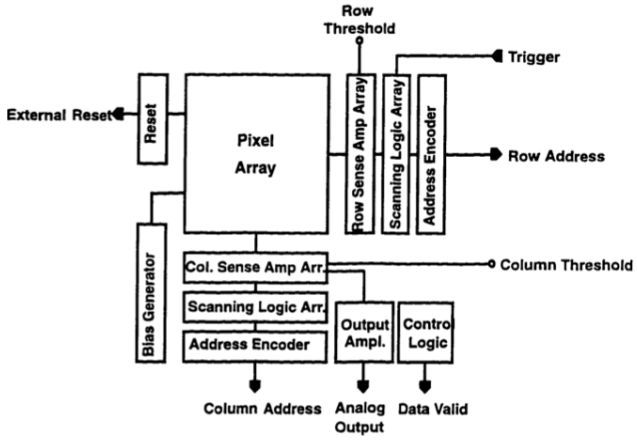

Fig. 5. Sensor Circuit Architecture

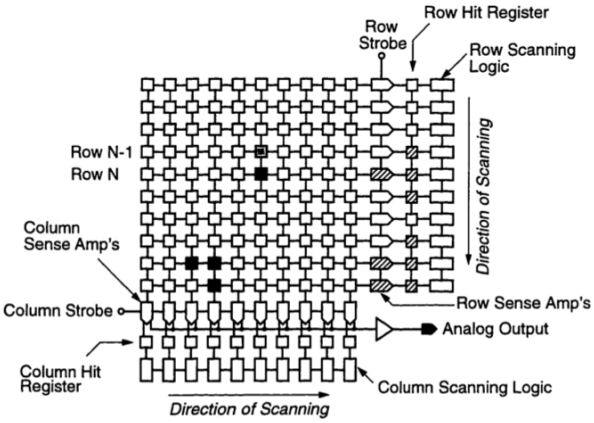

Fig. 6. Sparse-field readout

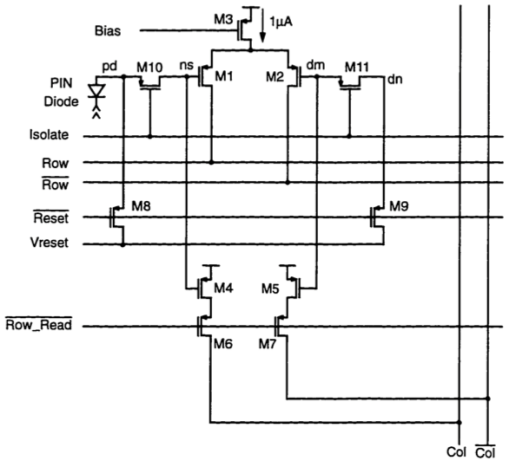

Fig. 7. Pixel Circuit

III. CIRCUIT

The circuit architecture is shown in Fig. 5 [4]. The array contains 32 by 32 pixels.

Sparse-field read-out operation is illustrated in figure 6. When the detector is externally triggered for read-out, the row scanning logic scans the rows to determine which ones have been hit, and activates those rows. The column scanning logic then scans the active rows to determine which pixels on those rows have been hit, and reads out their analog pulse heights.

PMOS pixel circuitry provides the first stage amplification of the signal. Each pixel is 65 m by 67 m. A schematic of the pixel circuit is shown in Fig. 7.

A. Circuit test results

Noise measurements are shown in Fig. 8, with a standard deviation of 1.6keV. Since a minimum ionizing particle traversing 300 m of silicon deposits 86keV (most probable value), the signal-to-noise ratio would be 54:1 for a particle physics application.

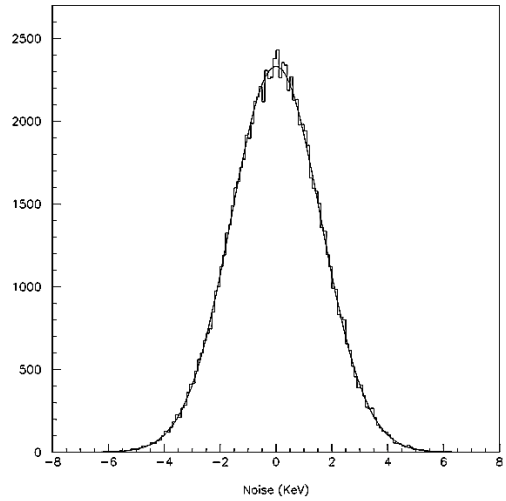

Fig. 8. Measured pixel noise with σ=1.6keV

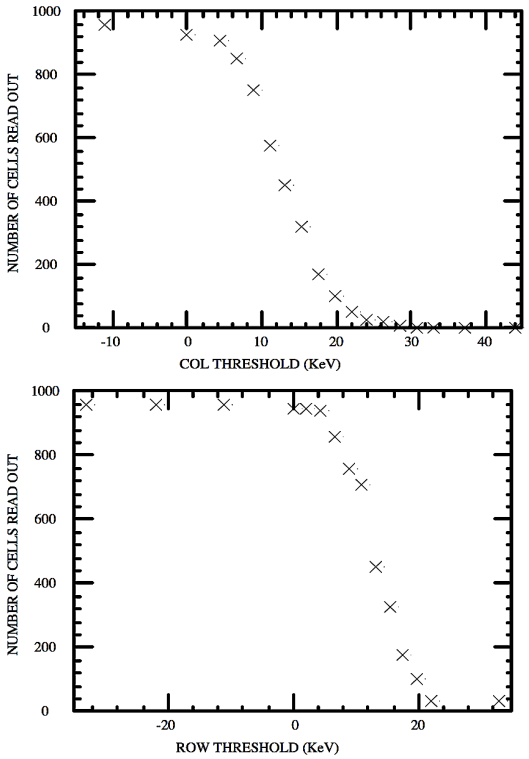

Fig. 9. Row and column threshold distributions

The row and column thresholds are shown in Fig. 9. Comparing the threshold spread to the signal from a minimum ionizing particle gives a measure of the efficiency of the detector in sparse field mode, or the chance that a real event will trigger the read-out. The worst case, or smallest, pixel signal for a minimum ionizing particle is 21keV, assuming that the charge is divided between four pixels. Both the row and column threshold spread, at 16keV and 20keV respectively, are low enough to expect close to 100% efficiency.

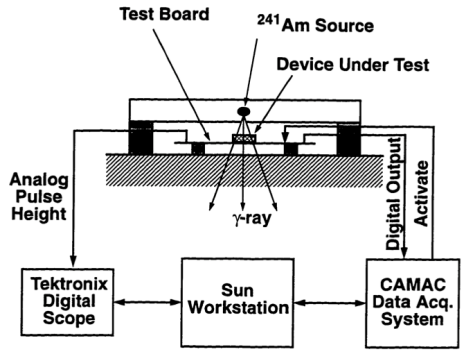

Fig. 10. Test set-up for γ-ray radiation tests

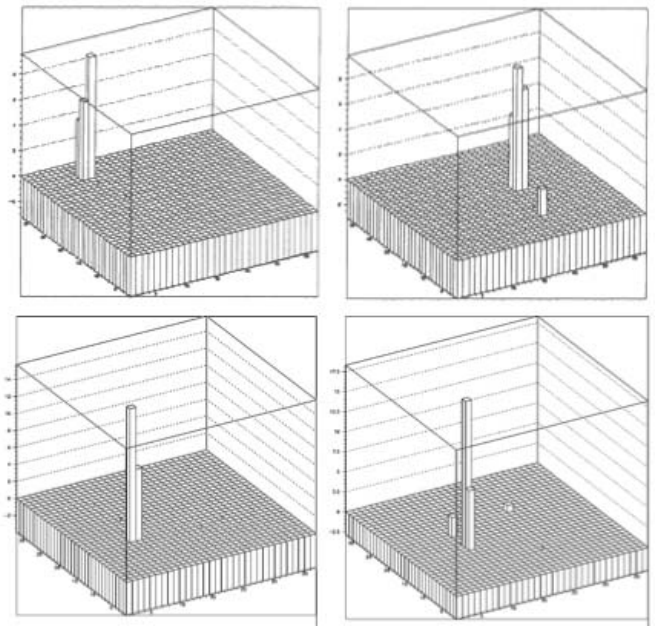

Fig. 11. Examples of single event γ-ray read-outs in sparse field mode

IV. Radiation Tests

Fig. 10 shows the set-up for testing the detector with γ-rays from a ^{241}Am source, which has a peak at 59keV. Fig. 11 shows several examples of single event read-outs in sparse field mode. Figs. 12 and 13 show the spectrum measured from the ^{241}Am source in non-sparse mode and sparse-field mode respectively. The energy reported on the plot is the sum of a cluster of pixels. In non-sparse mode, the peak is close to 59keV as expected. The sparse-field data shows a peak at 45keV instead of 59keV. This is probably because those pixels that received only a small share of the charge did not reach the triggering threshold of the sparse field readout, so the total energy recorded was less that the total deposited by the γ-ray. This performance may meet the requirements of an imaging application, but if not it could be corrected by automatically reading out the pixels adjacent those that trigger.

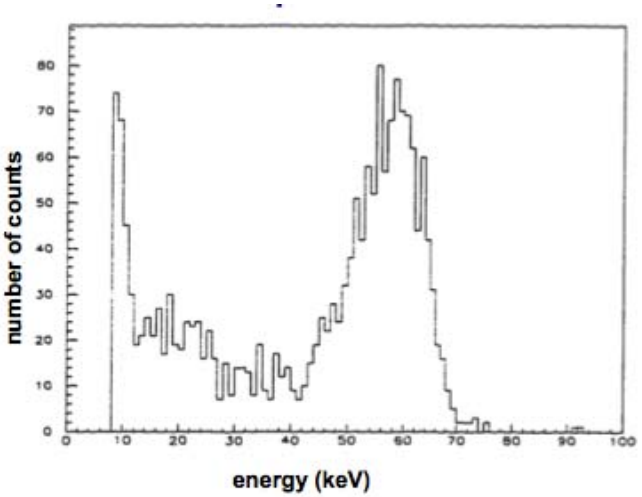

Fig. 12. ^{241}AM spectrum measured with the pixel detector in non-sparse field mode. The measured peak is 59keV, as expected.

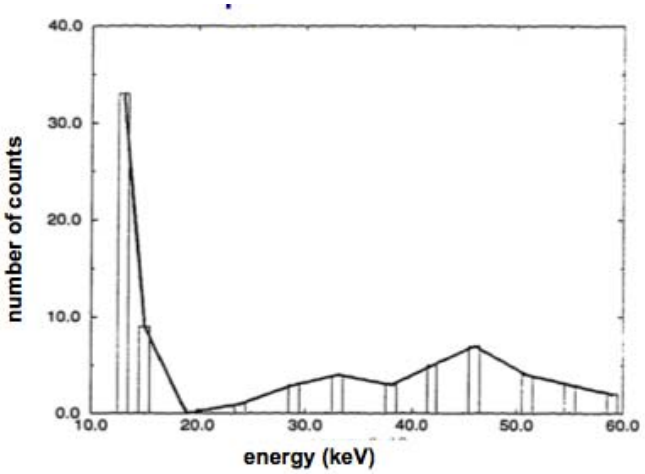

Fig. 13. ^{241}AM spectrum measured with the pixel detector in sparse field mode. The measured peak is 45keV, due to the sparse field mode triggering set-up.

V. Conclusion

We have developed and tested a second generation monolithic pixel detector, with full CMOS circuits built directly in the high-resistivity bulk silicon. A vertical high voltage junction termination structure was implemented to reduce yield loss caused by double sided wafer processing. CMOS circuits are fully functional, including sparse field readout. High minority carrier lifetime was maintained in the substrate after the full process. Radiation tests demonstrated the feasibility of our approach for particle physics or x-ray imaging applications.

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