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Habib, Samer Bou (Insitute of Electronic Systems, Warsaw University of Technology, Warsaw, Poland) *et al*

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Design of eight-channel ADC card for GHz signal conversion

Samer Bou Habib, Krzysztof Czuba
Insitute of Electronic Systems
Warsaw University of Technology
Warsaw, Poland

Wojciech Jalmuzna
Department of Microelectronics and Computer Science
Technical University of Lodz
Lodz, Poland

Tomasz Jezynski
DESY
Hamburg, Germany

***Abstract*—This paper describes the design of an eight-channel ATCA card suited for direct analog-to-digital conversion of 1.3 GHz signals with a maximum ADC clock frequency of 500 MHz. The undersampling operation is used for signal conversion. This card was designed for the needs of the LLRF system of the FLASH and XFEL accelerators. The designed module consists of a main ATCA board with eight ADCs, FPGA unit, memory, power supply and diagnostic circuits. The main ATCA card allows connecting a daughter board with IPMI, CPU and fast interfaces for communication purposes. This paper describes such issues as system organization allowing acquisition of data at such high data rates, circuit synchronization by high-quality clock signals, CPU and connectivity features, 20-layer PCB design and techniques used for high-frequency signals transmission and matching.**

***Index Terms*—LLRF, direct sampling, field detection, fast ADC, ATCA**

I. Introduction

The modern superconducting linear accelerator facilities such as the XFEL require an RF field stability of up to 0.01 degree in phase and 0.02% in amplitude [1]. The field stabilization is assured by the LLRF system and is based on the precision of the field measurement at the frequency of 1.3 GHz [2]. The most often used way for phase and amplitude measurements is to convert the 1.3 GHz RF signal to a lower, Intermediate Frequency (IF) and then sample the IF signal by ADCs [3]. Recently high resolution (>12 bits) ADCs became available with input bandwidth significantly exceeding 1 GHz. Therefore measurements of 1.3 GHz signal are possible directly, without using downconverters. It was demonstrated [4] that the 14-bit ADS5474 ADCs can be successfully used for the RF field measurement for the LLRF system purposes[1]. The most important advantages of the direct sampling are that it doesn't require a high performance LO signal and it is a much smaller and simpler measurement circuit with less sensitive RF and analog components.

The LLRF control system for one accelerator RF station must calculate a vector sum for controlling 32 superconducting cavities in 4 cryomodules. To provide control signals for the RF field source (klystron), transmitted, forward and reflected signals from each cavity are processed. This implies the necessity of processing almost 100 input channels at each RF station. Therefore a multichannel measurement receiver hardware development was launched. The newest LLRF system concept assumes the use of the xTCA [5] standard as the base for the system hardware. It was decided that an eight-channel direct sampling ADC ATCA card prototype was designed for investigations of multichannel direct sampling system performance.

[1]Additional tests were made using the 12-bit ADS5463 showing its validity for the purpose.

II. Field Detection and Undersampling

The input bandwidth of the ADS5474/ADS5463 (1.4 GHz and 2.3 GHz respectively) is several times higher than the sampling frequency (max. 400 MHz and 500 MHz respectively). With such parameters undersampling can be used to measure signals in the higher Nyquist band (Figure 1). The non-IQ sampling scheme [6] was selected for deriving the phase and amplitude of the measured signal. The clock signal brought to the ADCs should be synchronized with the measured RF frequency and the clock value can be determined by the formula below

$$f_s = \frac{f_0}{k + \frac{m}{n}}\,,\ k = 0, 1, 2, ... \tag{1}$$

where f_0 is the RF frequency, m and n represent the phase difference between two adjacent samples as given by the formula

$$\Delta\phi = \frac{m}{n} \cdot 2\pi \tag{2}$$

There is significant flexibility in selecting the f_s and the optimum value will be a subject of detailed study after the ATCA card is manufactured. Therefore the described board was designed to assure a broad range of clock settings up to 500 MHz.

III. System Conception

The main objective of the project was the design of an eight channel receiver allowing to test very high speed ADCs. The goal of the tests is to check the possibility of replacing standard techniques involving the usage of downconverters and slower ADCs, solely with the new faster ADCs. The device would allow deriving IQ from eight cavities, i. e. one cryomodule of the FLASH or XFEL accelerators. The designed receiver

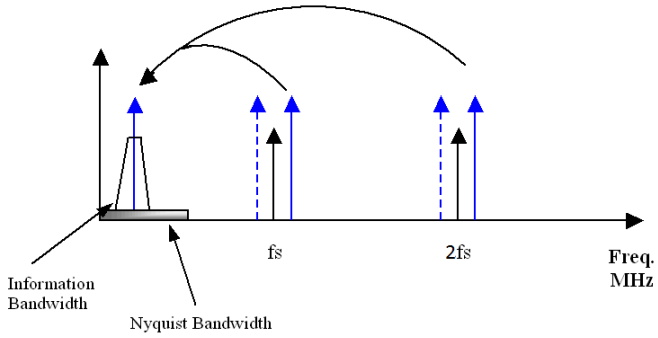

Figure 1. Harmonics moved to first Nyquist Bandwidth due to undersampling

consists of two boards: a full sized ATCA carrier board and a replaceable daughter board. An option was foreseen that the receiver can be even used as a stand-alone system with no need for the ATCA crate. The main system conception is illustrated on Figure 2.

Eight of the 1.3 GHz signals coming from the cavities will be sampled by eight ADCs. The high frequency analog signals must be impedance matched to the input of the ADCs. The converters must work synchronously with the input signals. Thus a reference signal coming from the accelerator's Master Oscillator unit is used for synthesis and distribution of very low jitter clock signals to the converters. Data from the ADCs is received simultaneously by an FPGA where detection algorithms are implemented to derive the required amplitude and phase information. The FPGA is furthermore used to configure all peripheral devices and manage communication with external devices. A processor daughter board provides additional processing power and supports communication with the ATCA-LLRF system. Finally, diagnostic circuits are implemented to allow monitoring of the board operation and temperature. The SRAM memory blocks are added for eventual data storage and post-analysis.

IV. System Design

In order to achieve proper functioning and desired performance, very precise, cutting edge analog, digital, clocking and power supply designing techniques were applied.

A. System Architecture

As stated earlier, the system consists of two boards:

- the ATCA mother board – containing the analog, clocking and digital parts of the system needed for proper acquisition of the data for the field detection process,
- the add-on CPU daughter board – allowing full integration of the boards with the ATCA-LLRF system. Moreover, the functionality of the daughter board allows configuring the system for stand-alone operation. The sampled data can then be sent via optical links to external devices without plugging the module into the ATCA crate.

The detailed system block diagram is shown in Figure 3. General information about the module's subsystems is presented in the following sections. More details can be found in [7].

B. Fast ADC Circuits

The board allows testing of two types of pin-compatible ADCs:

- ADS5474 – a 14-bit ADC with maximum sampling frequency of 400 MSPS, 1.4 GHz badwidth and nominal ENOB of 11.2 bits.
- ADS5463 – a 12-bit ADC with maximum sampling frequency of 500 MSPS, 2.3 GHz badwidth and nominal ENOB of 10.5 bits.

Both converters are based on a pipeline architecture with an internal digital error correction function. In order to reach best performance, the high frequency analog input signals are symmetrized and driven differentially and are precisely impedance matched to the input of the ADC. The board design also allows testing of different matching configurations by using optional small daughter boards for filtration, gain, or DC-coupling at the inputs of each ADC. The digital output data bus is also driven differentially using the LVDS standard.

C. Timing and synchronization

Phase synchronization of the RF input signals with ADC sampling frequencies is assured by a precise PLL device locked to a reference clock signal. The device can synthesize very low jitter clock signals (around 450 fs rms). Clocking and synchronization of the ADCs is realized in the LVPECL standard. The clocks are then distributed to the eight ADCs with the possibility of shifting the phase of each channel[2]. This operation can be used for experiments with interleaving.

D. FPGA, Memory and Interfaces

Data from the ADCs is received by the XilinX Virtex5 SX50T FPGA. This is a high speed FPGA able to process the incoming data at a rate of up to 500 MSPS (i.e. 4 GSPS from eight channels). Along with all the connected peripherals the FPGA has more than 400 used IO pins where almost 90% of them are configured to use differential standards. The reason behind choosing an FPGA from the SXT series is that it is enhanced with DSP and memory blocks that allow implementation of real-time algorithms for "IQ detection" and calibration and error decreasing algorithms.

In order to characterize the performance of the system four DDR 400MHz SRAM memory blocks are used additionally in the prototype. These high speed memories allow acquisition of samples from all ADCs simultaneously[3].

The Gigabit Ethernet is used to connect the board to the rest of the ATCA-LLRF system. In addition, there are two SFP cages mounted for using high speed optical links to connect the module with other devices and for increasing the reliability of the system. For testing purposes and general usage, a standard ethernet and USB connections have also been added.

[2]The drawback of this process is that , if used, it increases the clock jitter.

[3]All eight channels can be handled when the ADC clock frequency does not exceed 400MHz which is the general case of the system operation

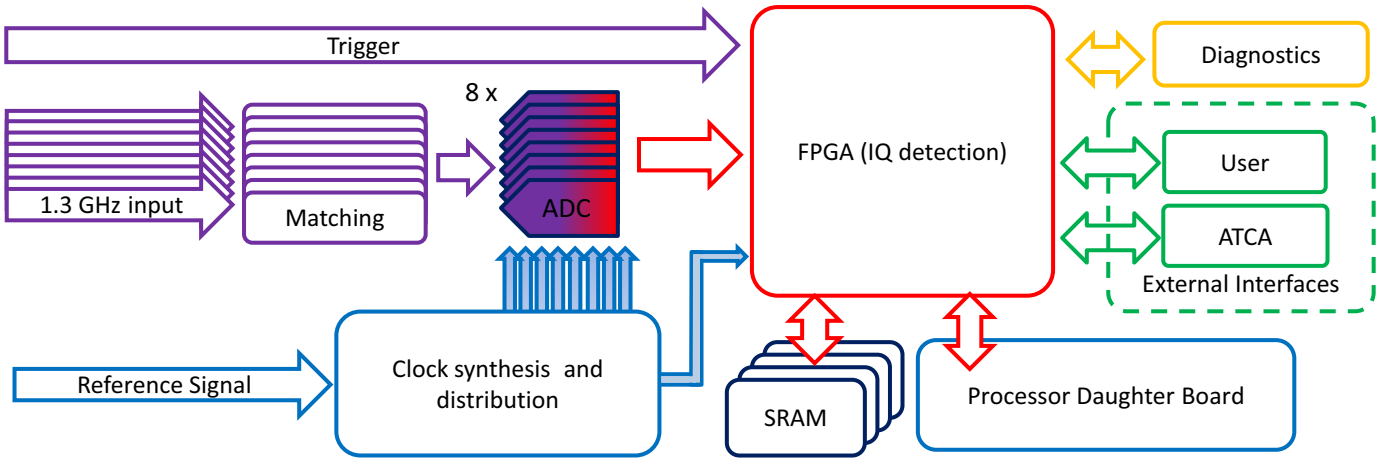

Figure 2. System general conception

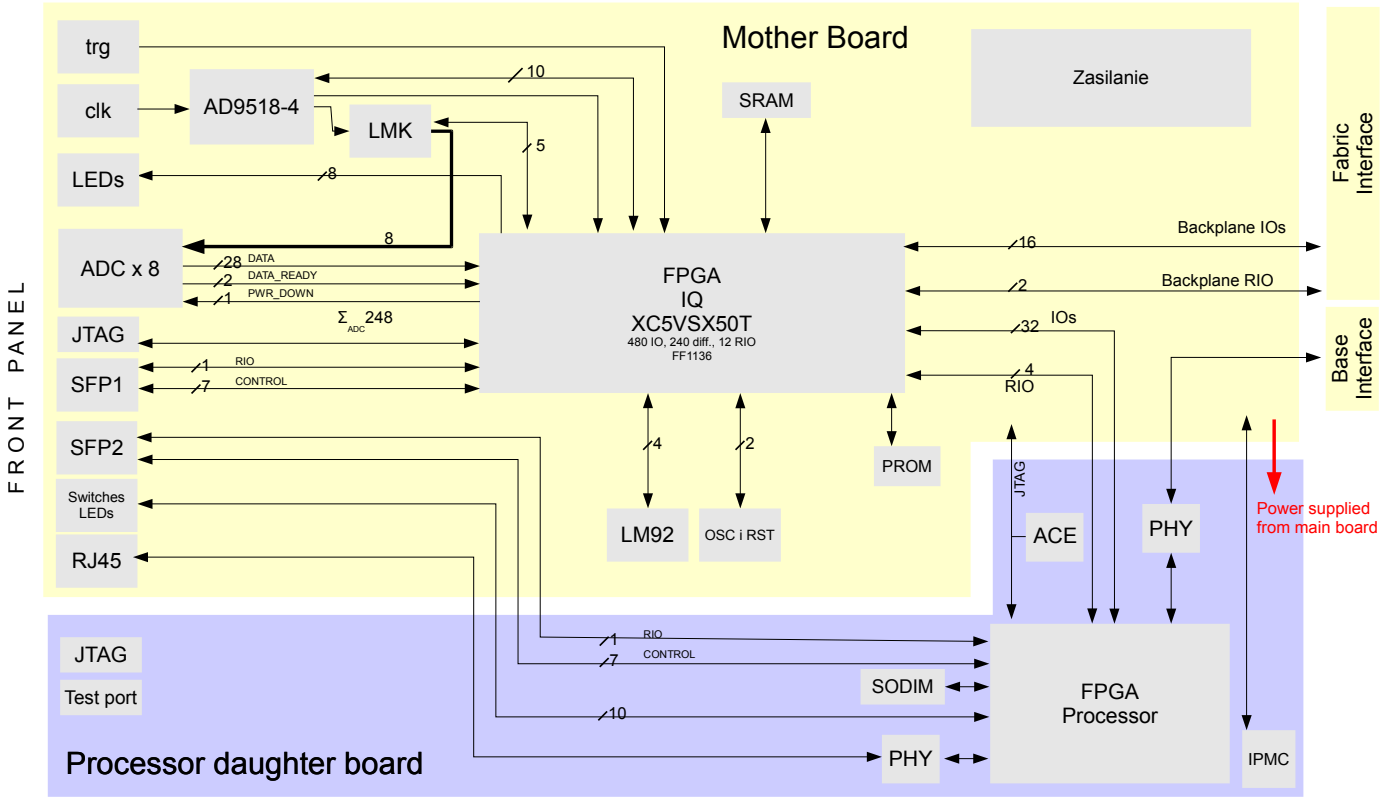

Figure 3. Two-board system architecture

E. CPU Daughter Board

The core of the CPU Daughter Board is a Virtex 5 FXT FPGA chip equipped with embedded PPC440 processor. In addition, the board accommodates such peripherals as SODIMM socket for DDR2 memories, Ethernet PHY and SystemACE chip together with a CF card slot. It can be connected to the carrier board using two QSF connectors.

The main purpose of the board is to provide various communication interfaces for ADC board. They include Gigabit Ethernet, custom Low Latency Links or ATCA specific functionality such as IPMI unit. Providing such functionality on a daughter board simplifies the main board design and provides additional modularity. Furthermore, due to the PPC440 usage, implementation of high level protocols can be fast and efficient. If necessary, the board can share its computation power and memory storage with the main board.

The features of the CPU Daughter board make it a universal communication interface adapter, which can be used for various applications. Due to the amount of memory space and computation power, it can be used to execute a large amount

of computation algorithms. Such algorithms can efficiently use available architecture to combine advantages of parallel FPGA computations, CPU flow control and fast interconnections with external systems [8].

F. Diagnostics

The board is equipped with two means of diagnosis:

- Device monitoring – mainly for clocking and power supply subsystems, it allows us to check proper functioning and performance of the entire device.
- Board temperature monitoring – for the safety of the board operation and for acquisition of information about system performance with respect to temperature changes.

V. ATCA Card Design

The ATCA card design involved state-of-the-art design in different fields of electronics to ensure signal integrity of digital signals and minimum noise and phase jitter in the system. 7 different DC/DC converters and almost 60 Low DropOut regulators are combined together in a very complex power supply and grounding design. This design is used to ensure isolation of analog, clocking and digital components with very stable and low noise supplied voltages.

Very precise element positioning and routing alignments were done in order to sustain proper synchronization of the ADC sampling process. Another very important fact is that all signals (analog, clocks and digital) are high frequency signals, where microwave phenomena start to affect the signal transmission even in the digital lines. In order to keep the required signals' quality, these phenomena had to be taken into serious consideration by transmission line impedance control and RF grounding techniques.

The PCB stack-up used for the design is a 20 layer upmarket board. The stack-up allows various through, blind and buried vias, provides proper isolation and grounding for routing high performance and low jitter signals. It also enables fanout of the large BGA devices i. e. the Virtex5 FPGA and SRAM blocks. Over 160 differential pairs including RocketIO signals and over a 100 single lines more were routed from the FPGA chip.

The topmost and bottom layers of the board are shown on Figure 4, where:

- A is an ADC with the input circuit (one channel out of eight);
- B is the clock synthesis circuit;
- C is the FPGA;
- D are the SRAM blocks;
- E is the processor board placement area where;
  - E' are the daughter board connectors;
- F are SFP cages;
- G is an alternate-matching daughter board connector (one out of eight);
- H is the main DC/DC converter;
- I are ATCA backplane connectors.

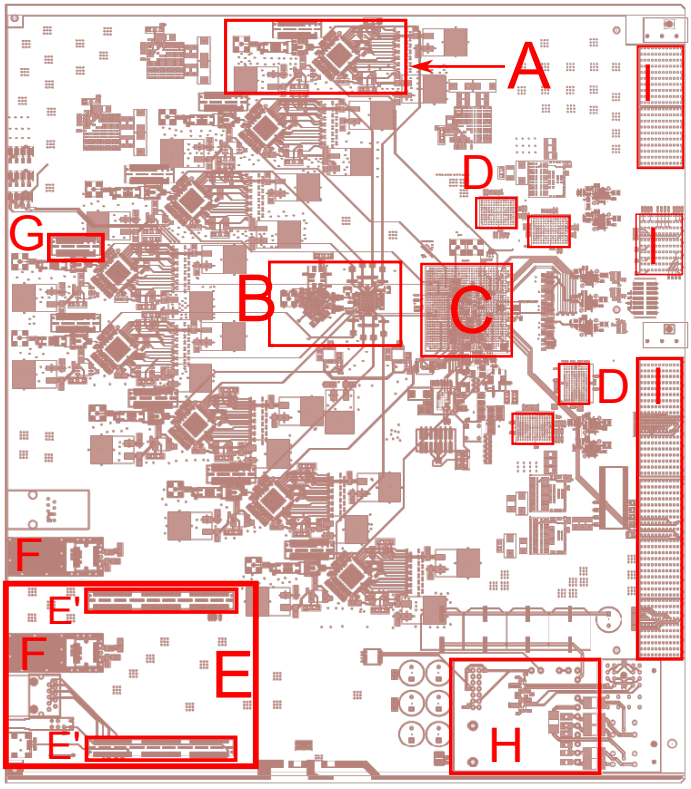

Figure 4. PCB mother board – top and bottom layers

VI. Summary

The eight channel fast ADC ATCA board conception and design is described. The module's complex architecture and design allows on-line processing of all the high-rate (up to 4 GSPS) data. The (7 Mbit) on-board memory can be used for storage and postprocessing of the acquired data blocks. The CPU daughter board extends system functionality and connectivity. The designed board will be used for extensive study of the LLRF system performance with the direct sampling receiver.

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