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ABSTRACT: The existing three-level ATLAS trigger system is deployed to reduce the event rate from the bunch crossing rate of 40 MHz to $\sim$200 Hz for permanent storage at the LHC design luminosity of 10^{34} cm^{-2} s^{-1}. When the LHC exceeds the design luminosity, the load on the Level-2 trigger system will significantly increase due both to the need for more sophisticated algorithms to suppress background and the larger event sizes. The Fast Tracker is a proposed upgrade to the current ATLAS trigger system that will operate at the full Level-1 accepted rate of 100 kHz and provide high quality tracks at the beginning of processing in the Level-2 trigger, by performing track reconstruction in hardware with massive parallelism of associative memories. The concept design is being advanced and justified with the performance in important physics areas, b-tagging, τ-tagging and lepton isolation. The prototyping with current technology is underway and R&D with new technologies has been started.

KEYWORDS: Trigger concepts and systems (hardware and software); Digital electronic circuits

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1 Introduction

The LHC will open a new energy regime in which to address the most important questions in particle physics. The cumulative results of experiments at lower energy suggest that phenomena never before observed will be seen in the LHC data. One of the most intriguing physics subjects is the Higgs particle search. Because the source of electroweak symmetry breaking couples in proportion to mass, heavy fermions are likely in the final state of Higgs decay, in particular b quarks and τ leptons. Triggering these processes requires sensitivity to the enormous background from QCD originated light quark and gluon jets, which can be suppressed using tracking information. The b jets can be identified with a secondary vertex or tracks not pointing to the beam line, while τ jets can be separated from background using the number of tracks within a narrow signal cone and the number in a larger isolation region. Lepton triggers can also be improved, particularly at high luminosity, by using track based isolation while traditionally isolation is applied with the calorimeter information and the performance gets worse at high luminosity because of the additional energy from pileups.

The ATLAS detector [1] is designed to study proton proton collisions at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to reduce this rate to the level at which only interesting events will be fully reconstructed, a three-level trigger system has been deployed [2]. The level 1 trigger (LVL1) reduces the rate down to 75 (100) kHz via custom electronics. The Region of Interest Builder (RoIB) delivers the Region of Interest (RoI) records to the level 2 trigger (LVL2) which runs the selection algorithms with commodity processors and brings the rate further down to $\sim$3 kHz. Finally the Event Filter (EF) reduces the rate down to $\sim$200 Hz for permanent storage. To handle the RoIs at LVL2 and the full event at the EF level, the time budget in the current architecture for LVL2 processing is $\sim$40 ms and EF $\sim$1 s. Therefore it is impossible to perform detailed tracking before the EF level. A hardware track finder being proposed, the Fast TracKer (FTK), will provide global track reconstruction immediately after the

ATLAS LVL1 accept. The offline-like tracks and increased available processing time will allow the improvement of downstream triggers.

2 System overview

FTK is a custom electronics system that rapidly finds and fits tracks in the ATLAS inner track detectors for every event that passes the LVL1 accept. A concept design is close to complete. It uses all 11 silicon layers, 3 of the pixel detector (PIX), 8 of the SemiConductor Tracker (SCT), over the full rapidity range covered by the barrel and the disks. It receives a parallel copy of the PIX and SCT data at the full speed of the LVL1 accept from the detector specific ReadOut Drivers (ROD) to the ReadOut Systems (ROS). After processing the hits FTK sends out the helix parameters of all tracks with transverse momentum p_T above a minimum value, typically 1 GeV/c. The FTK system is a scalable system and can be easily expanded to operate at higher luminosities.

The core algorithm consists of two sequential steps. In step 1, pattern recognition is carried out by a dedicated Associative Memory (AM) device, which finds track candidates in coarse resolution patterns, i.e., roads. This step uses massive parallelism to carry out what is usually the most CPU intensive aspect of tracking by processing hundreds of millions of roads nearly simultaneously as the silicon data pass through. When a road has hits in all silicon layers or all but one, step 2 is to perform the fit with the full resolution hits in the road to determine the track helix parameters and a goodness of fit. Only those tracks that pass a χ^2 cut are kept. The road width must be optimized to balance the workload between the two steps. Too narrow roads would require too large AM size therefore too high cost, while too wide roads would increase the track fitting time drastically.

2.1 System architecture

In order to sustain a 75(100) kHz LVL1 rate, FTK is organized as a set of independent engines, each covering a different detector region. The detector coverage is divided into azimuthal regions. The potential inefficiency at region boundaries is remedied by having overlap between regions. At the luminosities up to 3×10^{34} cm^{-2}s^{-1}, 8 ϕ regions of 45° width with an overlap of 10° can ensure high efficiency for tracks with p_T of 1 GeV/c and above. Each region will have its own core processing units installed in one 9U VME crate (core crate) which works independently. Each region is further segmented into $\eta-\phi$ towers, each with its own AM board and track fitter board. The η range of each region is divided into four intervals, and the ϕ range of each region is divided into two 22.5° halves plus 10° overlap. A core crate could hold up to 16 AM boards, with 128 AM chips on each. With such a detector segmentation, the data can be distributed on 8 parallel buses at the full 75(100) kHz rate for the detector occupancy expected at the LHC design luminosity. For higher luminosities, more core crates could be added if it is necessary to segment further with respect to higher detector occupancy.

2.2 Component functionality

The sketch of a concept design is shown in figure 1. The PIX and SCT data are transmitted from the RODs and received by the Data Formatters (DF) which perform cluster finding. The cluster centroids in each logical layer are sent to the Data Organizers (DO). The DFs are not partitioned

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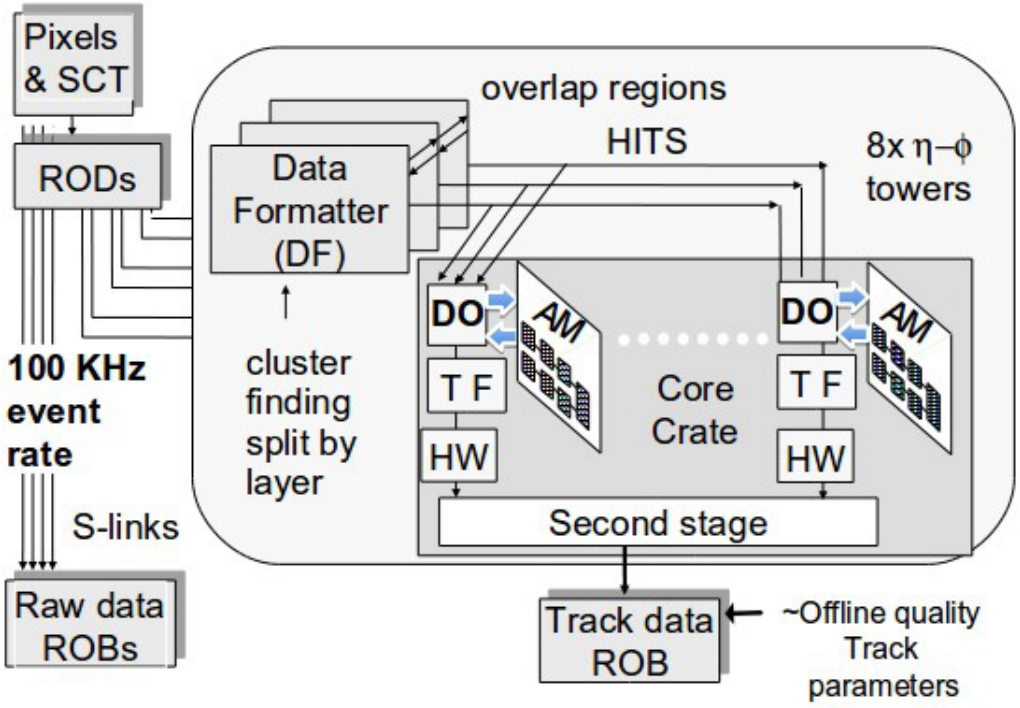

Figure 1. Functional sketch of an FTK.

into regions but organize the detector data into the FTK $\eta - \phi$ tower structure and deliver to the core crates, including the data in the overlap range.

The DO boards store full resolution hits and also convert hits to coarser resolution superstrips (SS) appropriate for pattern recognition in the AM. The DOs hold the smart databases where full resolution hits are stored in a format that allows rapid access based on the pattern recognition road ID and then retrieved when the AM finds roads with the requisite number of hits.

The AM boards hold AM chips which contain a very large number of preloaded patterns, corresponding to the possible combinations for real tracks passing through a SS in each silicon layer. These are determined in advance from a full ATLAS simulation of single tracks using detector alignment extracted from real data. The AM is a massively parallel system in that each hit is compared with all patterns almost simultaneously.

When a road is found, the AM sends the road back to the DOs. A DO immediately fetches the associated full resolution hits and sends them and the road to the Track Fitter (TF). Because each road is quite narrow, the TF can obtain helix parameters with high resolution via a linear fit with the local coordinates in each layer. Such a fit is extremely fast and a modern FPGA can fit approximately 10^9 track candidates per second.

3 R&D status

The AM chip, also known as Content Addressable Memory (CAM) chip, is the core technology needed for FTK. A critical figure of merit for the AM-based track reconstruction system is the number of patterns that can be stored in the memory bank. An AM chip using 180 nm CMOS

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technology and strictly standard cell was developed for the CDF SVT project [3]. This chip can hold up to ∼5K patterns and work at up to 40 MHz. Compared to the SVT project, the FTK is much more challenging and must provide very high efficiency and high quality track reconstruction in a much large detector with ∼86 million channels. Furthermore the higher luminosity will increase the complexity of events. Consequently a very large bank (could be up to 10^9) is necessary in order to ensure more than 95% efficiency for candidate tracks in the whole tracking detector ($|\eta| < 2.5$) and with transverse momentum down to 1 GeV/c. Moreover the pattern recognition has to cross 11 silicon detector layers with a reasonable resolution to reduce drastically the number of fakes and the track fitting processing time.

R&D has been started to increase the available area using 3D technology to stack multiple dies in the same package. It is planned to switch to the 65 nm technology as soon as it becomes affordable. The full custom cell layout will be further improved. Finally a few bits per layer will be added to implement the "don't care" option. Using the "don't care" as in ternary CAMs, variant pattern size becomes possible and the effective number of patterns is at least doubled. This will allow a more efficient use of the AM chip. These technologies together will increase the number of patterns per AM chip by a factor of ∼50 and make the total 10^9 patterns at reasonable cost feasible.

4 Expected performance

While the standard ATLAS Monte Carlo (MC) simulation framework is being used to produce physics data samples, some dedicated tools are developed to simulate the FTK hardware functionalities. Within the timing simulation tool, FTK system is represented with functional blocks described in the previous sections. With focus on the most time consuming steps, between DO write mode and TF, we estimate the processing time with *WH* events simulated with pileups at the luminosity of 3×10^{34} cm^{-2}s^{-1}. The FTK finishes global tracking in ∼25 μs on average, in contrast with hundreds ms or more needed for running full tracking at the current LVL2 system.

FTK tracks show similar efficiency, helix parameter resolution and fake rates, to the offline tracks. The immediate availability of FTK tracks following a LVL1 accept would free the entire 40 ms for more sophisticated tagging algorithms, and open the probability for the LVL2 Trigger to have the offline b tagging performance and light jet rejection power. Particularly the latter will be crucial at very high luminosities. In hadron collider experiments τ jet identification is usually track based with requiring the presence of 1 or 3 tracks in a very narrow cone with little or no track activity in a surrounding isolation cone. With FTK tracks the LVL2 can perform rapid rejection of the QCD background for τ selection. The preliminary results based on MC physics sample studies show that FTK tracking does nearly as well as offline tracking for b tagging and τ selection, and gives similar efficiencies and background rejection at high luminosities.

FTK tracks can be used for lepton isolation at LVL2. The muon efficiency with FTK track based isolation as a function of pile-up is roughly flat even for events with up to 100 pileup interactions, while the muon efficiency with calorimeter based isolation deteriorates dramatically when the pileups increases. The track based isolation gives a background rejection factor of 10 when the overall efficiency reaches approximately 80%.

The FTK performance in these areas will meet the physics requirements. At the LHC design luminosity or lower, the processes above will be less challenging and FTK will work even better.

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5 Conclusions

With FTK, the ATLAS trigger system will be greatly enhanced. When the LHC luminosity increases, the track availability from FTK will ensure a great performance of b tagging, τ dentification and lepton isolation.

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